ISSCC 2023 Tutorials

All-digital PLLs
From Fundamental Concepts to Future Trends

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Live Q&A Session: Feb. 19, 2023,

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Self-introduction

- **Akihide Sai**
- M.D. in EE from Waseda Univ., Tokyo, 2004
- R&D Fellow with Toshiba Corp.
  - Now within LiDAR R&D Group as Project Leader
  - 19 years in Toshiba Corp.
- Interests in high-performance mixed-signal circuit
  - Digital/analog phase-locked loops(PLLs)
  - Low power transceivers
  - Automobile LiDAR SoCs

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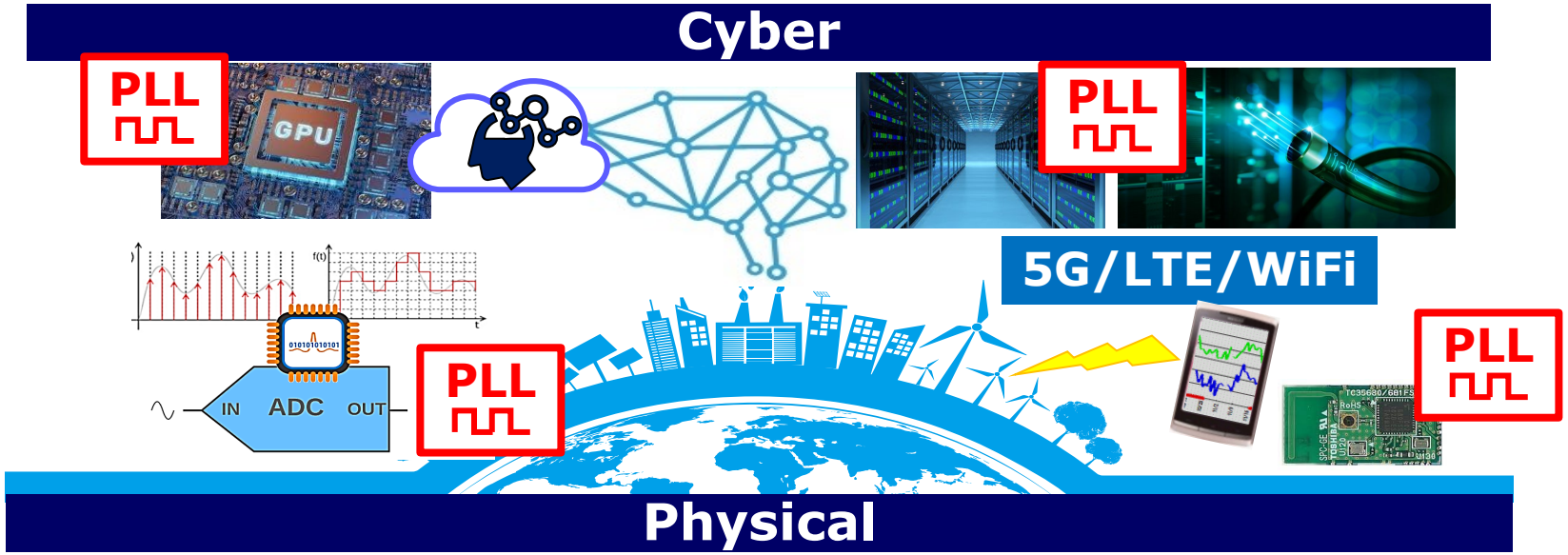
Motivation of Tutorial



- Recently, **Phase-Locked Loop (PLL)** has become more and more indispensable. Almost all components for Cyber-Physical IoT systems (GPU/CPU, data center, wireline/wireless…) need PLL for system clocking, data recovery, RF mixing!
- First of all, grasp basic of frequency synthesis including PLL, and then analyze the principle and benefit of **Digital-PLL**, with the technique evolution trend.
- Finally, try to analyze and predict the **future evolution trend**.

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Outline

- Background of Frequency Synthesis
  - Design Challenges for Jitter, Phase noise, Lock up
- Basic All-Digital PLL
  - Fractional-N Operation, Spurious Tones
  - Digital Implementation
  - Time-to-Digital Converter (TDC)
- Advanced Digital PLL
  - Basic and Fundamentals
  - High performance TDCs and Fractional Spur Cancellation Techniques
  - Performance Trends Analysis
- Future Trend Prediction
- Summary & conclusions

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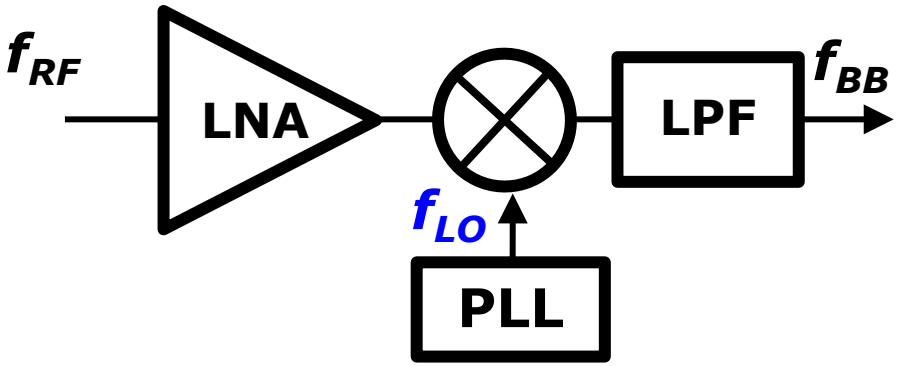
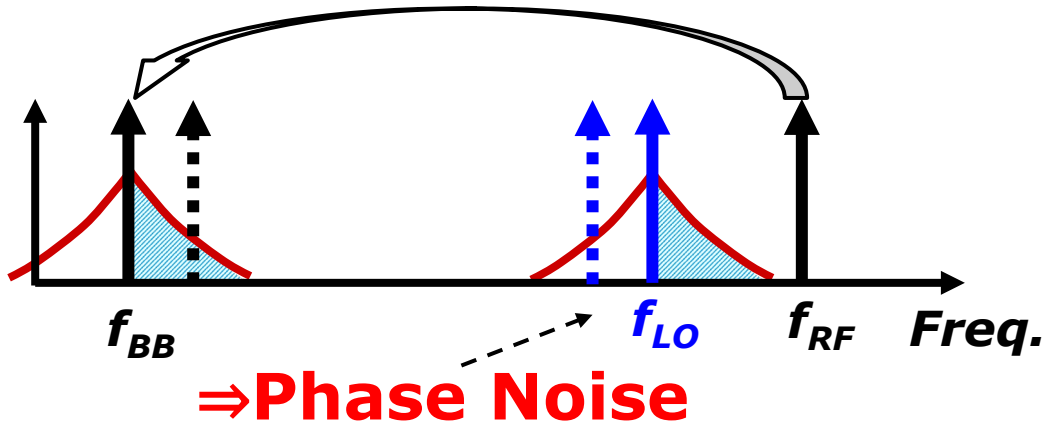
Frequency synthesis: Applicative constraints

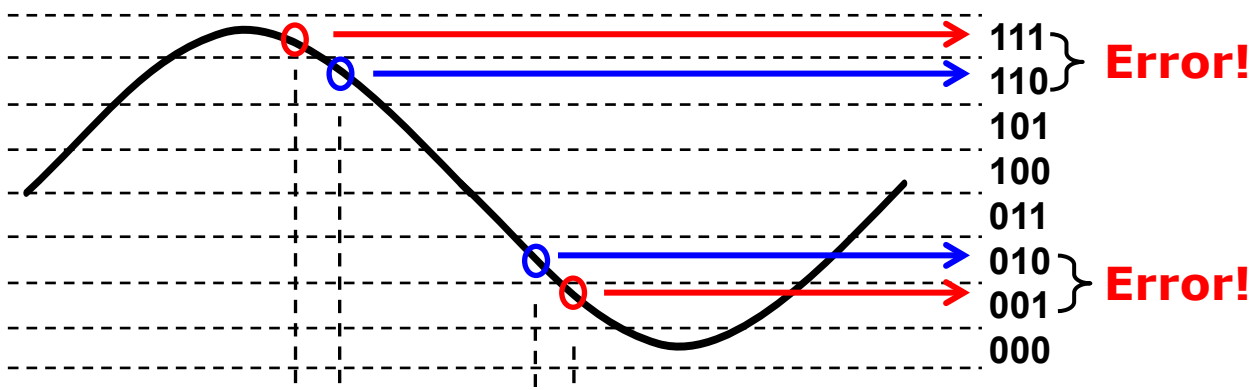
Mixing



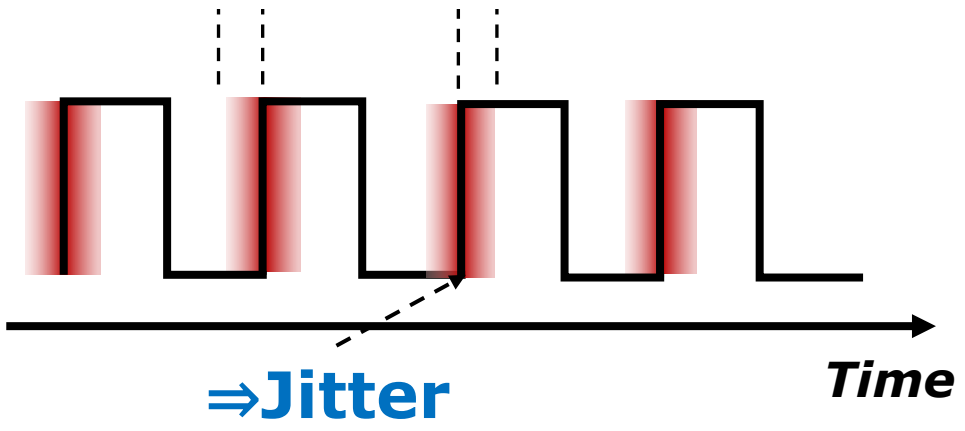
Low noise in frequency domain



Sampling



Low noise in time domain



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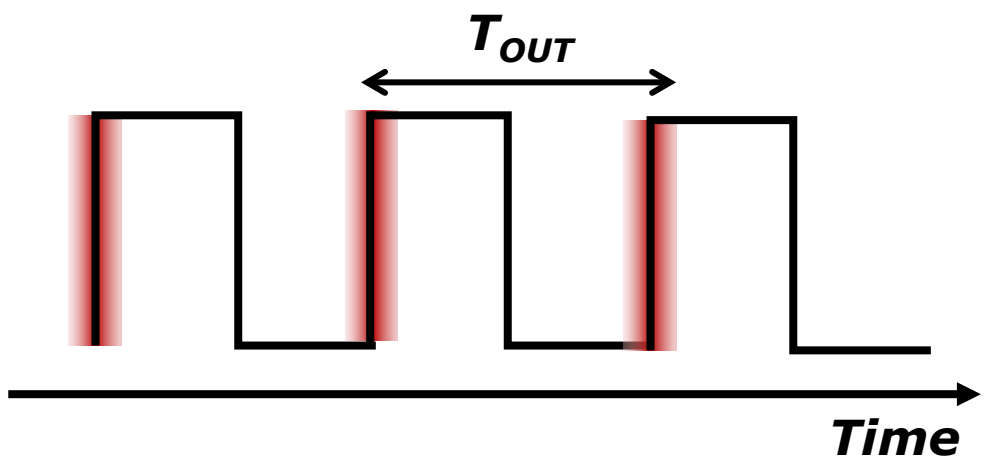
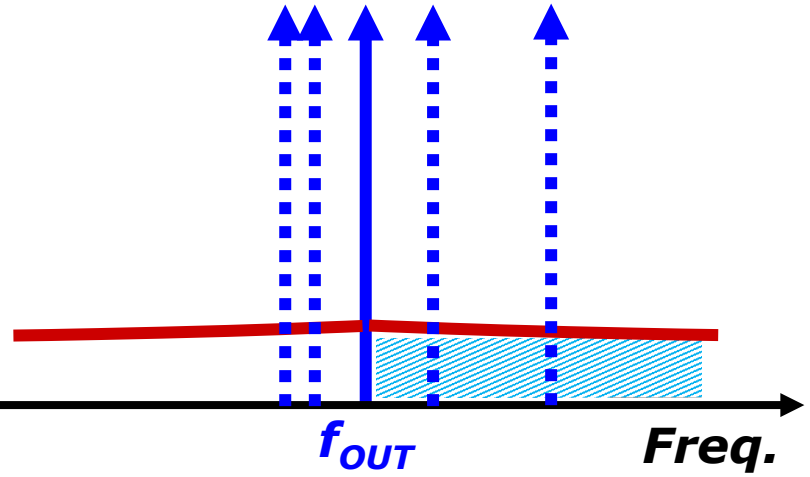
Period Jitter and Frequency Noise

- **Period Jitter** : **1-cycle fluctuation** expressed in **time domain**
- **Frequency Noise** : **1-cycle fluctuation** expressed in **frequency domain**

Period jitter [sec rms]



Frequency Noise [dBc/Hz]



$$T_{OUT} = \frac{1}{f_{OUT}}$$

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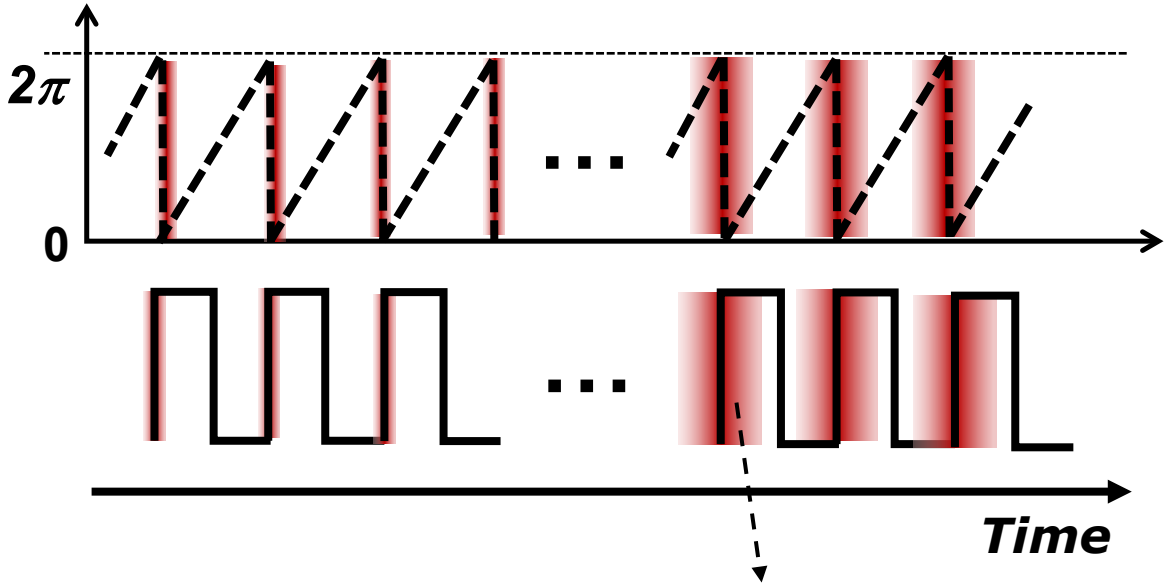
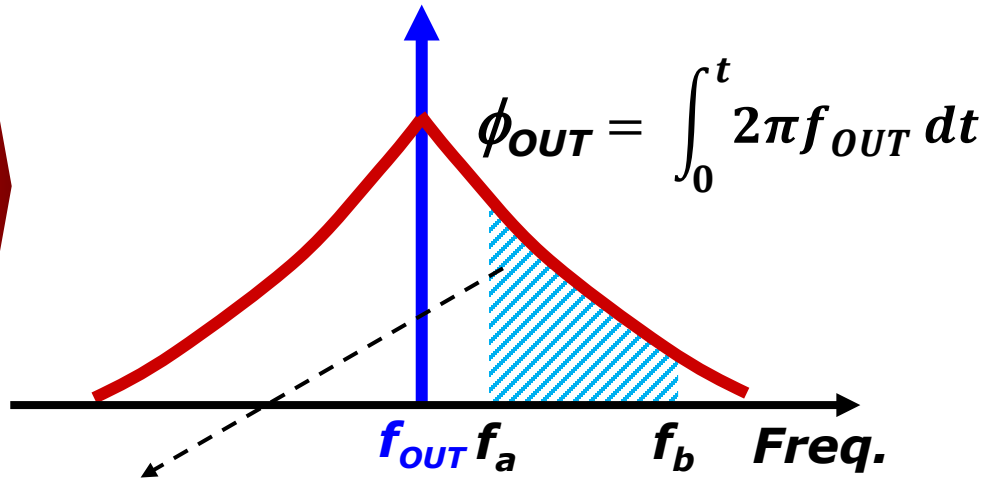
Phase Jitter and Phase Noise

- **Phase Jitter** : **long-term fluctuation** expressed in **time domain**
- **Phase Noise** : **long-term fluctuation** expressed in **phase domain**

Phase jitter [sec rms]



Phase Noise [dBc/Hz]



$$Phase\ jitter = \frac{1}{2\pi f_{OUT}} \sqrt{\int_{f_a}^{f_b} PSD[\phi_{OUT}]\, df} \qquad [sec_{rms}]$$

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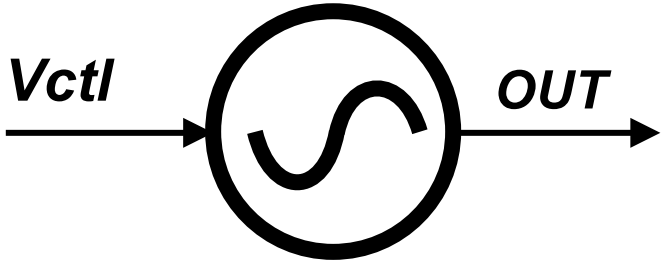
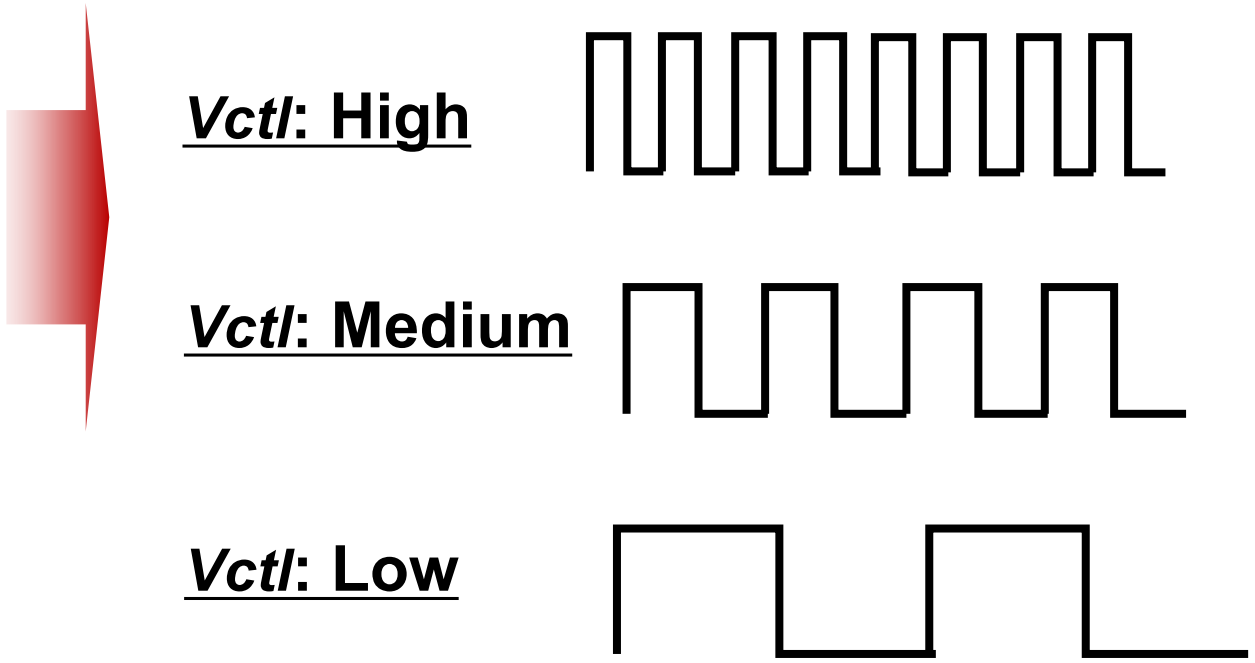
Free-running Oscillator

- Open-loop free-running oscillator is most simple clock generation
- **V**oltage **C**ontrols **O**scillator Frequency → **VCO (Voltage Controlled Oscillator)**





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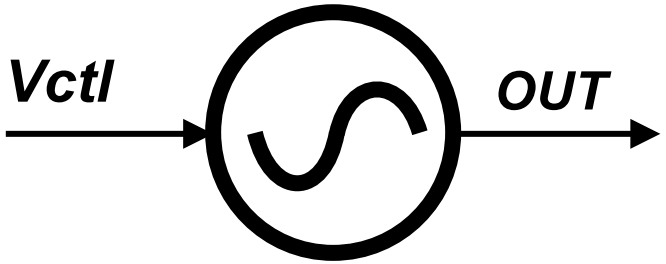
Free-running VCO

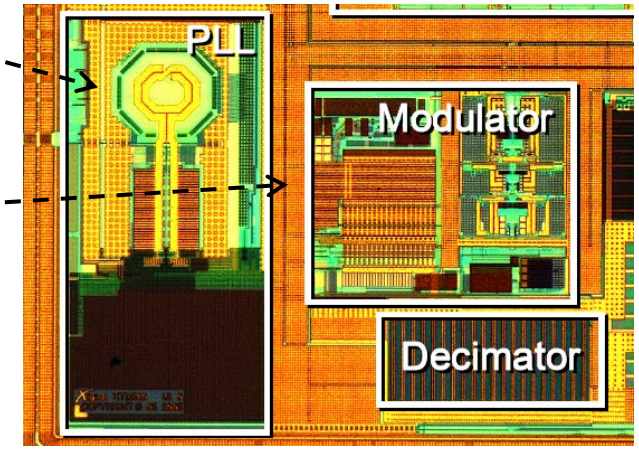
- Two major VCO types, LC/Ring, have critical design trade-off

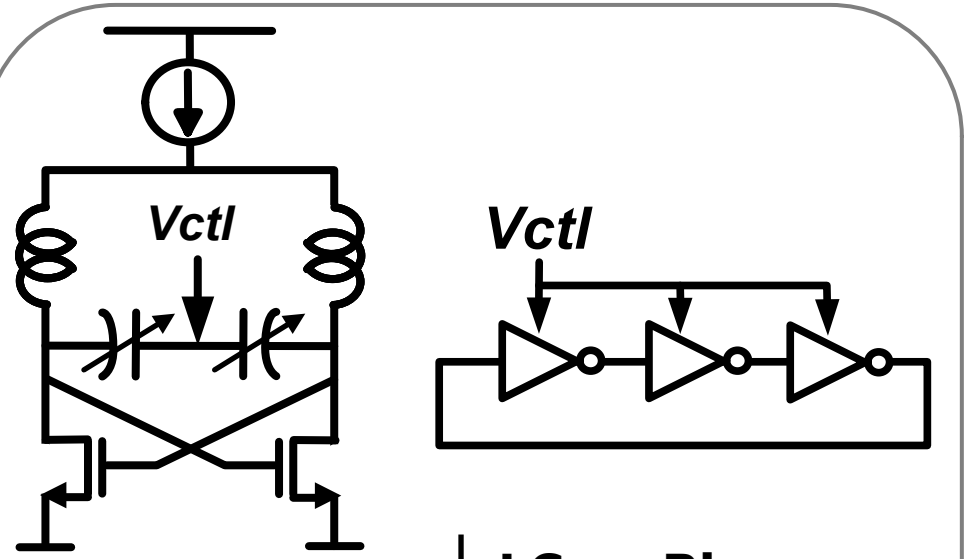


[Mitteregger,ISSCC'06]

LC VCO for CLK PLL

14bit ΔΣ ADC





	LC	Ring
Phase Noise	☺	☹
Chip Area	☹	☺

LC VCO for sampling clock may larger than ADC itself !!

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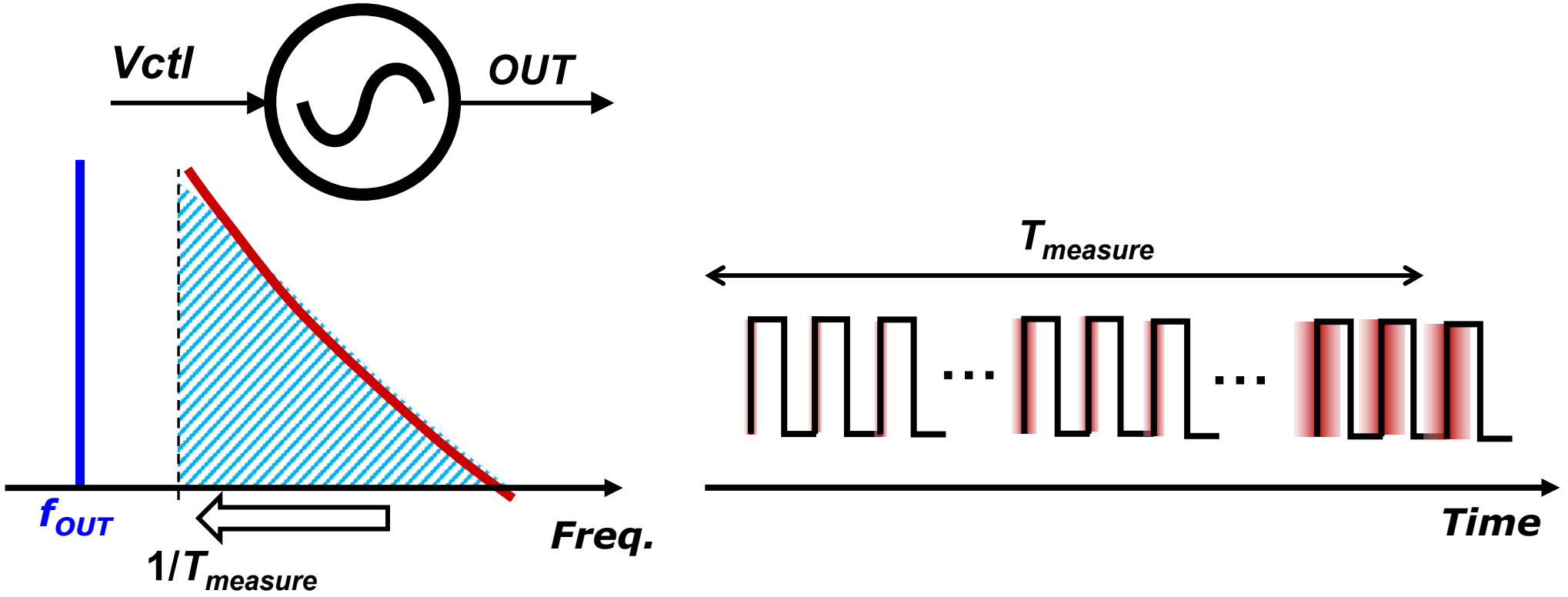
Issues with Free-running Oscillator

- Poor phase noise and jitter performance of VCO
  - No feedback controls enable jitter to diverge to infinity!



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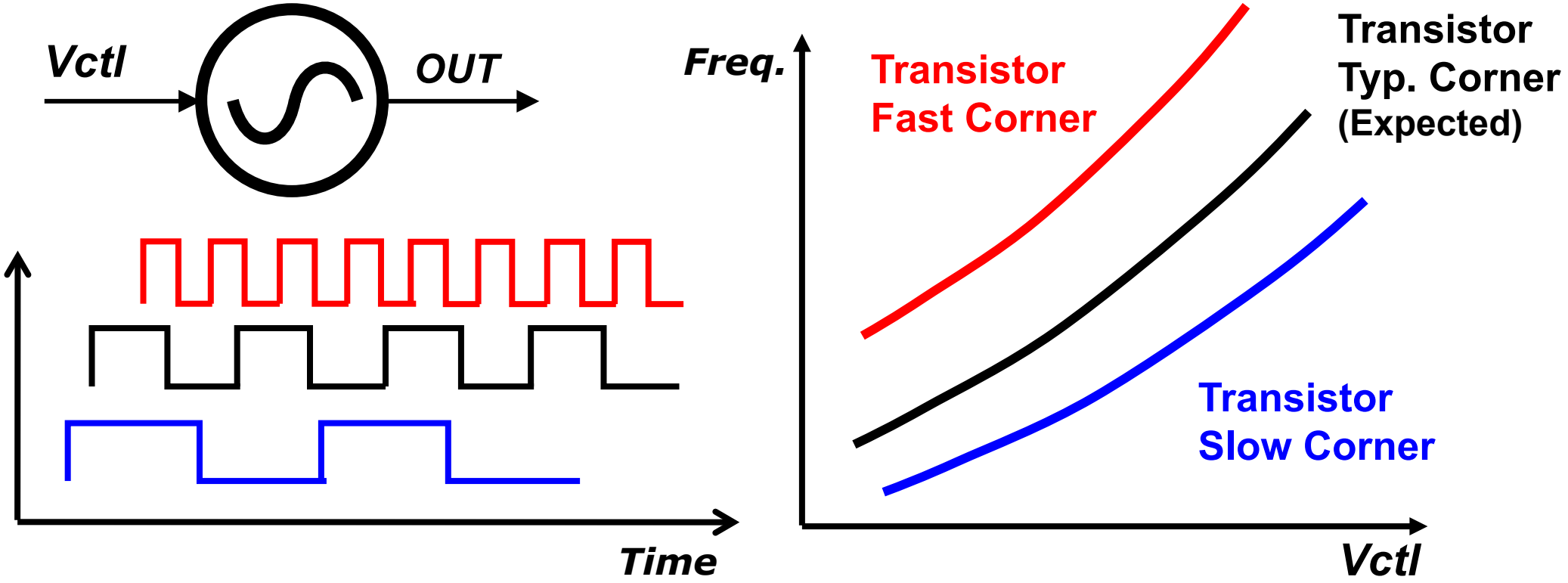
Issues with Free-running Oscillator

- Poor frequency accuarcy
  - Oscillation frequency can easily change with PVT variation



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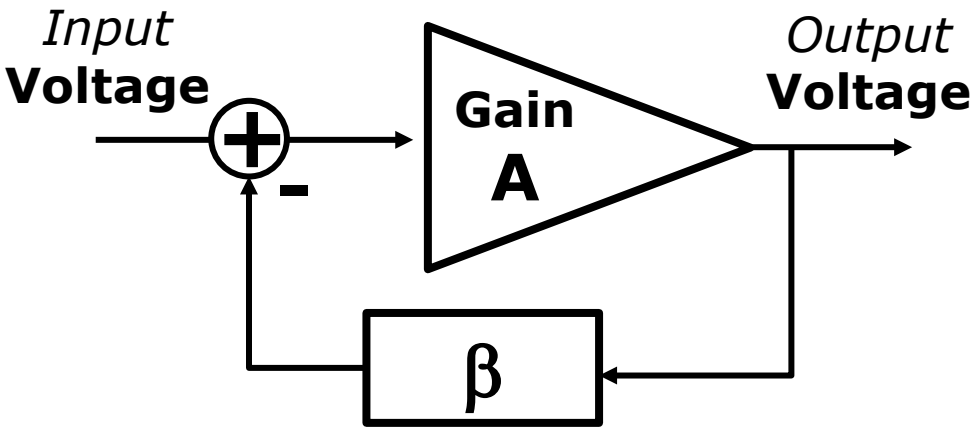
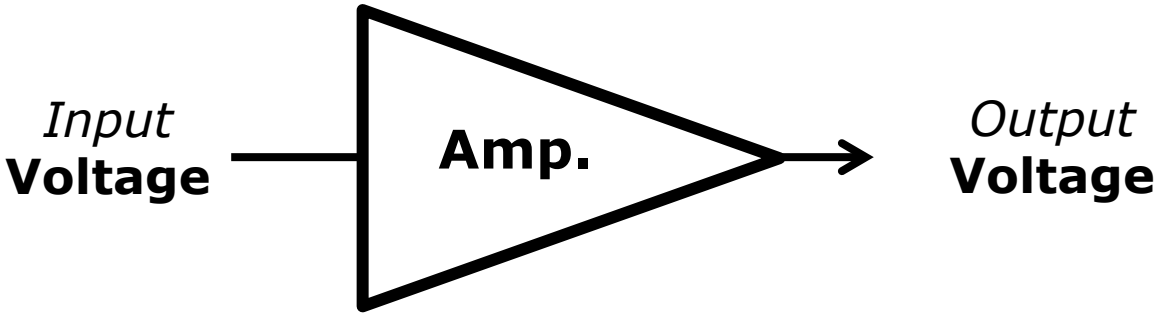
Amplifier: How to Create Accurate Output?

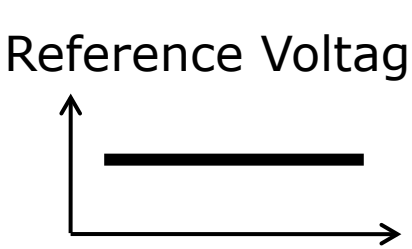
- Negative feedback can generate accurate output in voltage domain
  - Key points are **large feedforward gain A,** and **feedback factor** β

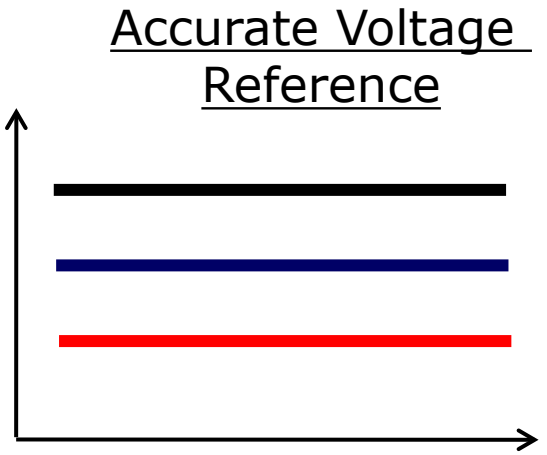


$$\frac{Output}{Input} = \frac{1}{1/A + \beta} \doteq \frac{1}{\beta}$$

A>>1







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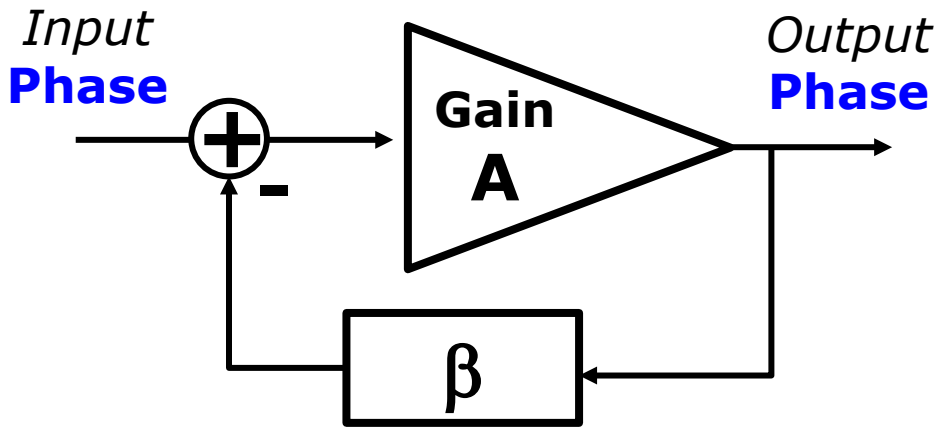
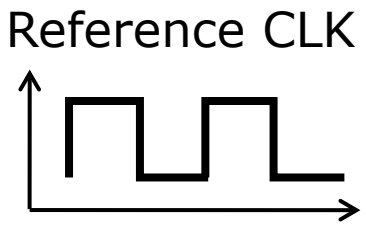
PLL: How to Create Accurate Clock?

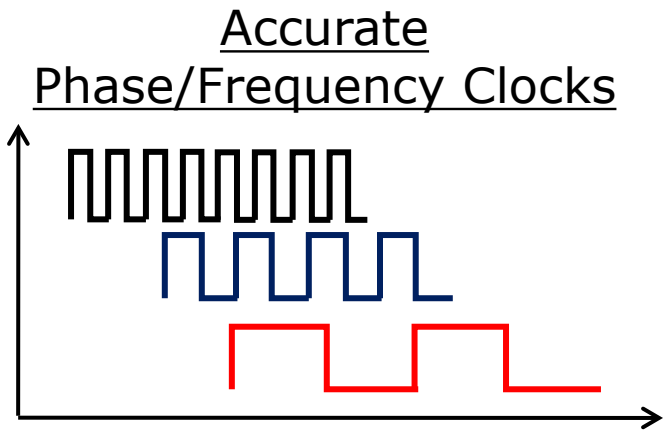
- **Phase-domain negative feedback** can generate accurate output ?
  - **'Accurate' means low phase noise and high frequency accuracy**



$$\frac{Output}{Input} = \frac{1}{1/A + \beta} \doteq \frac{1}{\beta}$$

A>>1





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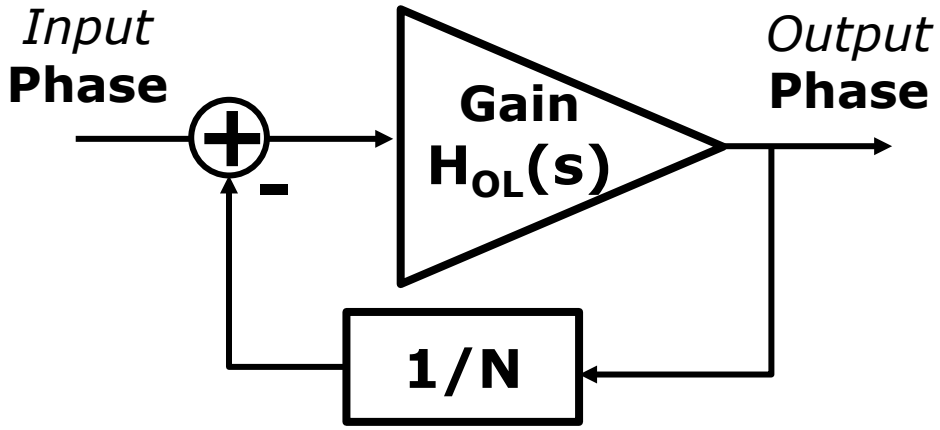
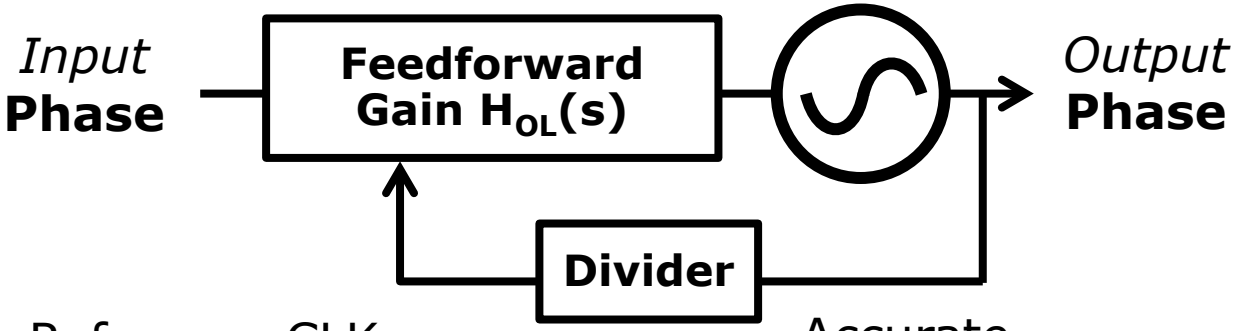
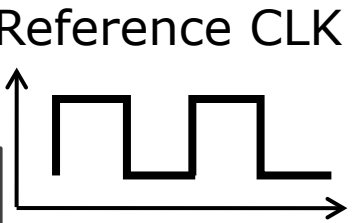
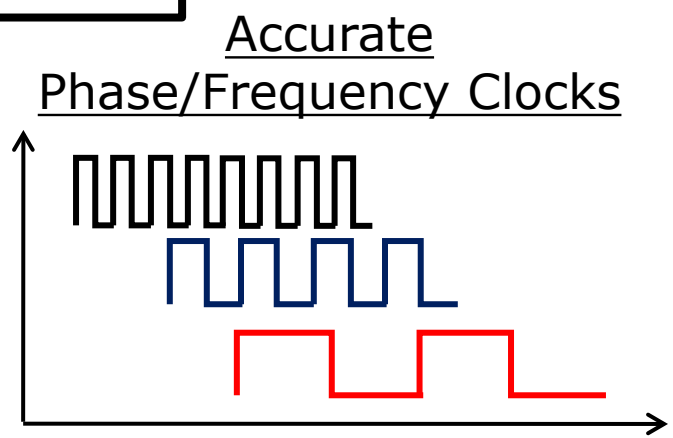
PLL: How to Create Accurate Clock?

- Feedback is constrained to clock division ratio
- Feedforward gain over the frequency spectrum determines PLL performance









$$\frac{Output}{Input} = \frac{1}{1/H_{OL}(s) + 1/N} \doteq N$$

$H_{OL}(s)$ >>1 N: Divider Ratio

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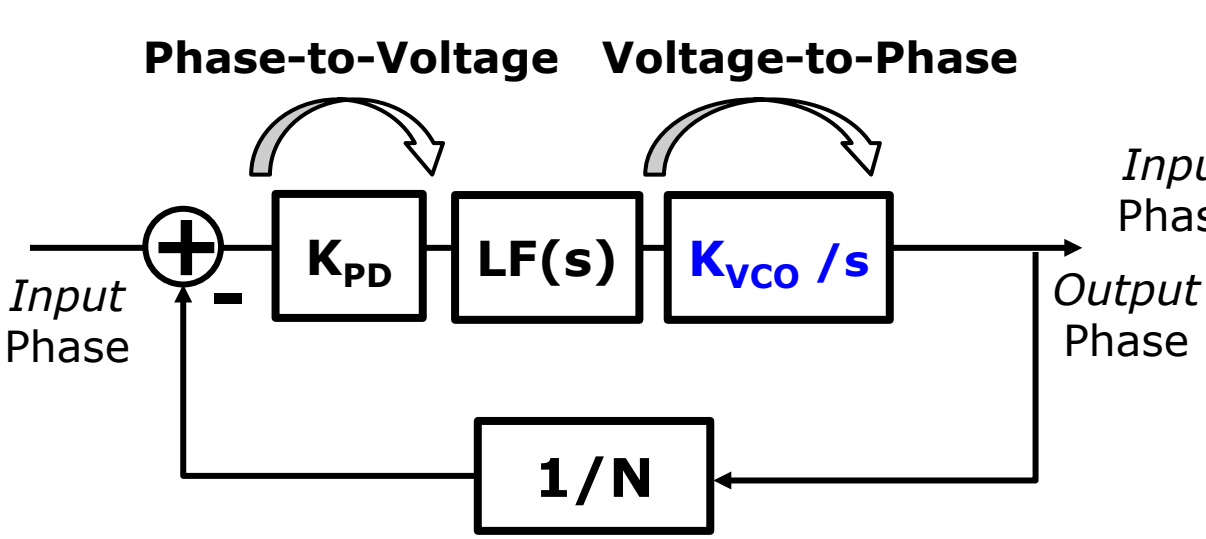
Type-I Analog PLL

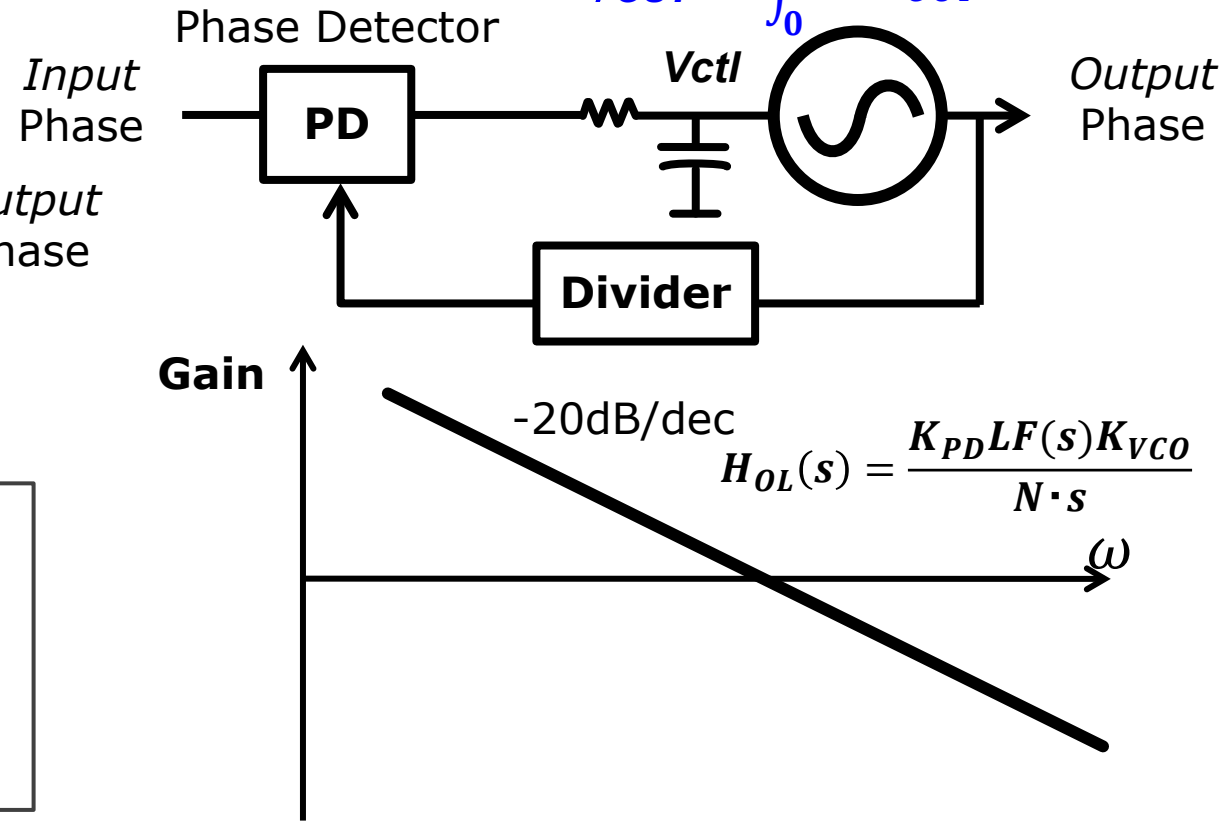
- Type-I PLL has one integrator of VCO frequency-to-phase conversion



$$\frac{Output}{Input} = \frac{1}{1/H_{OL}(s) + 1/N} \doteq N$$

$H_{OL}(s)$ >>1 N: Divider Ratio

$$\phi_{OUT} = \int_0^t 2\pi f_{OUT}\, dt$$



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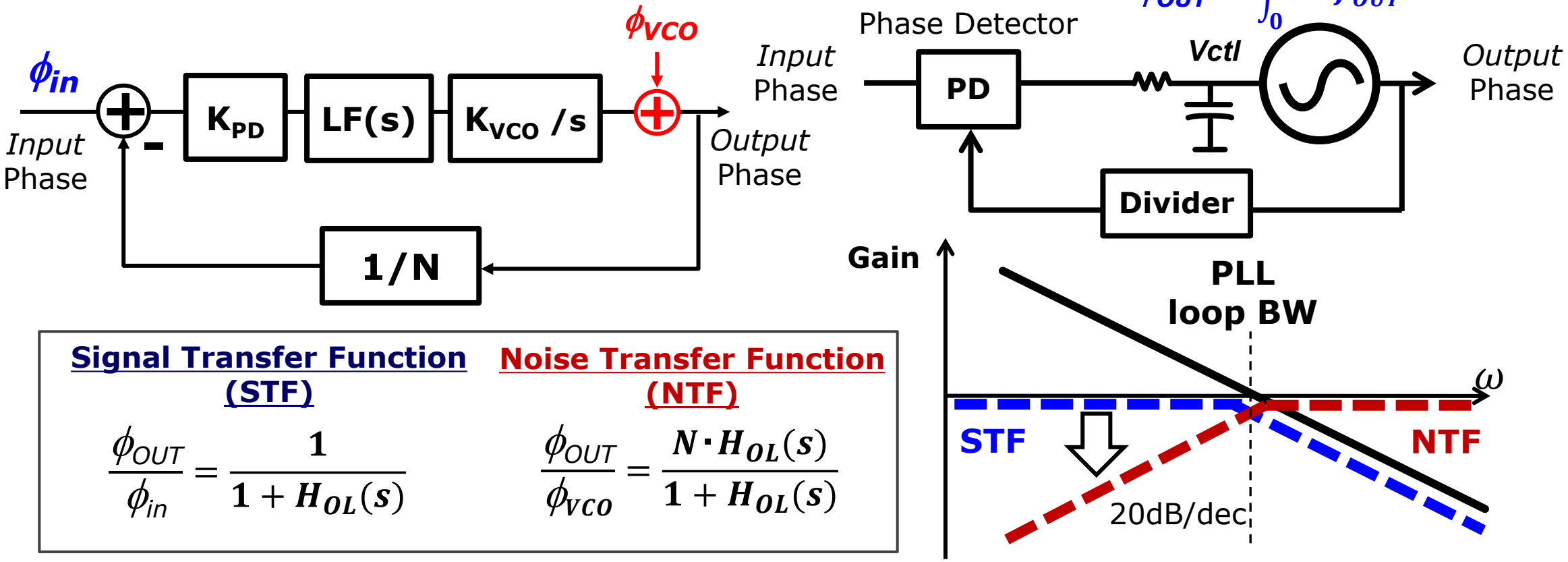
Type-I Analog PLL

- PLL loop bandwidth(BW) is determined by unity gain frequency of $H_{OL}(s)$
- Type-I PLL suppress VCO phase noise by 1st-order HPF



Signal Transfer Function (STF)

$$\frac{\phi_{OUT}}{\phi_{in}} = \frac{1}{1 + H_{OL}(s)}$$

Noise Transfer Function (NTF)

$$\frac{\phi_{OUT}}{\phi_{VCO}} = \frac{N \cdot H_{OL}(s)}{1 + H_{OL}(s)}$$

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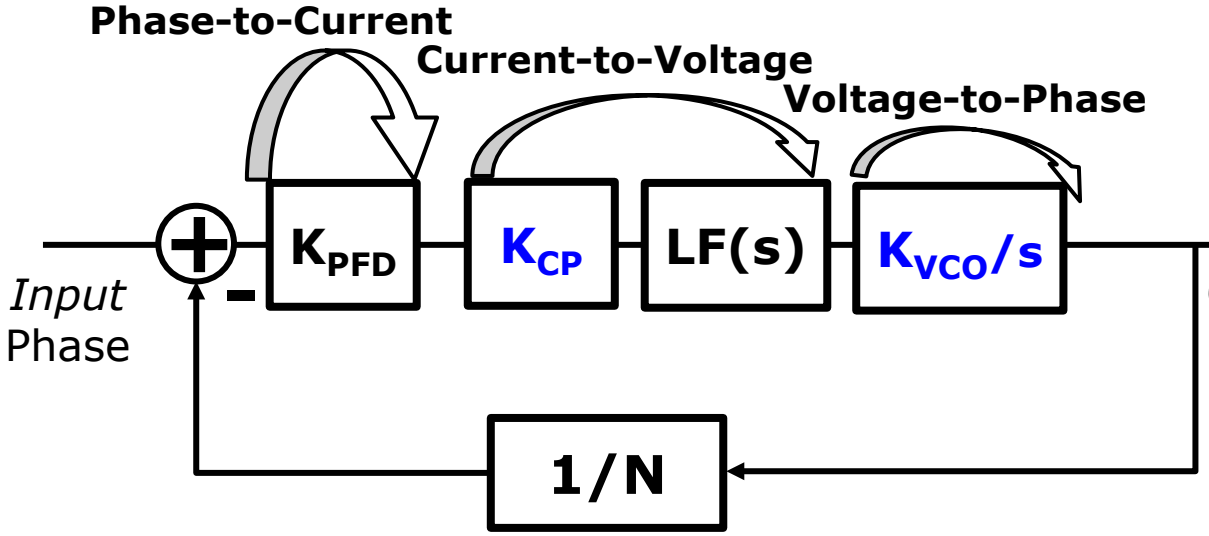
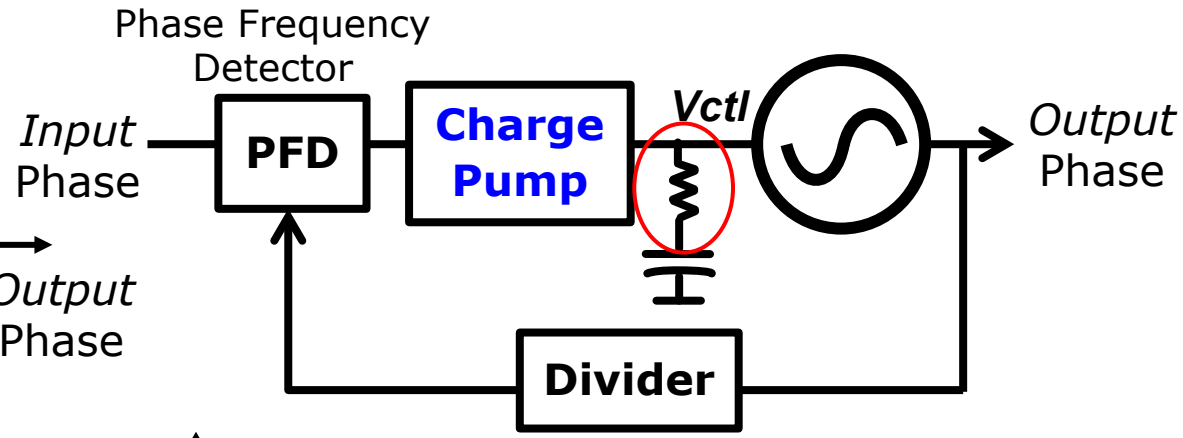
Type-II Analog PLL

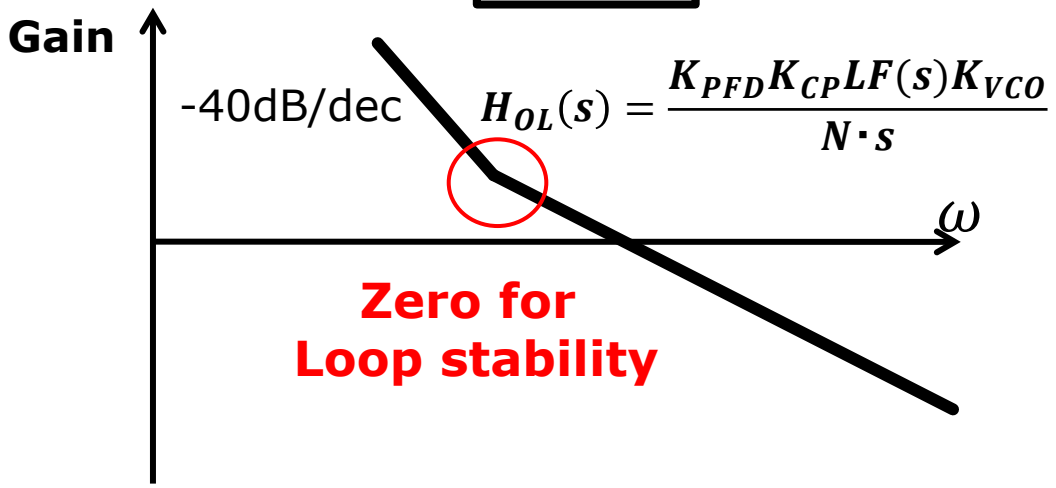
- Type-II PLL has additional integrator of charge pump and loop filter





$$\frac{Output}{Input} = \frac{1}{1/H_{OL}(s) + 1/N} \fallingdotseq N$$

$H_{OL}(s)$ >>1 N: Divider Ratio



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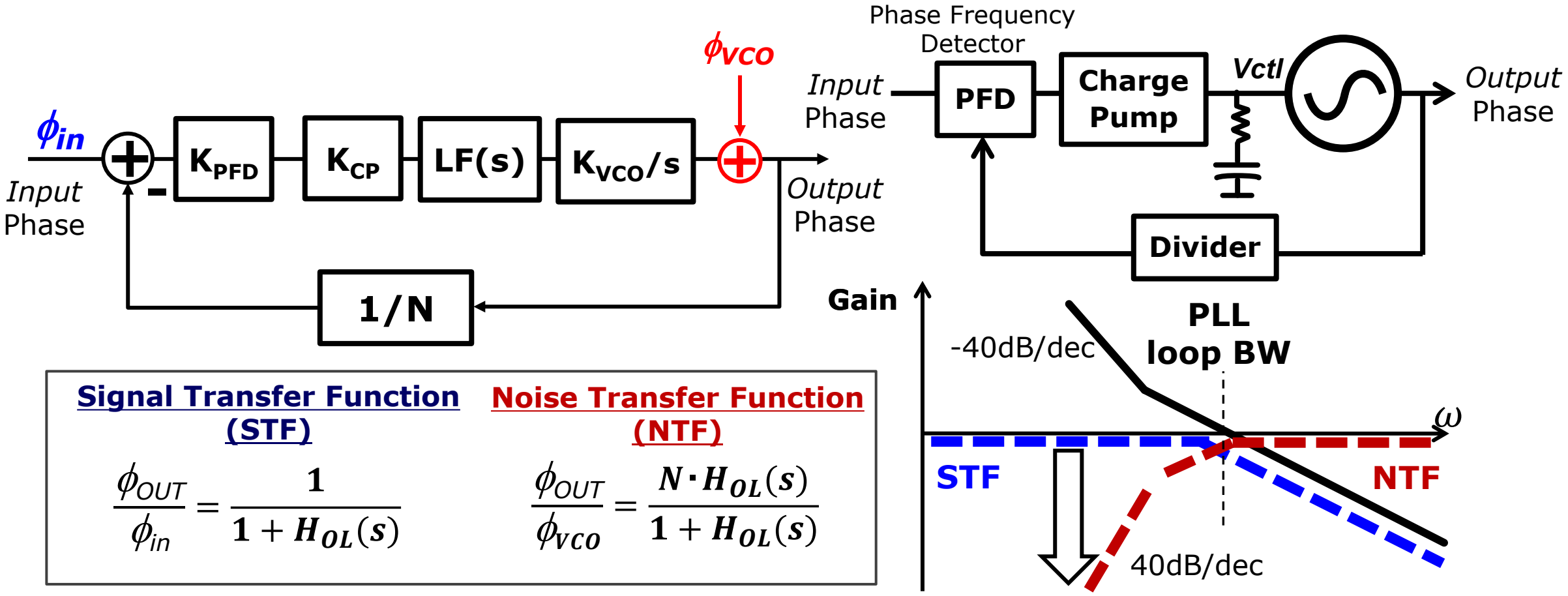
Type-II Analog PLL

- Type-II PLL suppresses VCO phase noise by 2nd-order HPF



Signal Transfer Function (STF)

$$\frac{\phi_{OUT}}{\phi_{in}} = \frac{1}{1 + H_{OL}(s)}$$

Noise Transfer Function (NTF)

$$\frac{\phi_{OUT}}{\phi_{VCO}} = \frac{N \cdot H_{OL}(s)}{1 + H_{OL}(s)}$$

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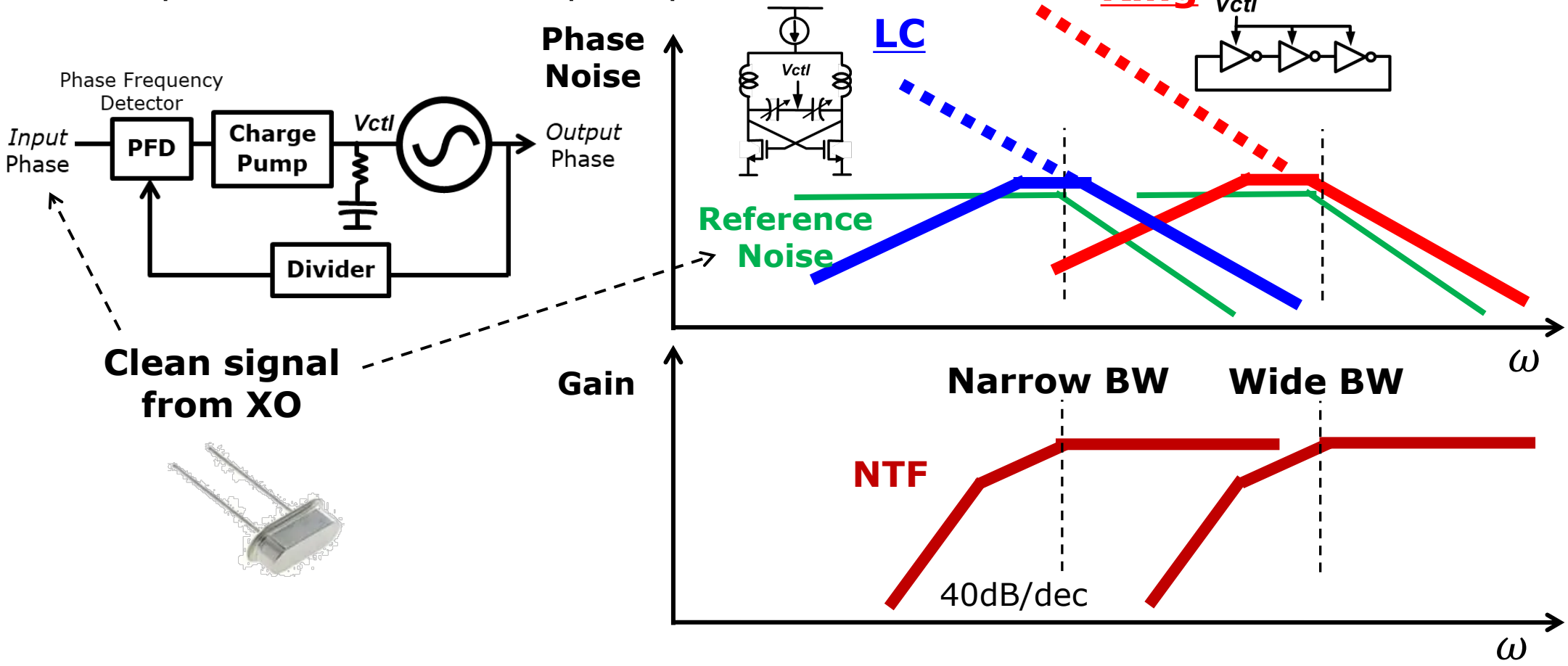
Loop BW Design Consideration (1/3)

- Wide loop BW is effective for poor phase-noise VCO



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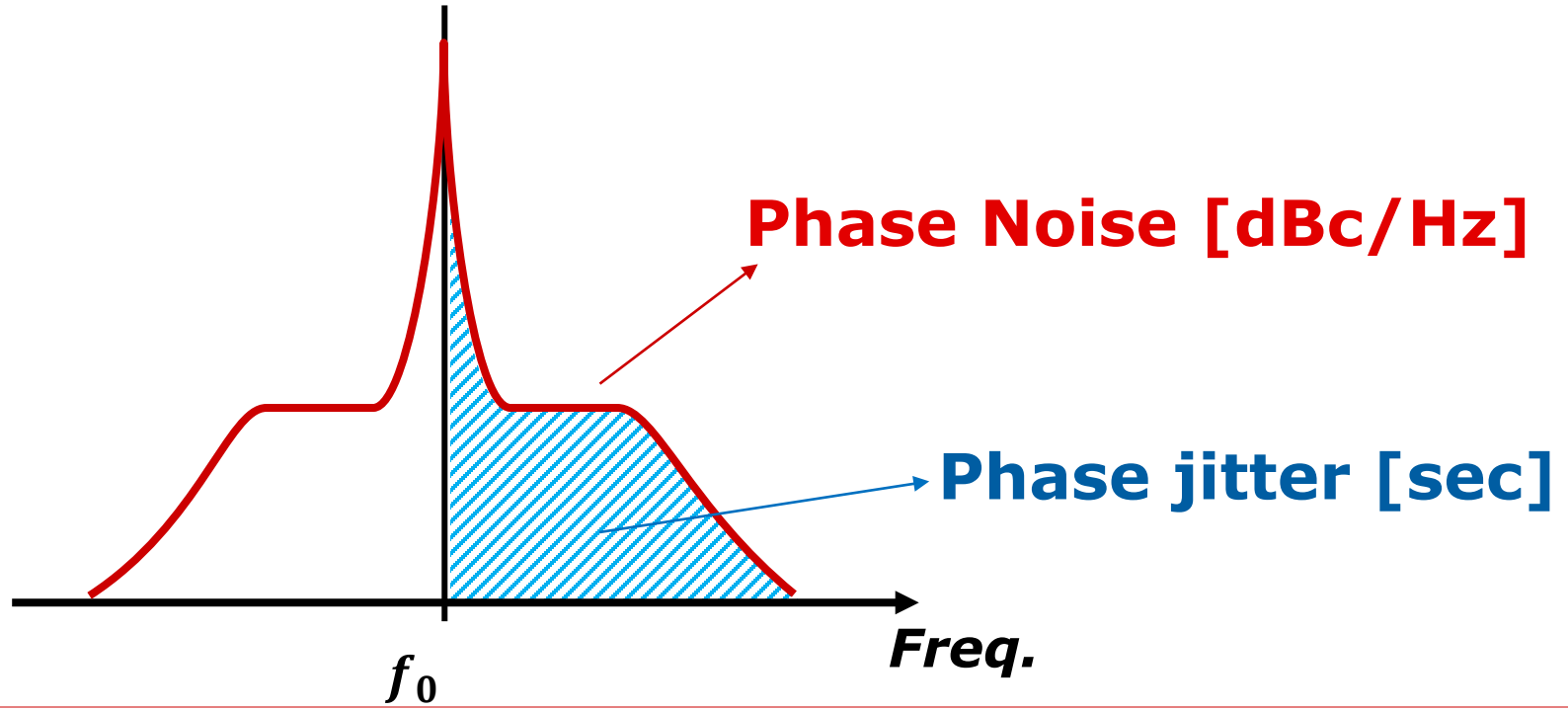
PLL Jitter Figure-of-Merit(FoM)

- Definition

$$FoM_{jitter} = 10\log_{10}\left[\left(\frac{\text{RMS jitter}}{1\text{sec}}\right)^2\left(\frac{\text{Power}}{1\text{mW}}\right)\right] \quad [\text{dB}]$$



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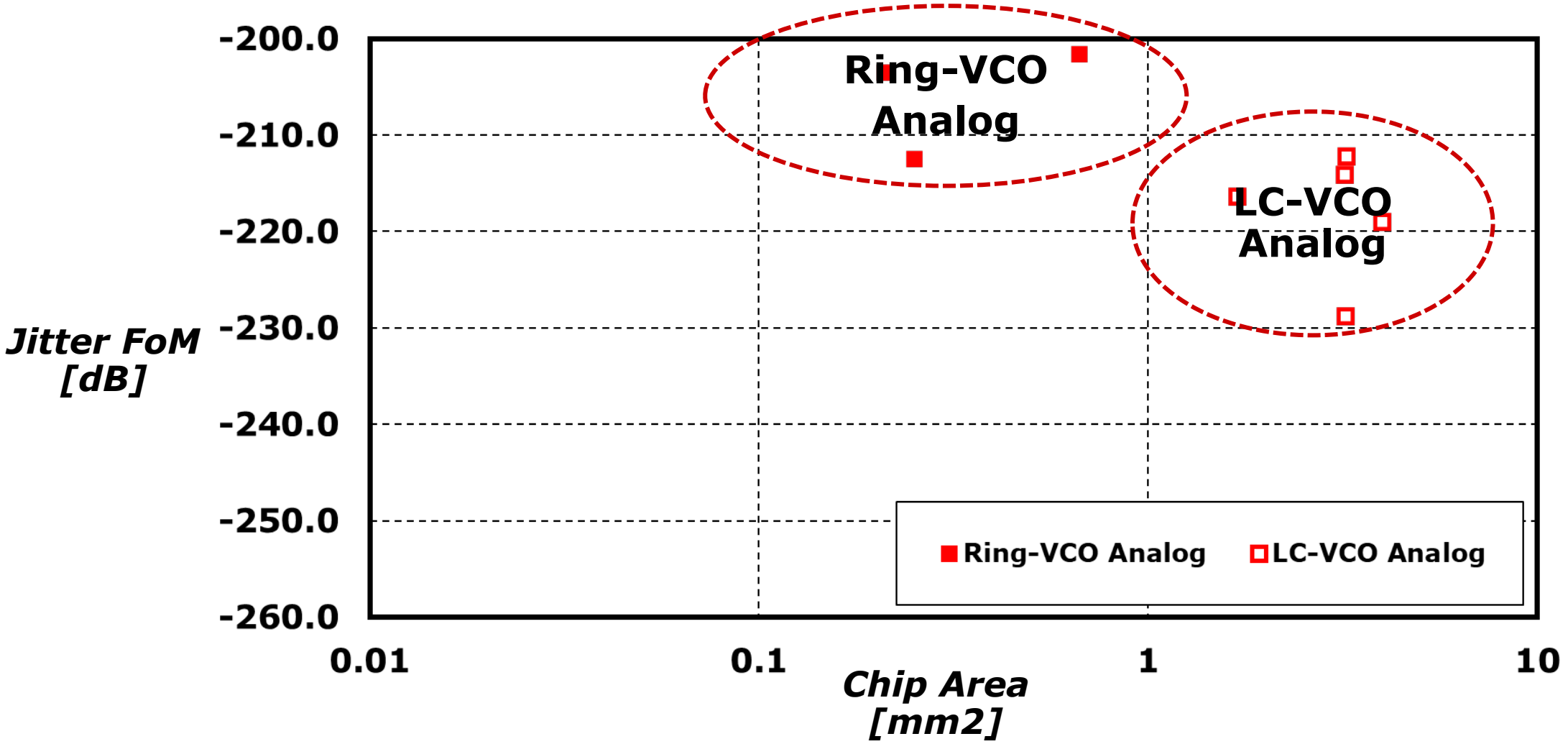
PLL Performance Trend(~2005)



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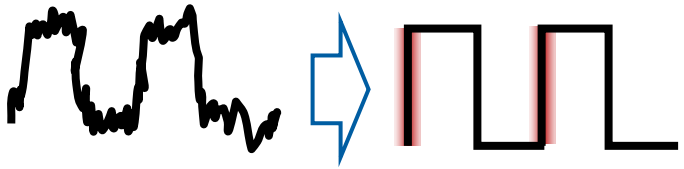
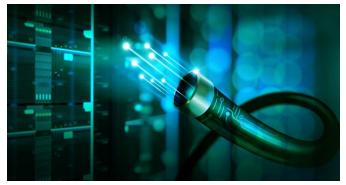
Loop BW Design Consideration (2/3)

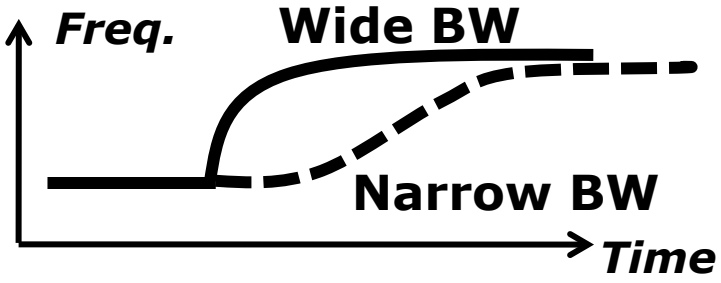
Clock Data Recovery

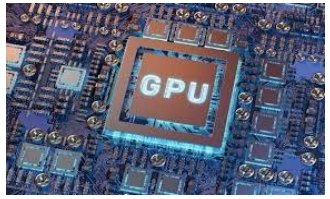
Noisy Reference

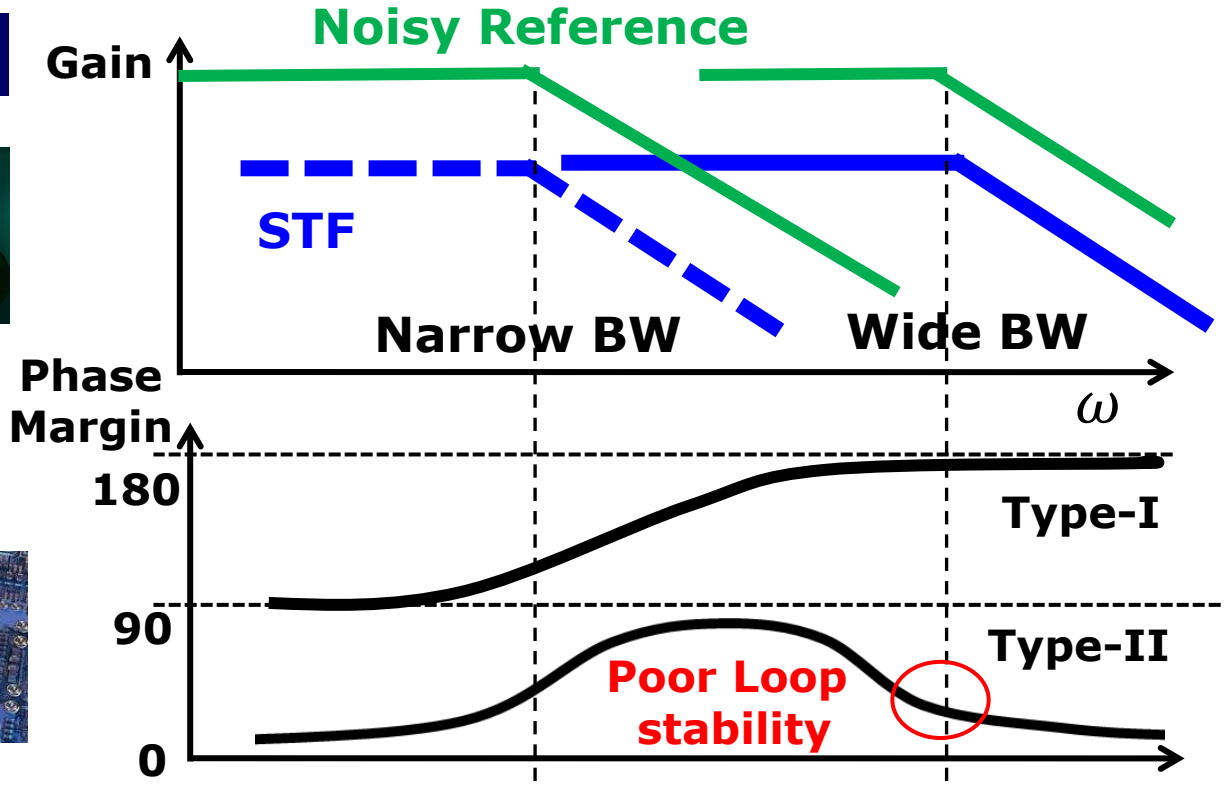




Dynamic Voltage and Frequency Scaling







- Narrow-loop-BW PLL can behave as noise filter for dirty input signal
- Lock-up responsivity is proportional to loop BW
  - Type-I has better stability than that of type-II PLL

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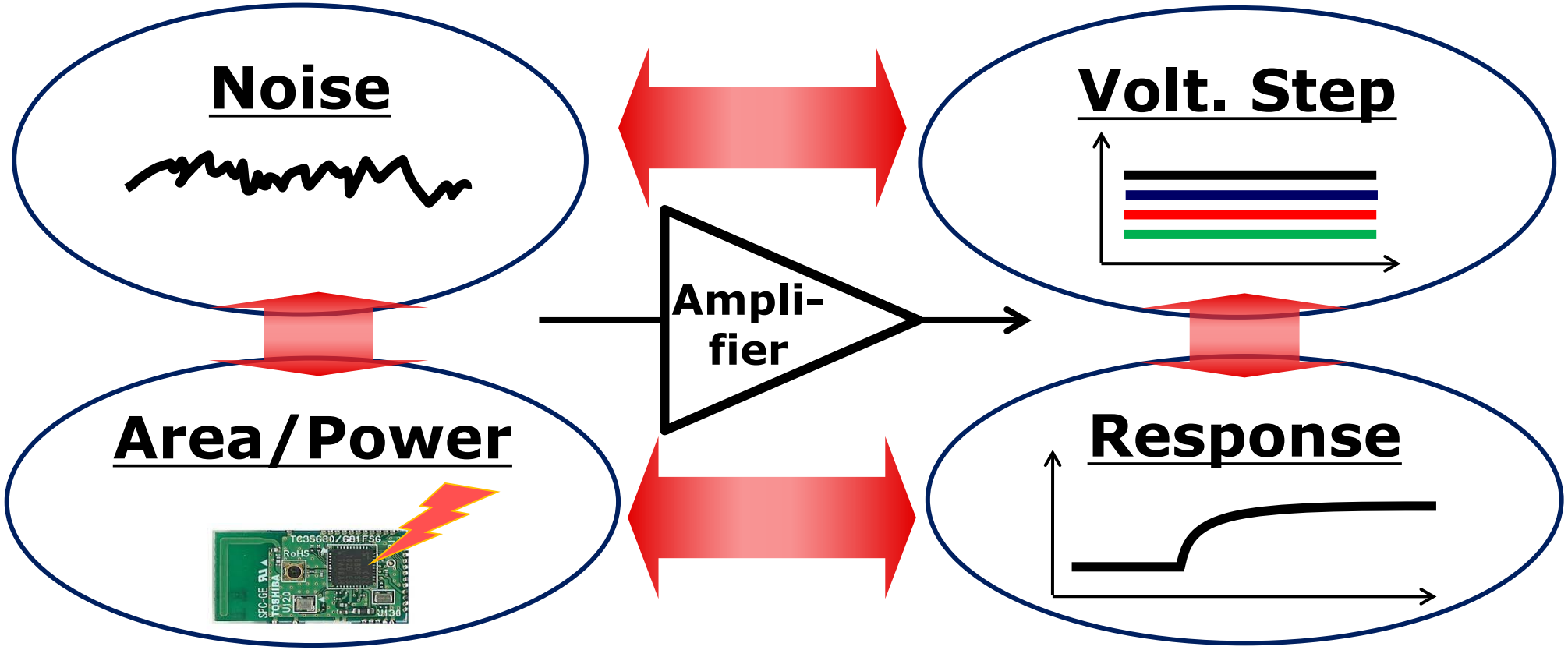
Amplifier Design Trade-off

- Key factors are **feedforward gain, gain BW, feedback factor.**



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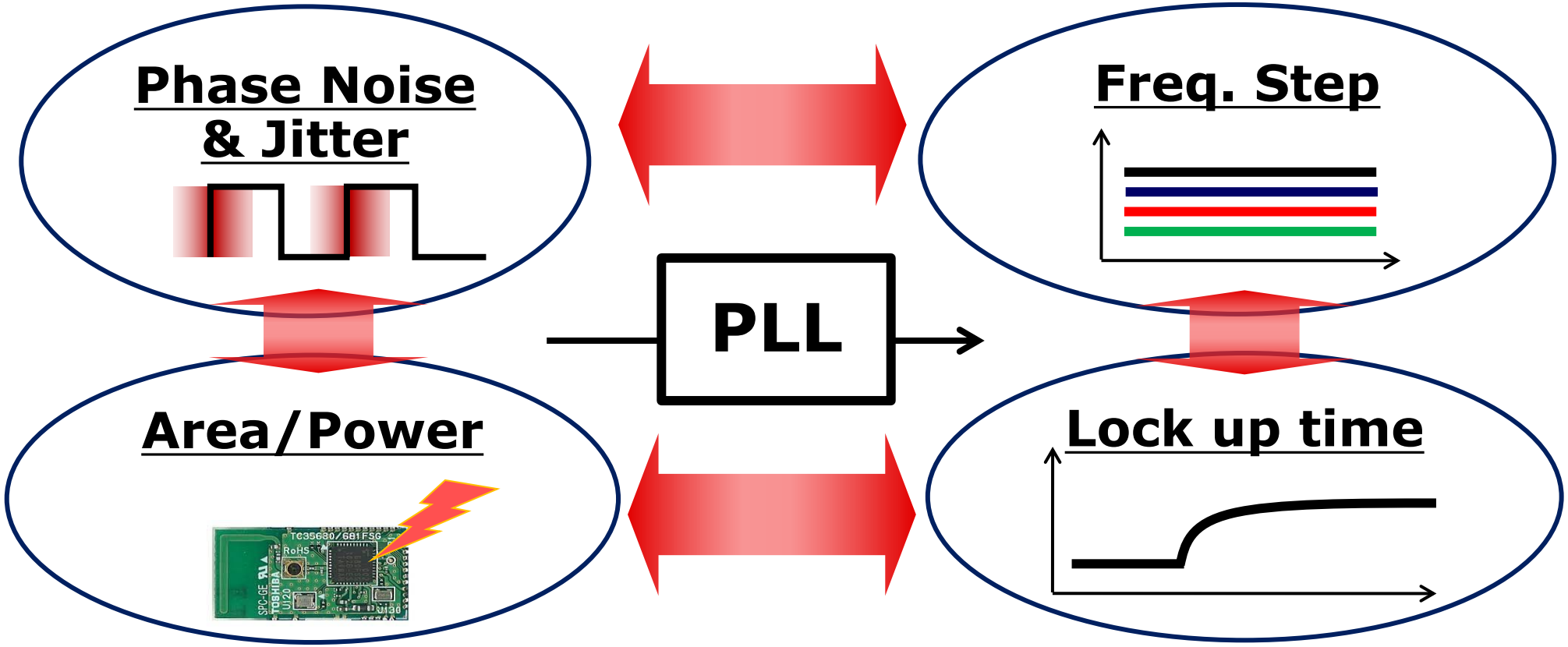
PLL Design Trade-off

- Key factors are **loop gain & BW, Type-I/II & VCO selection.**



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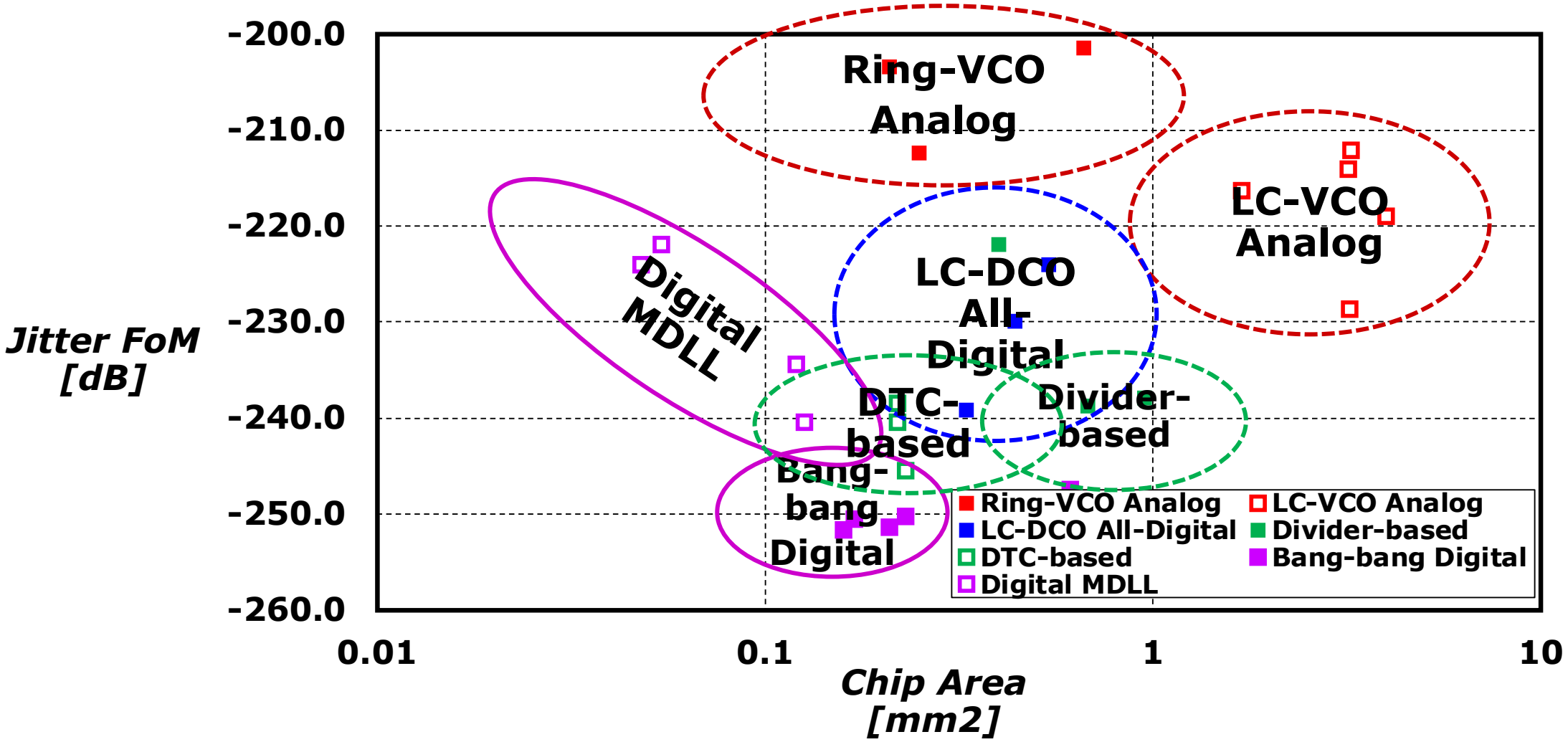
PLL Performance Trend(~2022)



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  - Design Challenges for Jitter, Phase noise, Lock up
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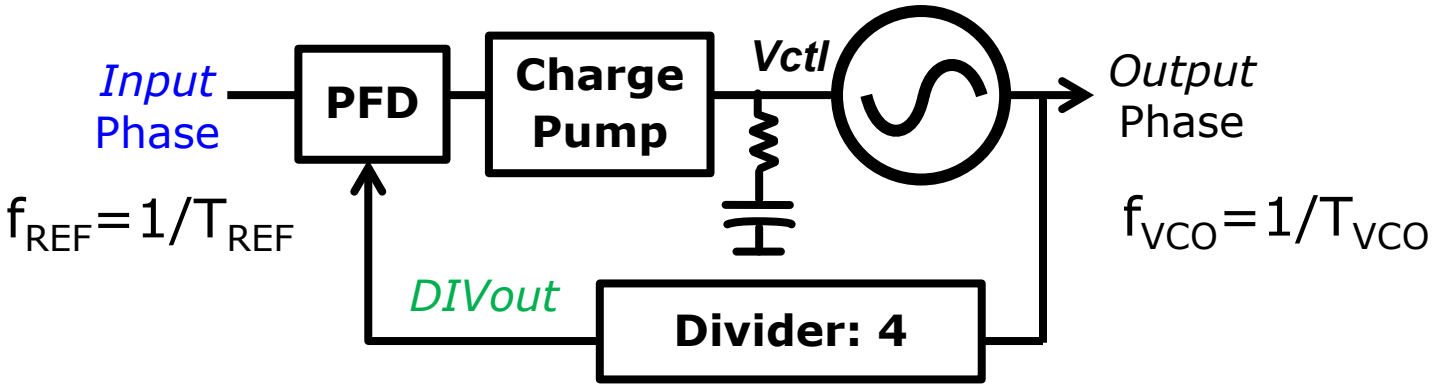
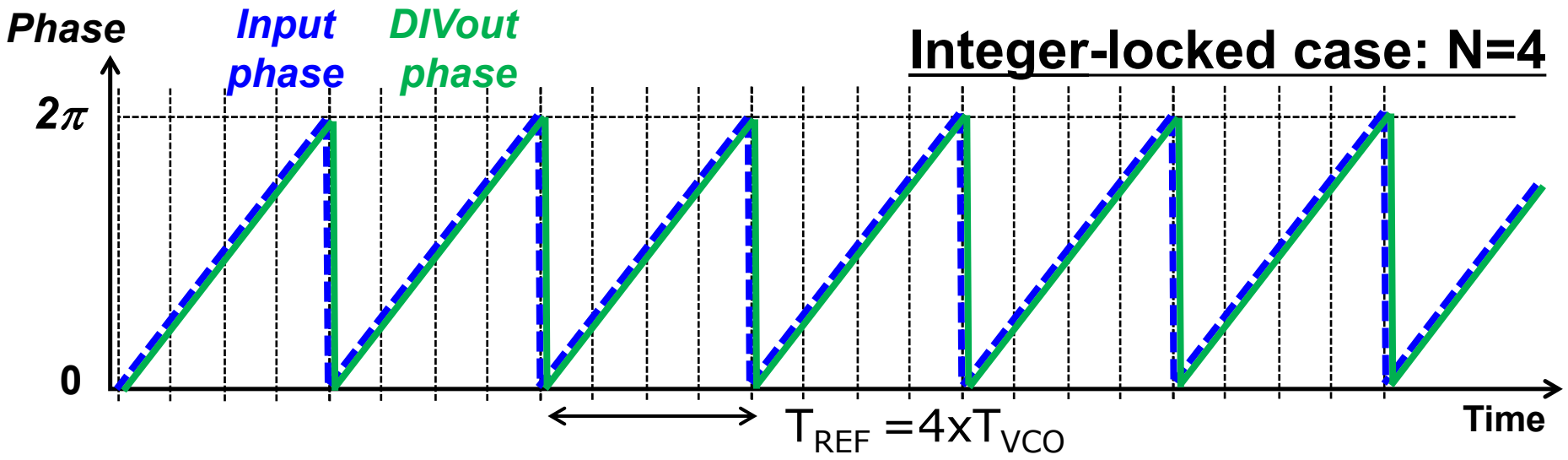
Integer-N vs Fractional-N Operation (1/2)





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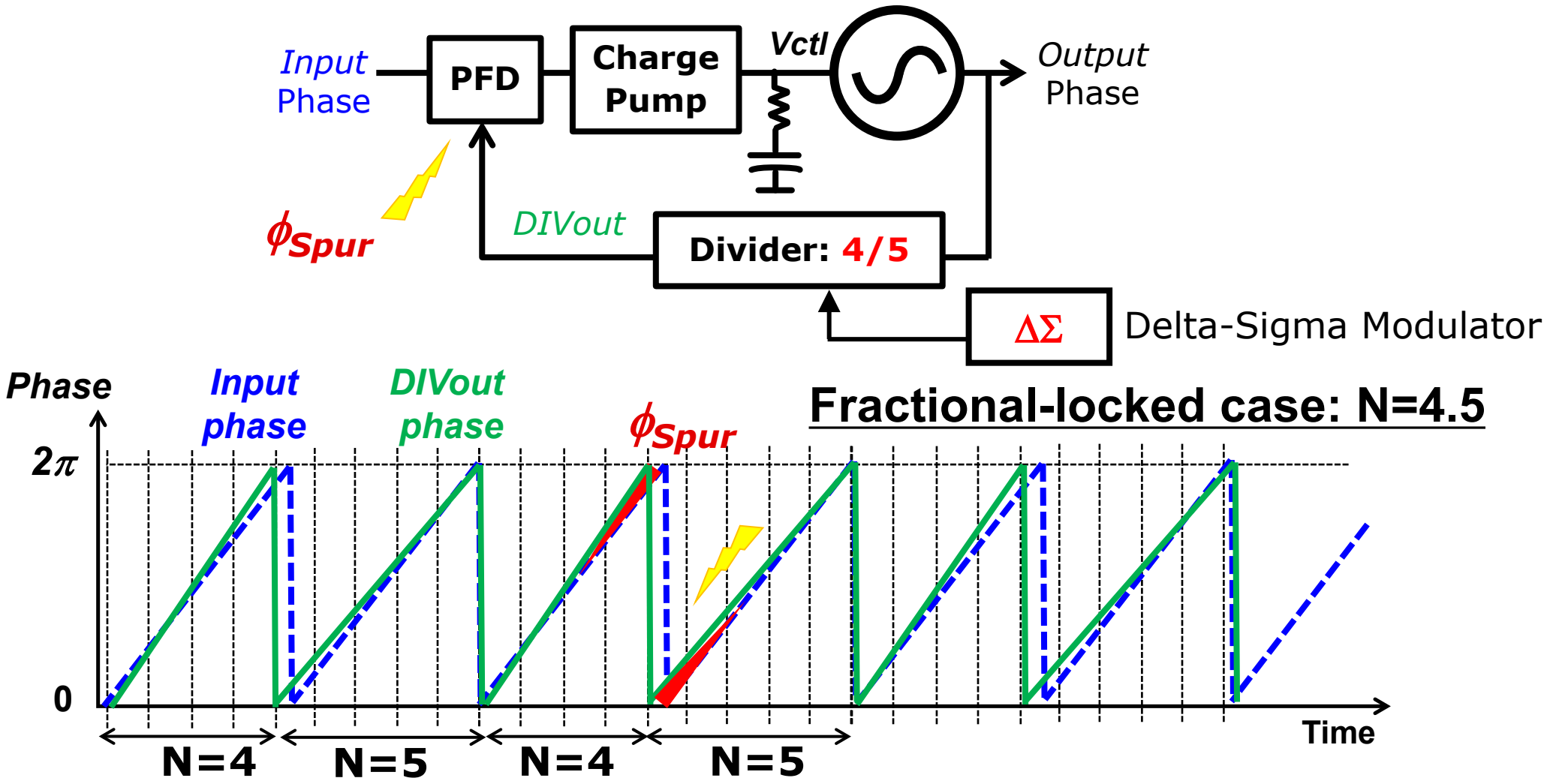
Integer-N vs Fractional-N Operation (2/2)



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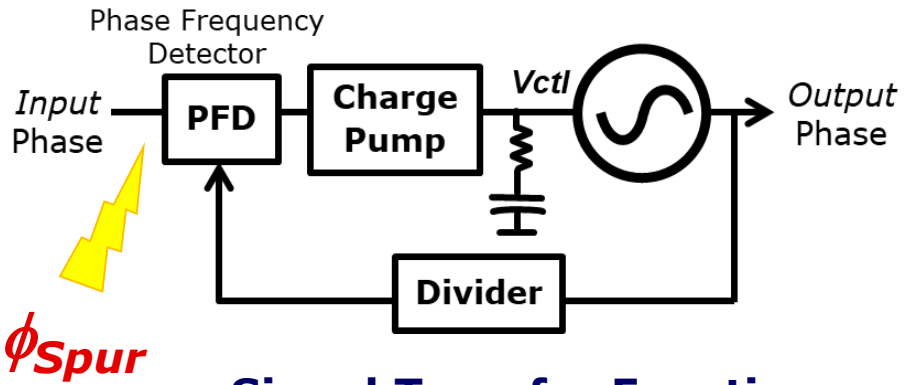
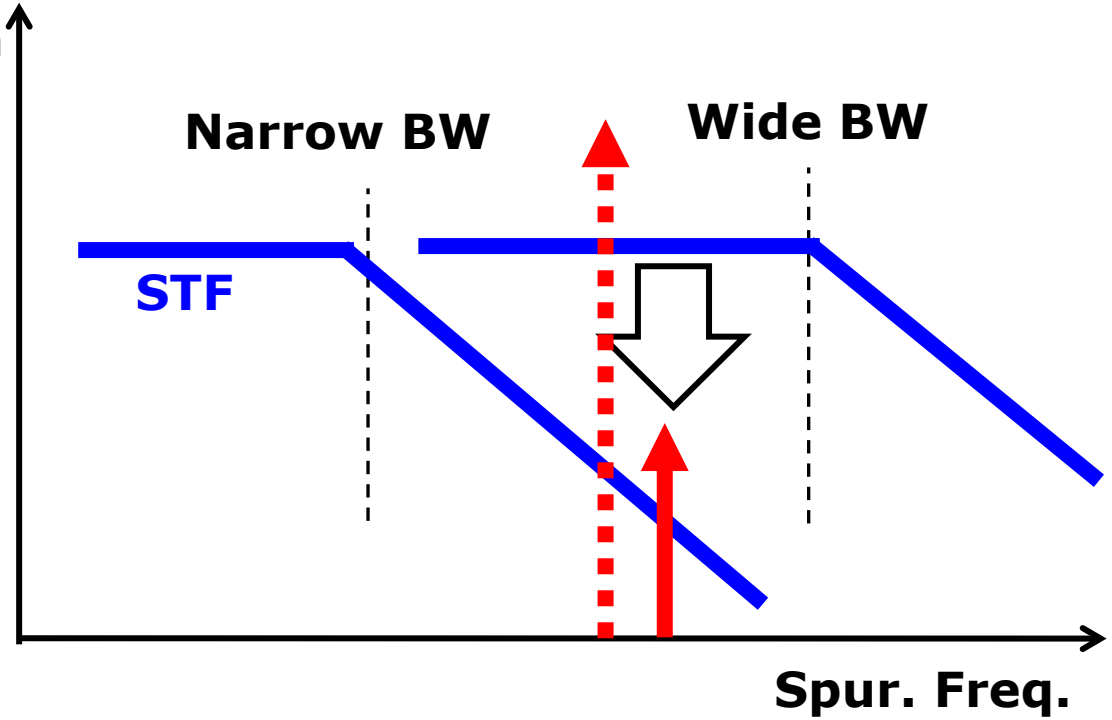
Loop BW Design Consideration (3/3)

- Narrow loop BW is effective for fractional spurs
  - However, **around 10kHz-cut-off analog filter is required,** if spur frequency and attenation are 100kHz and 20dB, respectively



Signal Transfer Function (STF)

$$\frac{\phi_{OUT}}{\phi_{in}} = \frac{1}{1 + H_{OL}(s)}$$



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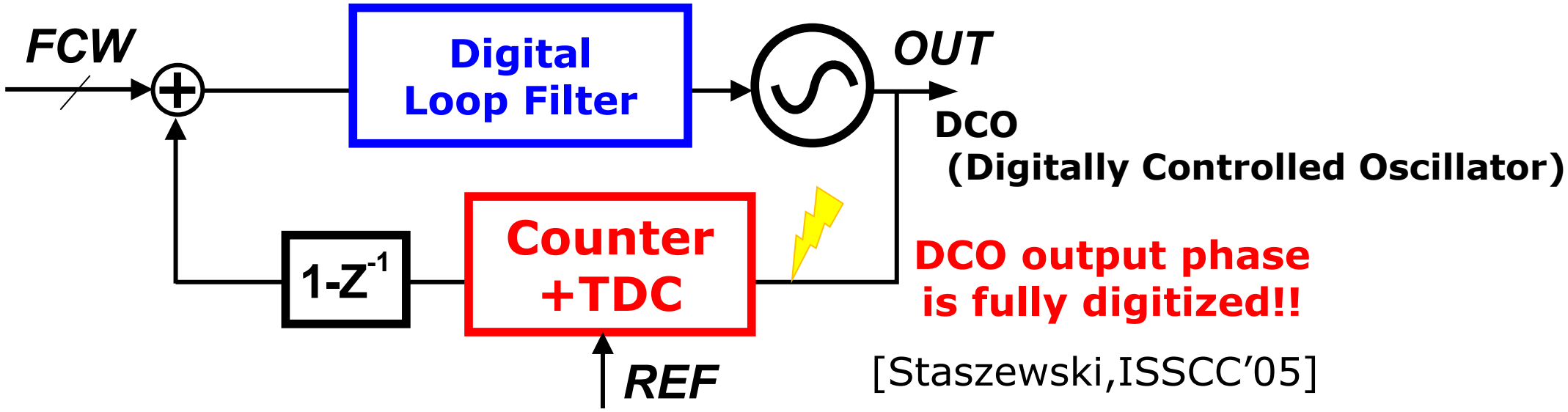
Innovation: All-Digital PLL



- **Free from Analog-filter and Divider**
- **Great benefit from CMOS scalability**
  - Chip-area and Power shrinking, Low development cost
  - Robustness to PVT variation

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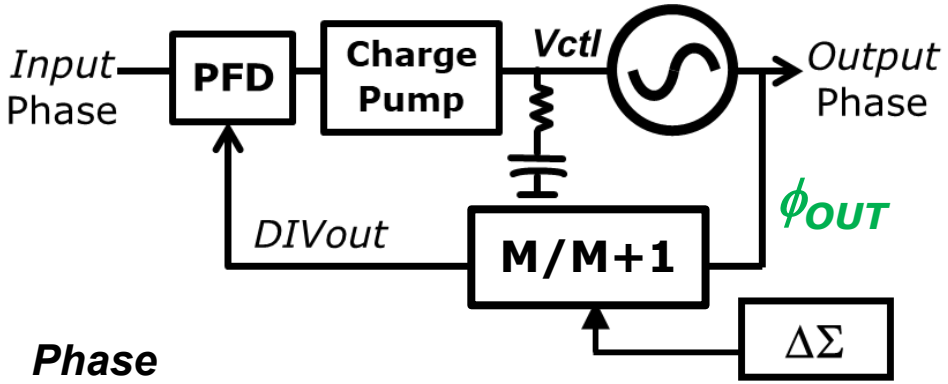
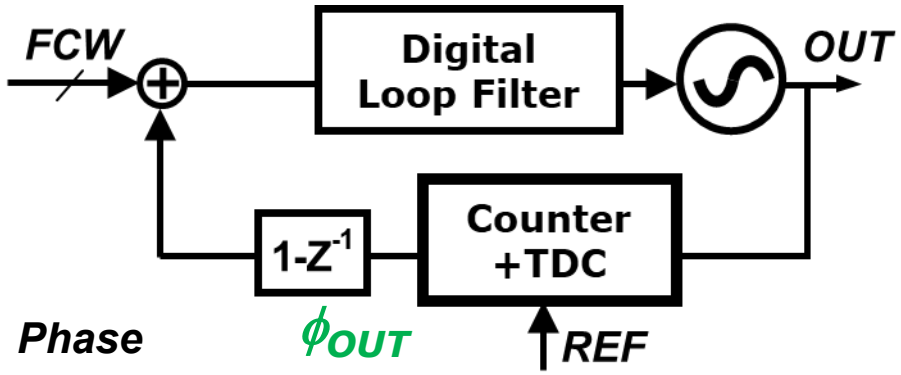
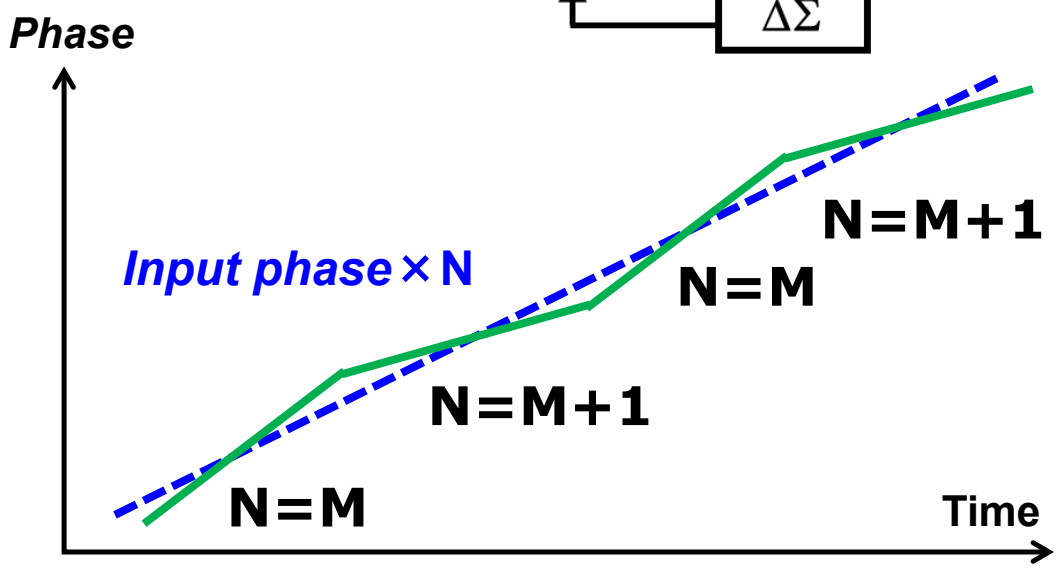
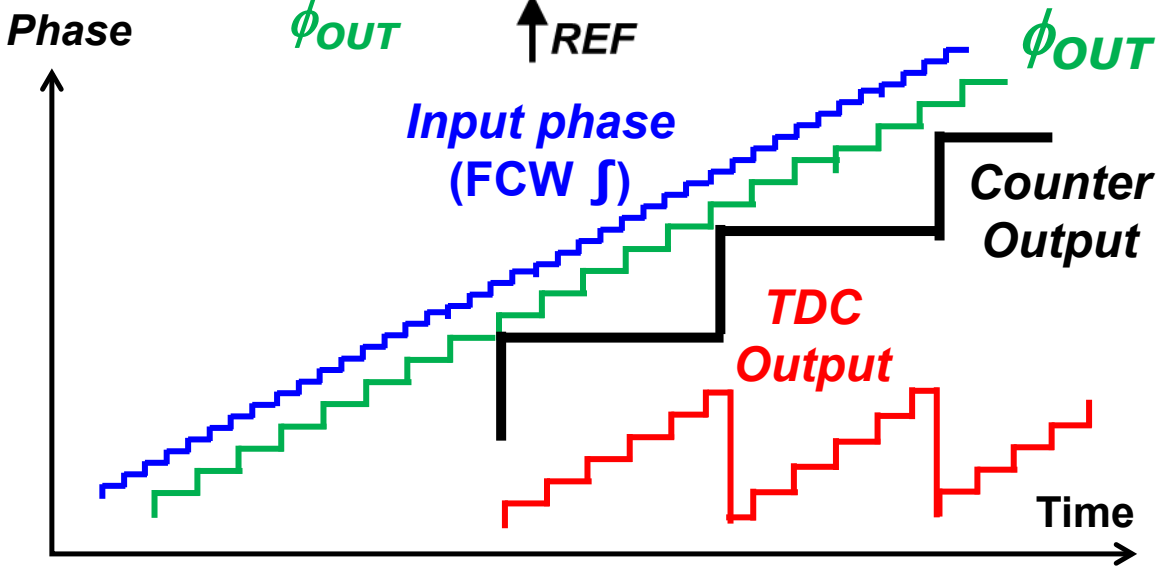
All-Digital PLL: Operation

- DCO phase quantization of TDC much mitigates spur periodicity









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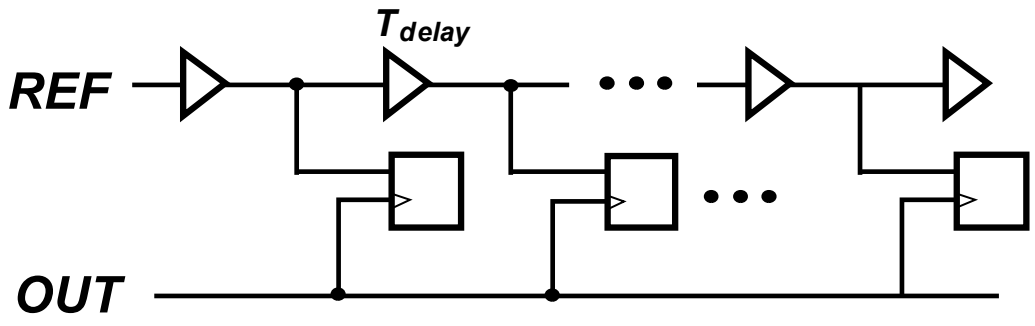
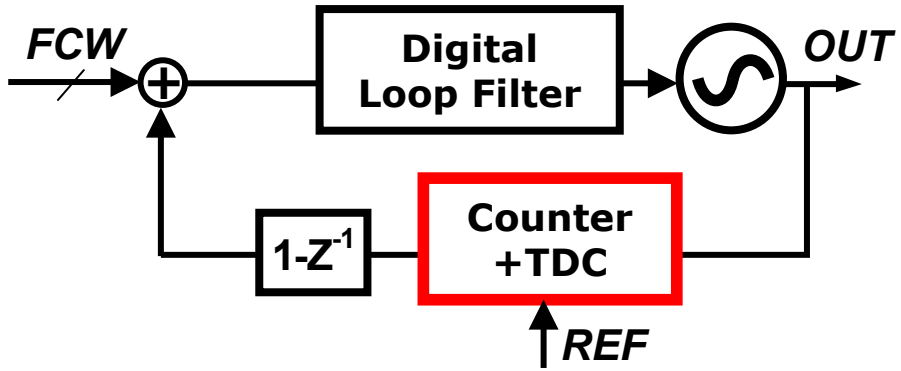
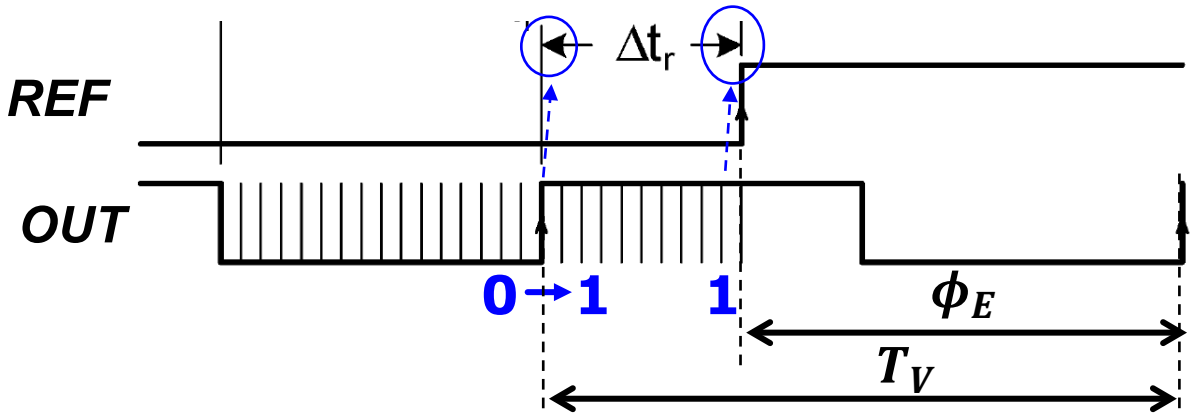
All-Digital PLL: TDC Operation (1/3)







$$\phi_E = 1 - \Delta t_r / T_V$$

Δt_r : REF and DCO time difference
T_V : DCO Period

- TDC quantizes Φ_E using inverter delay, T_{delay}, as LSB(Least Significant Bit)
- Φ_E is calculated from DCO Rise/Fall transition data sampled by delayed REF

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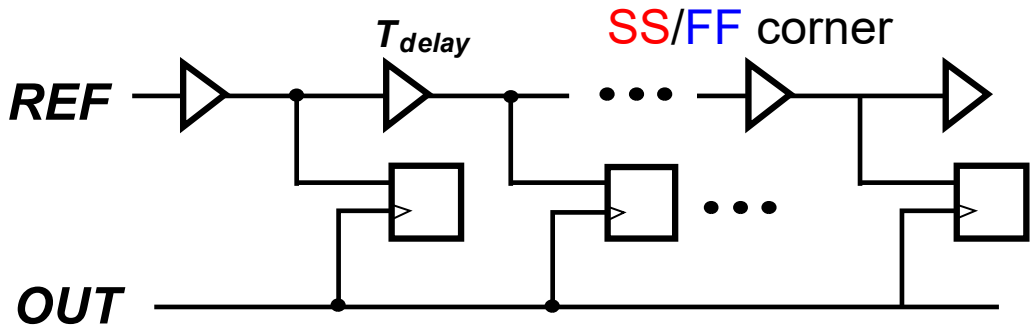
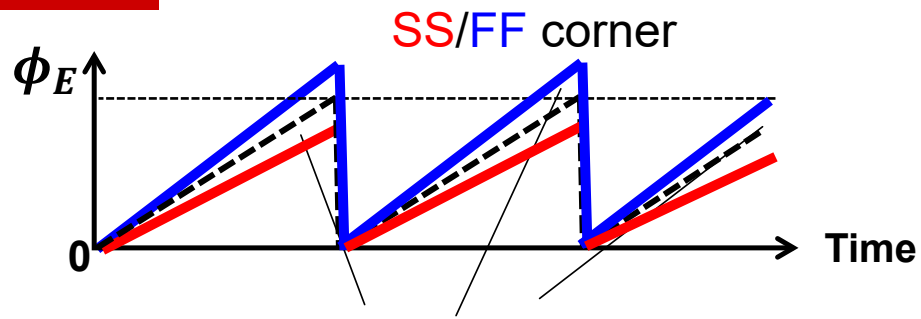
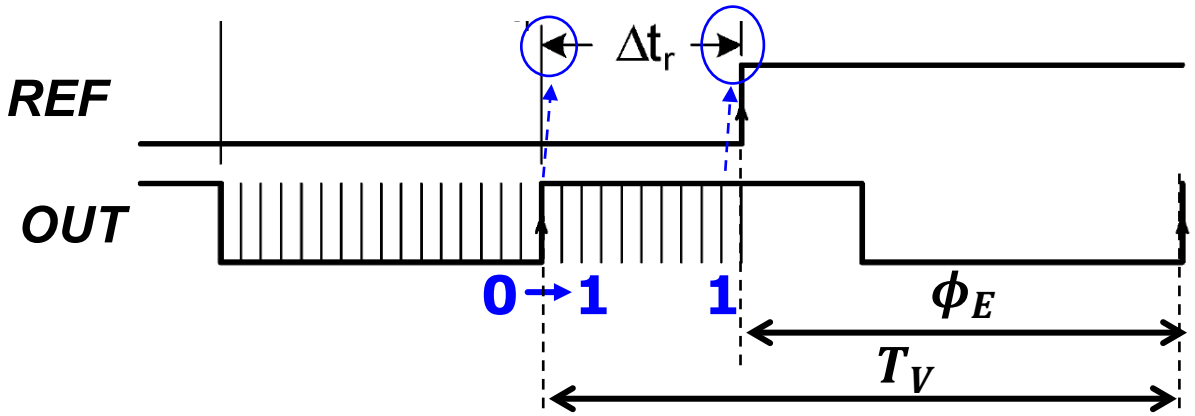
All-Digital PLL: TDC Operation (2/3)





Full-Scale Error



Larger fractional spur & jitter

$$\phi_E = 1 - \Delta t_r / T_{V(Fix)}$$

Δt_r : REF and DCO time difference
$T_{V(Fix)}$: Estimated DCO Period

- PVT variation of inverter delay causes significant Full-Scale(FS) Error

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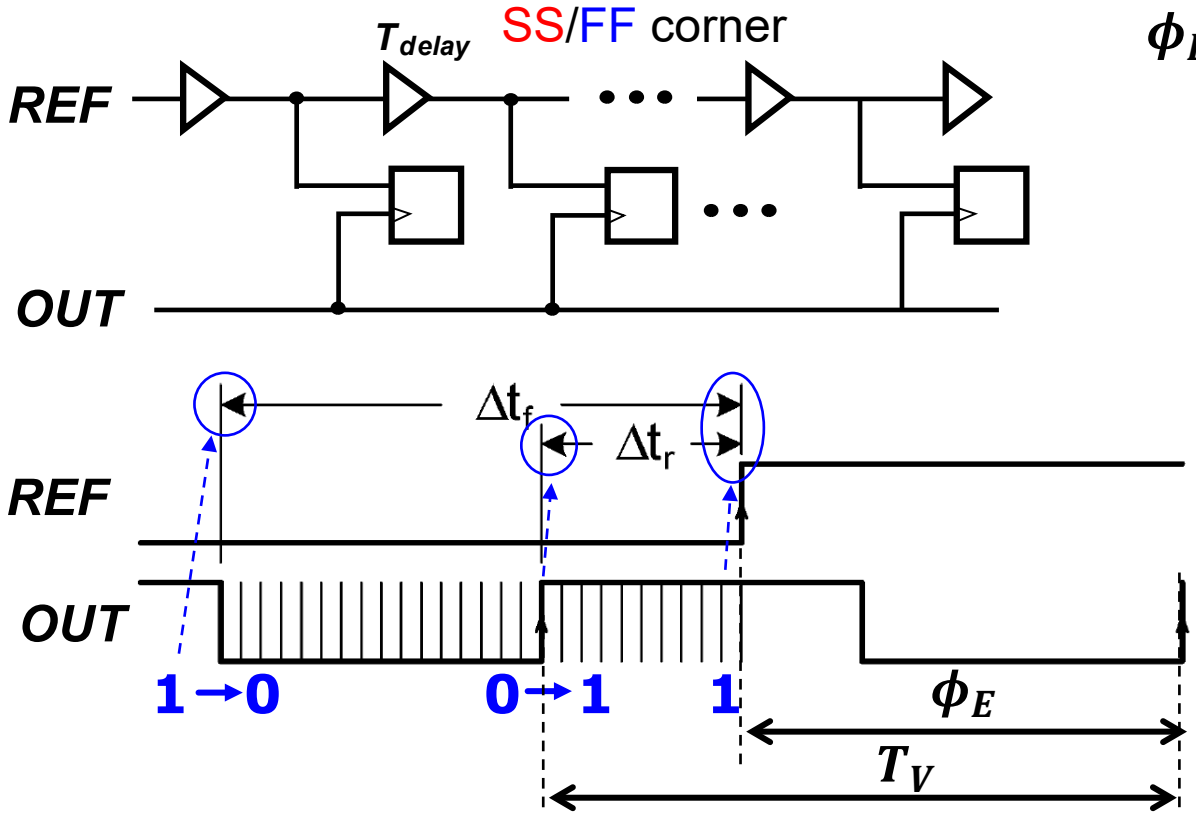
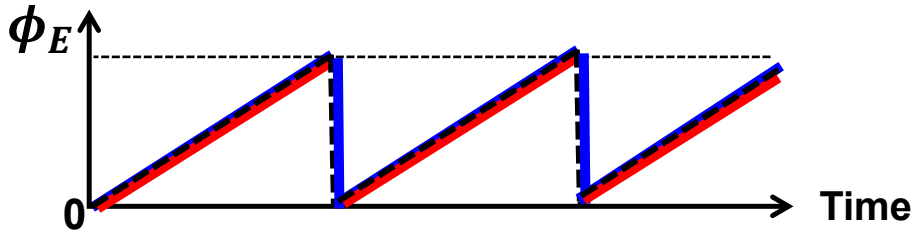
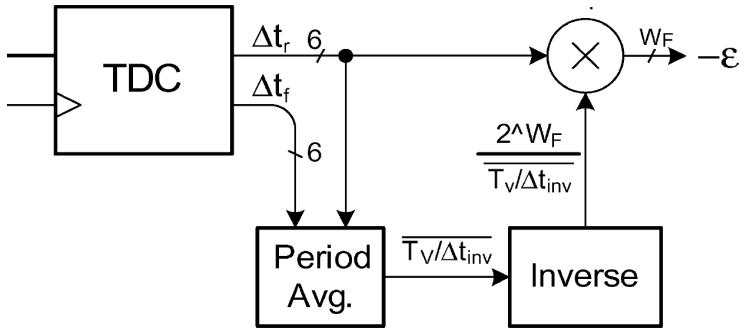
All-Digital PLL: TDC Operation (3/3)







$$\phi_E = 1 - \Delta t_r / T_{V(Actual)}$$

$$T_{V(Actual)} = \overline{2(\Delta t_f - \Delta t_r)}$$

- PVT variation of inverter delay causes significant Full-Scale(FS) Error
- TDC Error normalization using DCO period average circuit fixes the problem

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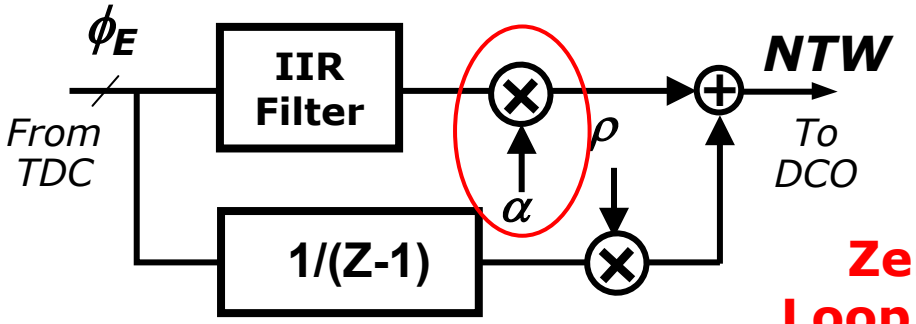
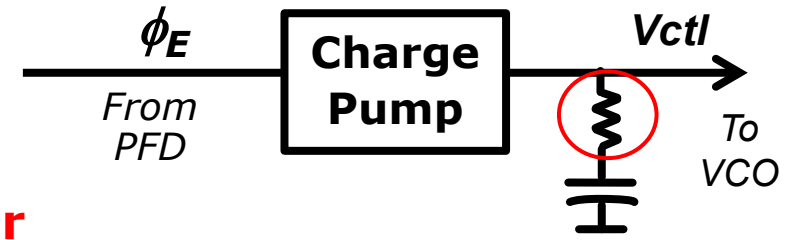
All-Digital PLL: Type-II Digital Filter





Zero for Loop stability

Z-domain → S-domain Model

$$DLF(s) = \frac{\rho f_R + s\alpha IIR(s)}{s}$$

S-domain Model

$$K_{CP}LF(s) = \frac{I_{CP}}{2\pi}\left(\frac{1+sCR}{sC}\right)$$

- **Small Area, Process scalability**
- Software programmed PLL loop: Gentle transition from type-I to type-II

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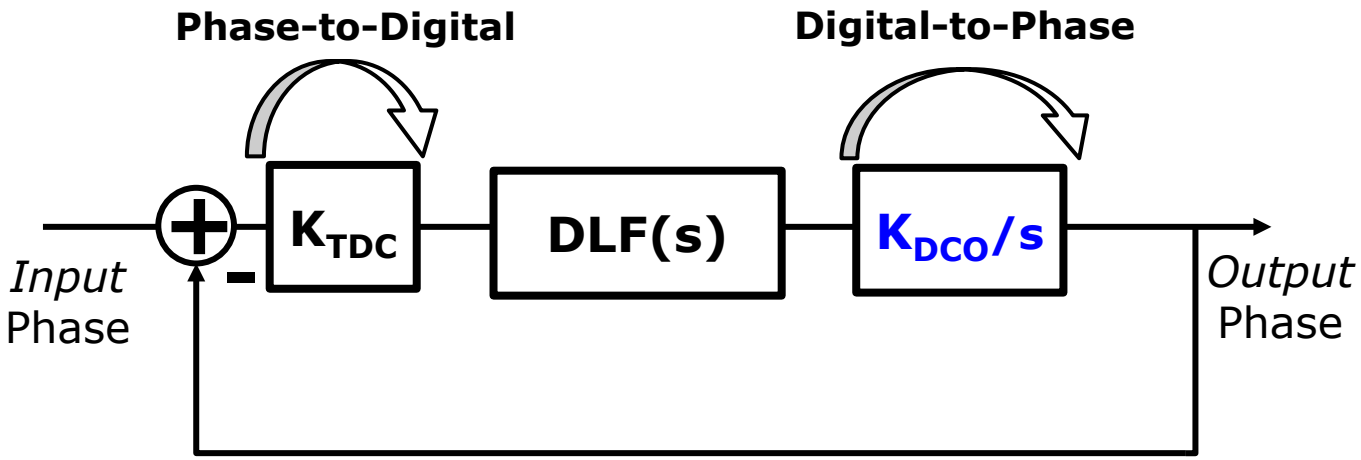
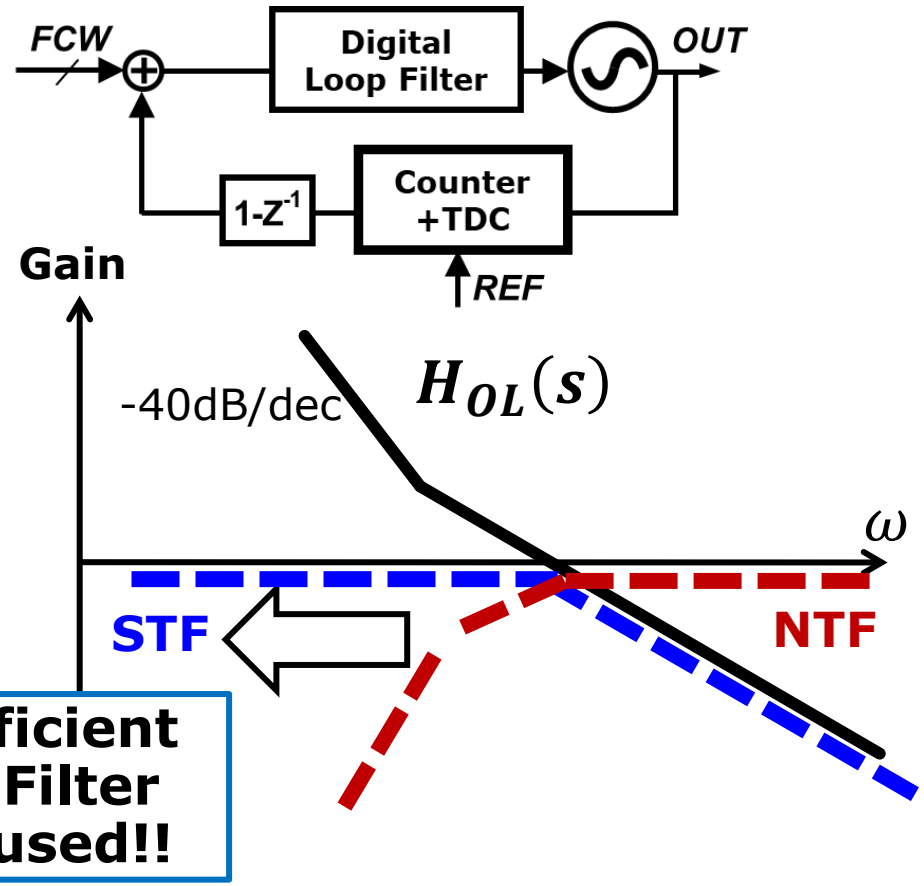
All-Digital PLL: Z to S-domain Model

- All-digital PLL can realize the same STF/NTF as Type-II analog PLL



$$H_{OL}(s) = \frac{\rho f_R^{\,2}}{s} \frac{1 + \frac{s}{\rho f_R/\alpha}}{s} IIR(s)$$



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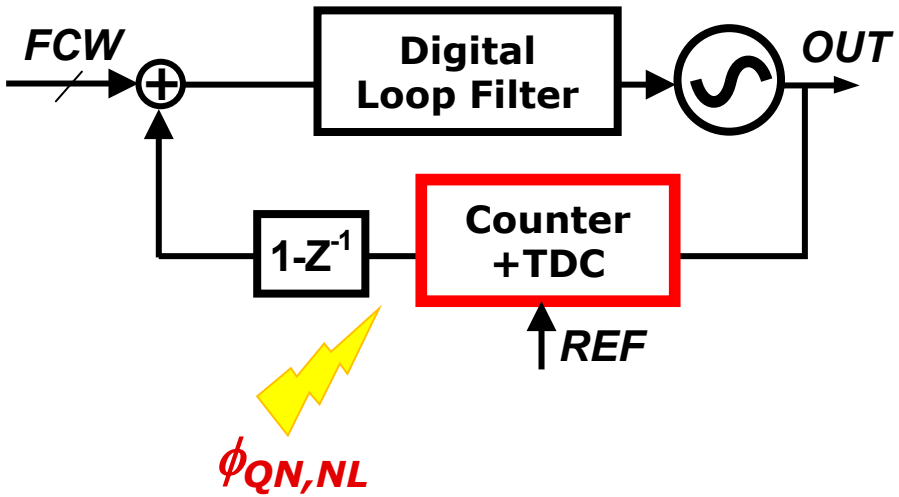
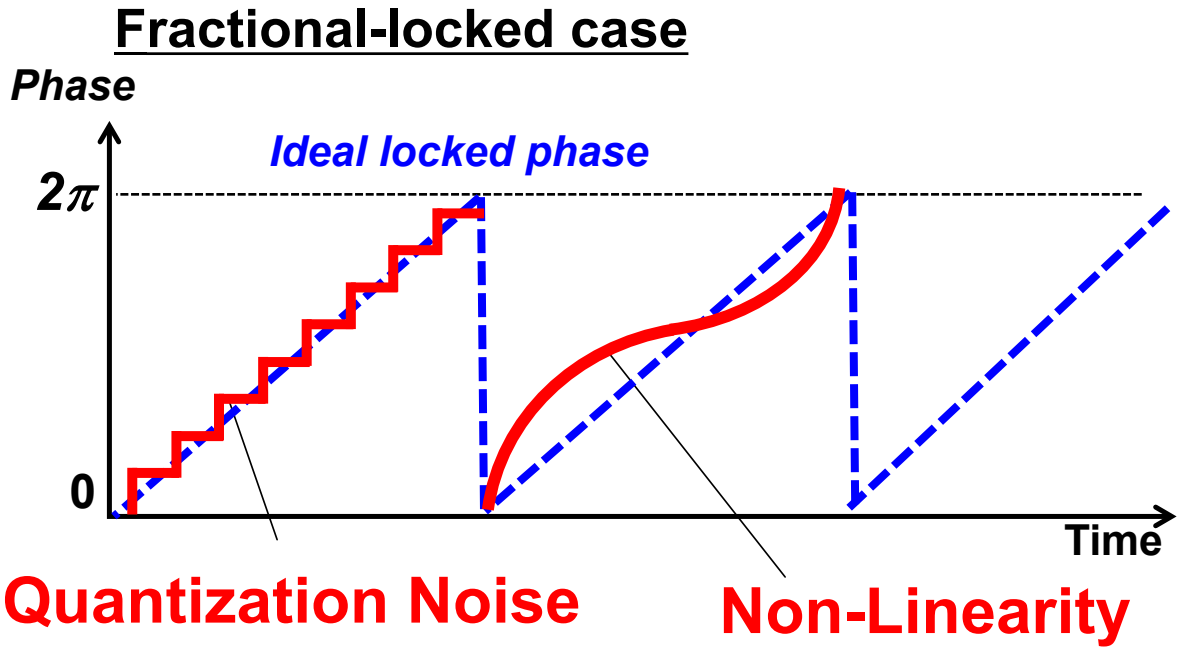
All-Digital PLL: Poor TDC Noise





TDC noise performance critically limits All-Digital PLL

- TDC **Quantization Noise(QN)** and **Non-Linearity(NL)** are converted to spurs or noise concentrated at fractional frequency away from PLL carrier

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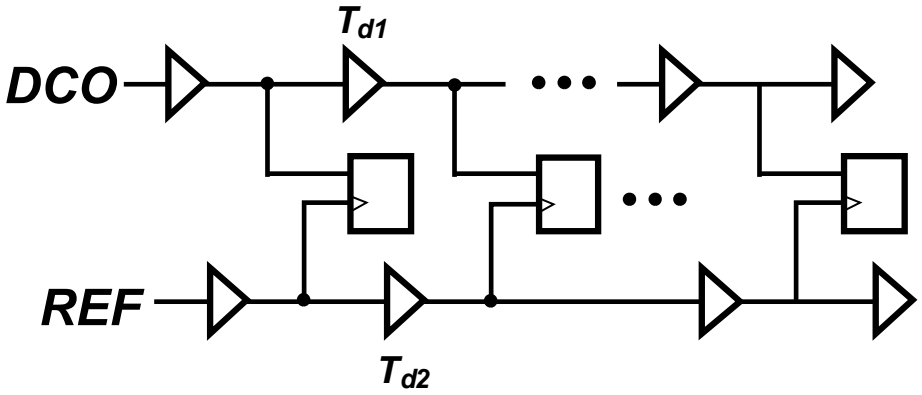
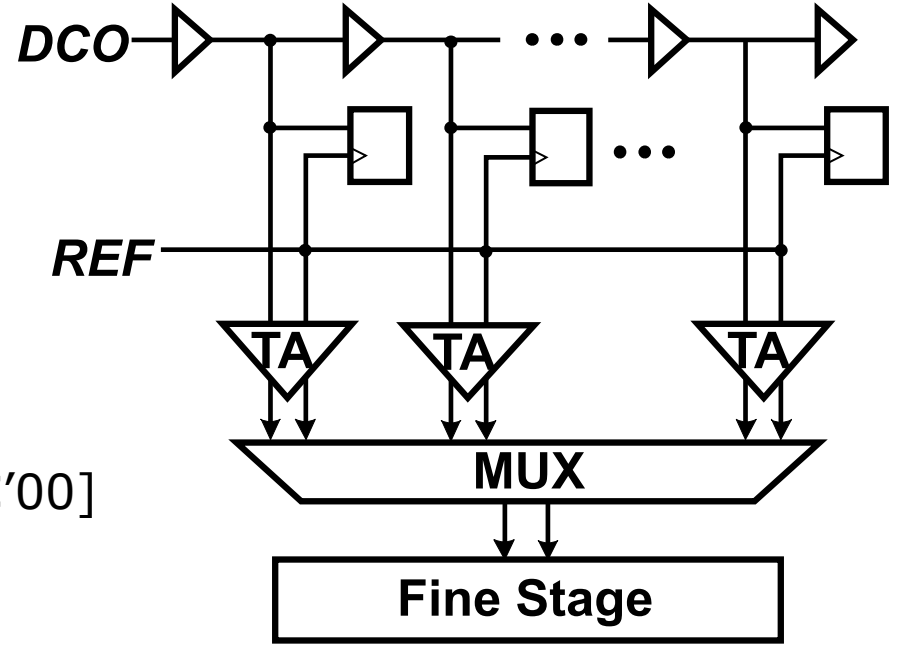
Challenge: High-Resolution TDC



Vernier Delay Line(VDL) [Dudek,JSSC'00]



Time Amp(TA) [Lee,JSSC'09]

- VDL time resolution can be enhanced from Td to |Td1-Td2|
- TA can amplify time difference using meta-stability of latch

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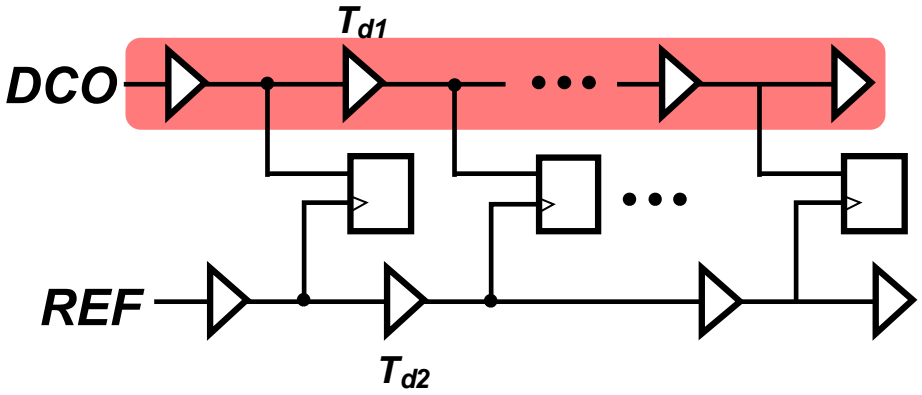
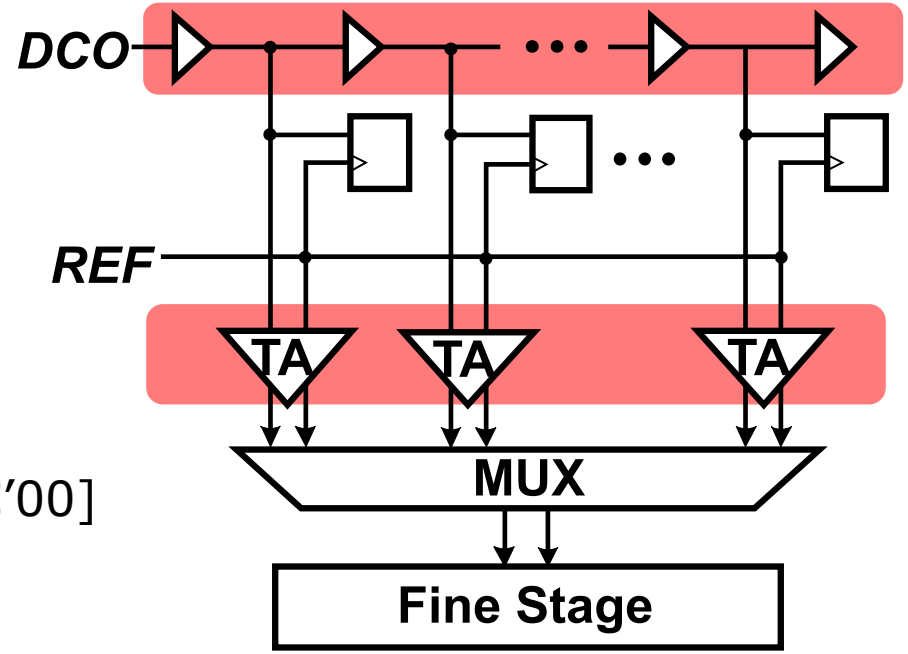
Challenge: High-Resolution TDC



Vernier Delay Line(VDL) [Dudek,JSSC'00]



Time Amp(TA) [Lee,JSSC'09]

Pros: Low QN
Cons: Power hungry

- **However, multiple circuits operated at DCO output speed are needed**

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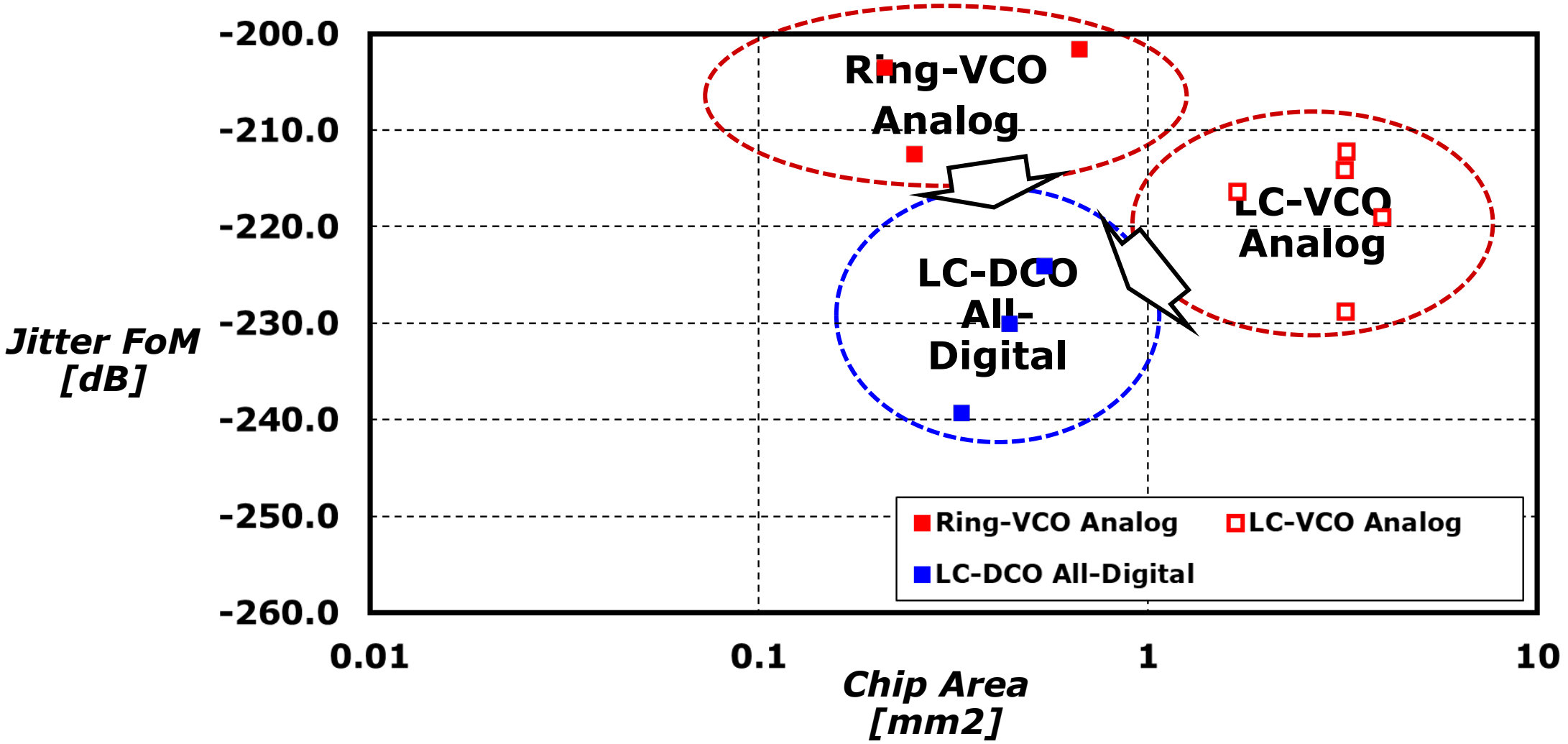
PLL Performance Trend(~2010)



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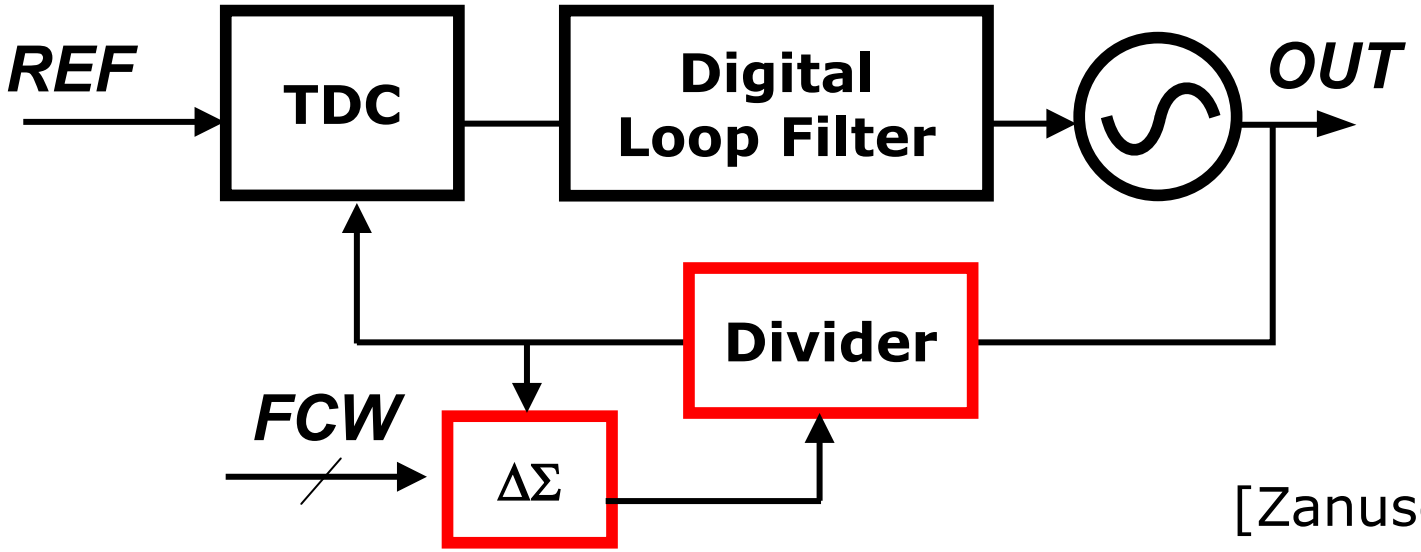
Advanced Digital PLL(Divider-based)



[Zanuso,JSSC'11]

- **Down-speeded DCO output make large benefit for TDC**
- **Great benefit from CMOS scalability is still maintained**
  - Chip-area and Power shrinking, Low development cost
  - Robustness for PVT variation

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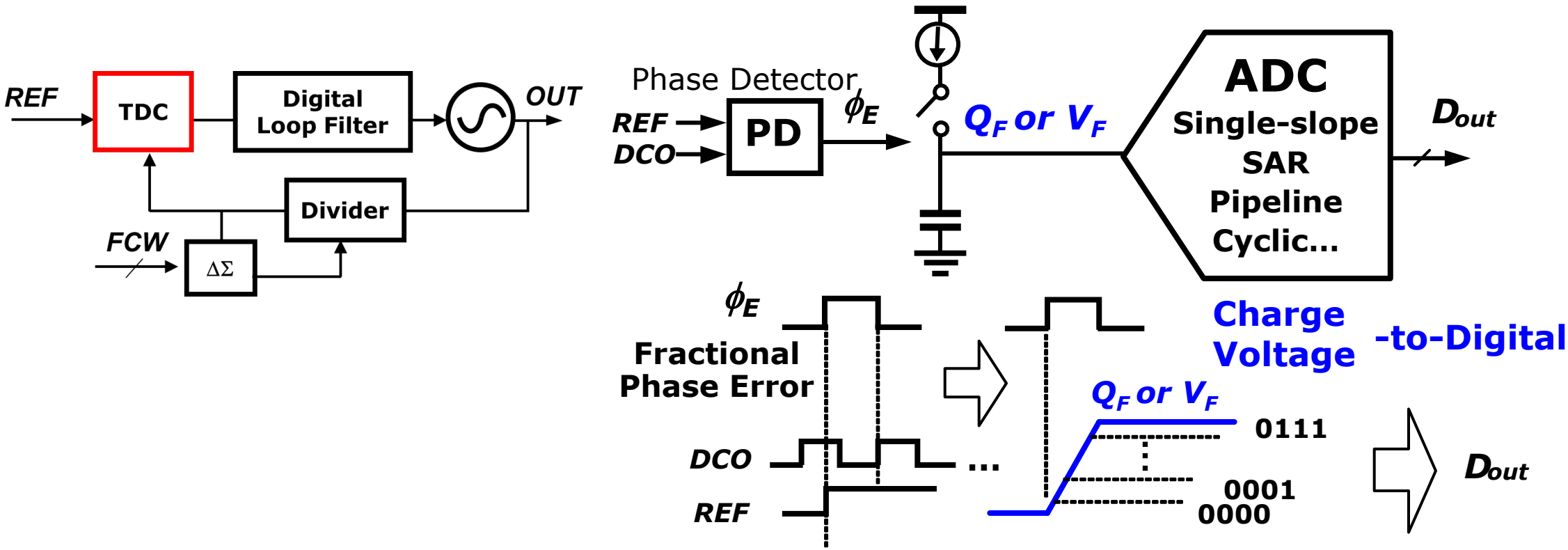
Time Stored TDC

- **Time-Stored type TDC can improve QN and NL by using voltage resolution**
- Once Φ_E is stored as charge/voltage, high digital affinity ADC can be used



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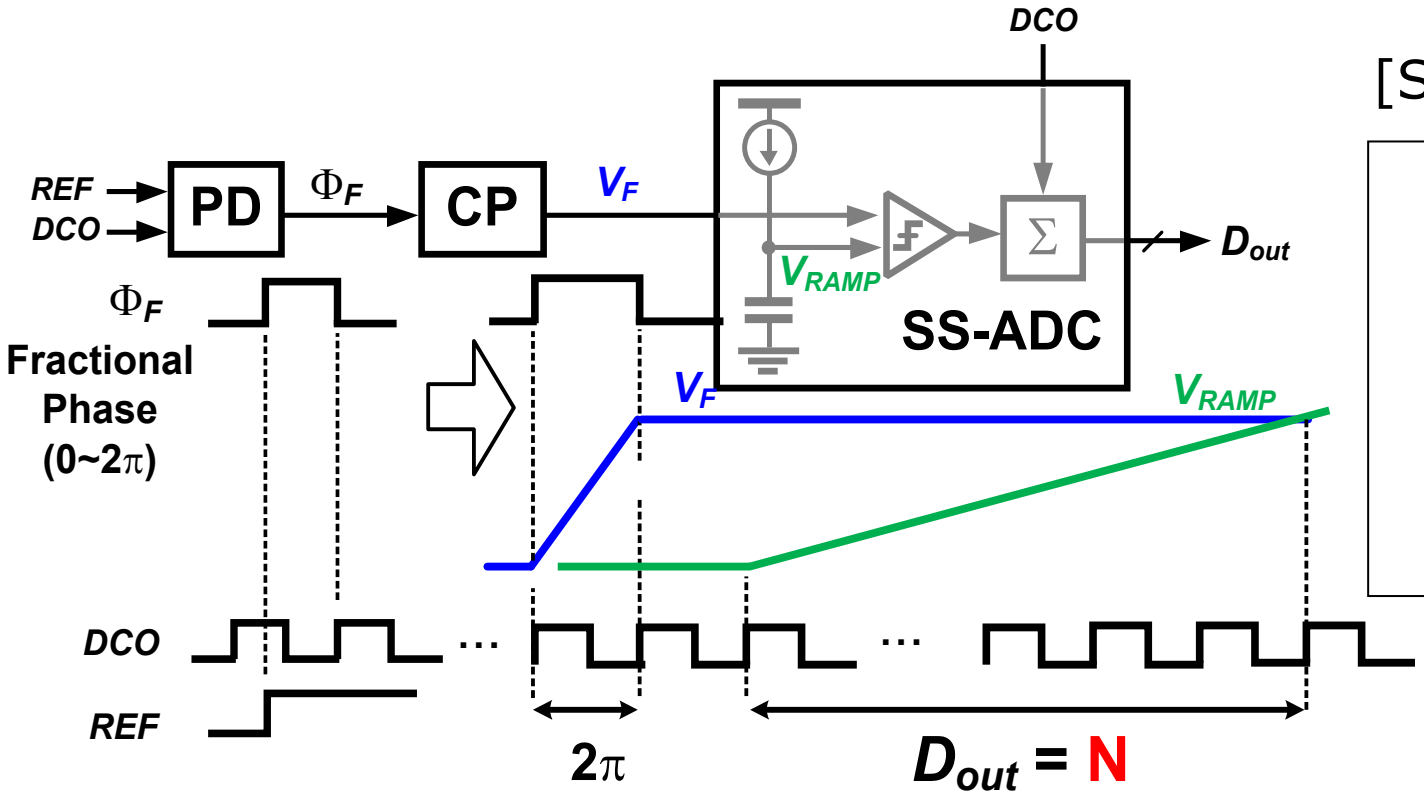
Time Stored TDC: Single-slope



[Sai,ISSCC'16]

Major performance(CMOS 65nm)

- Resolution :6.0ps
- INL :**1.6ps**
- Power :**0.36mW**
- Sample-rate :40MS/s
- Calibration :No

- Charge-pump NL and full-scale error cancellation by sharing current source
- Counter is shared with that of AD-PLL integer-phase for power reduction

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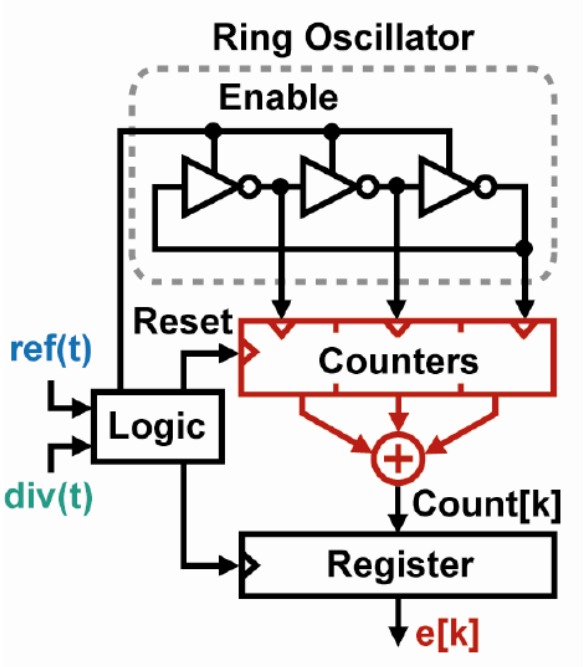
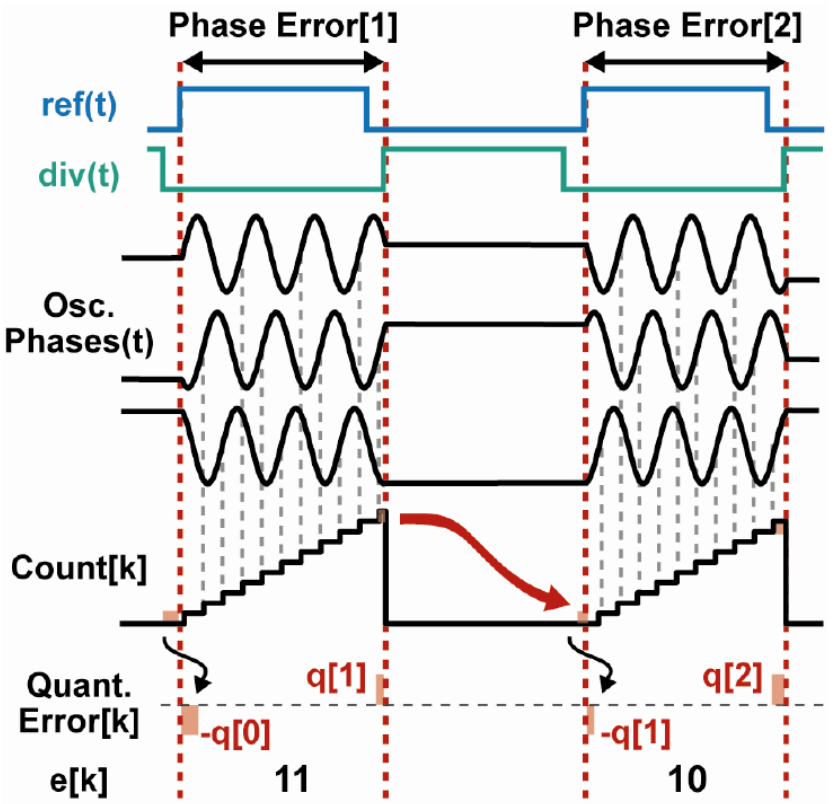
Time Stored TDC: Gated Ring Oscillator(GRO)

[Hetal,VLSI'08]





- Maintain ring oscillator phase in the interval between measurements
- **TDC QN becomes first order noise shaped**
  - e[k] = Phase Error[k] + q[k] – q[k-1]
  - Leverages PLL STF filtering to achieve improvement in resolution

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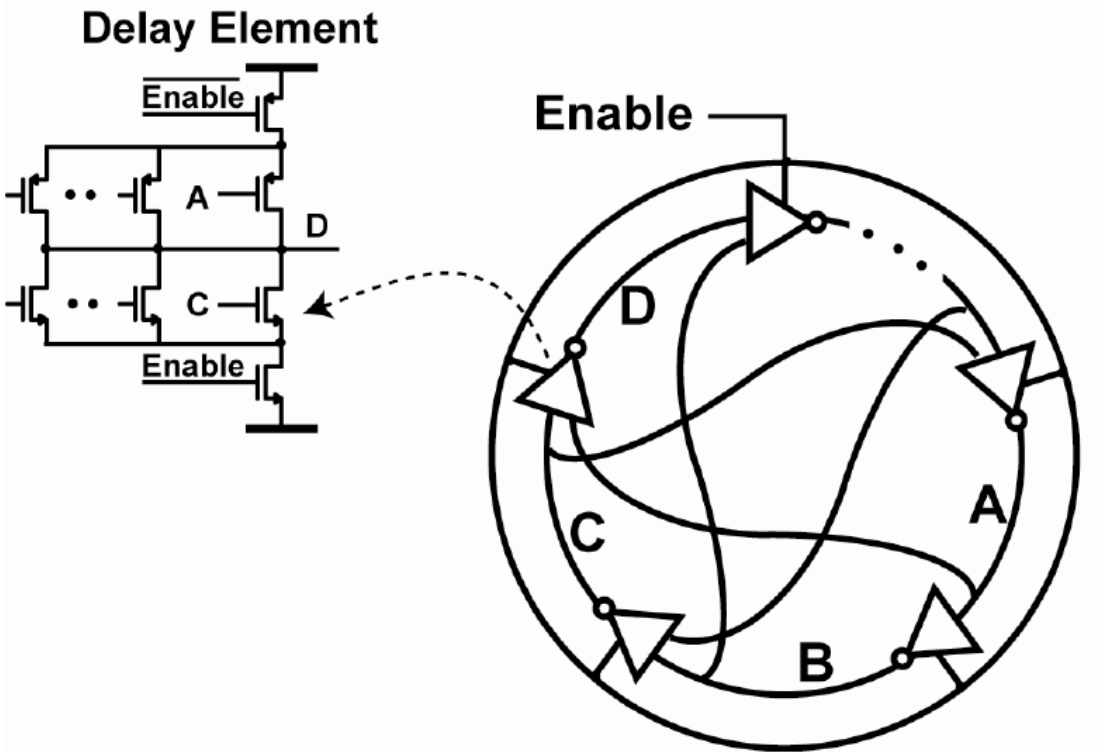
Time Stored TDC: Gated Ring Oscillator(GRO)



[Hsu,ISSCC'08]

- Major performance(CMOS 130nm)
  - Resolution :6.0ps
  - Power :3.45mW
  - Sample-rate :50MS/s
  - Calibration :No

- TDC Resolution is proportional to an effective stage-delay
- Effective stage delay per stage is reduced from 35ps to 6ps by leveraging edges from several previous delay stages

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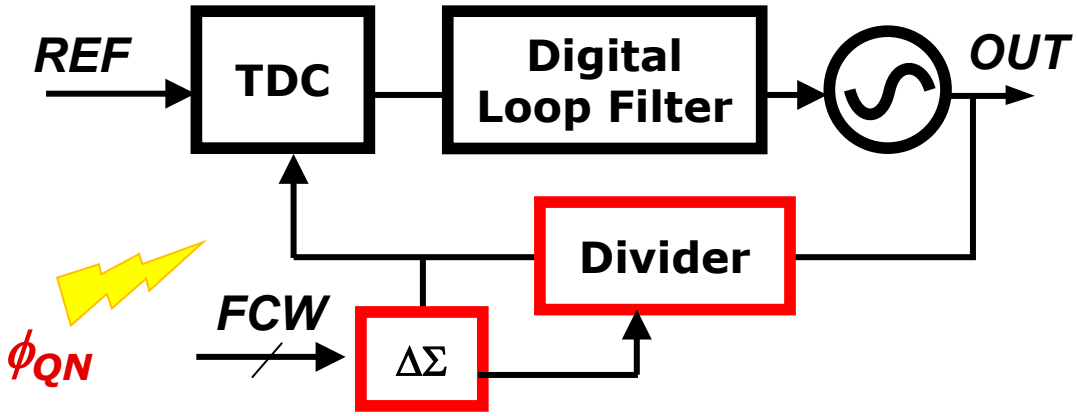
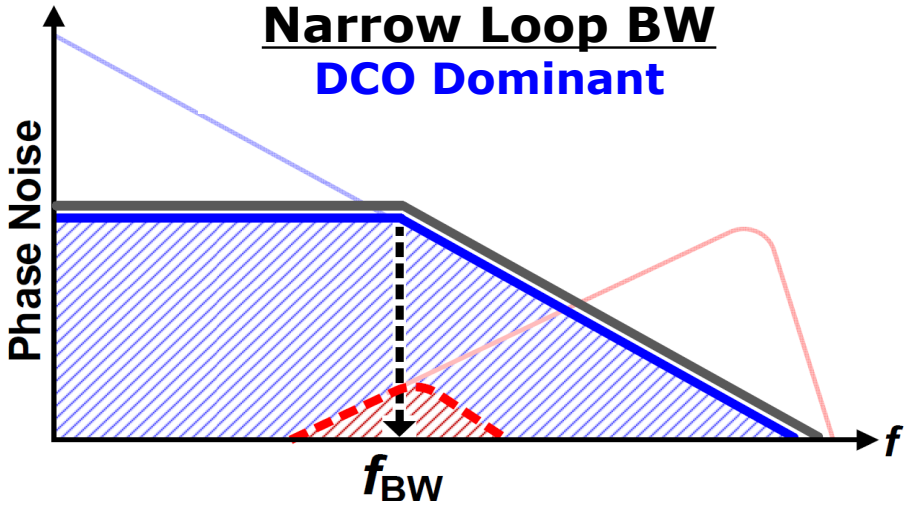
Delta-Sigma Modulator(ΔΣM) Q-Noise

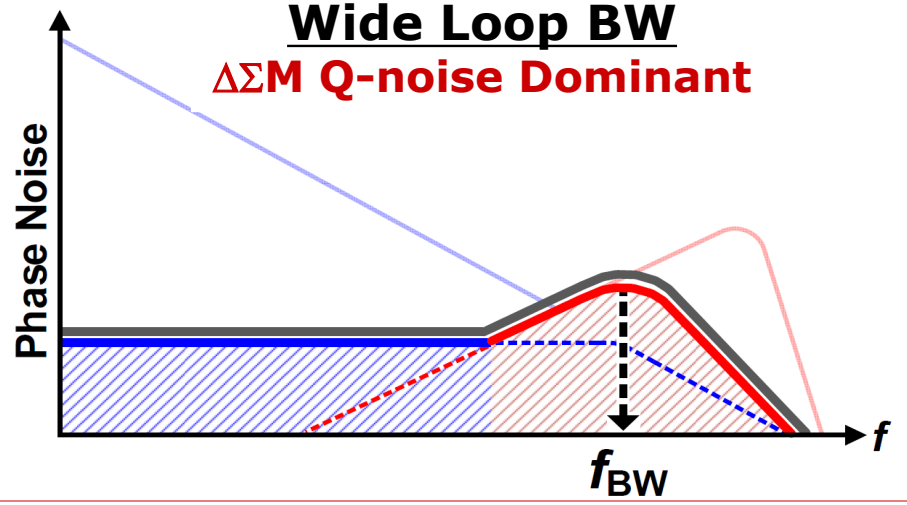




Signal Transfer Function(STF)

$$\frac{\phi_{OUT}}{\phi_{QN}} = \frac{1}{1 + H_{OL}(s)}$$

DCO phase noise
ΔΣM Quantization noise
Total noise



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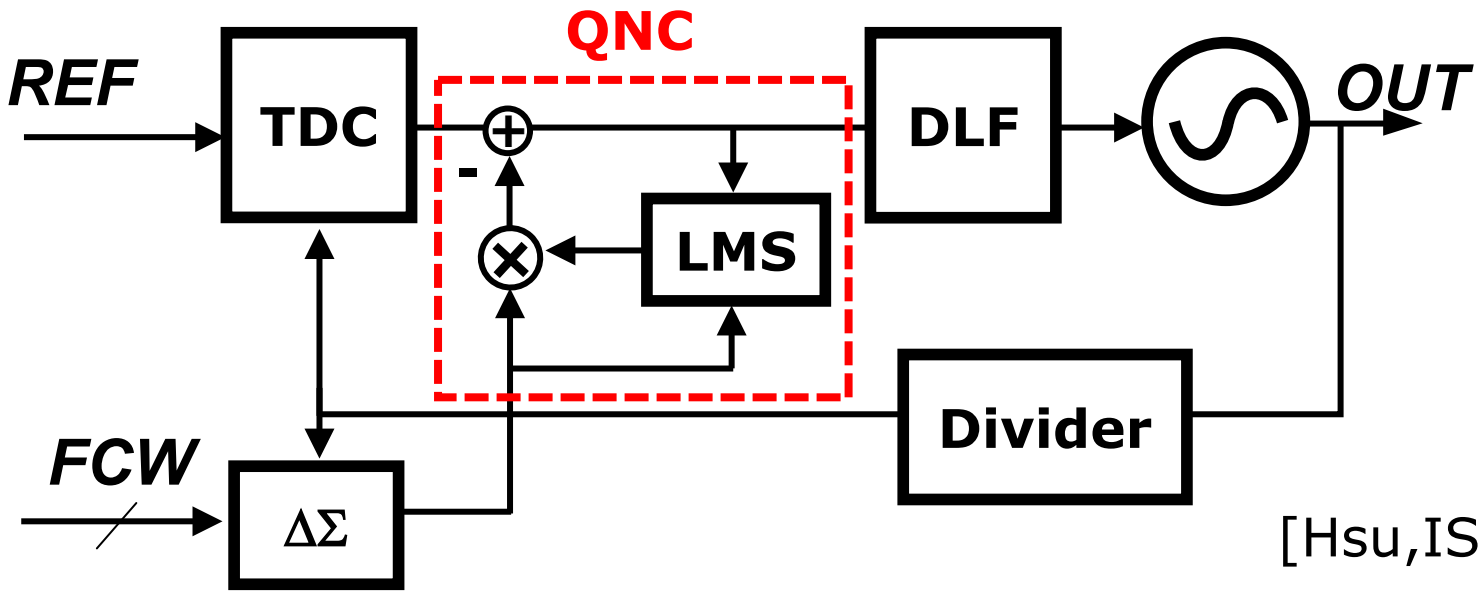
ΔΣM Q-Noise Cancellation(QNC) (1/2)



[Hsu,ISSCC'08]

- **ΔΣ Q-noise is greatly suppressed without analog mismatch**
- **Benefit from Down-speeded DCO output is still maintained**
  - Easy to use Time-Stored type and improve QN and NL of TDC

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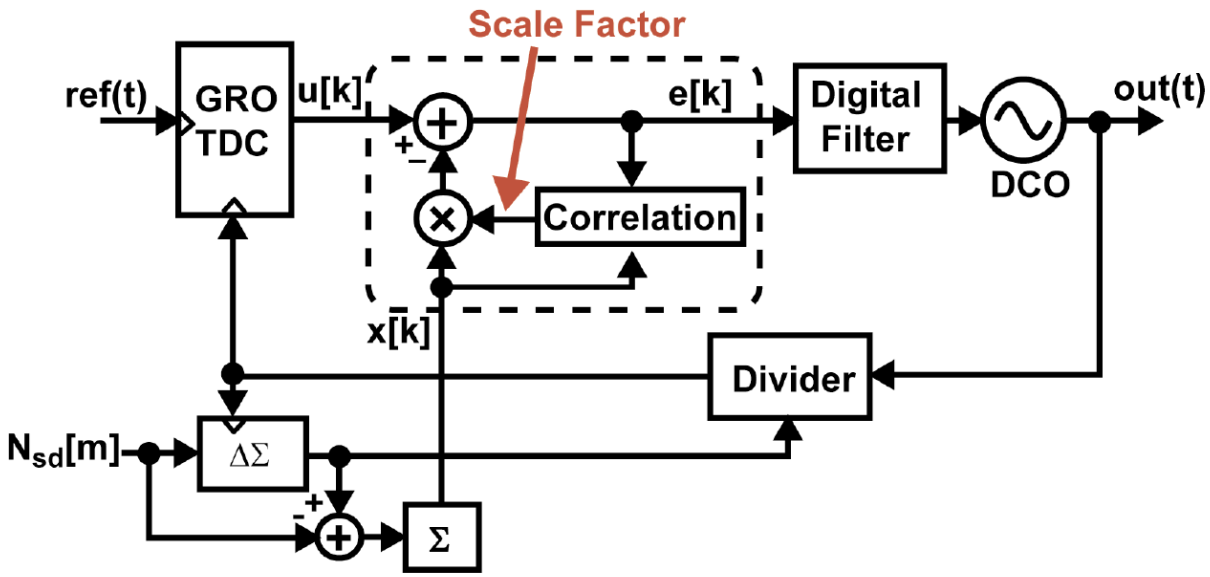
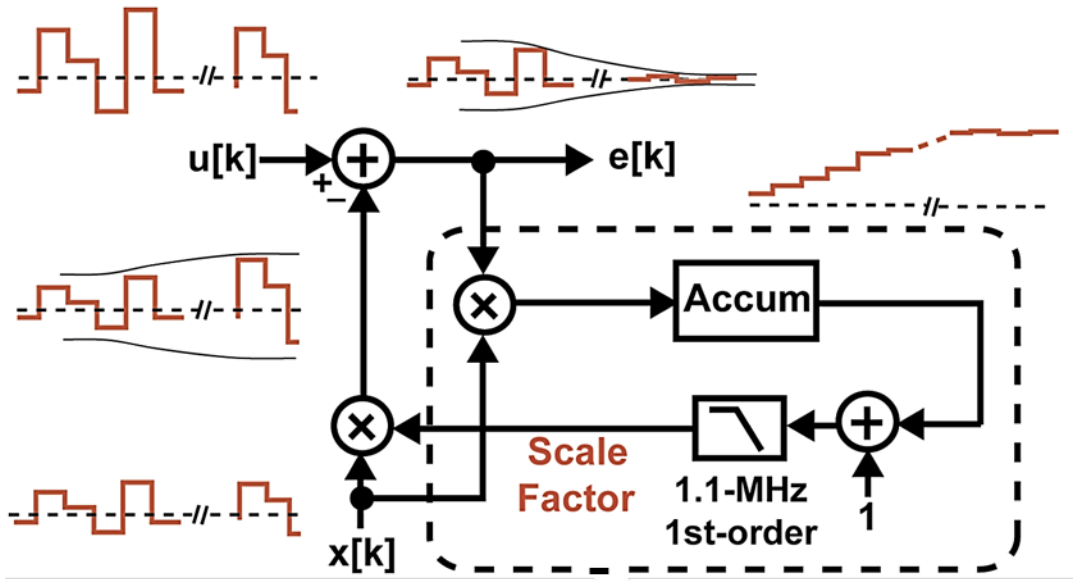
ΔΣM Q-Noise Cancellation(QNC) (2/2)





- Phase error due to ΔΣ is predictable by accumulating ΔΣ quantization error
- Correlator out is accumulated and filtered to achieve scale factor

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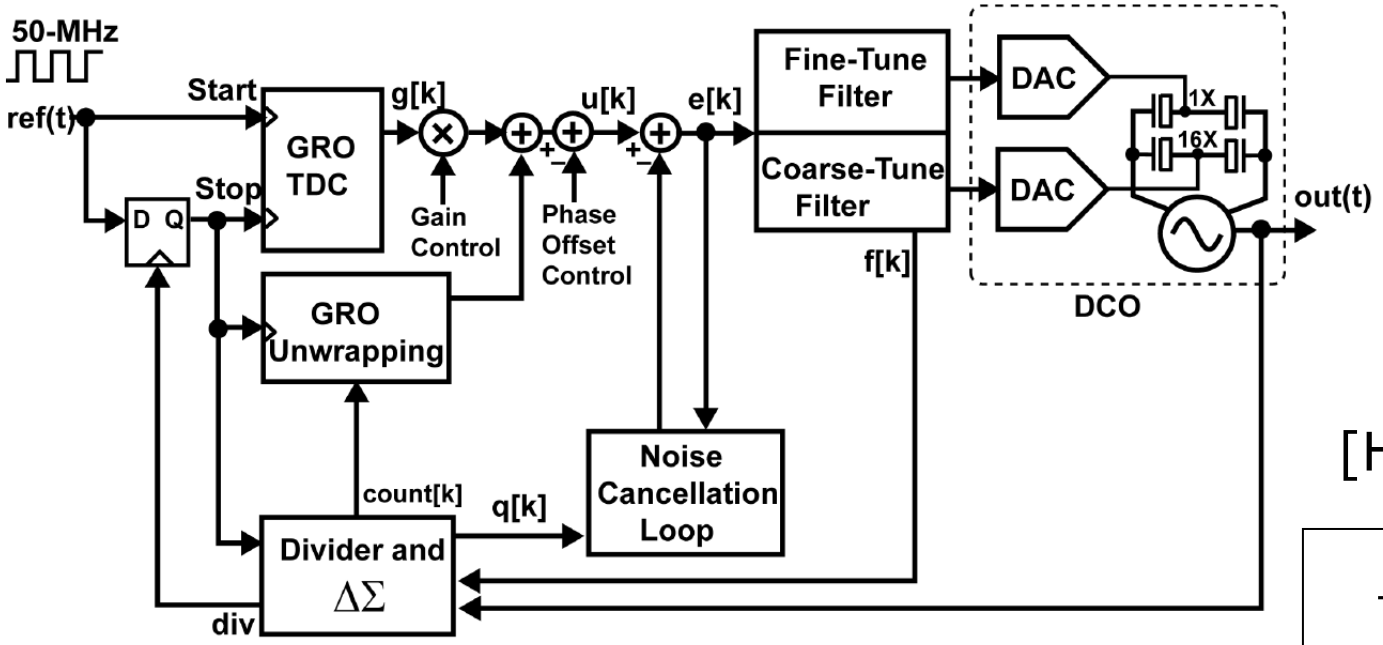
Divider-based Digital PLL: QNC & GRO



[Hsu,JSSC'08]

- Effect of QNC/GRO on divider/TDC quantization noise realizes outstanding jitter performance
- Relatively large power and area due to less process scaling merit

Major performance(CMOS 130nm)

Jitter	**:0.2ps**
FoM	:-237.9dB
Power	**:46.7mW**
Area	**:0.96mm2**
Frequency	:3.67GHz

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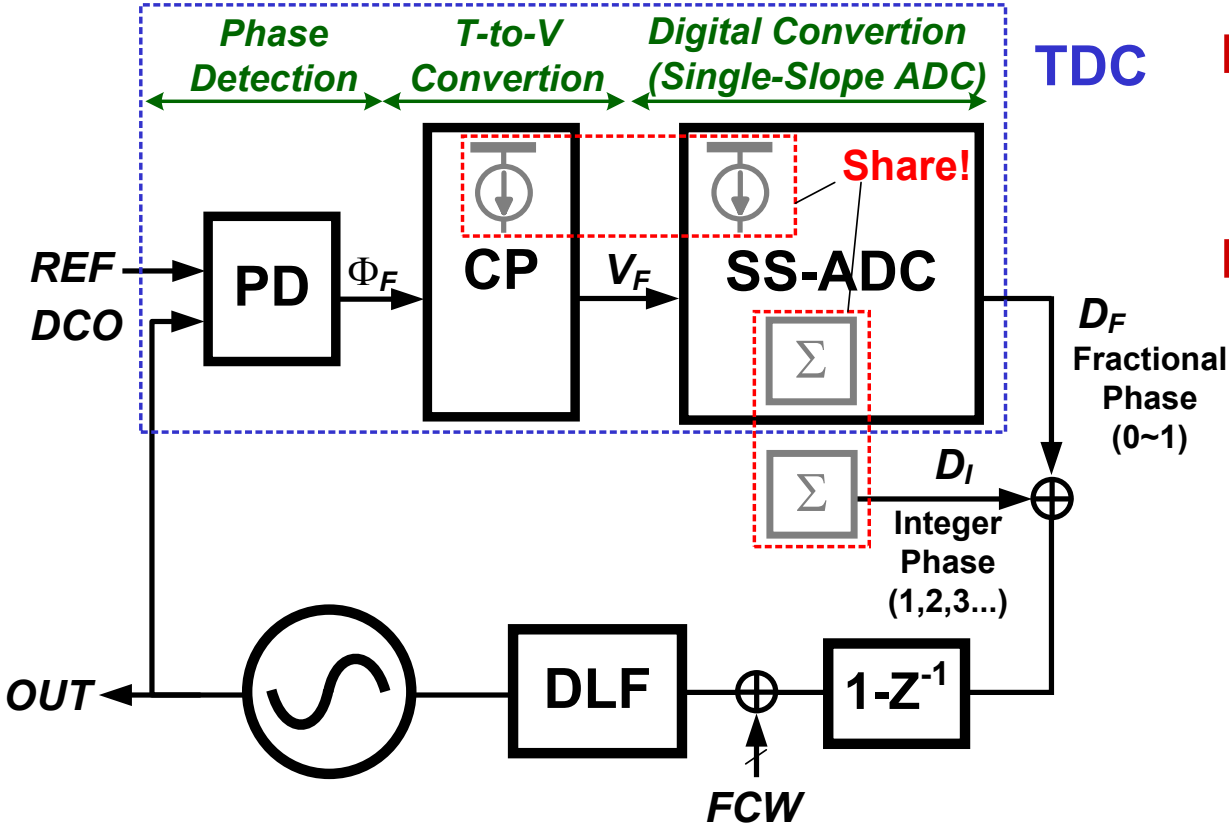
Divider-based Digital PLL: Single-Slope TDC



- Down-speeded TDC input and counter sharing technique realize much power reduction
- Divider ratio limits TDC resolution

[Sai, Kondo JSSC'16]

Major performance(CMOS 65nm)

- Jitter :**0.8ps**
- FoM :-237dB
- Power :**3.0mW**
- Area :**0.23mm2**
- Frequency :2.2-2.4GHz

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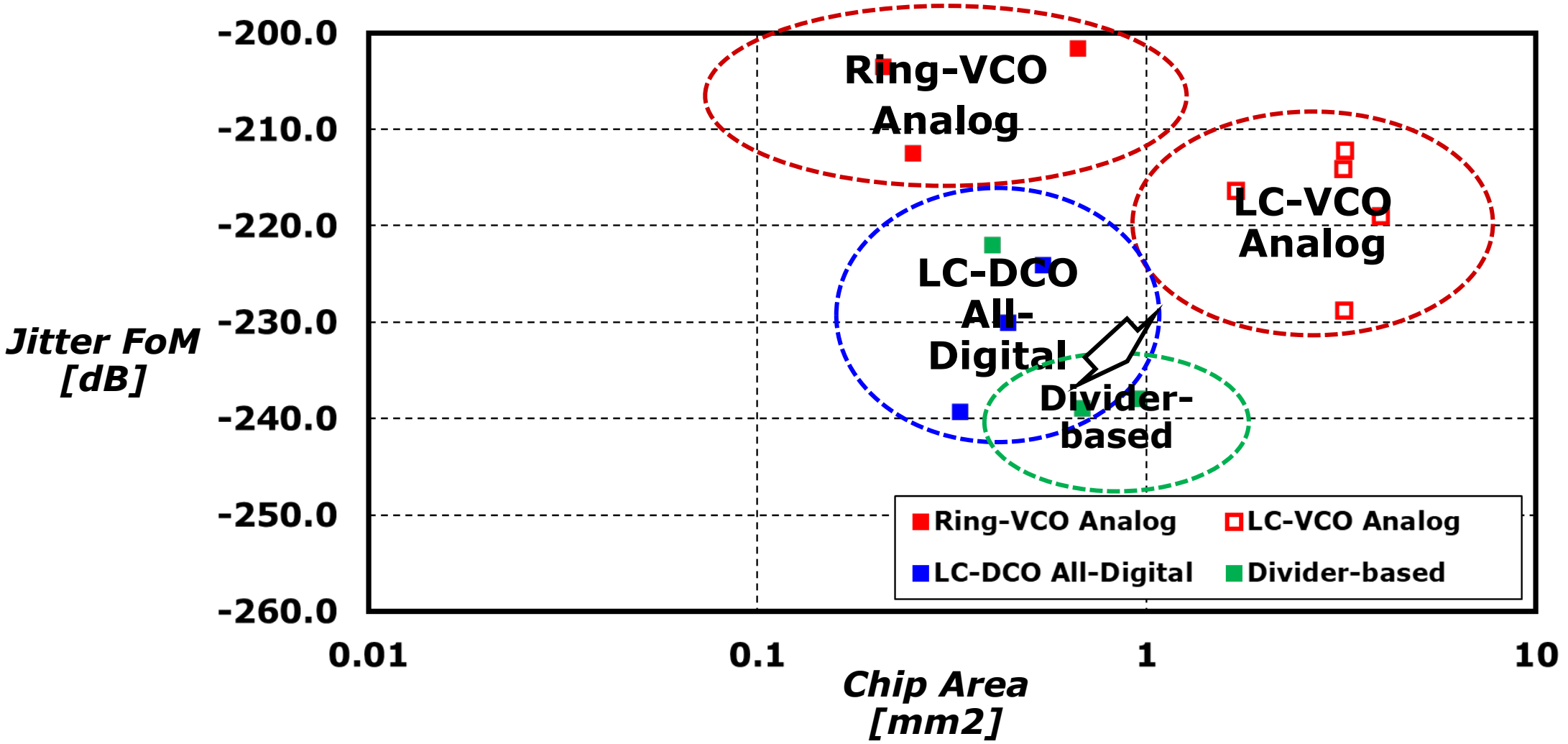
PLL Performance Trend(~2015)



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Outline

- Background of Frequency Synthesis
- Divider-less All-Digital PLL
  - Basic and Fundamentals
  - Noise analysis & Performance enhancement techniques
- Divider-based Digital PLL
  - Basic and Fundamentals
  - High performance TDCs and ΔΣM Q-Noise Cancellation
  - Performance Trends analysis thorough DTC introduction
- Future Trend Prediction
- Summary & conclusions

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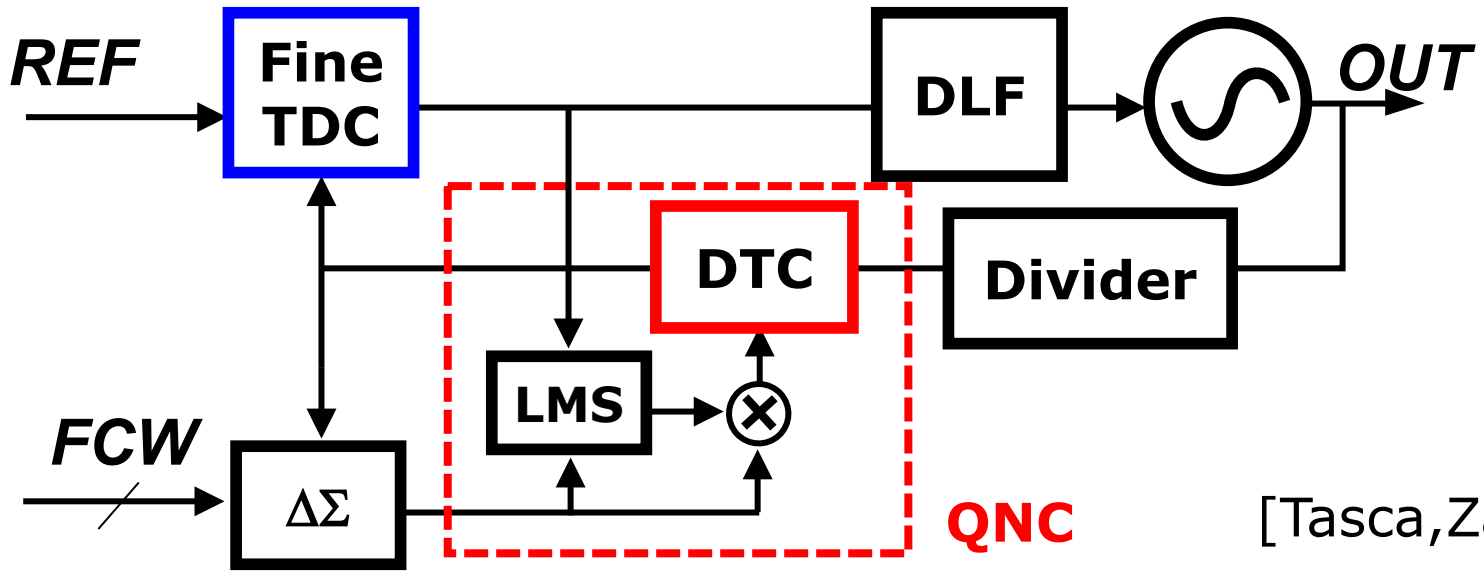
Innovation: Digital-to-Time Converter



[Tasca,Zanuso, JSSC'11]

- **DTC can make TDC dynamic range very narrow**
- **ΔΣ Q-noise suppression and down-speeded DCO are maintained**
  - ΔΣ Quantization error is canceled by simple LMS without analog mismatch

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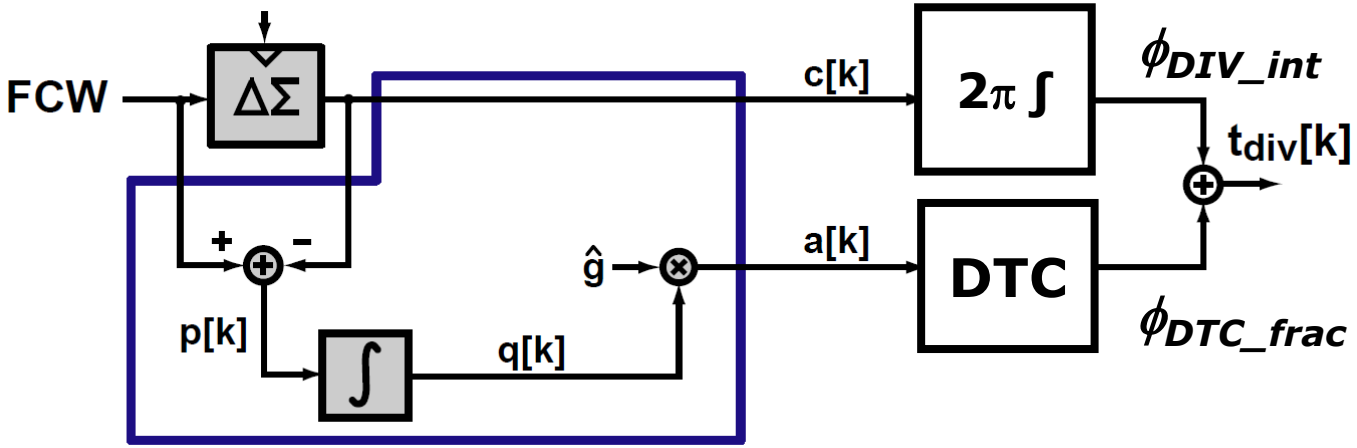
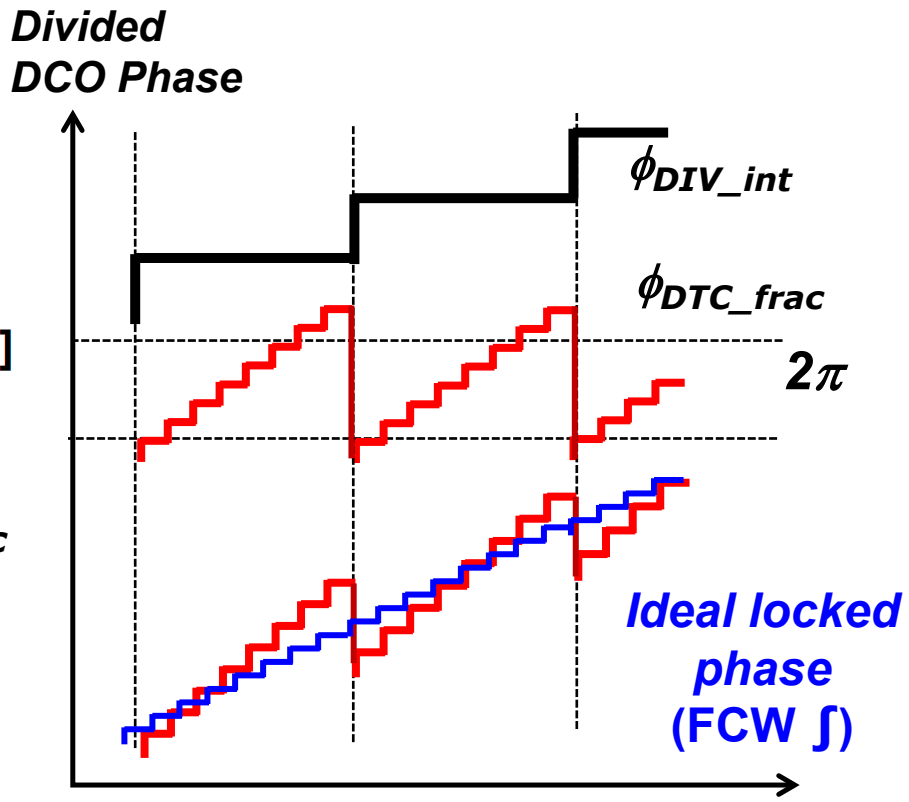
DTC: High Resolution Divider Function

DTC Time-domain Model





- ΔΣ Q-noise and required TDC input range are reduced by DTC time resolution
- However, DTC gain "g" must be adjusted so that the full scale becomes 2π

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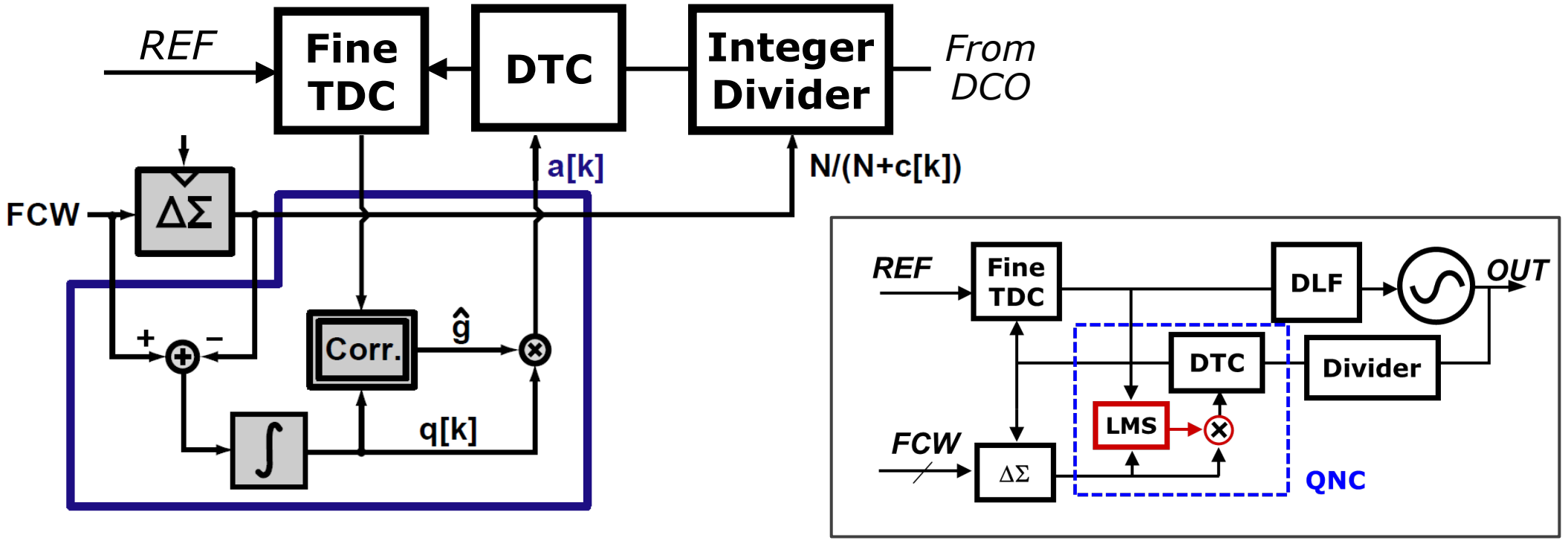
DTC: Gain Calibration



- DTC delay gain "g" is estimated from TDC error information in background

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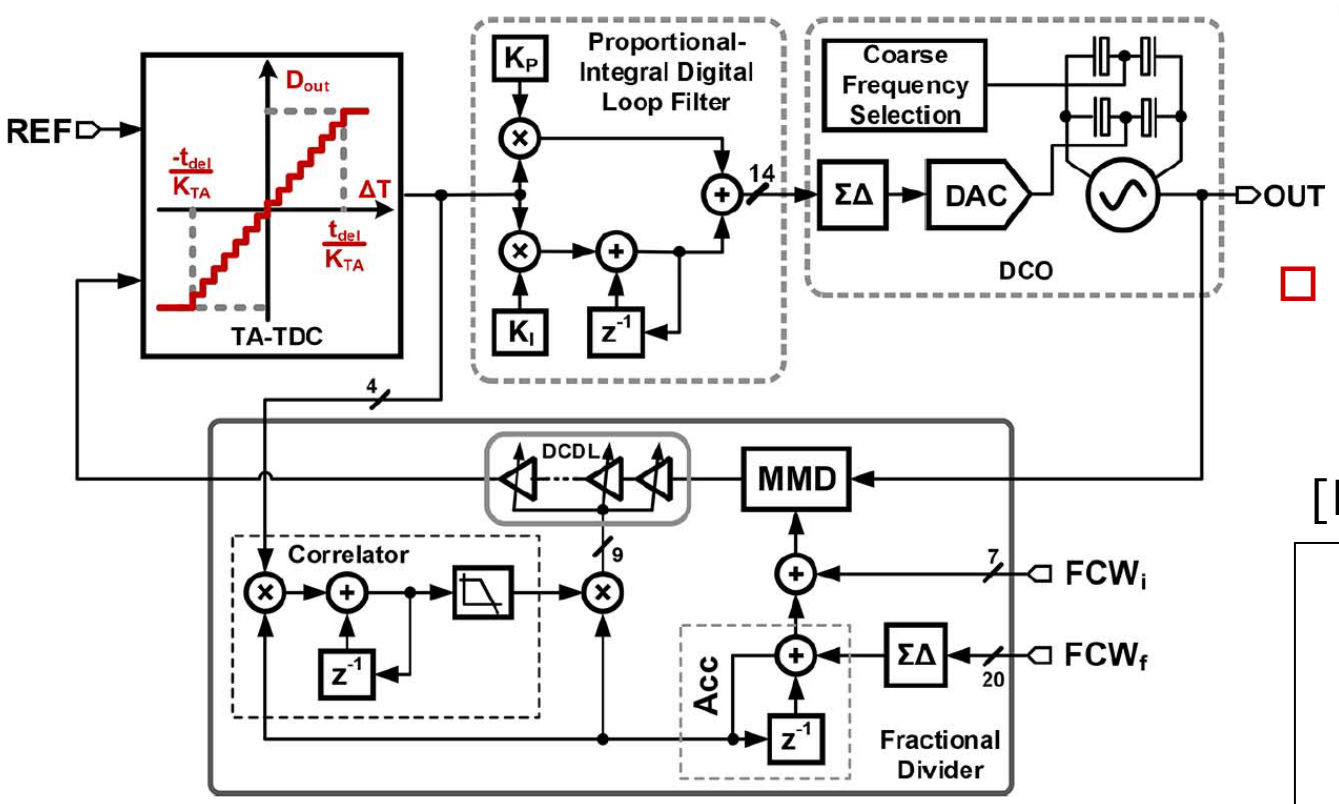
DTC based-Digital PLL: Recent Papers(1/2)



- DTC enables to use high-resolution and narrow-range time-amplifier (TA) based TDC with low power

[Elkholy,JSSC'15]

Major performance(CMOS 65nm)

- Jitter :**0.49ps**
- FoM **:-240.5dB**
- Power :**3.7mW**
- Area :0.22mm2
- Frequency :4.4-5.2GHz

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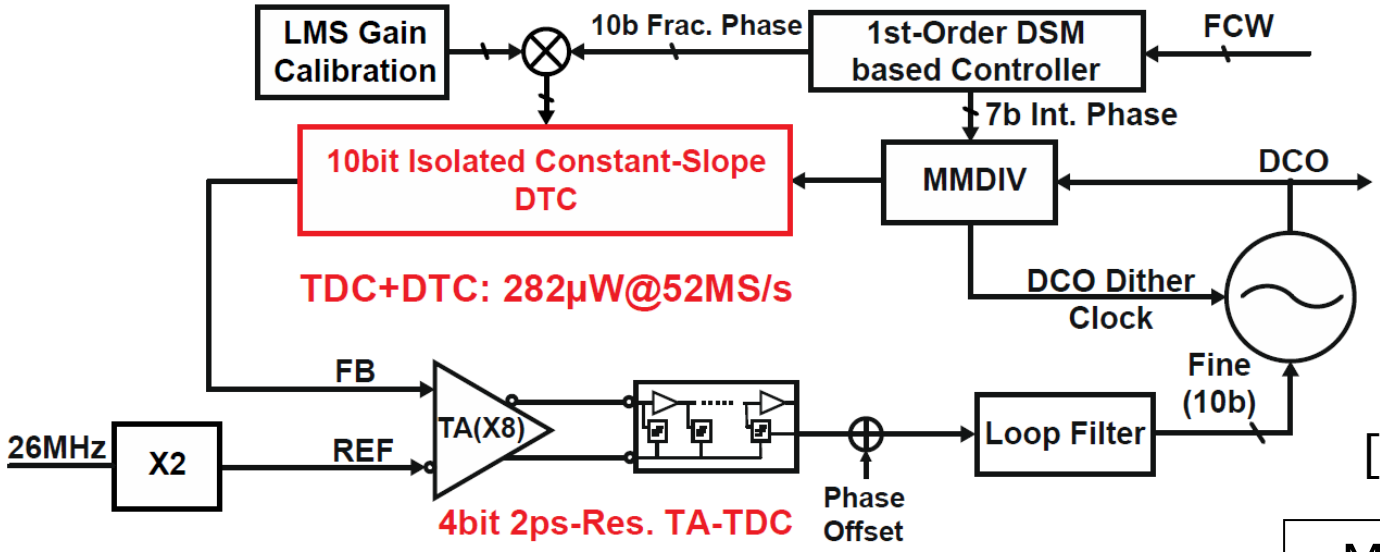
DTC based-Digital PLL: Recent Papers(2/2)



[Liu,ISSCC'18]

- DTC enables to use high-resolution and narrow-range time-amplifier (TA) based TDC with low power
- Single-slope based DTC realizes much lower power consumption

Major performance(CMOS 65nm)

- Jitter :**0.53ps**
- FoM :**-246dB**
- Power :**0.98mW**
- Area :0.23mm2
- Frequency :2.0-2.8GHz

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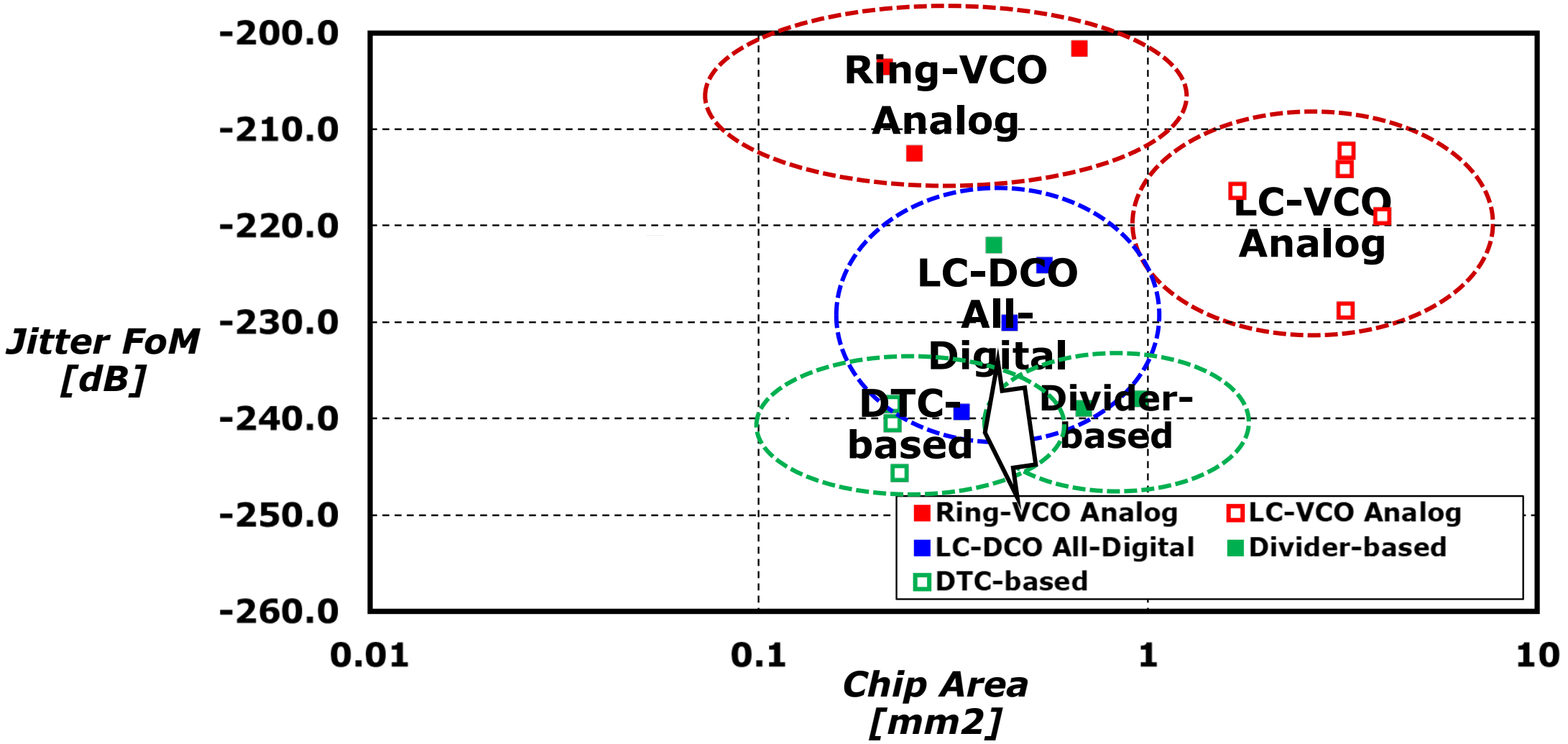
PLL Performance Trend(~2020)



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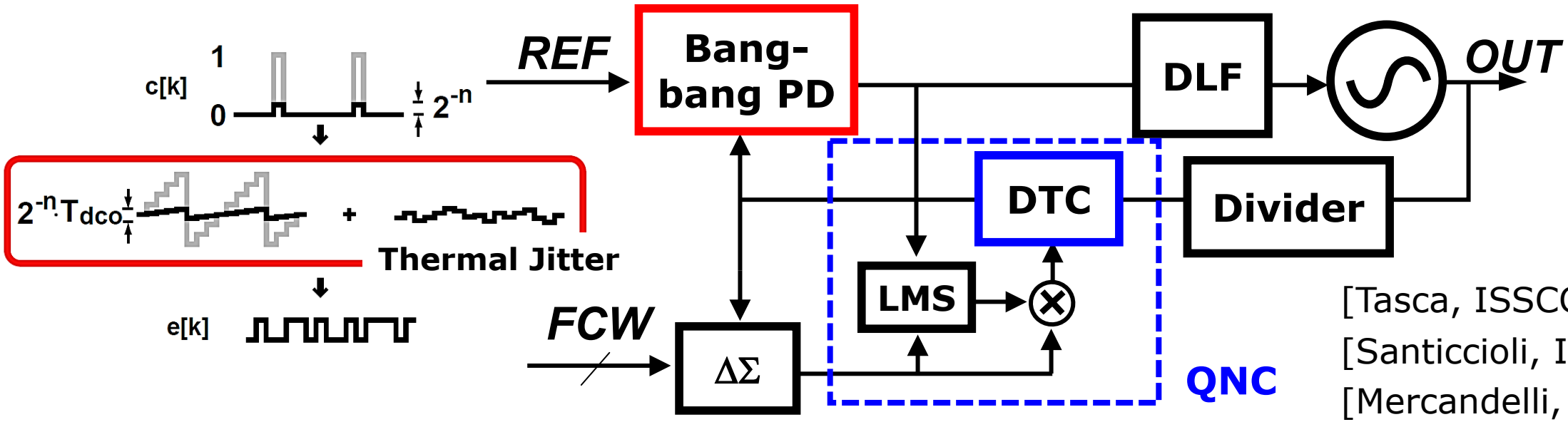
Recent Trend: Bang-bang Digital PLL



[Tasca, ISSCC'11]
[Santiccioli, ISSCC'20]
[Mercandelli, ISSCC'21]
[Santiccioli, ISSCC'22]

- **DTC enables to use ultimate form of 1-bit TDC, bang-bang PD**

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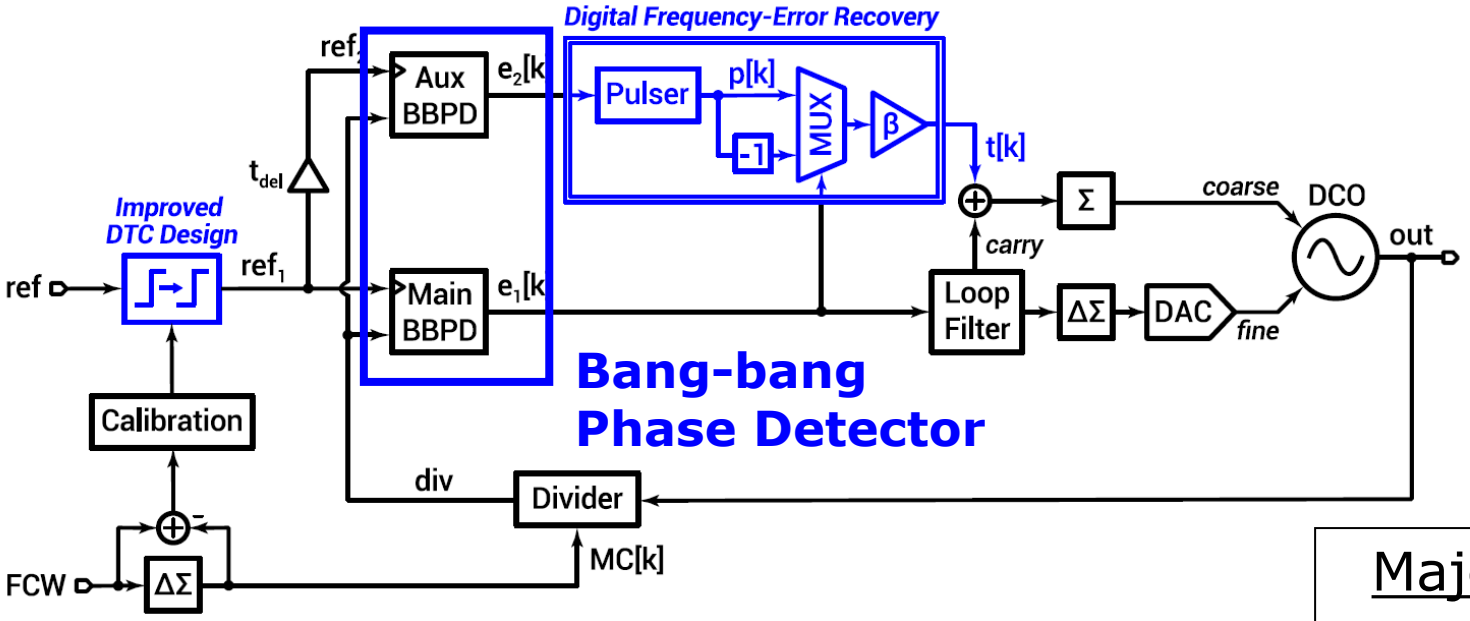
Bang-bang Digital PLL: Recent Papers(1/2)



[Santiccioli,ISSCC'20]

- **High-resolution DTC and 1-bit bang-bang PD realizes much lower jitter performance**

Major performance(CMOS 28nm)

- Jitter :**66.2fs**
- FoM :**-250.6dB**
- Power :19.8mW
- Area :**0.17mm2**
- Frequency :12.8-15.2GHz

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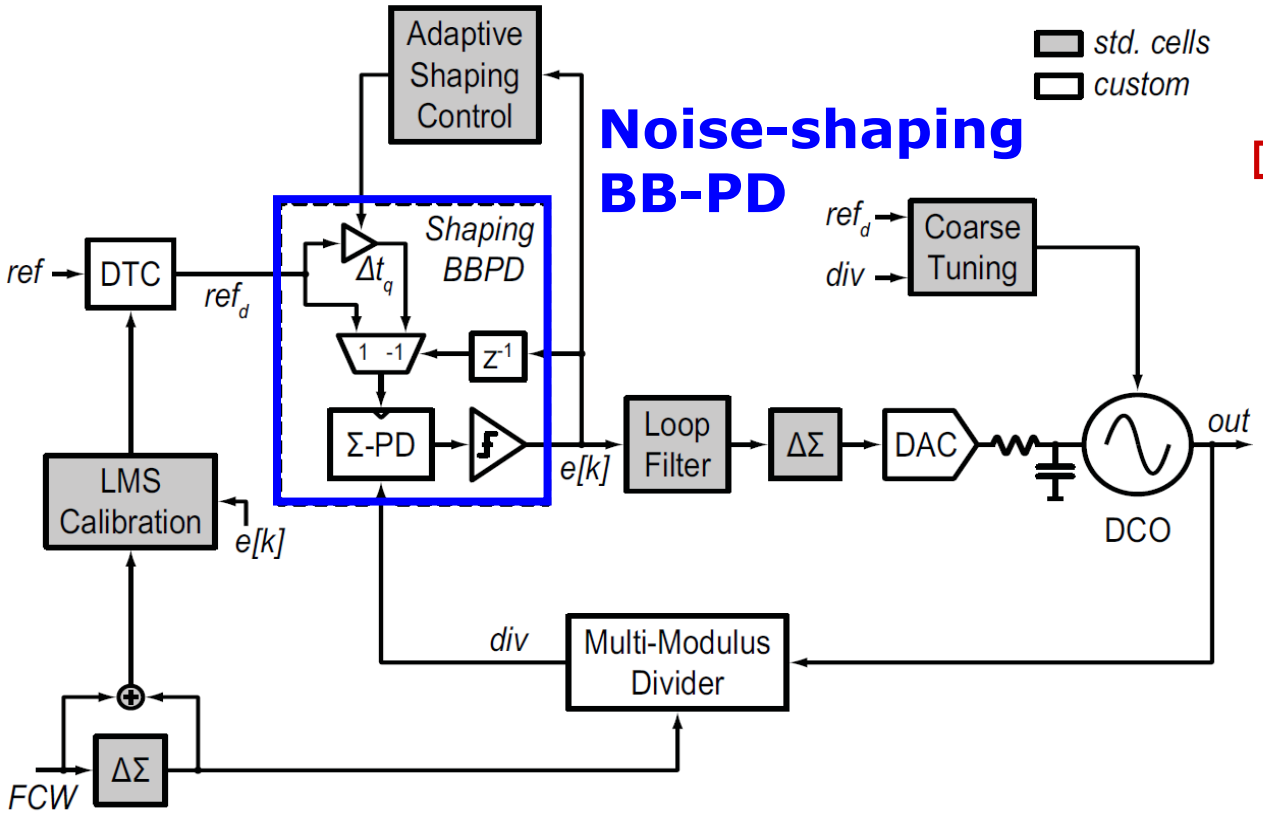
Bang-bang Digital PLL: Recent Papers(2/2)



- **High-resolution DTC and 1-bit bang-bang PD realizes much lower jitter performance**

[Mercandelli,ISSCC'21]

Major performance(CMOS 28nm)

- Jitter :**79.5fs**
- FoM :**-251.7dB**
- Power :10.8mW
- Area :**0.21mm2**
- Frequency :12.9-15.1GHz

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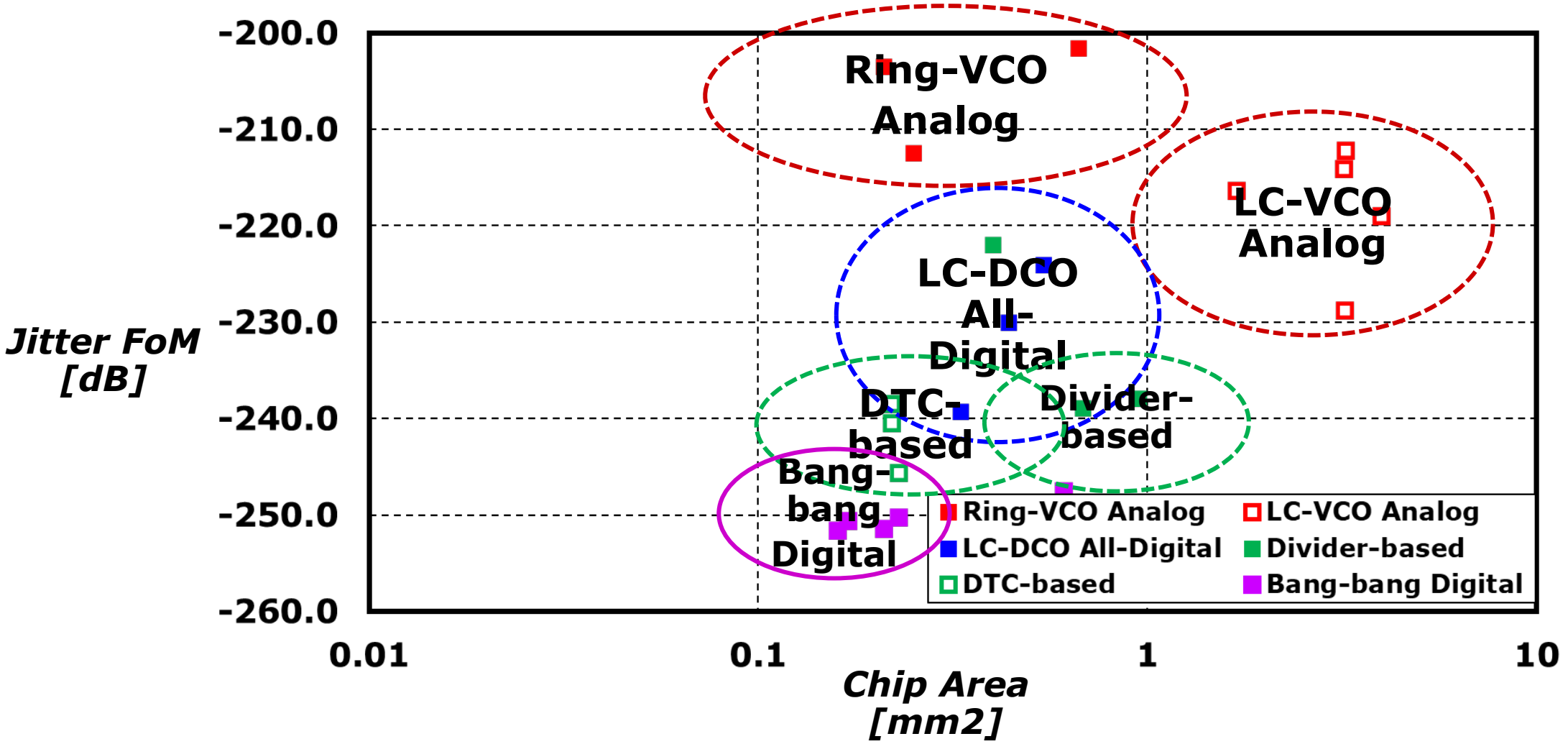
PLL Performance Trend(~2022)



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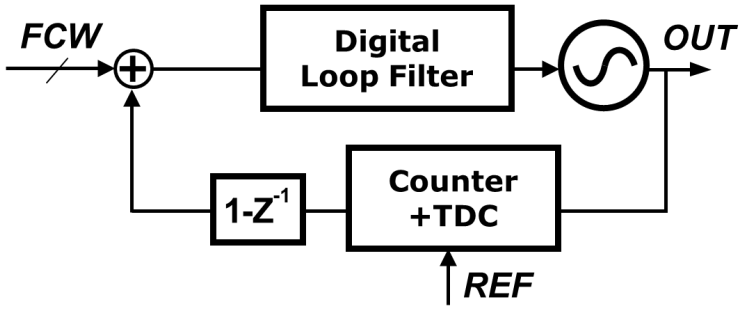
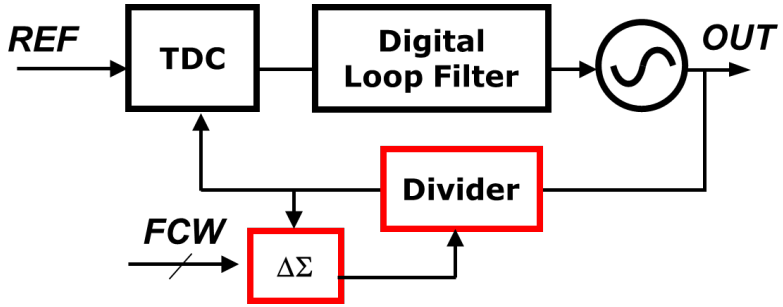
Digital PLL Evolution Summary

All-Digital Divider Less



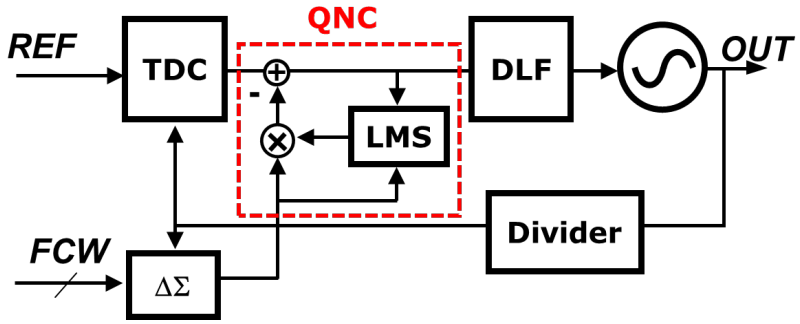
- Free from complex analog design

Divider-based Digital PLL



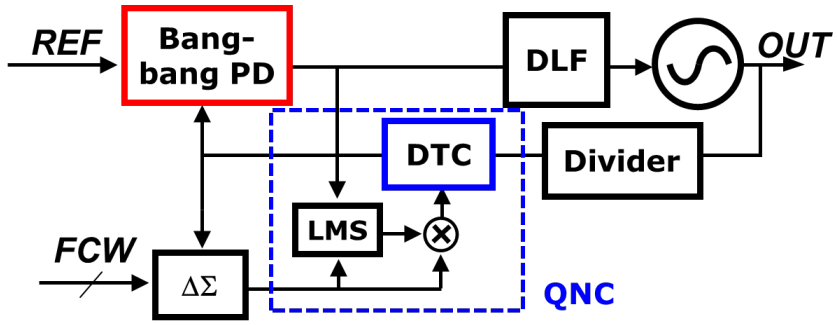
- High performance time-stored TDC

Digital PLL with QNC



- Quantization noise suppression

DTC-based bang-bang Digital PLL



- Ultimate 1-bit TDC implementation

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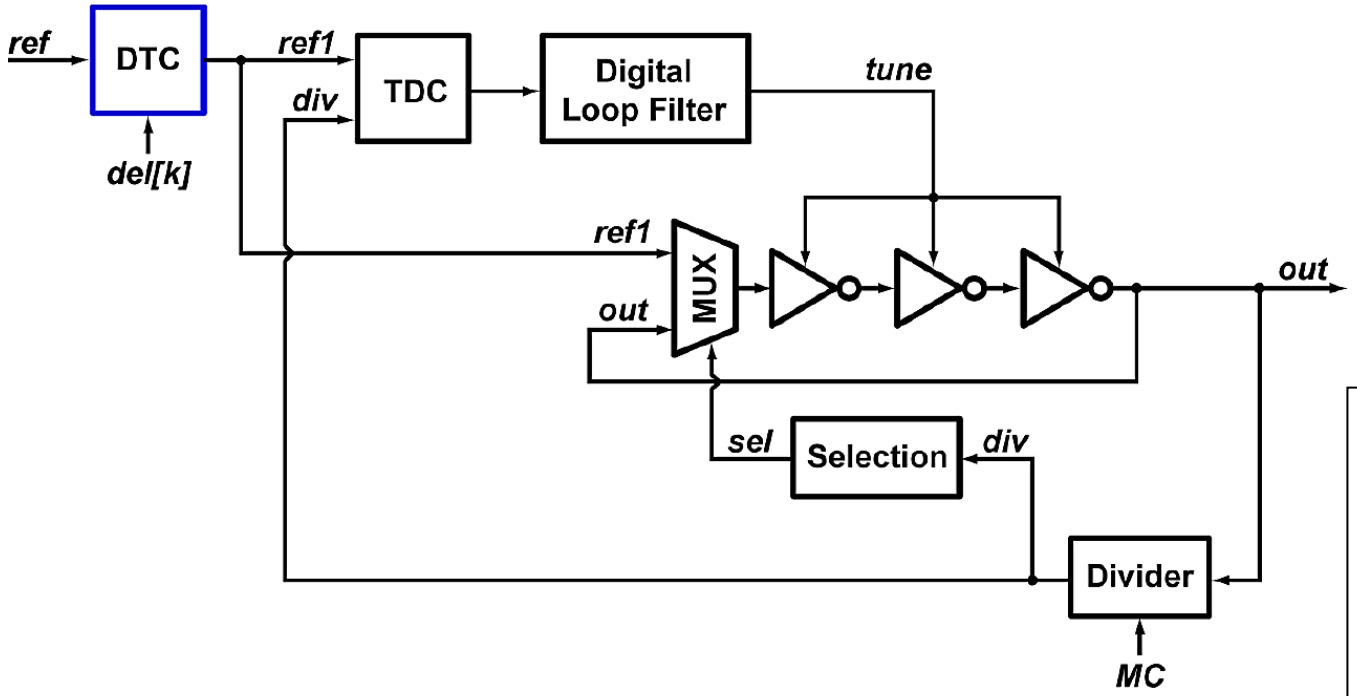
Digital MDLL using DTC/Bang-bang PD



- **All standard-cell implementation allows low-cost and high-flexibility design**
- **Poor phase noise and mismatch of delay line dominate jitter and fractional spur**

[Marucci,ISSCC'14]

Major performance(CMOS 65nm)

- Jitter :**1.4ps**
- FoM :**-232dB**
- Frac. Spur :**-47dBc**
- Power :**3mW**
- Area :**0.4mm2**
- Frequency :1.6-1.9GHz

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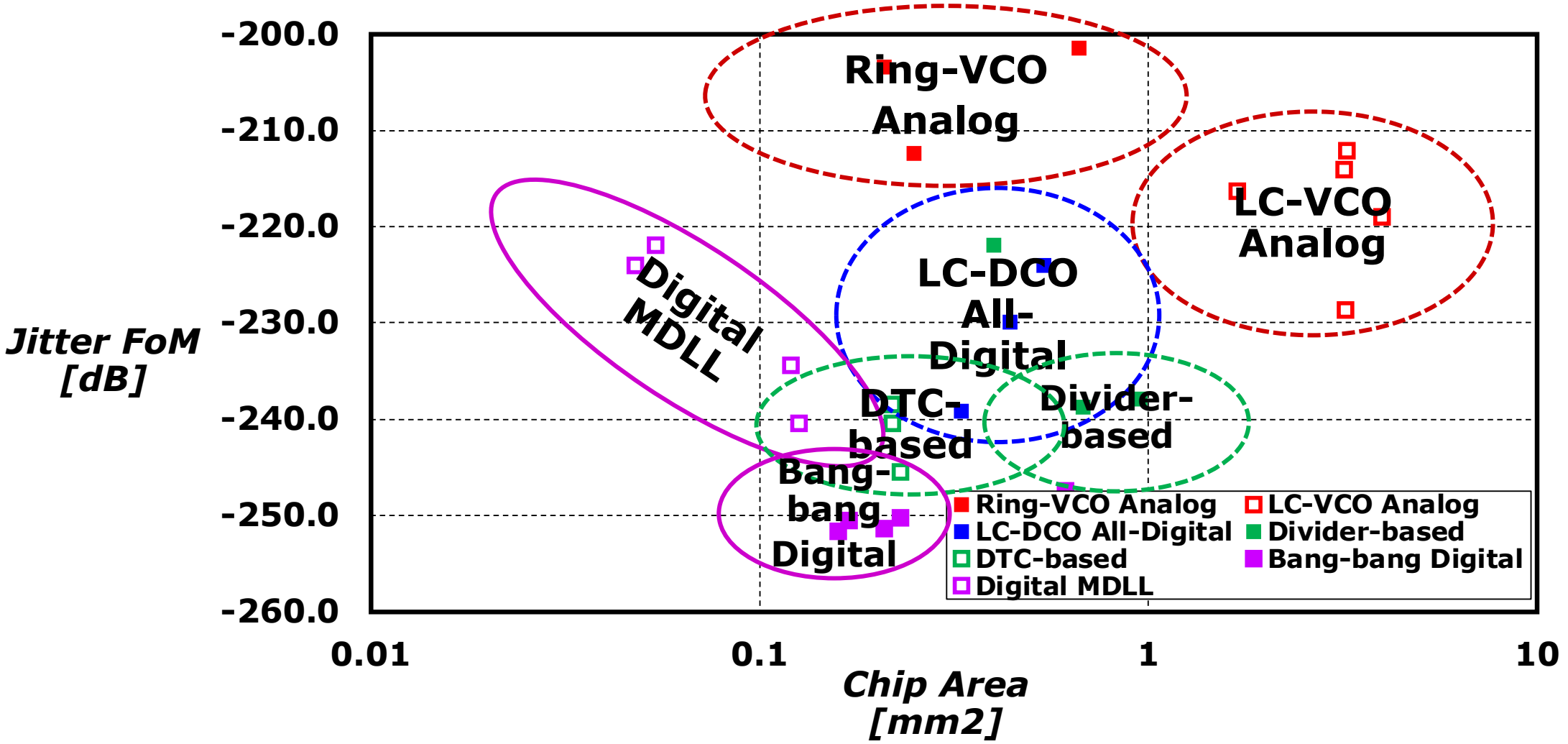
PLL Performance Trend(~2022)



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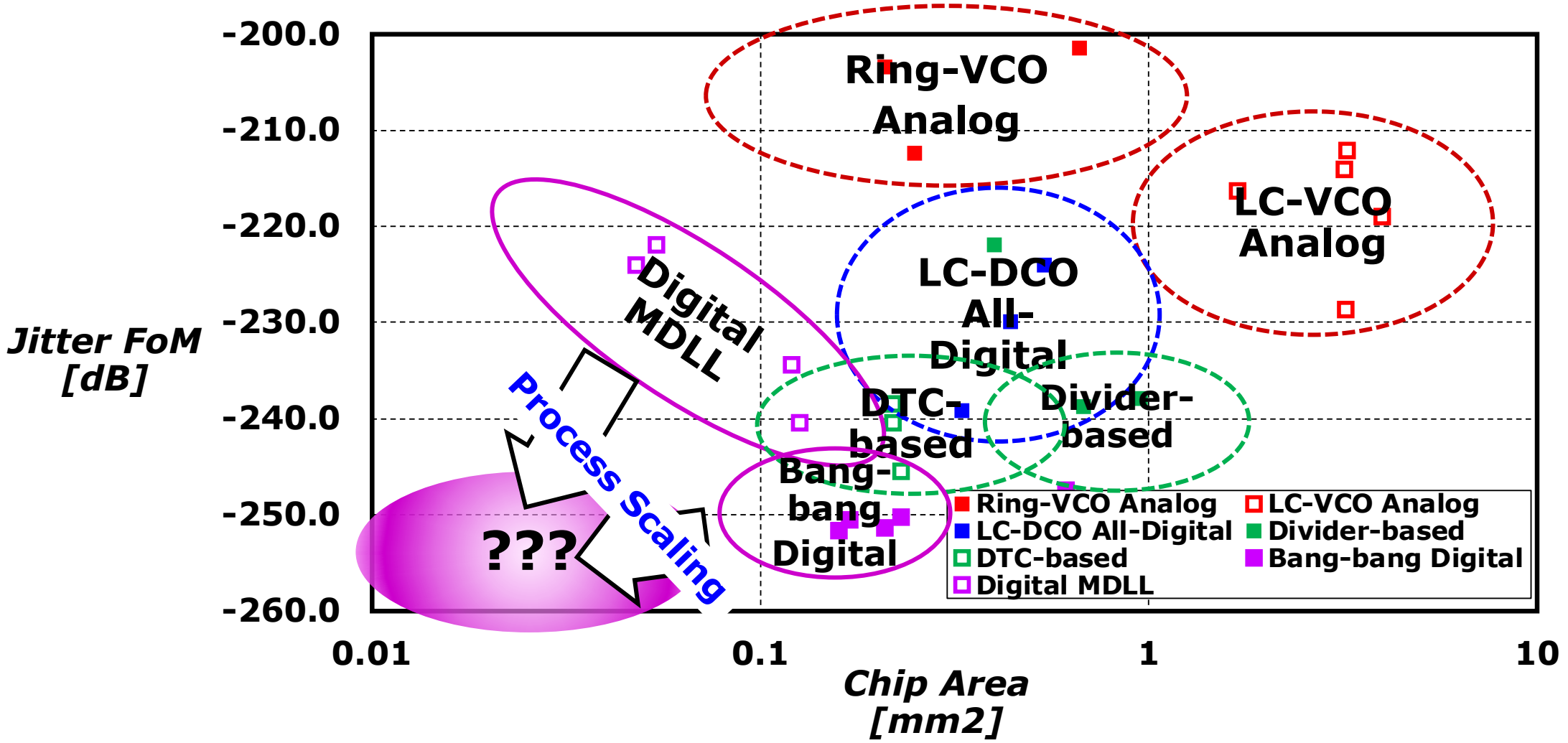
PLL Performance Trend(2023~)



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Summary

- Frequency synthesis and PLL has become more and more indispensable for recent growing demand of IoT systems.
- PLL is phase-domain feedback system to generate accurate frequency/phase output ; major applicative constraints and design challenges are fractional-N operation with low jitter, low phase noise, and low fractional spur.
- All digital PLL is major breakthrough in frequency synthesis; greatly mitigates tradeoff between loop bandwidth and area penalty of loop filter
- Advanced digital PLL with divider and DTC continue to improve jitter FoM by cancelling ΔΣM Q-Noise and by making required TDC dynamic range very narrow; ultimate TDC implementation is 1-bit bang-bang phase detector.
- While bang-bang digital PLL with divider and DTC continues being mainstream, it must be taken into consideration that bang-bang digital MDLL benefit much from CMOS process scaling.

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Papers to See This Year

Session 4 Relevant Papers:

- 4.2: good example of ring-VCO based analog PLL
- 4.3 and 4.5: good example of DTC-based bang-bang digital PLL

Session 14 Relevant Papers:

- 14.1: Fractional-N MDLL with excellent DTC NL cancellation
- 14.2: Innovative DTC INL Calibration technique using auxiliary PLL

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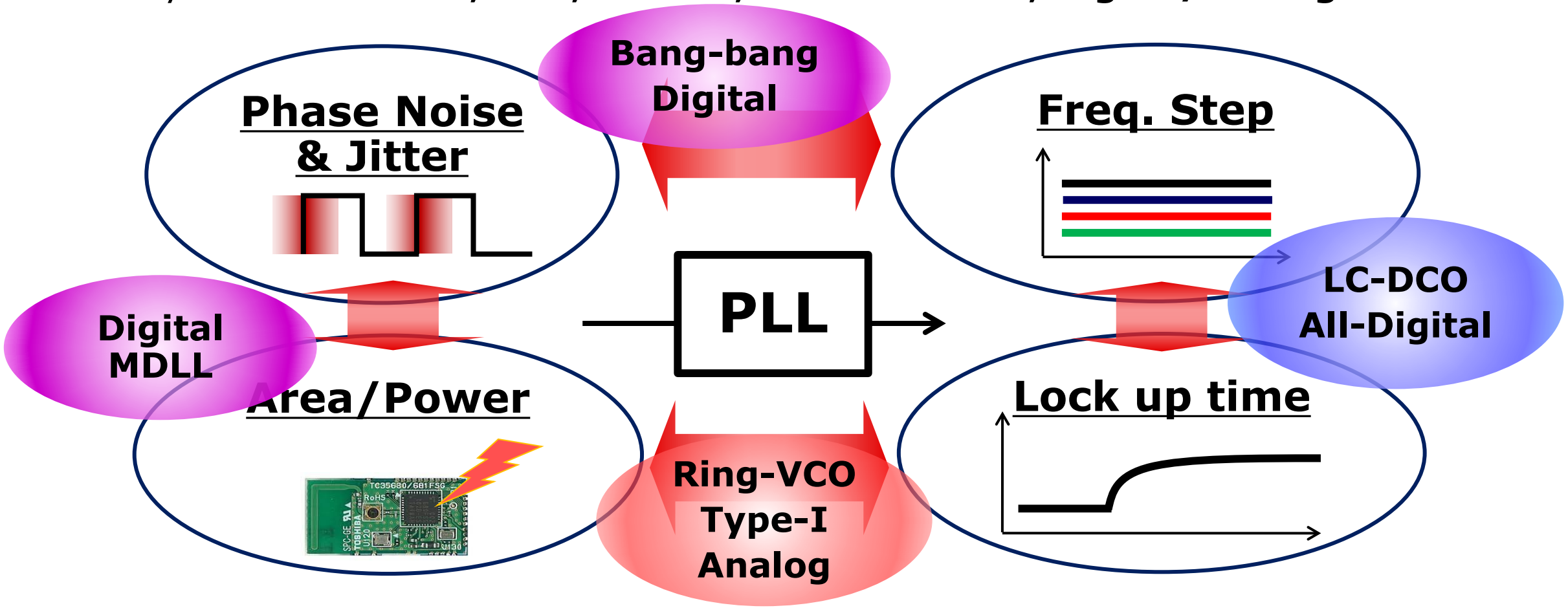
Right PLL in the Right place !!!

- Key factors are **TDC, DTC, Divider, DCO selection, Digital/Analog.**



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