Calibration Techniques in ADCs

Ahmed M. A. Ali
Analog Devices, Inc.

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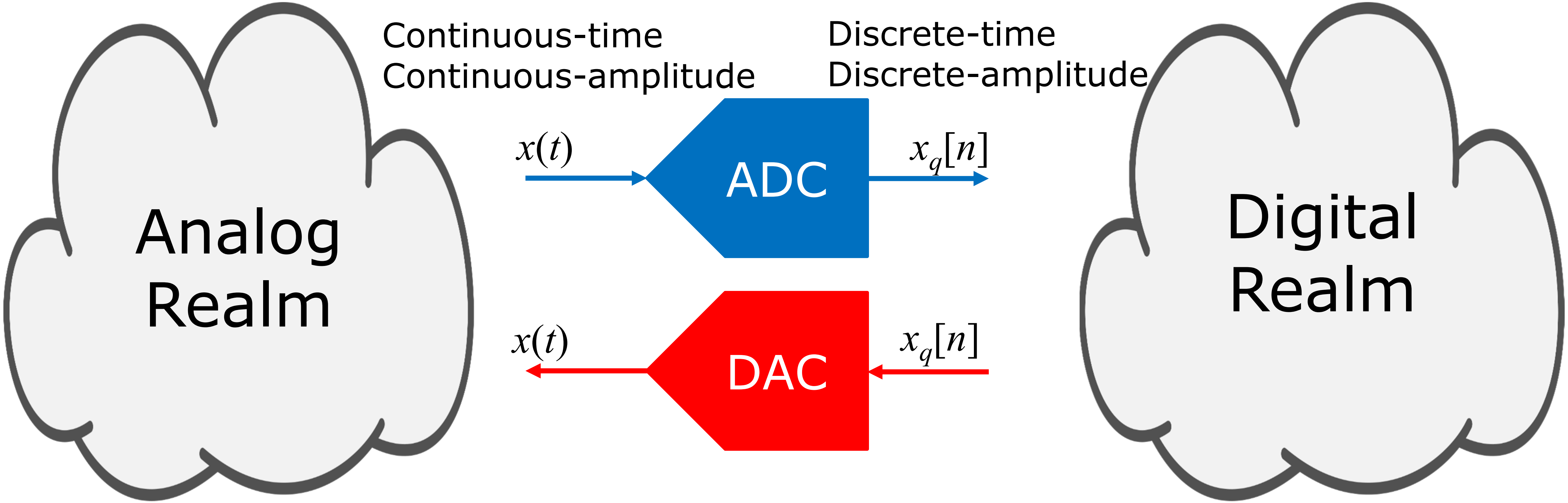
Self Introduction

- B.SC. and M.Sc. from Ain Shams University in Cairo, Egypt
- Ph.D. from the University of Pennsylvania
- Fellow at Analog Devices
- Work on high-speed data converters and digital-assistance algorithms
- Author of “High Speed Data Converters”, published in 2016 by the Institution of Engineering & Technology (IET)

Outline

- Introduction to data converters
- Performance metrics of data converters
- Pipelined ADCs and their non-idealities
- Some ADC calibration techniques (Digitally assisted A/D converters)
  - Impairments of pipelined ADCs as an example of multi-step ADCs
  - Correlation-based (dither-based) calibration techniques

Data Converters



Real World

Processing World

Applications

Wireless Communication

Defense

Medical

EVERYWHERE

Wired Communication

Satellite

Instrumentation

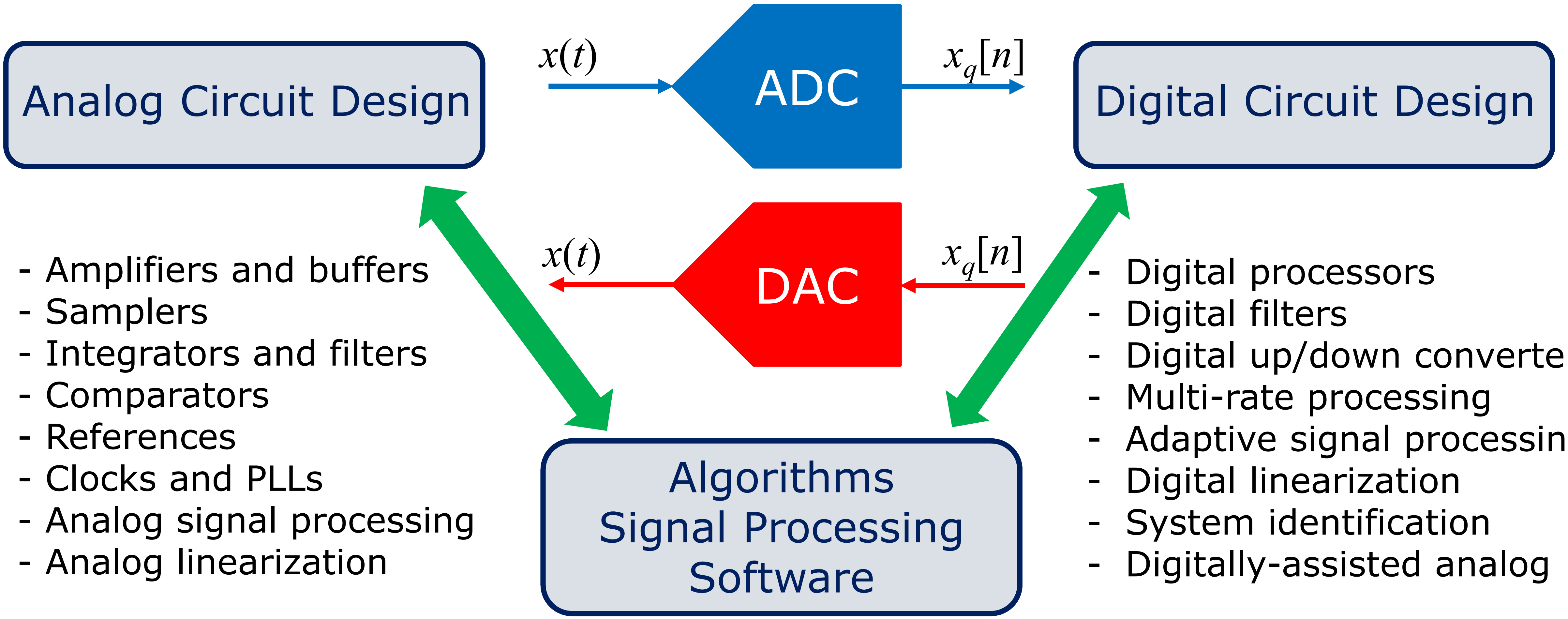
Video

Automative

IoT

Radar

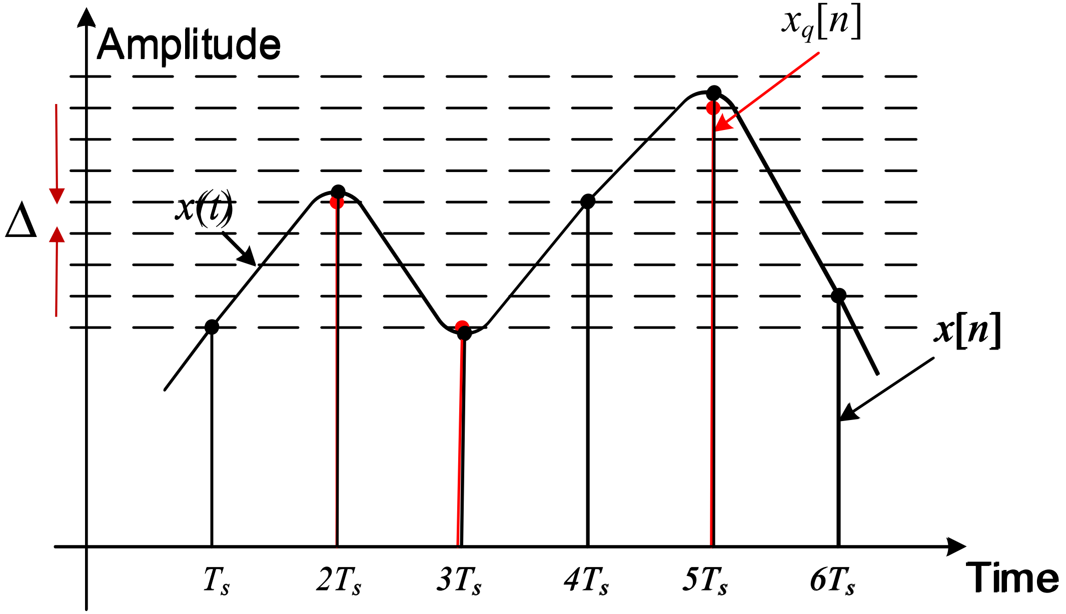
Data Converters (Multi-Disciplinary)

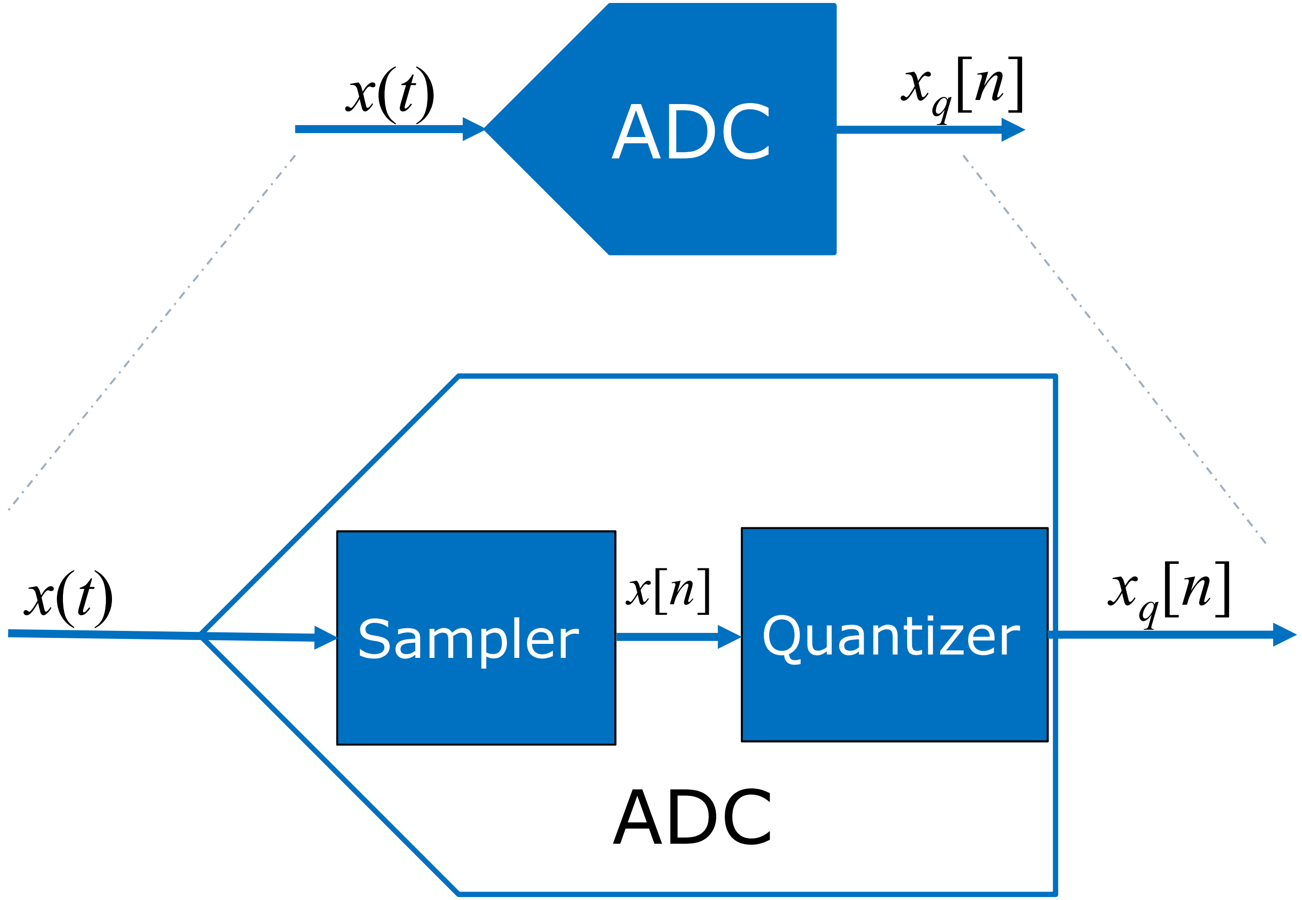


- Amplifiers and buffers
- Samplers
- Integrators and filters
- Comparators
- References
- Clocks and PLLs
- Analog signal processing
- Analog linearization

- Digital processors
- Digital filters
- Digital up/down converters
- Multi-rate processing
- Adaptive signal processing
- Digital linearization
- System identification
- Digitally-assisted analog

A/D Converter (ADC)



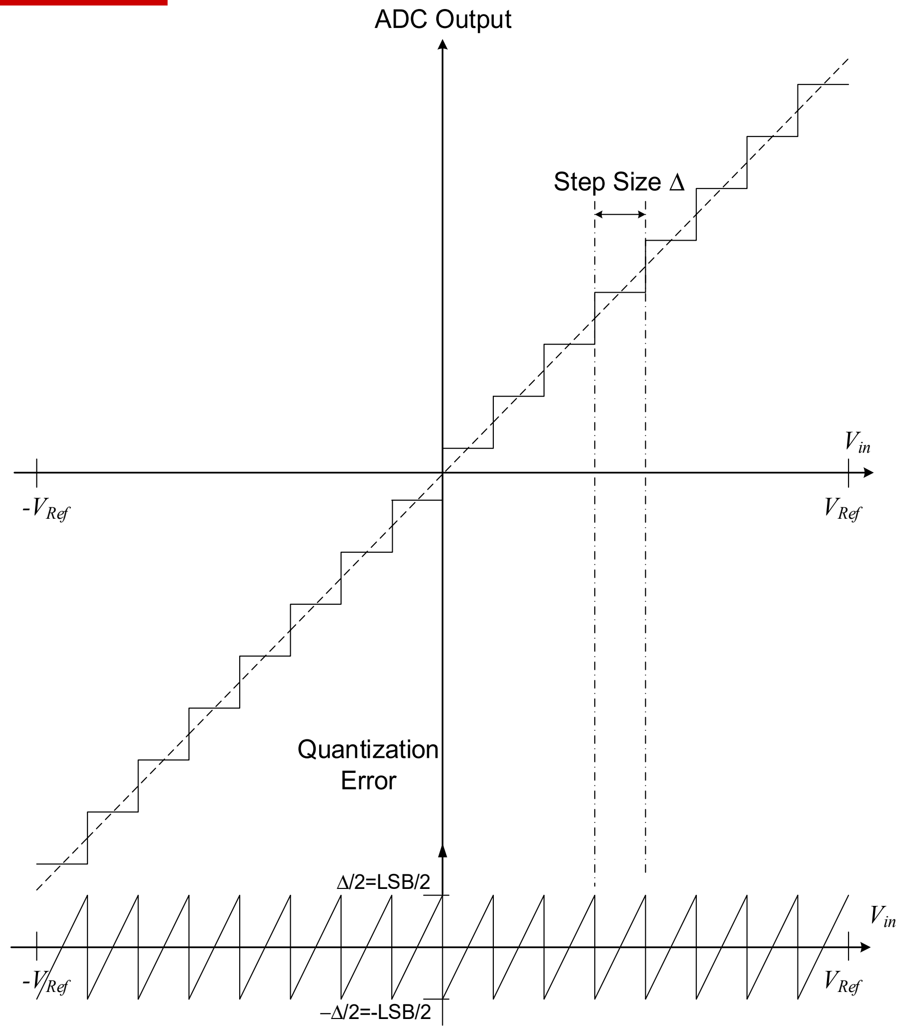


Sampling Rate: $f_s = 1/T_s$

Resolution N: $\Delta = V_{FS}/2^N$

Ideal A/D Converter Quantizer

- ADC Output = $\left[\dfrac{2^N V_{in}}{2V_{Ref}}\right]$
  - Where:
    - [x] is the integer value closest to x
    - N is the number of bits
    - V_{in} is the analog input signal
    - V_{Ref} is the ADC reference voltage
  - Usually in fully differential ADCs:
    - $V_{FS} = 2V_{Ref}$
  - The step size Δ is given by:
    - $\Delta = V_{FS}/2^N$



PERFORMANCE METRICS

Common ADC Performance Metrics

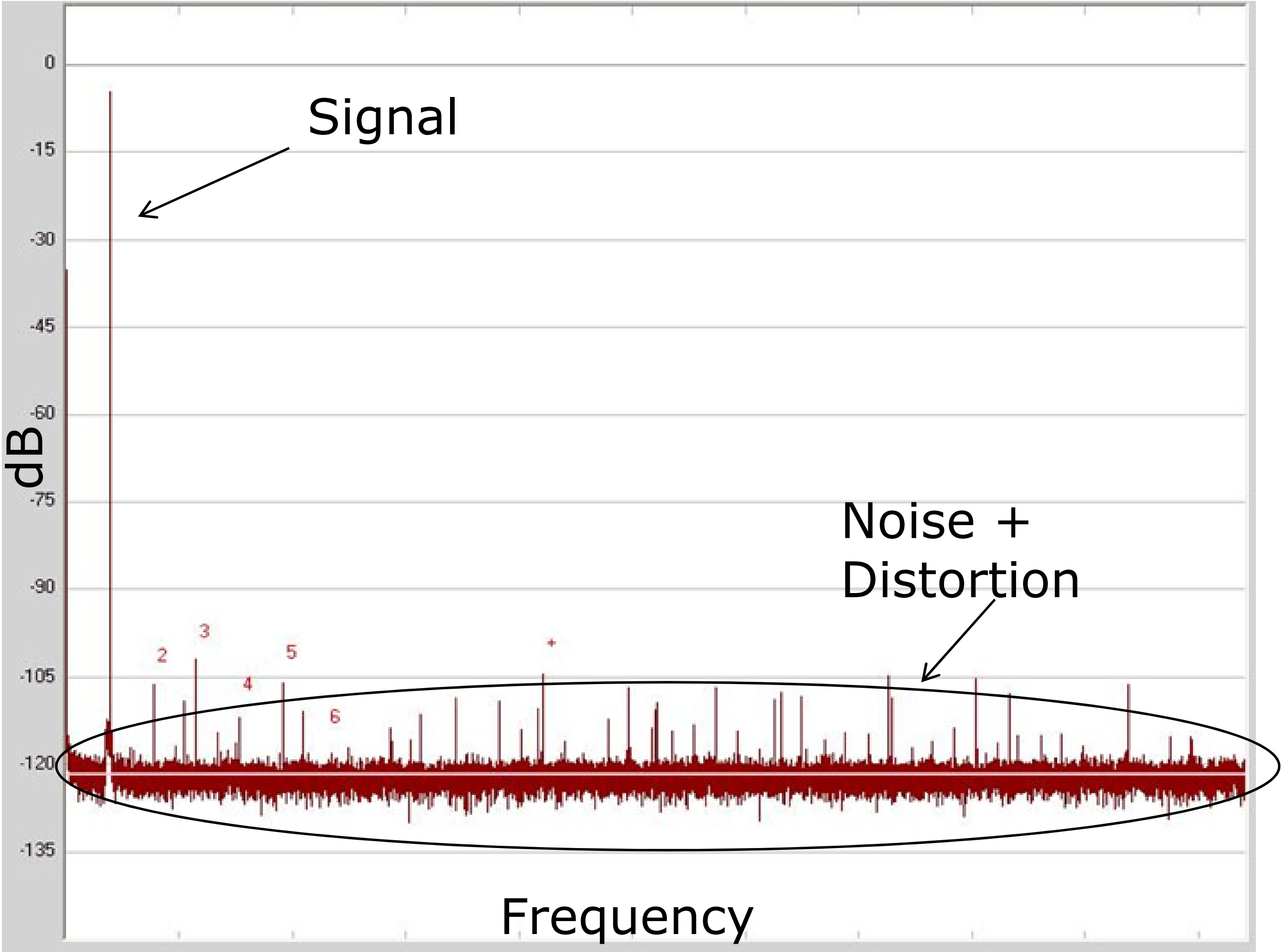
- Sampling Rate
- Resolution

Define the converter

- Signal-to-Noise Ratio (SNR)
- Signal-to-Noise-and-Distortion Ratio (SNDR or SINAD)
- Noise Spectral Density (NSD)
- Spurious-Free Dynamic Range (SFDR)
- Total Harmonic Distortion (THD)
- Inter-modulation Distortion (IMD)
- Integral Non-linearity (INL)
- Differential Non-linearity (DNL)
- Offset error
- Gain Error
- Bit-Error-Rate (BER)
- Power consumption
- Clock jitter
- Input bandwidth
- Input impedance
- Input full-scale range

Signal-to-Noise Ratio[1]

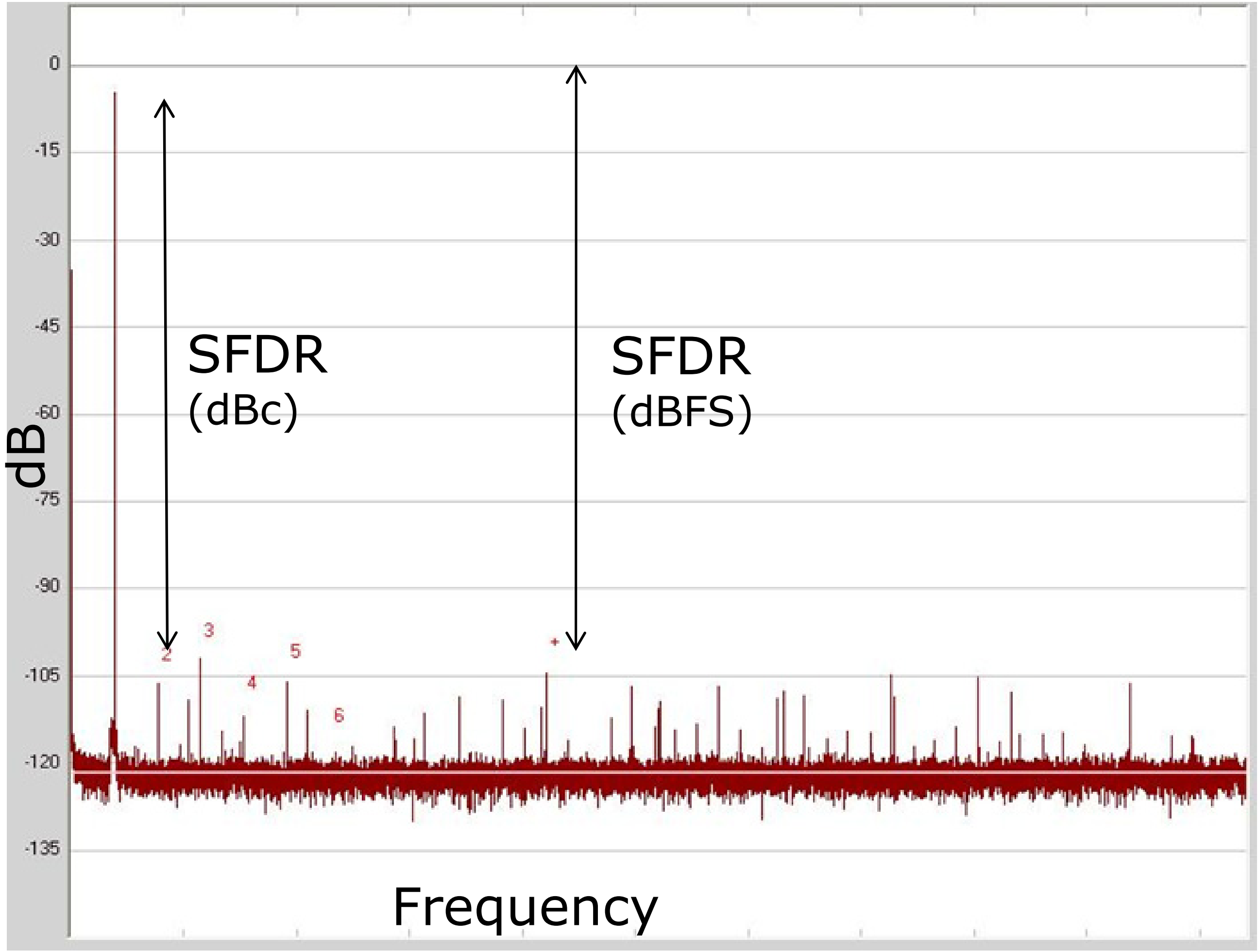
- SNR/SINAD are defined as the ratio of the signal power to the noise power excluding DC:
  - SNR (dBc) = 10log(Signal Power / Noise Power)
  - SINAD/SNDR (dBc) = 10log(Signal Power / (Noise + Distortion Power))
  - SNR (dBFS) = 10log(ADC FS Power / Noise Power)
  - SINAD/SNDR (dBFS) = 10log(ADC FS Power / (Noise + Distortion Power))
- NSD is the noise spectral density in dB/Hz:
  - NSD=-SNR-10log(f_s/2)



Spurious-Free-Dynamic-Range [1]

$$SFDR(\text{dBc}) = 10\log\left(\frac{\text{Signal Power}}{\text{Worst Harmonic or Spur Power}}\right)$$

$$SFDR(\text{dBFS}) = 10\log\left(\frac{\text{ADC Full Scale Power}}{\text{Worst Harmonic or Spur Power}}\right)$$

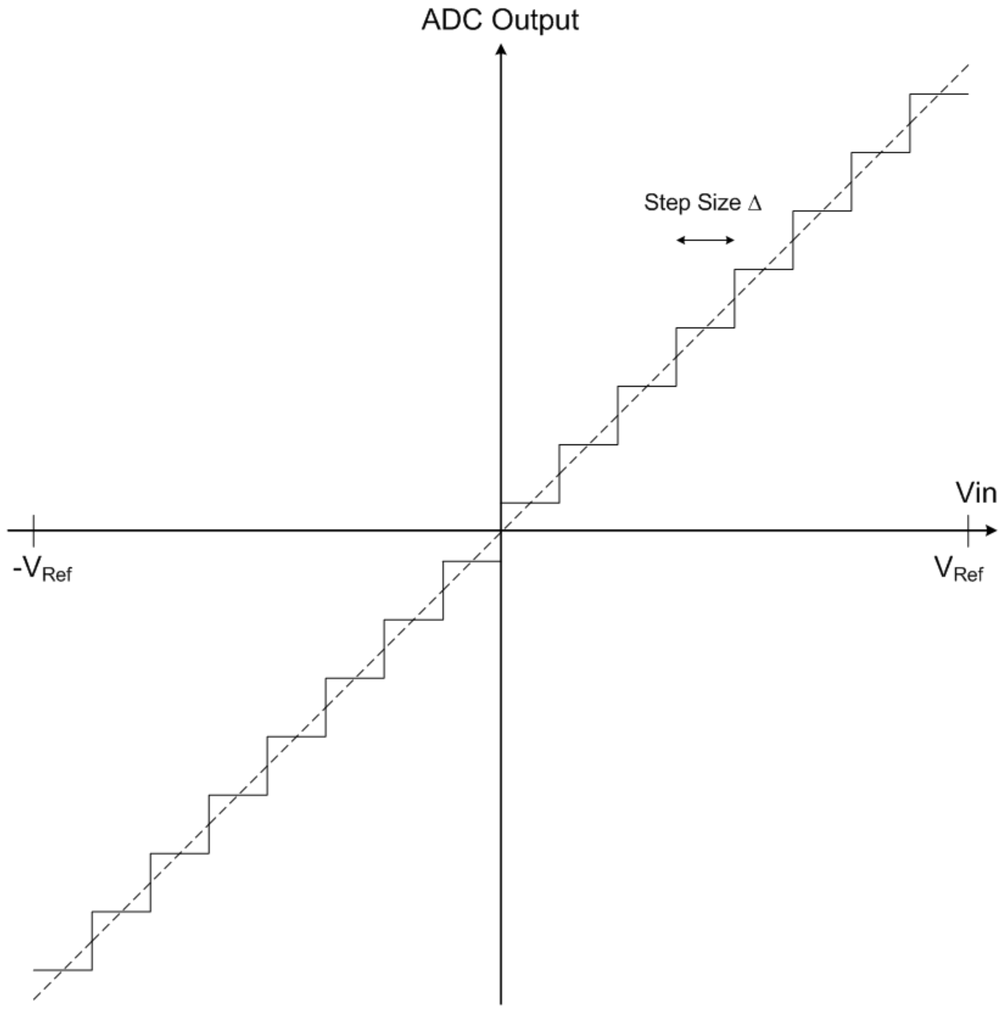


Ideal Quantizer

Shown:

- Offset = 0
- Gain error = 0
- DNL = 0
- INL = 0

- The DNL and INL capture the deviation of the transfer characteristic from the ideal stair-case



Non-Ideal Quantizer

Shown:

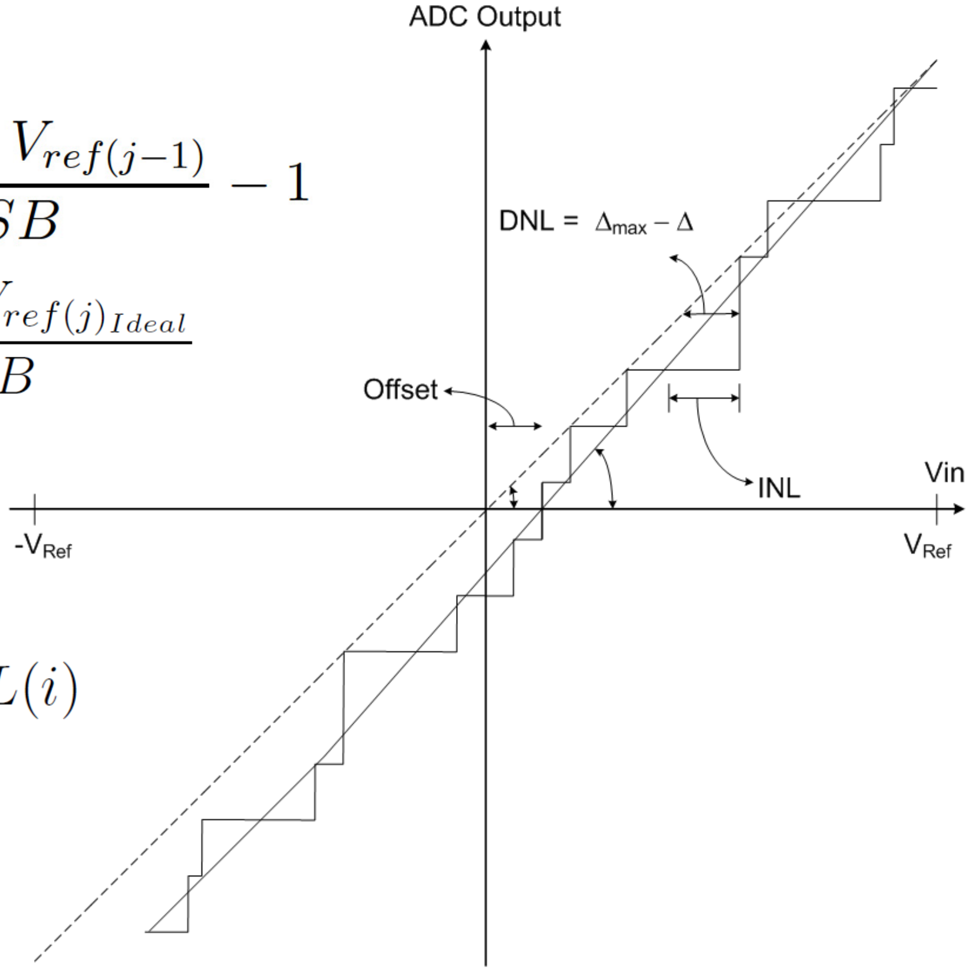
- Offset
- Gain error
- DNL
- INL

- Poor large signal non-linearity (INL)
- Poor small signal non-linearity (DNL)

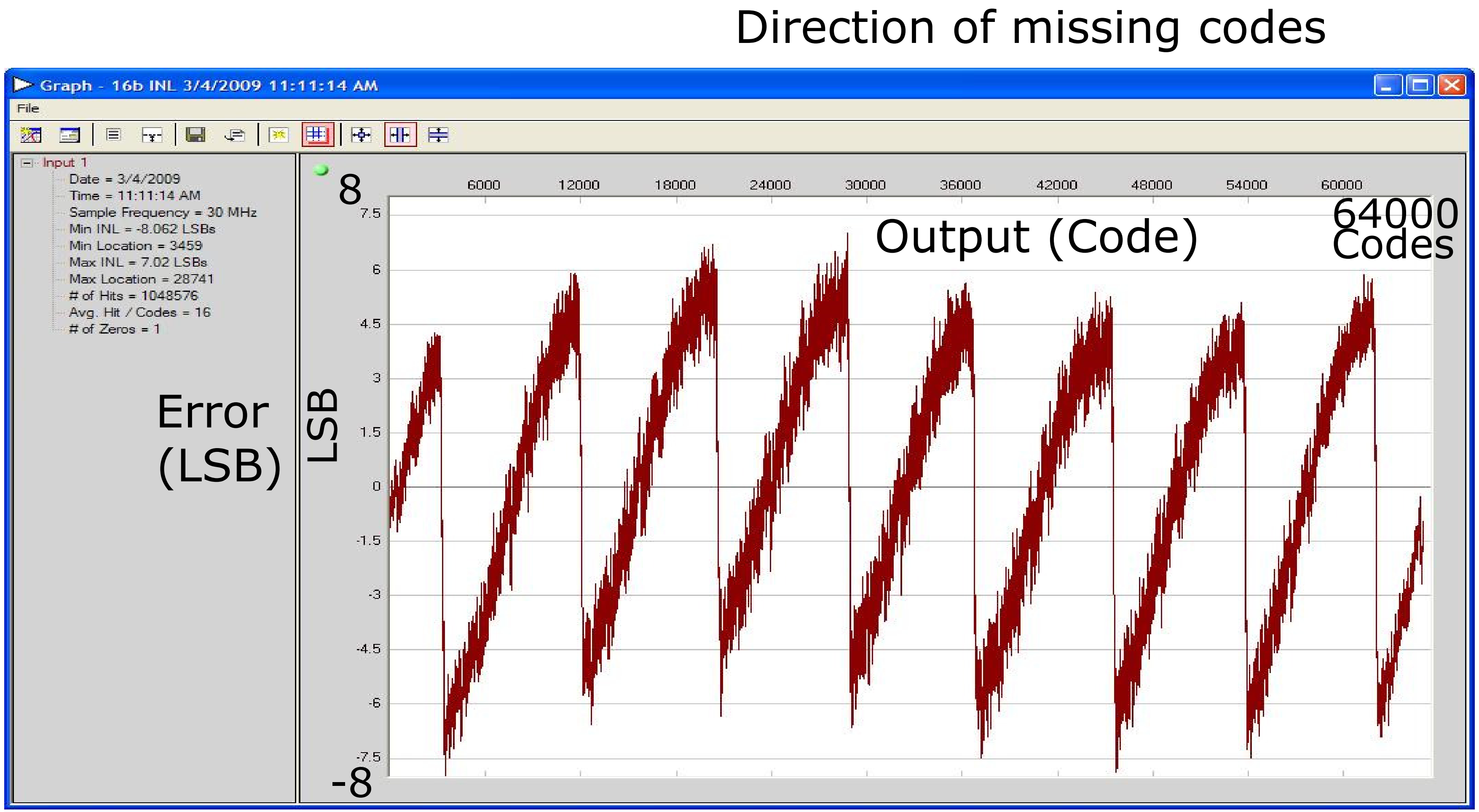
$$DNL(j) = \frac{V_{ref(j)} - V_{ref(j-1)}}{LSB} - 1$$

$$INL(j) = \frac{V_{ref(j)} - V_{ref(j)Ideal}}{LSB}$$

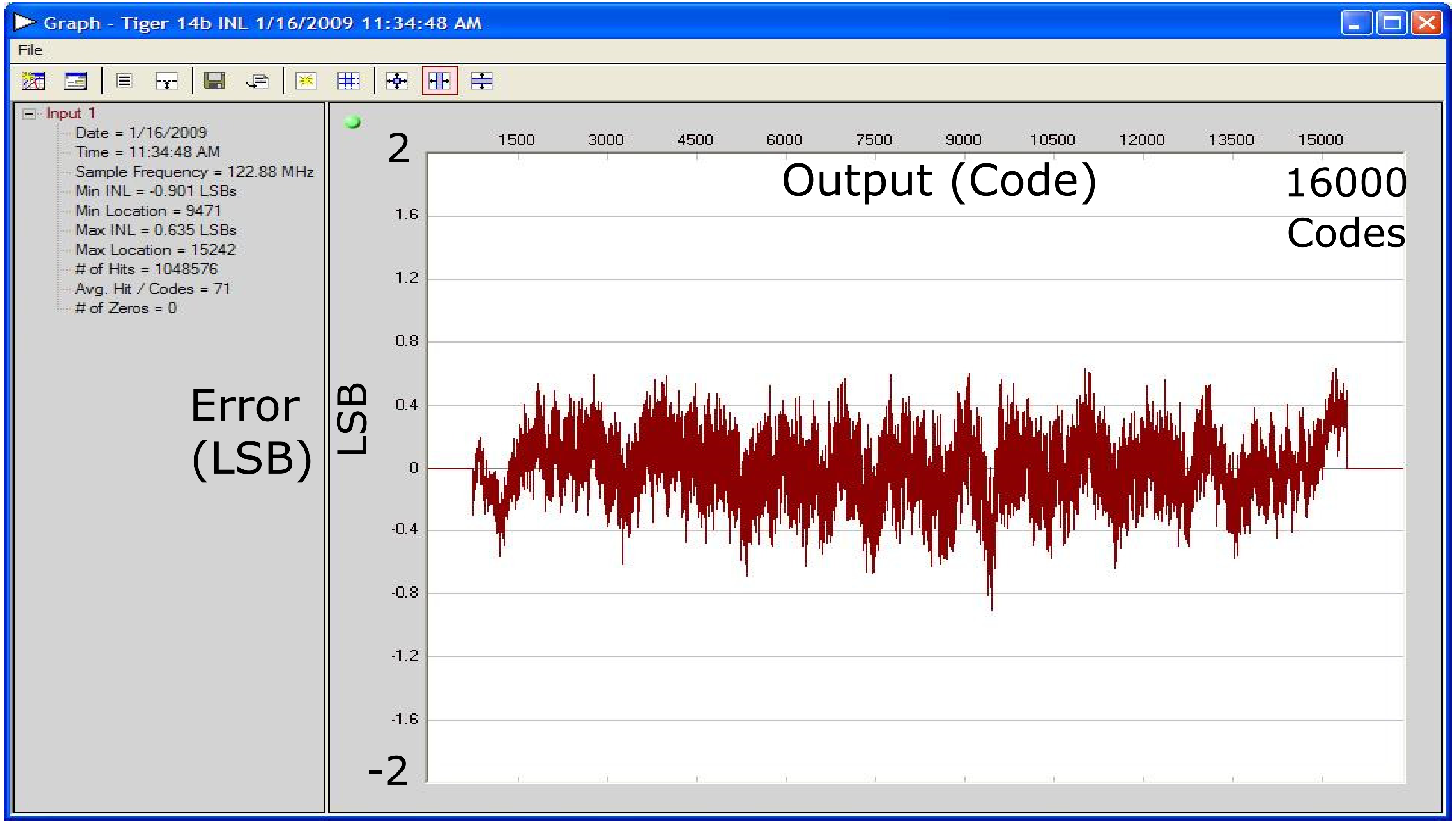
$$INL(j) = \sum_{i=1}^{j} DNL(i)$$



INL with Inter-stage Gain Error [1]



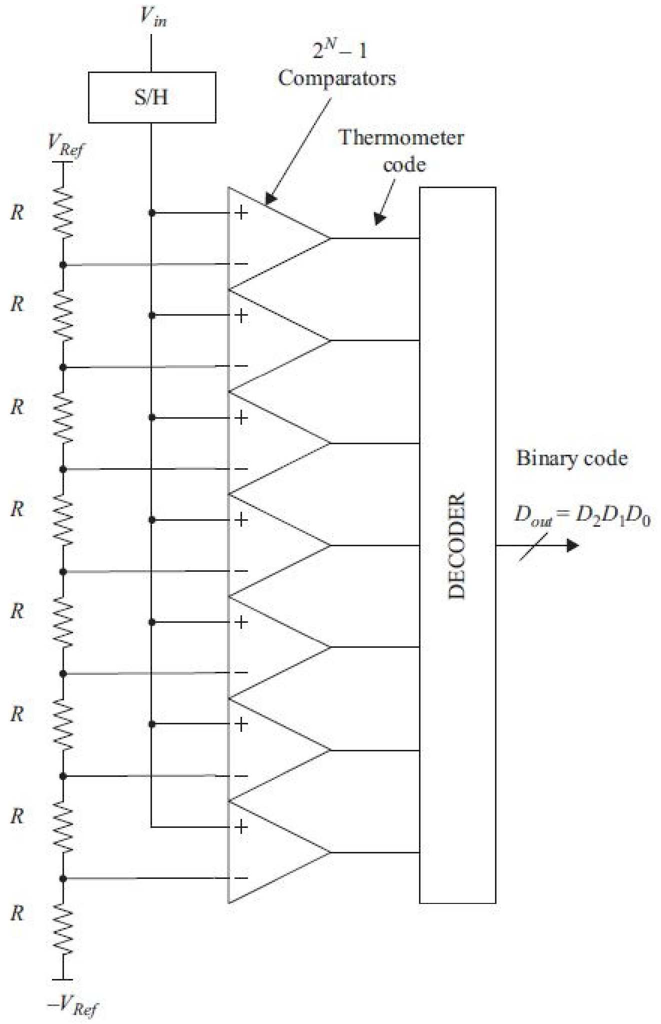
INL with Sub-LSB Error [1]



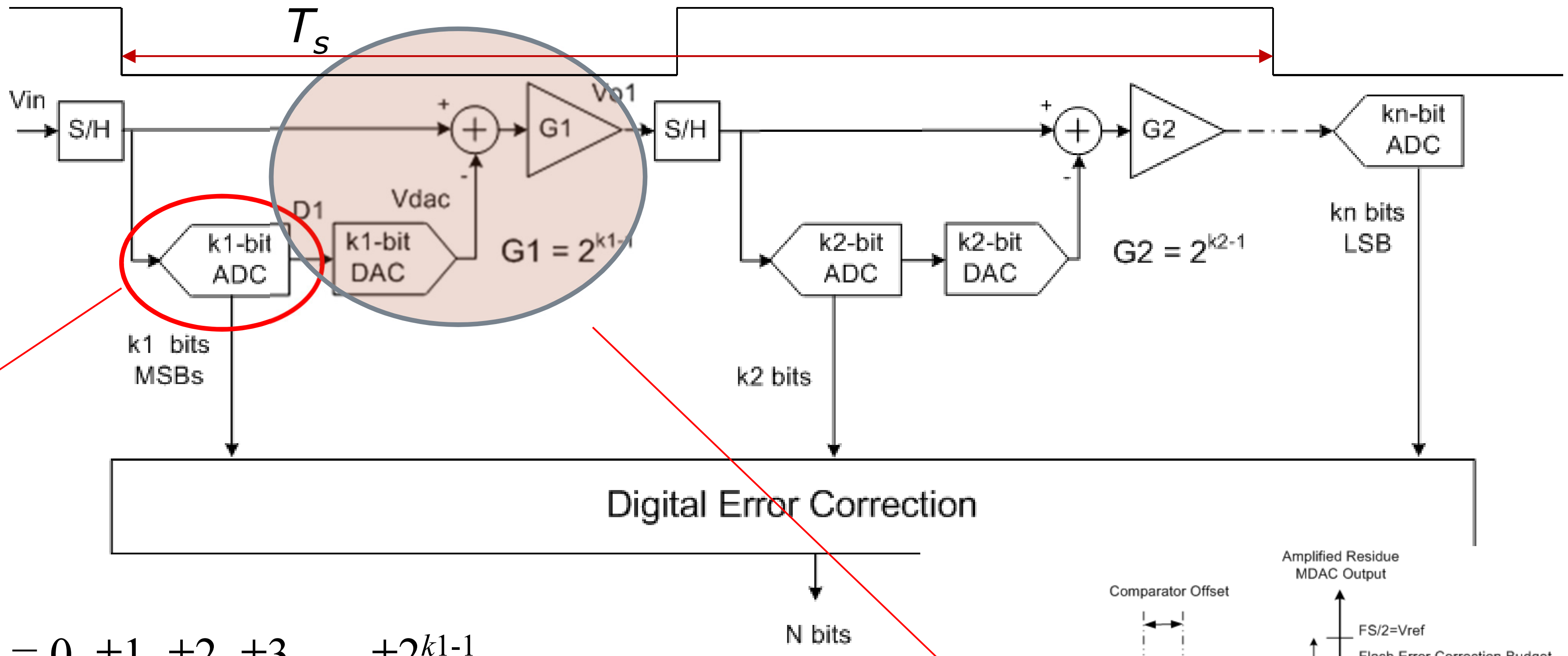
PIPELINED ADCS

Flash A/D Converter

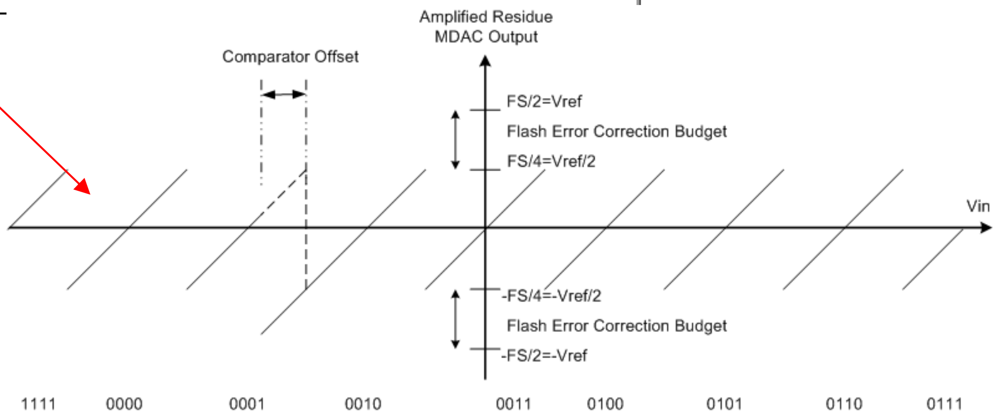
- Compares input to all threshold levels simultaneously
- Very high speed (f_s ~ GS/s):
- Not efficient for high resolutions:
  - Area & Power α 2^N
- Limited accuracy: ($\lesssim$ 6bit)
- For higher resolutions, multi-step ADCs are usually used



Pipelined A/D Converter



Accuracy not critical



$$D_1 = 0, \pm 1, \pm 2, \pm 3 \ \ldots, \pm 2^{k1\text{-}1}$$

$$V_{o1} = G_1(V_{in} - V_{dac})$$

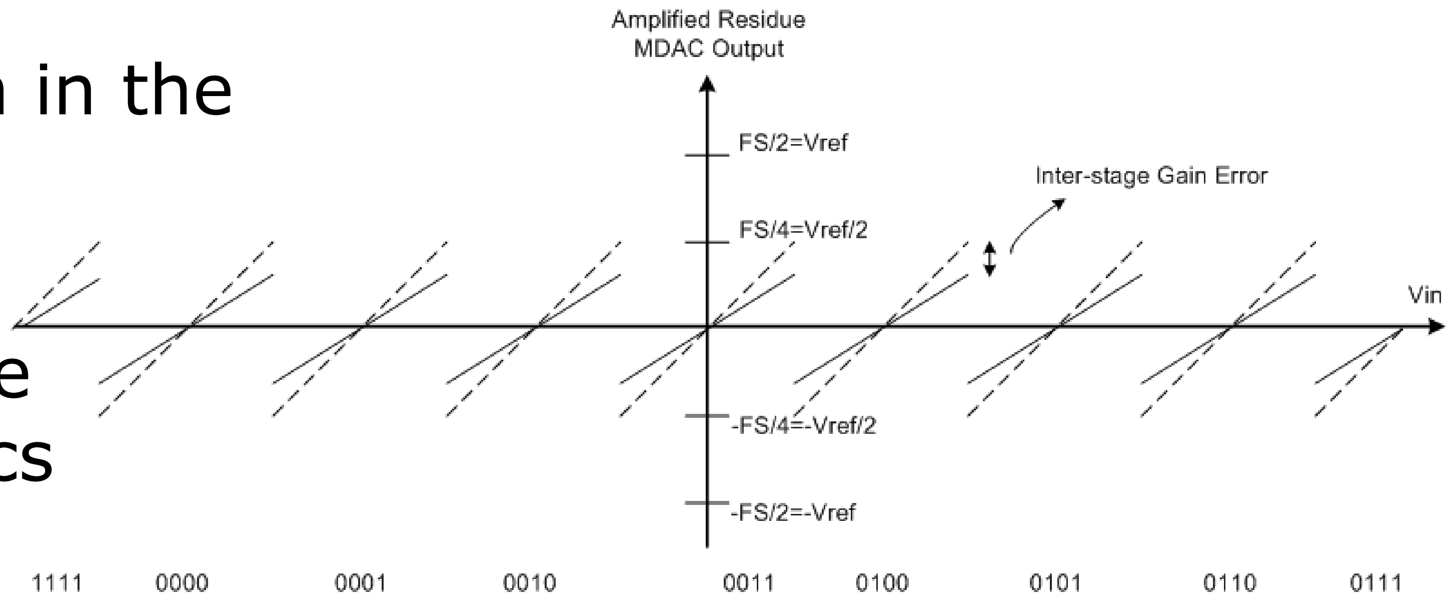
$$V_{o1} = G_1\left(V_{in} - \frac{D_1 \cdot V_{Ref}}{2^{k1-1}}\right)$$

$$G_1 = 2^{k1-1}$$

NON-IDEALITIES IN PIPELINED ADCS

Inter-stage Gain Errors

- In pipeline and pipe-SAR ADCs
- Due to non-ideal gain in the inter-stage amplifier
- Leads to breaks in the transfer characteristics



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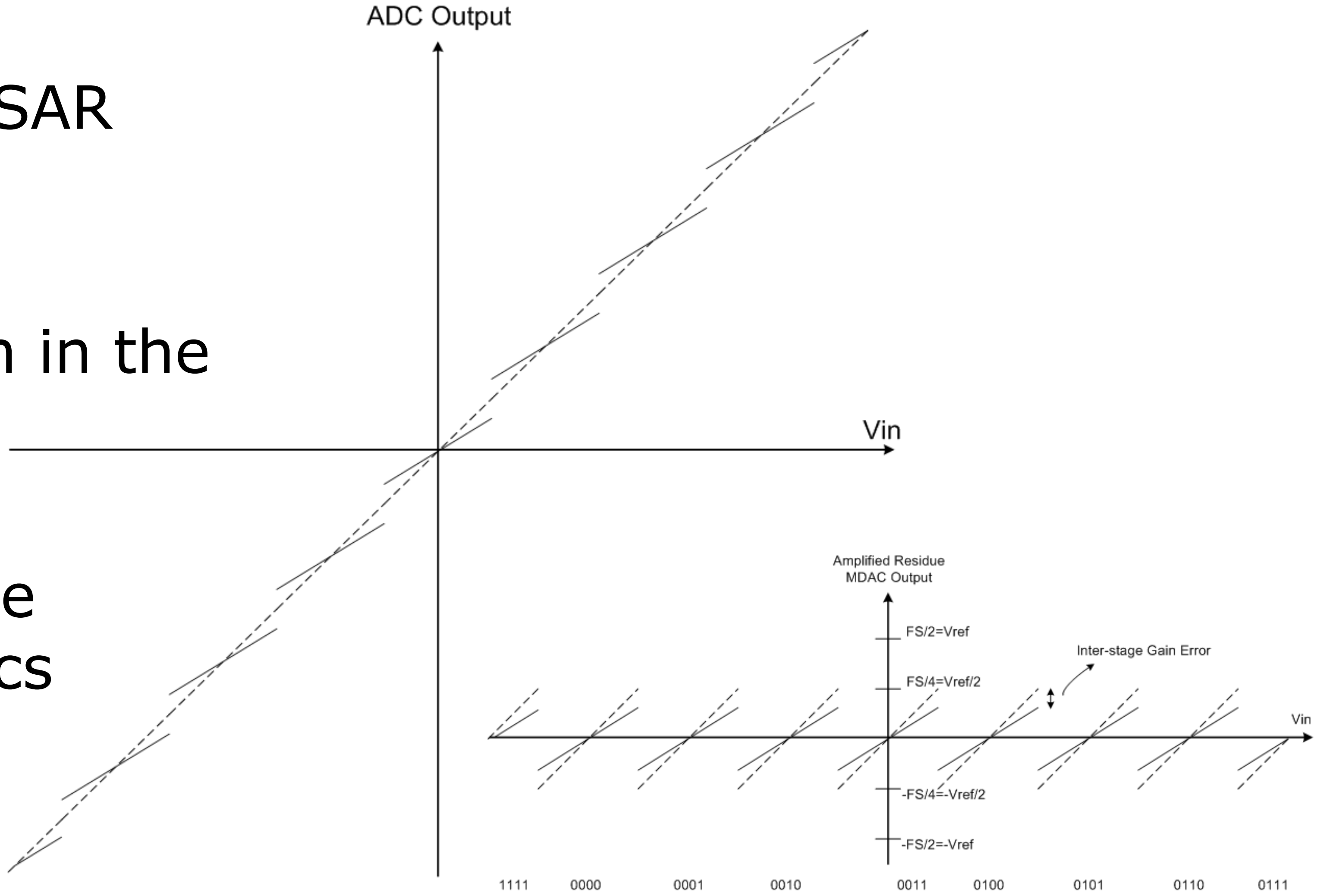
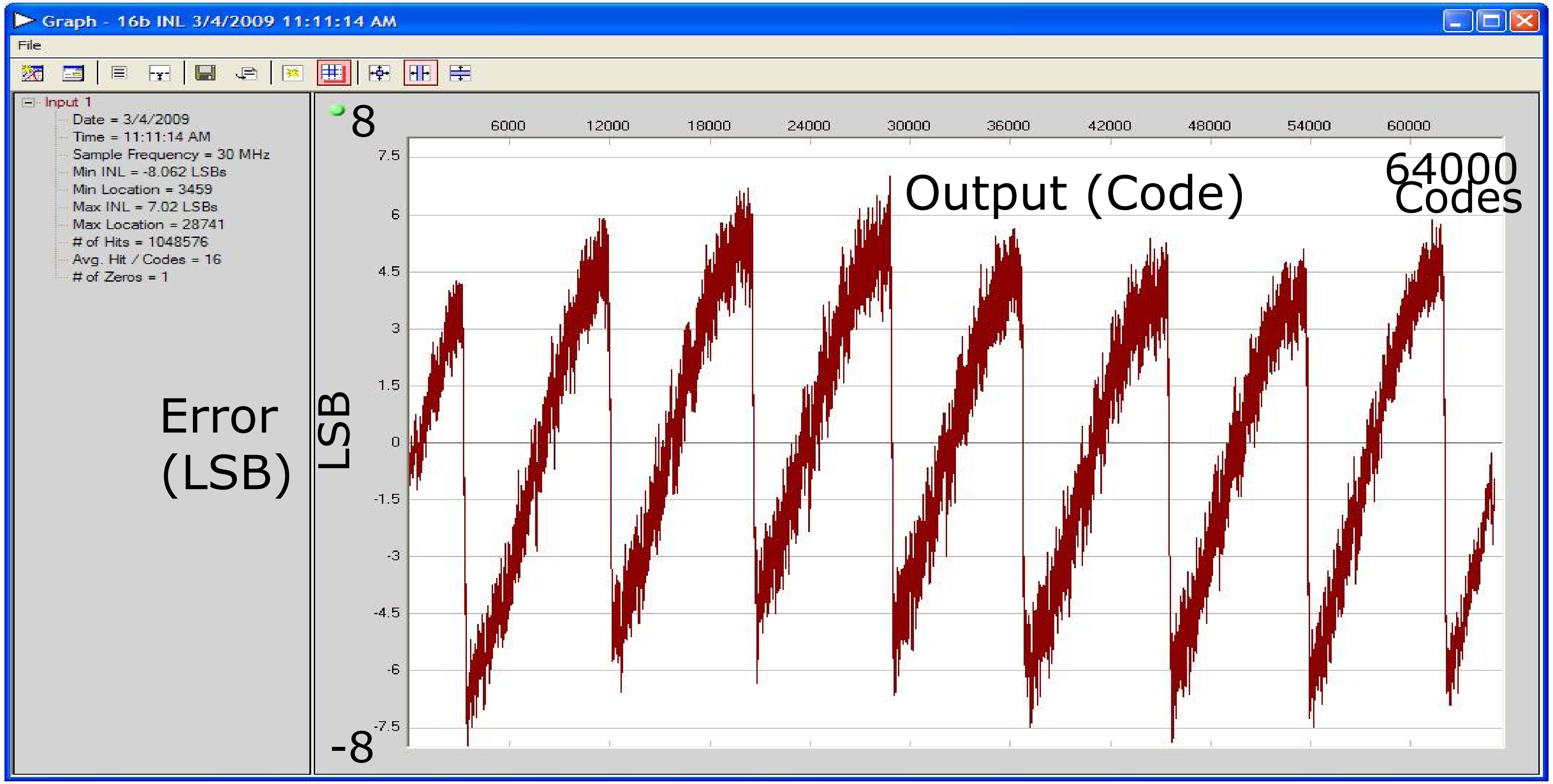
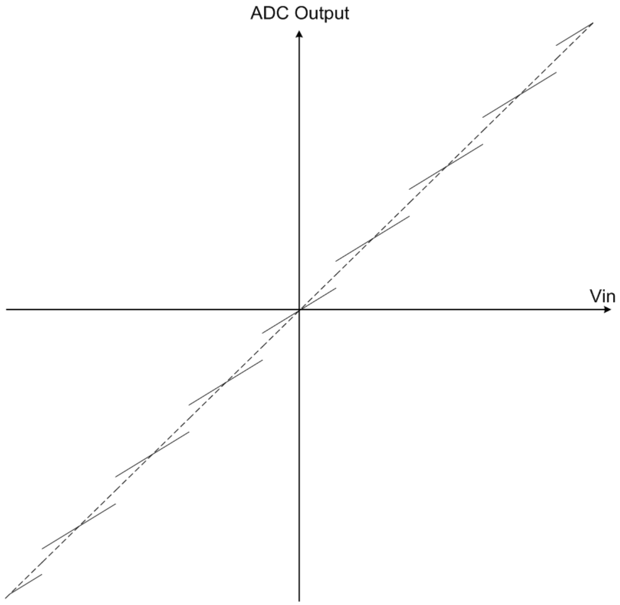


INL with Inter-stage Gain Error [1]

Direction of missing codes

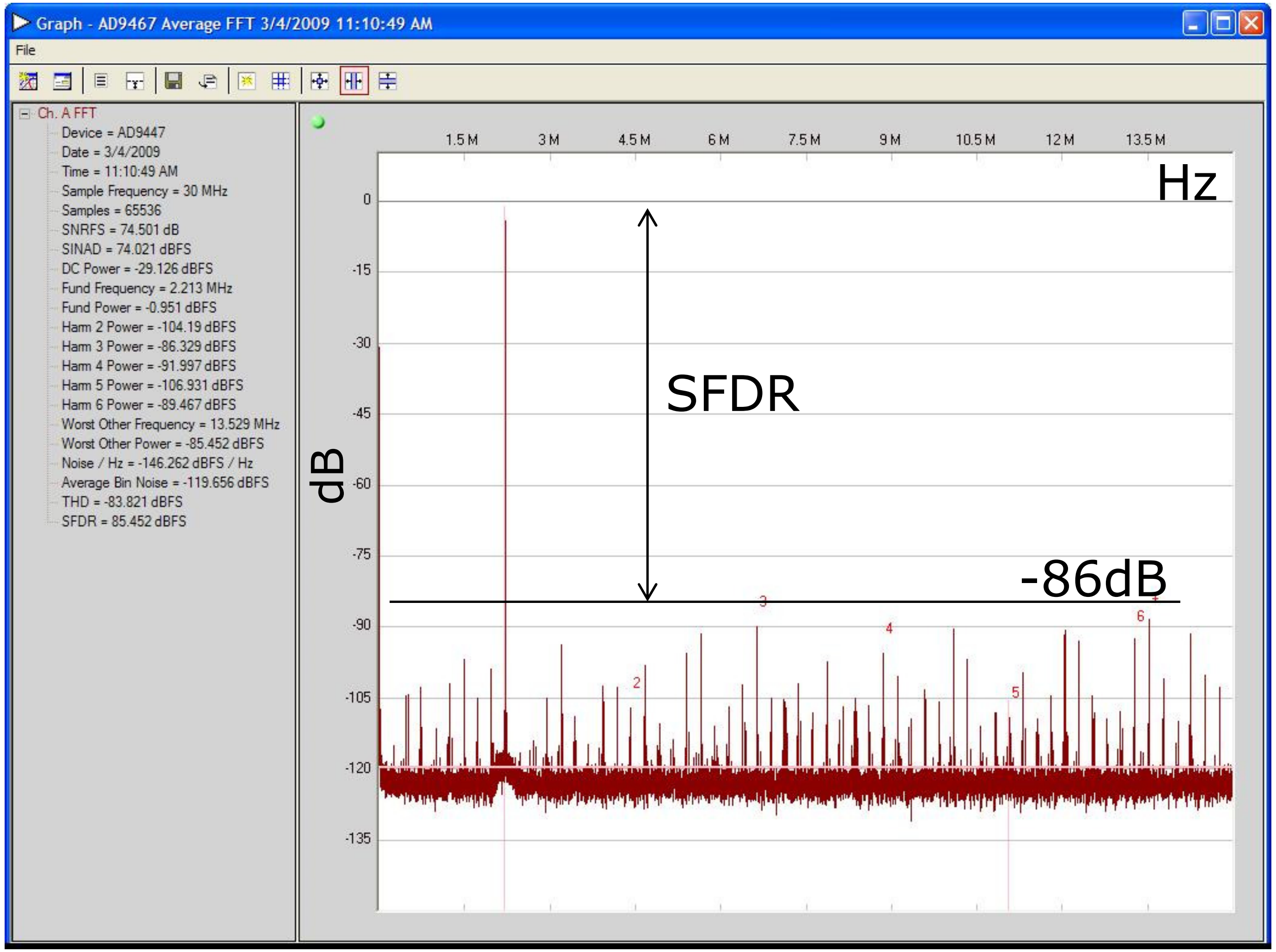


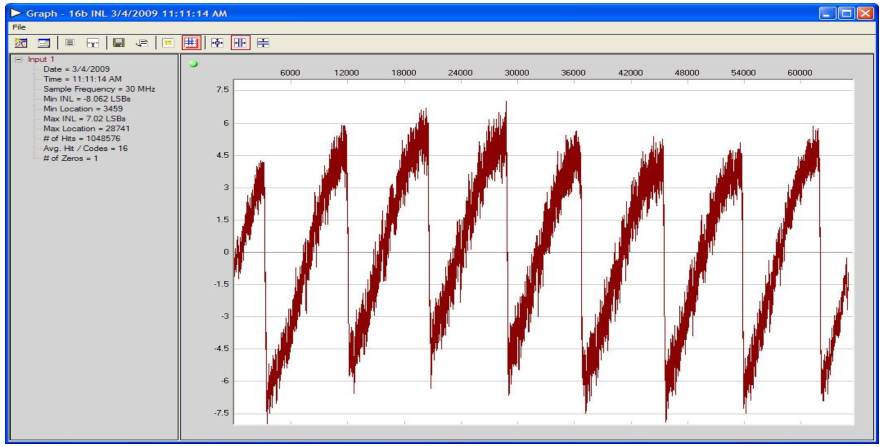


n1~3, n~13
SFDR~6n+3n1~87dB*

* H. Pan and A.A. Abidi, "Spectral Spurs due to Quantization in Nyquist ADCs," *IEEE Trans. Circuits and Systems-I: Regular Papers*, 51(8), pp. 1422–1438, August 2004.

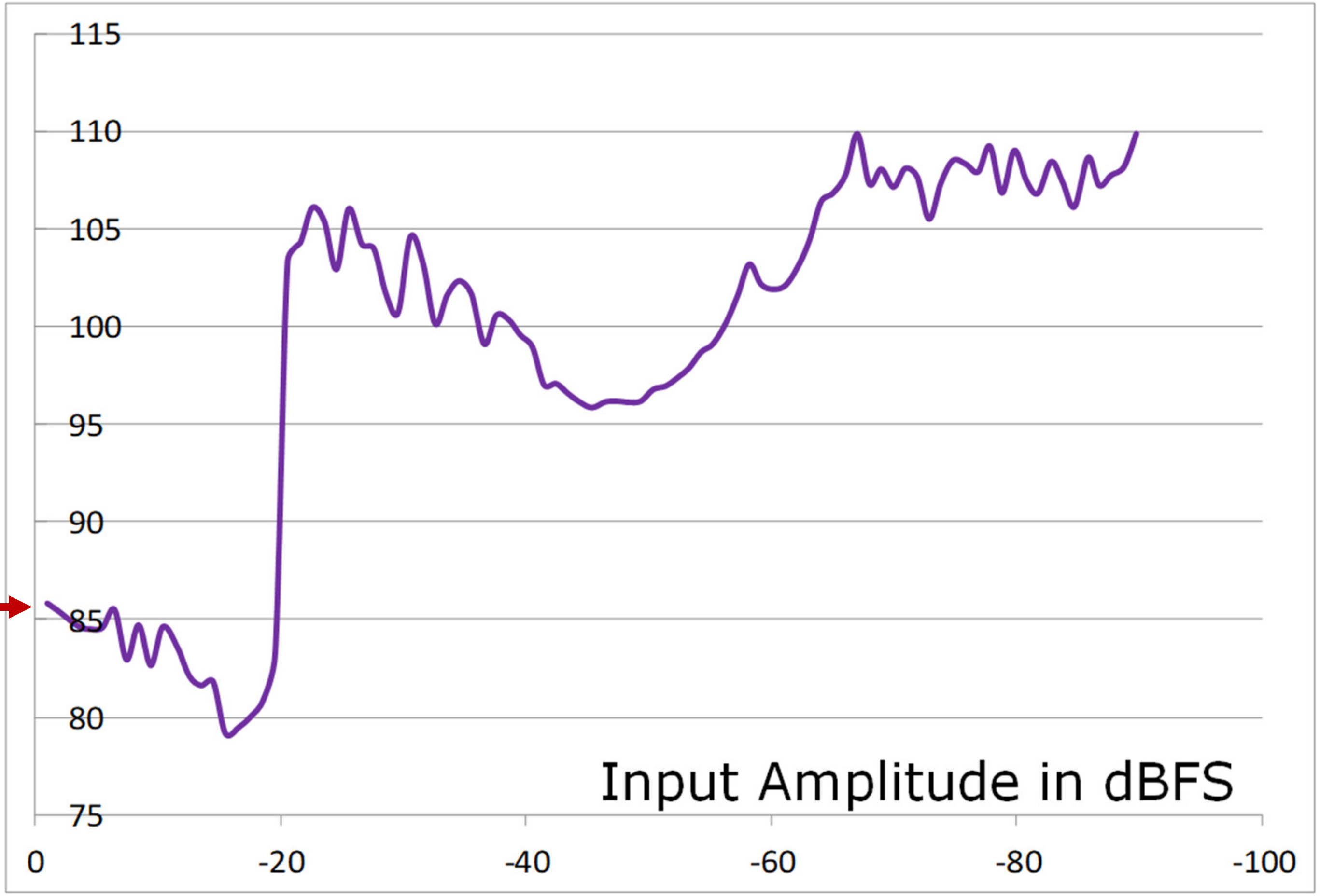
Example: FFT with IGE Errors [1]
SNR~75dB, SFDR~86dB

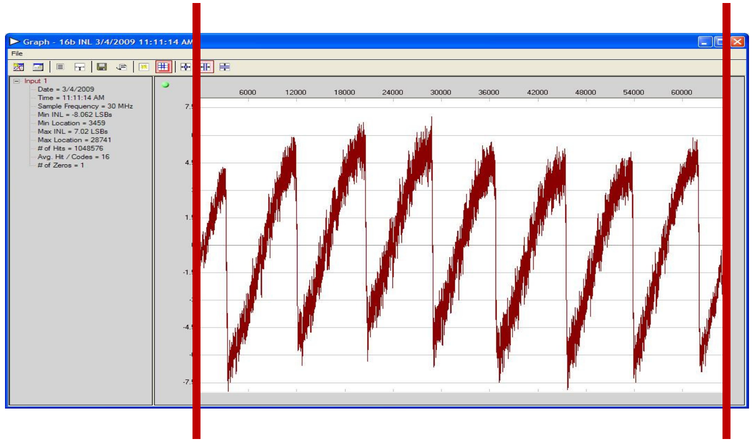




n1~3, n~13
SFDR~6n+3n1~87dB

Effect of INL Sawtooth Error on SFDR*
At 0dBFS, SFDR ~ 86dB



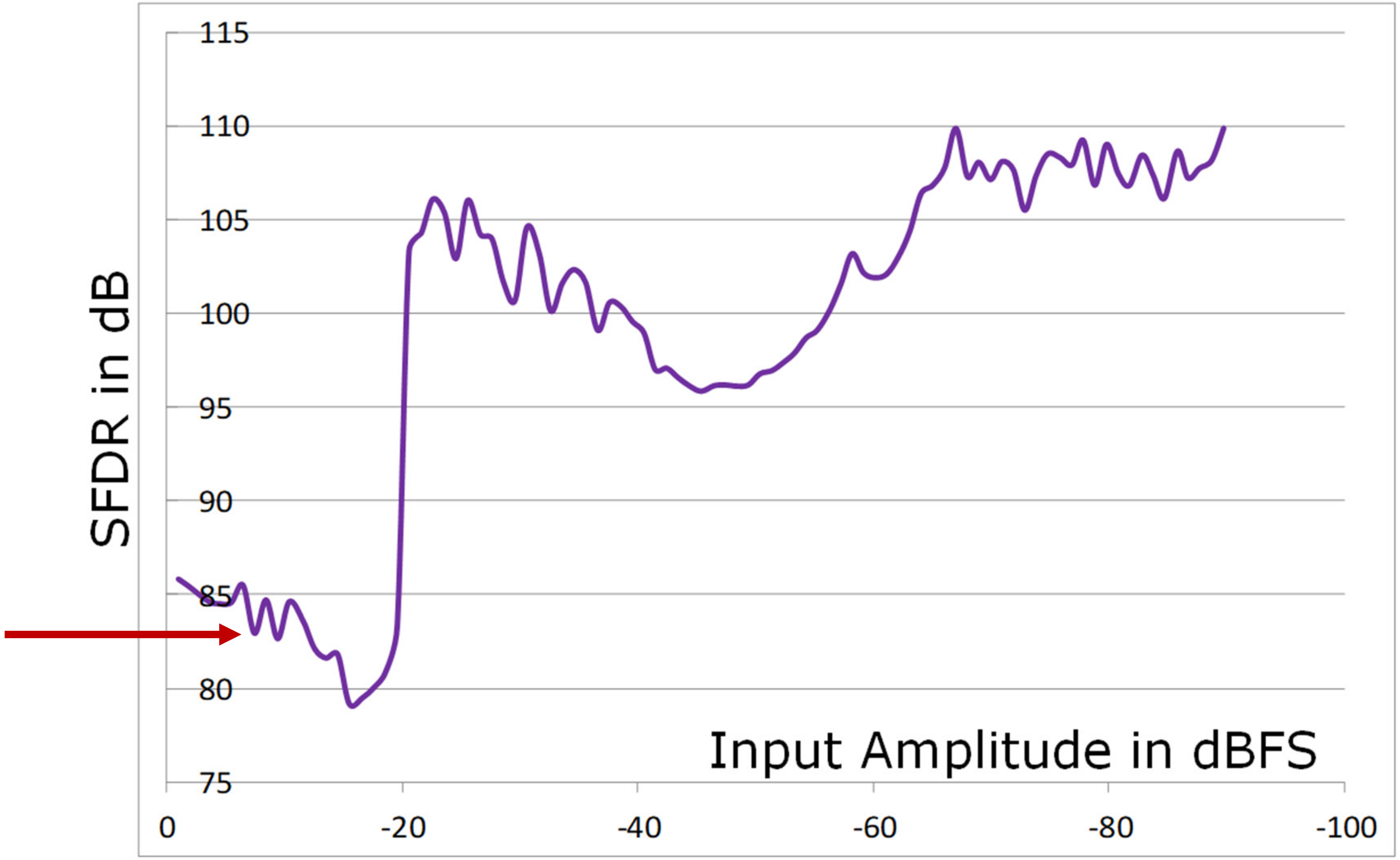


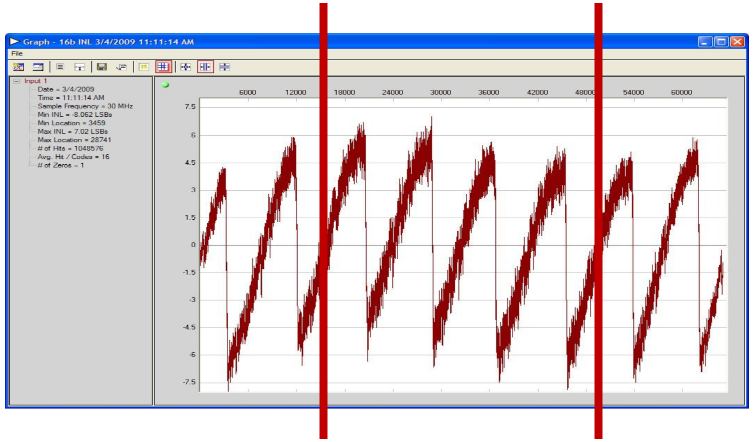
n1~3, n~13

SFDR~6n+3n1~87dB

* A.M.A. Ali, *High speed data converters*, Institution of Engineering and Technology (IET), London, UK, 2016.

Effect of INL Sawtooth Error on SFDR*
At -6dBFS, SFDR ~ 84dB

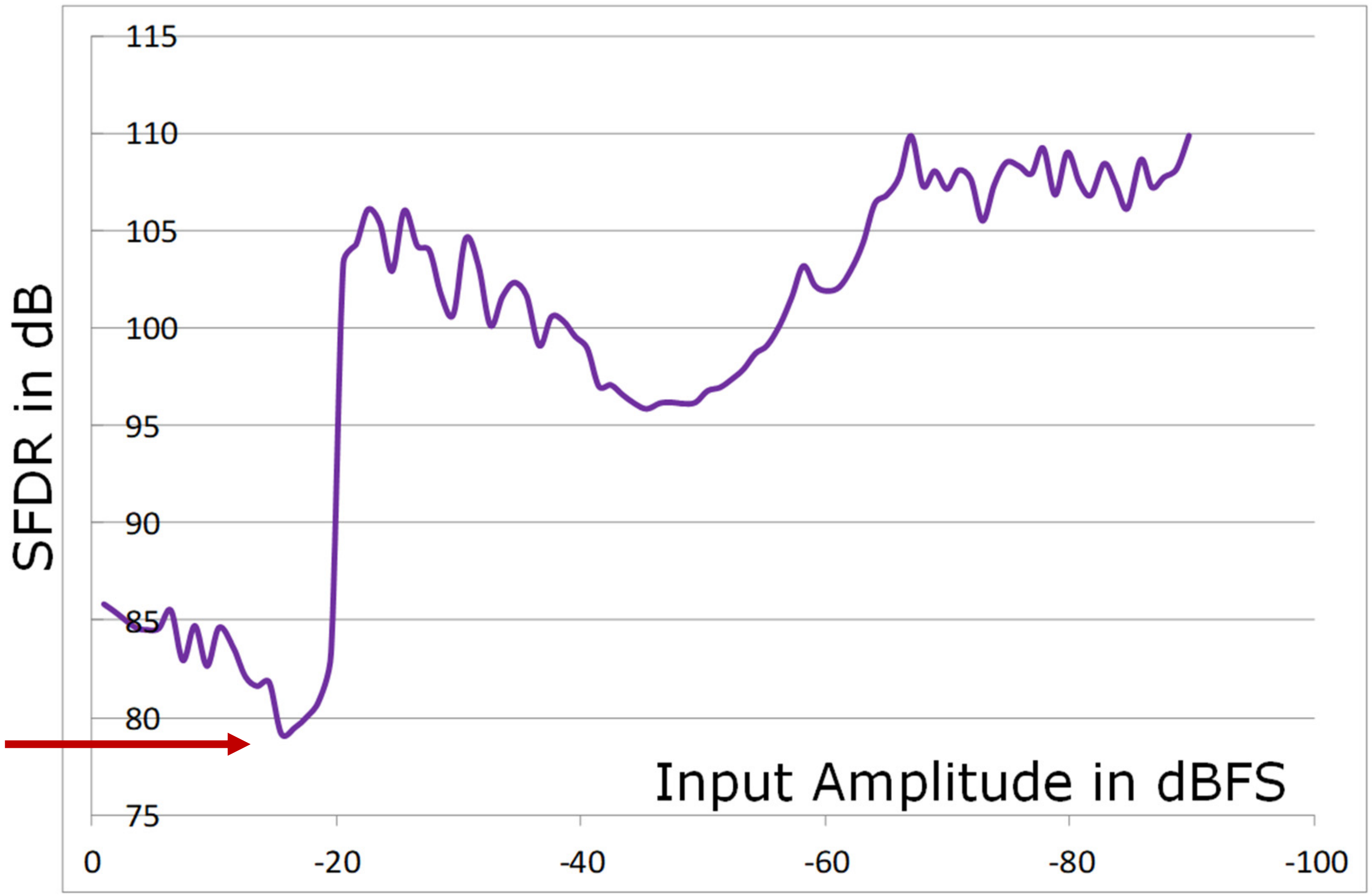


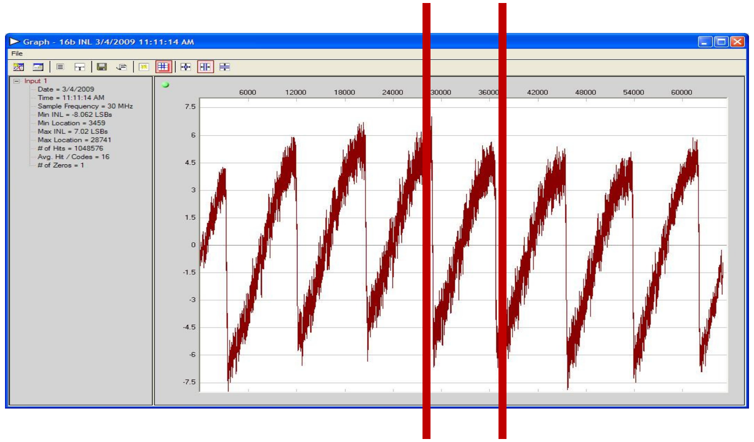


n1~2, n~13
SFDR~6n+3n1~84dB

* A.M.A. Ali, *High speed data converters*, Institution of Engineering and Technology (IET), London, UK, 2016.

Effect of INL Sawtooth Error on SFDR*
At -18dBFS, SFDR ~ 78dB



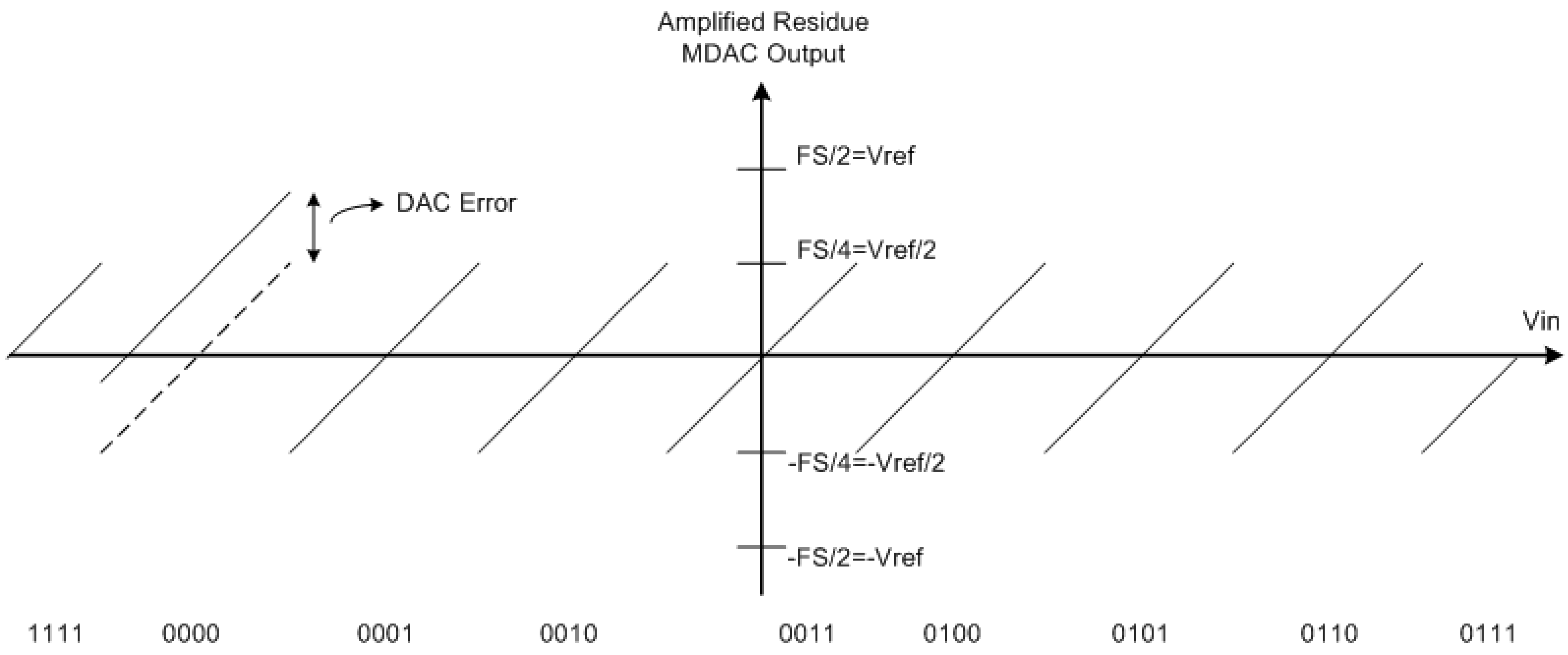


n1~0, n~13
SFDR~6n+3n1~78dB

* A.M.A. Ali, *High speed data converters*, Institution of Engineering and Technology (IET), London, UK, 2016.

First Stage Residue with Stage DAC Error

- In pipeline and pipe-SAR ADCs
- Due to non-idealities in the stage DAC
- Leads to breaks in the transfer characteristics



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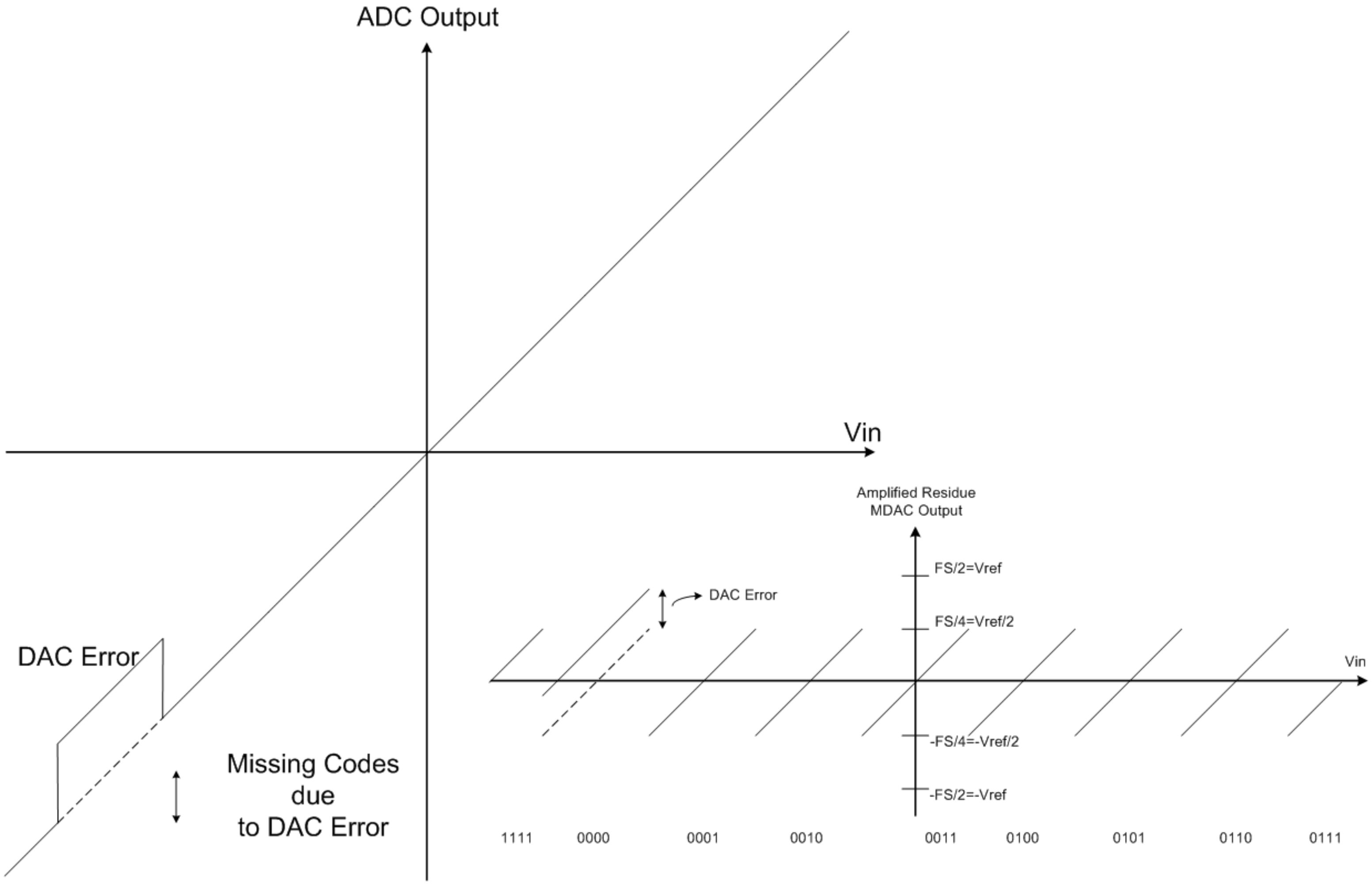
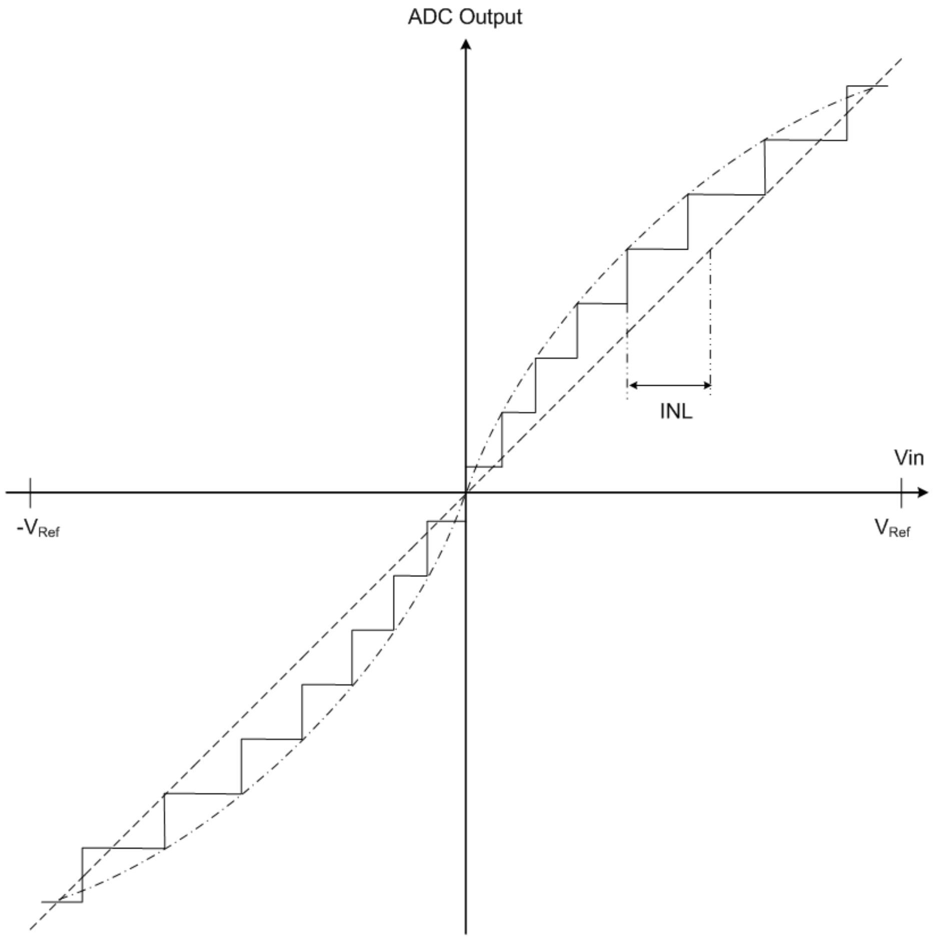


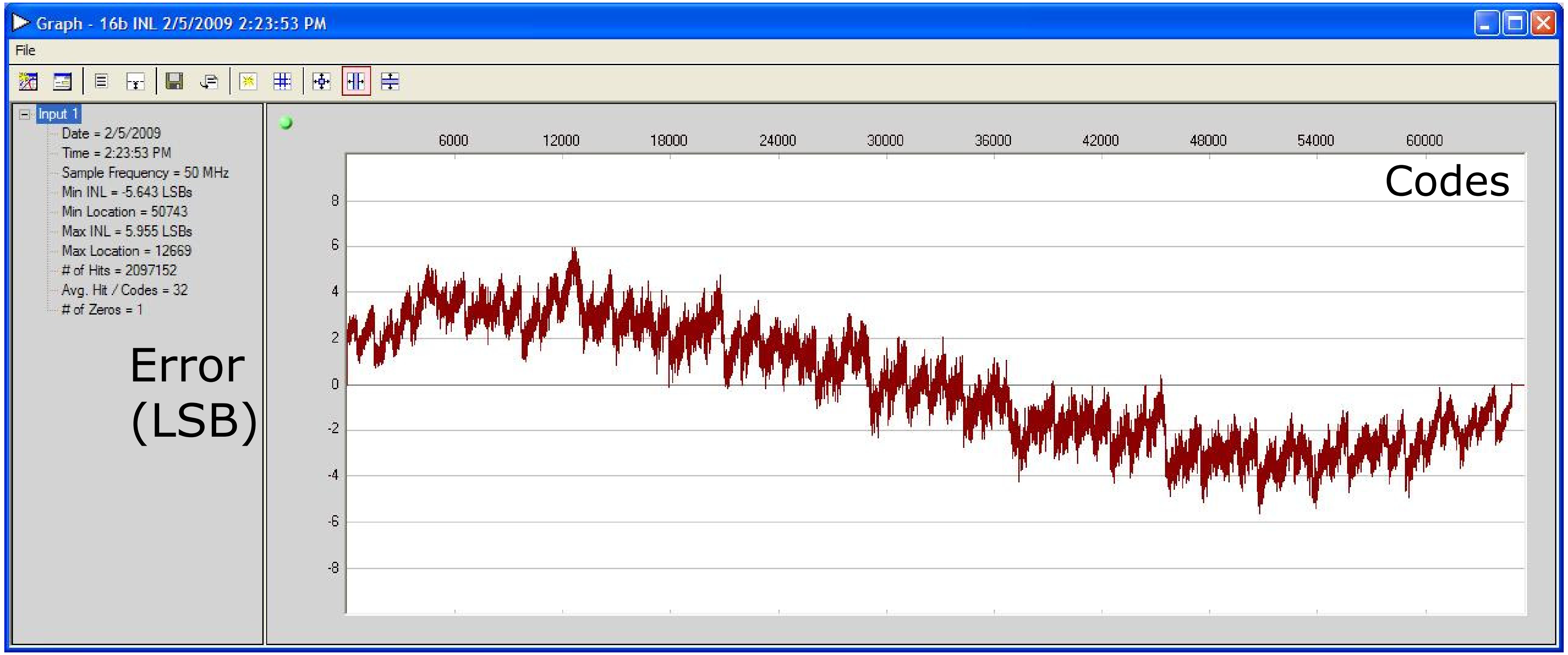
INL Showing DAC Errors [1]

Low Order Harmonic Distortion

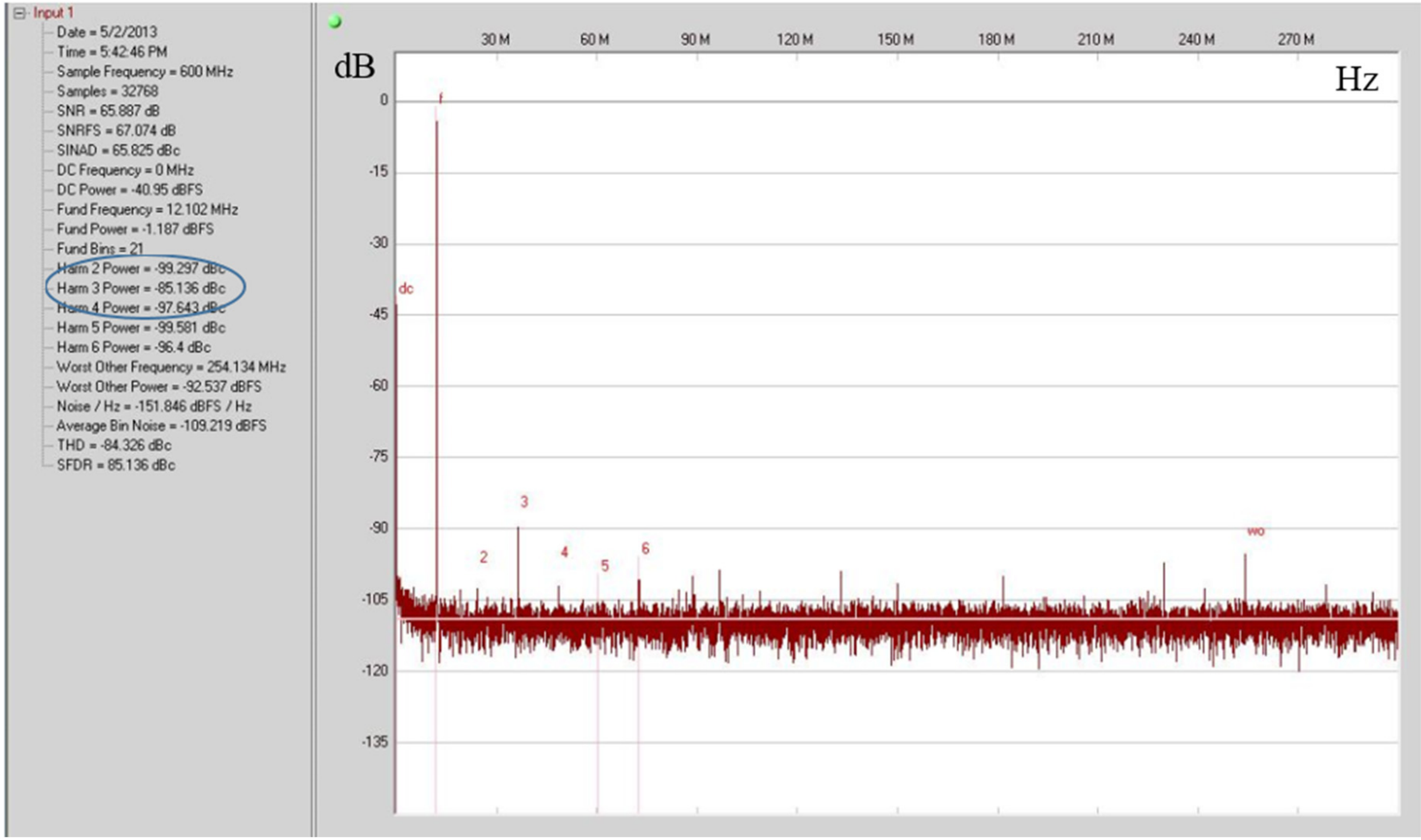
- Poor large signal non-linearity
- Harmonic distortion is generated in the frontend
- Third order compressive non-linearity



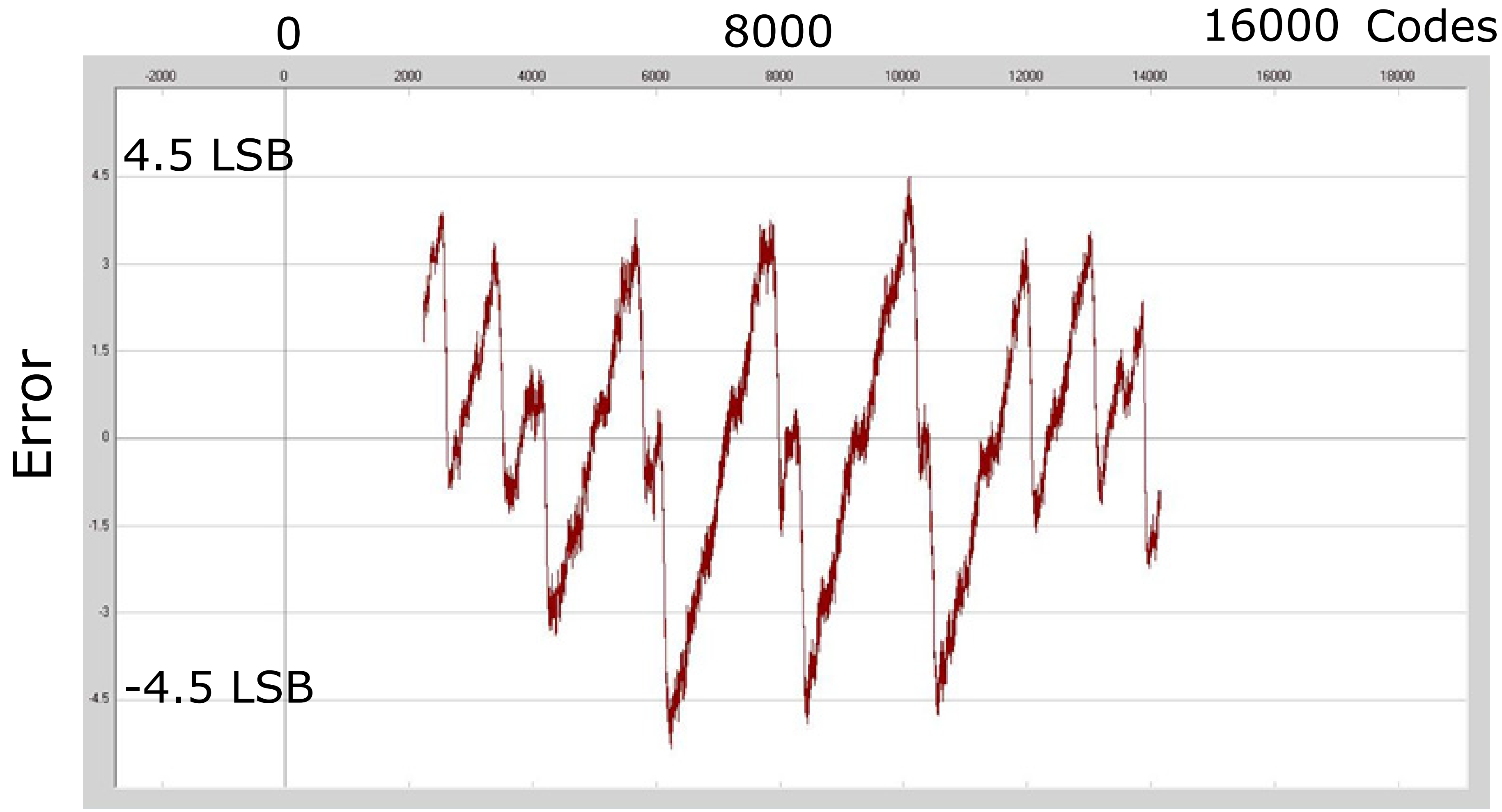
INL Showing 3rd Order Non-Linearity [1]



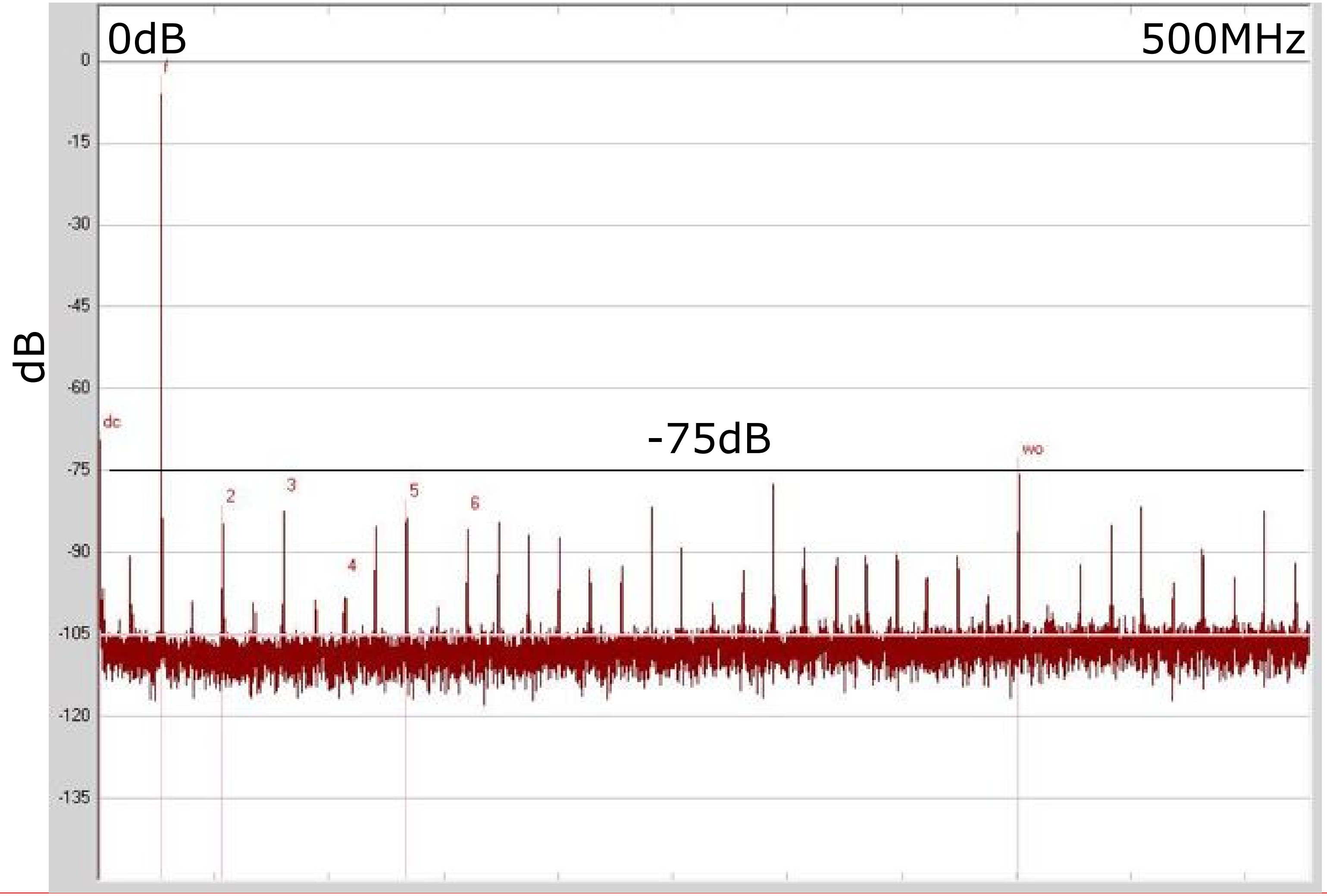
FFT Showing HD3 Non-linearity [1]



Memory and kick-back errors [1, 2]



Memory and kick-back errors [1, 2]



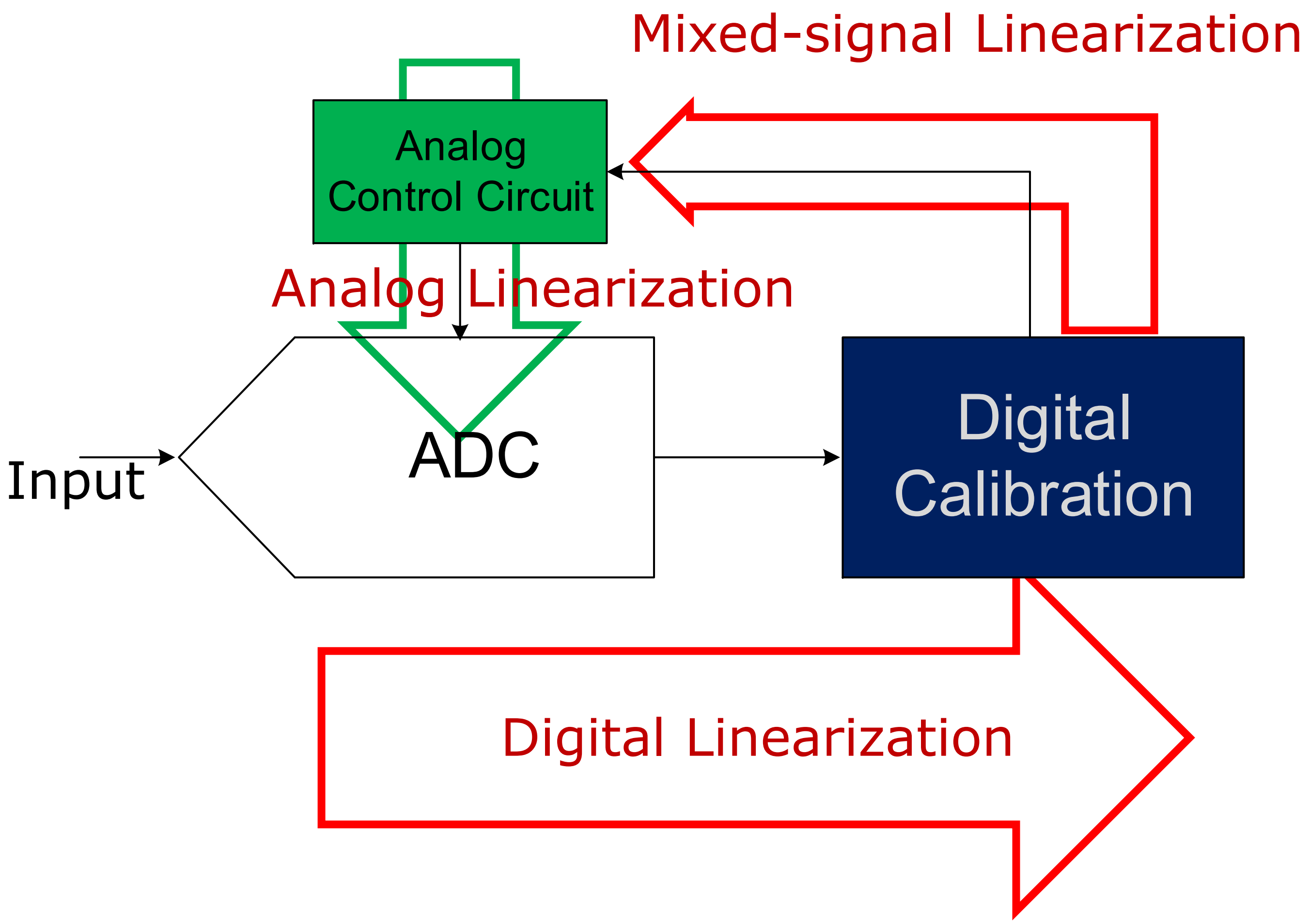
CALIBRATION TECHNIQUES: DIGITALLY-ASSISTED CONVERTERS

Why Calibration? Process Scaling

- Digital circuits have become more efficient with process scaling
- Analog circuits get more challenging and can be even less efficient
- In planar processes, finer geometry gives:
  - Faster switches
  - Lower parasitics
- But …
  - Lower output impedance
  - Lower intrinsic gain
  - Worse dynamic range
- FinFETs are more analog friendly, but are not getting faster
- Digital processing can be used to correct for analog and interleaving non-idealities

Calibration Types and Components

- Using a combination of analog and digital signal processing
- Correction and estimation
- Foreground Calibration
  - Fixed
  - May need an input stimulus
- Background Calibration
  - Converters can measure their own performance without disrupting normal operation and adaptively fix their non-idealities
  - Tracks process, supply, temperature, aging, etc.



Real World Challenges

- Improve performance and lower power consumption
- No disruption to normal operation => background
  - Combine foreground and background calibrations as needed
- Robustness with input amplitude, input frequency, sample rate, supply, temperature, etc.
- Convergence time
- Manufacturability

ADC Impairments

- Quantizer impairments:
  - Inter-stage gain and settling errors (IGE)
  - Inter-stage memory errors (IME)
  - DAC errors
  - Reference errors
  - MDAC amplifier non-linearity
- Sample-and-hold impairments:
  - Kick-back errors
  - Front-end non-linearity
- Interleaving impairments:
  - Offset and gain mismatch errors
  - BW/timing mismatch errors

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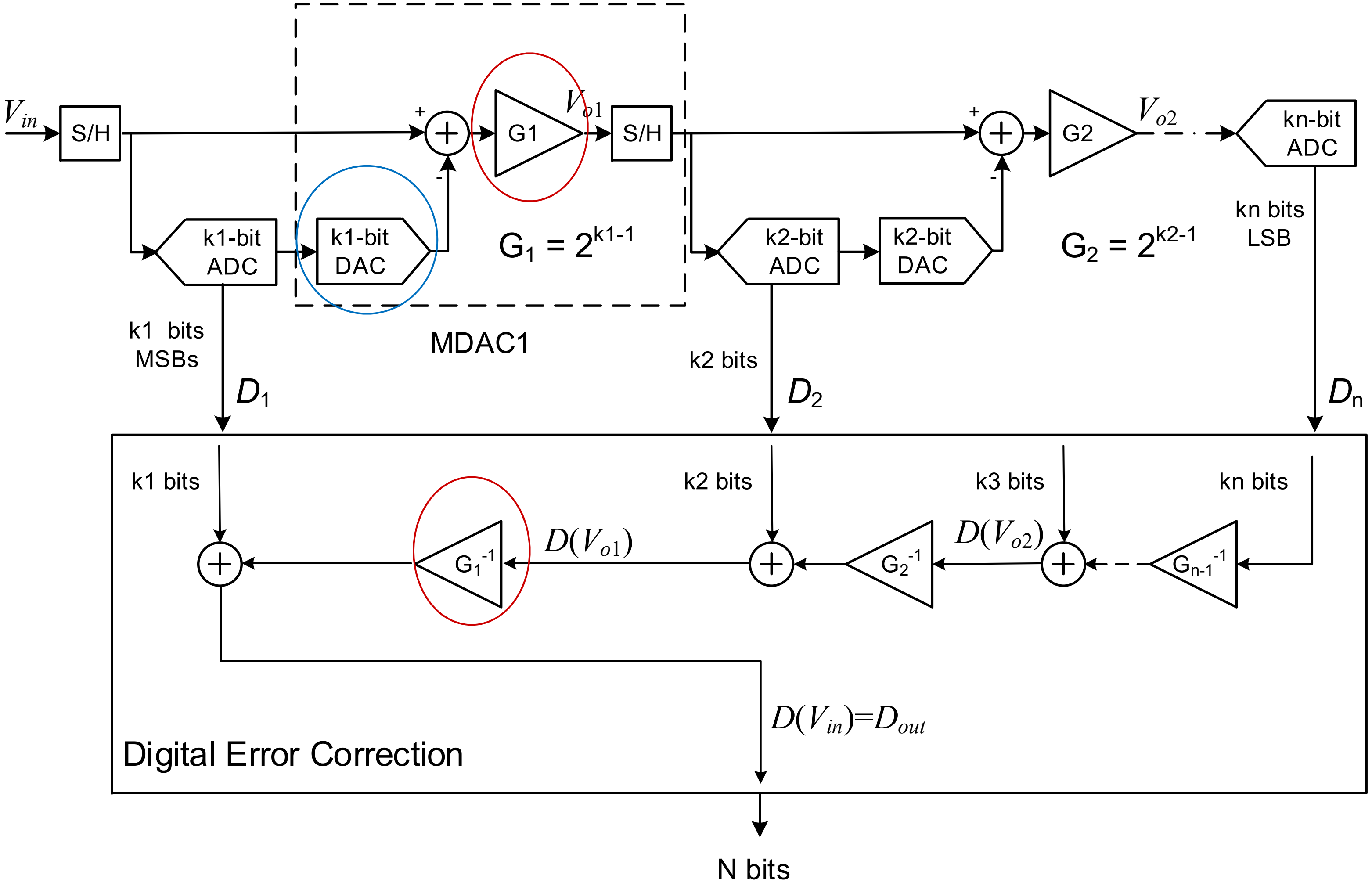
} Not covered in this tutorial

Digital Error Correction [1]



Calibration Techniques

- Correlation-based (dither-based) calibration [15, 2, 5, 8-11]
- Calibration techniques not covered in this tutorial:
  - Using reference ADC [16, 17]
  - Split ADC method [18]
  - Summing node calibration [3, 14]
  - Using statistical methods [19-21]

Calibration of ADC Impairments [15, 2]

- Quantizer impairments:
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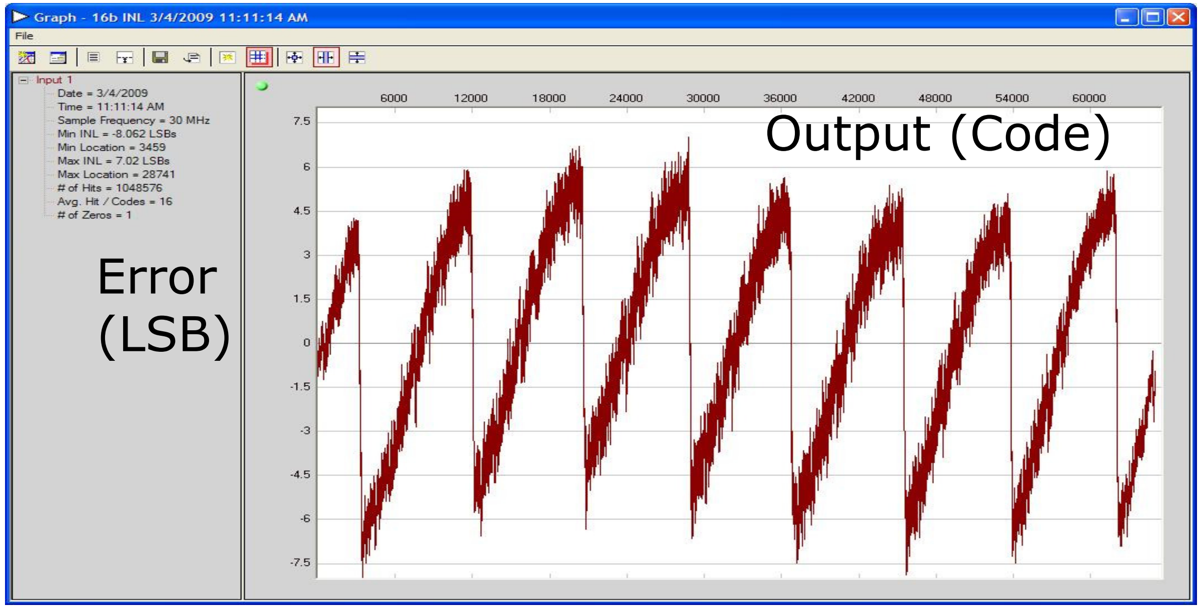

INL Plot

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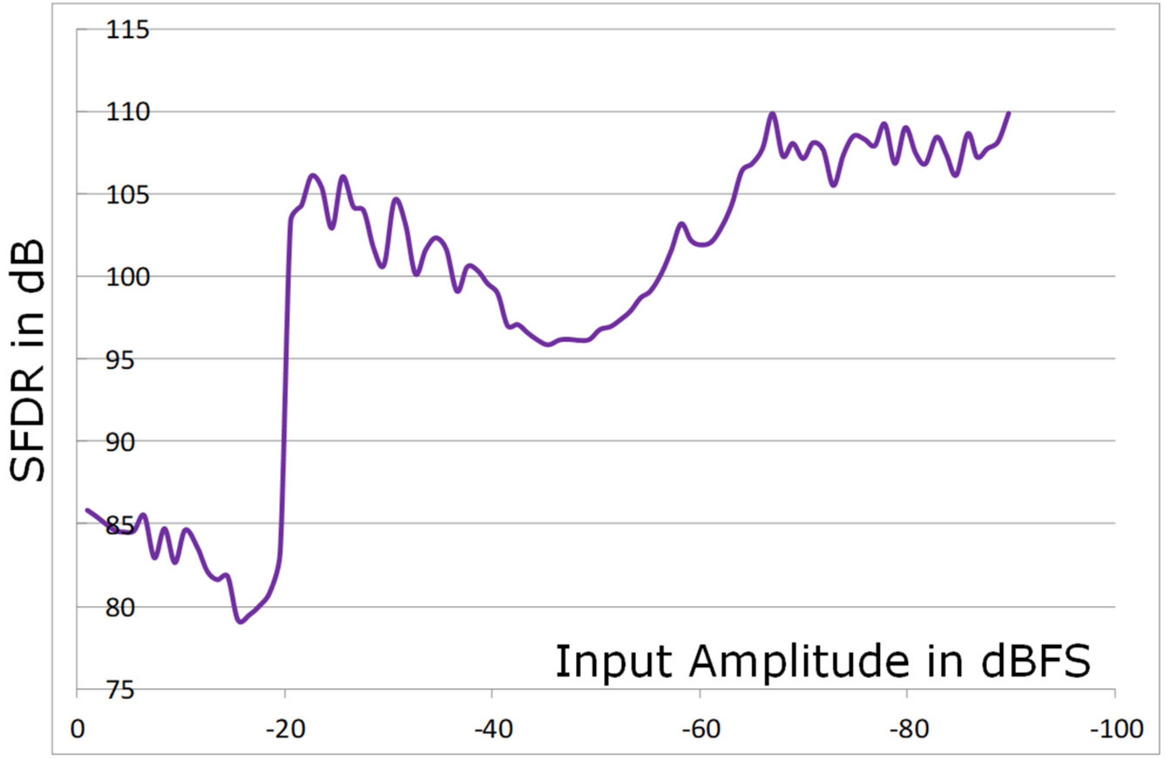

Calibration of ADC Impairments [10, 11, 2]

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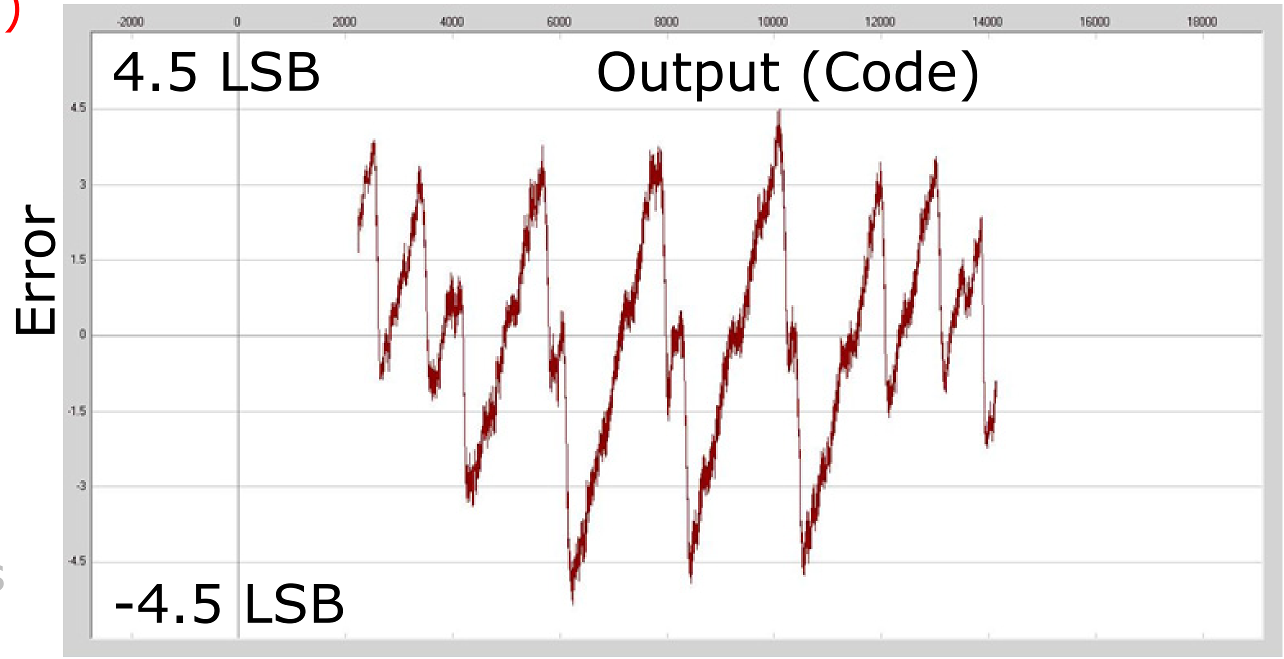

INL Plot

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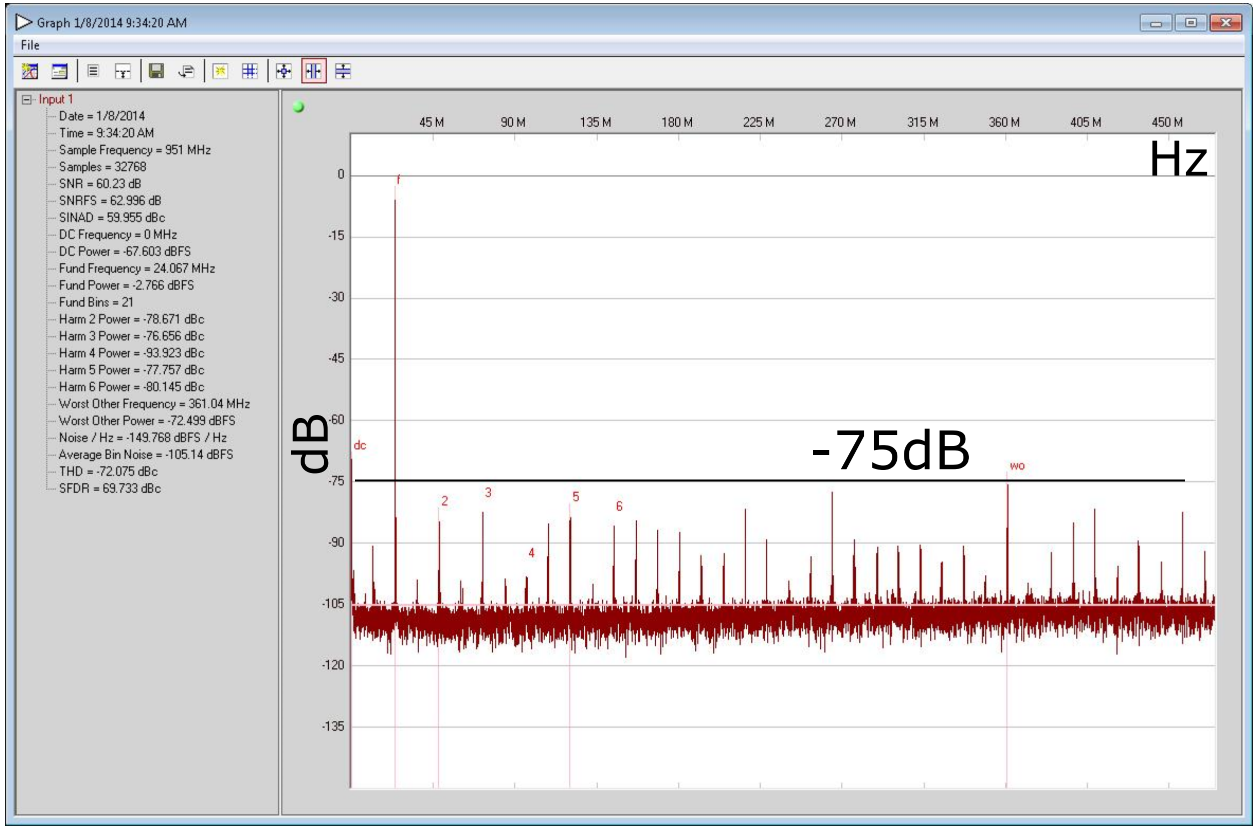
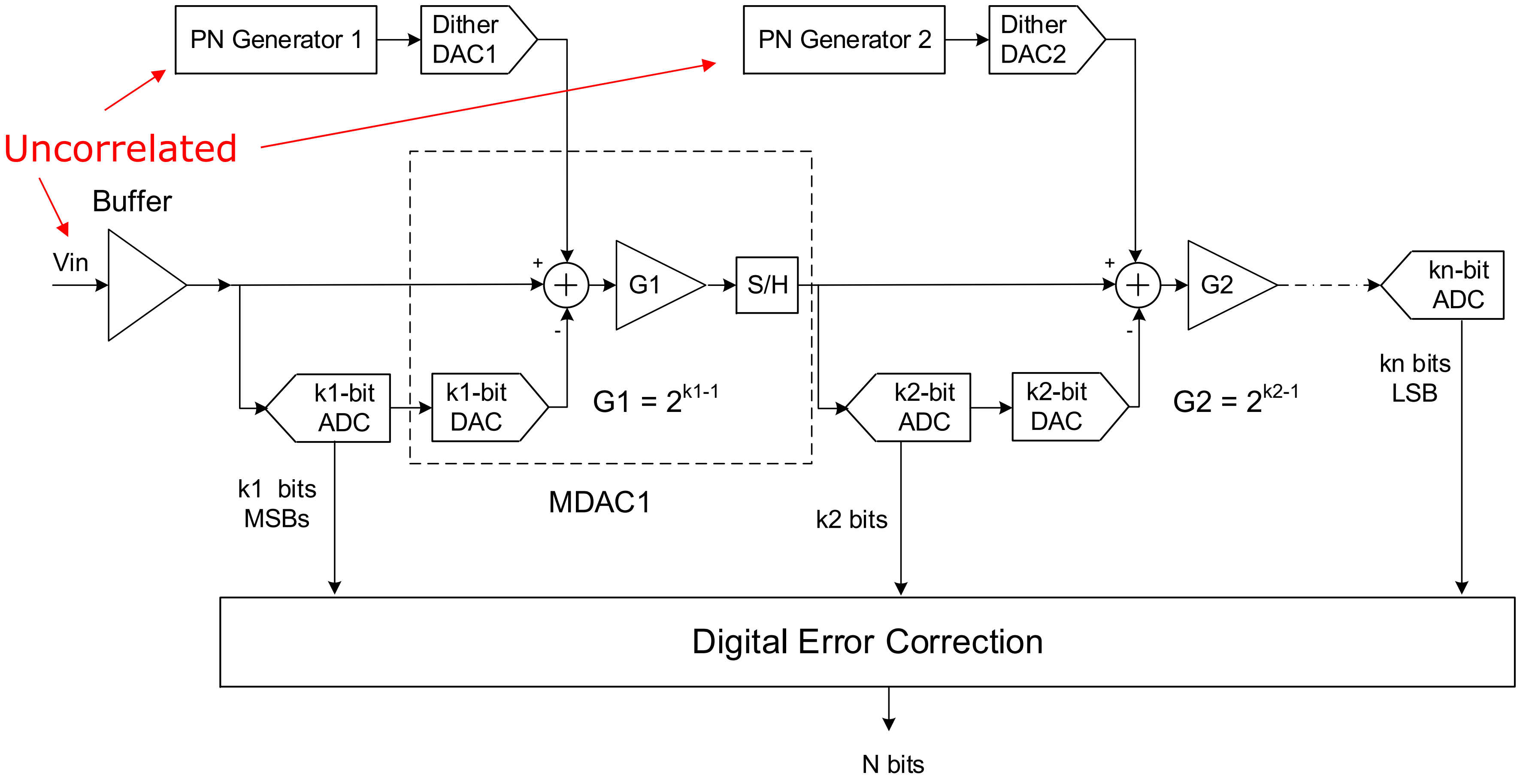
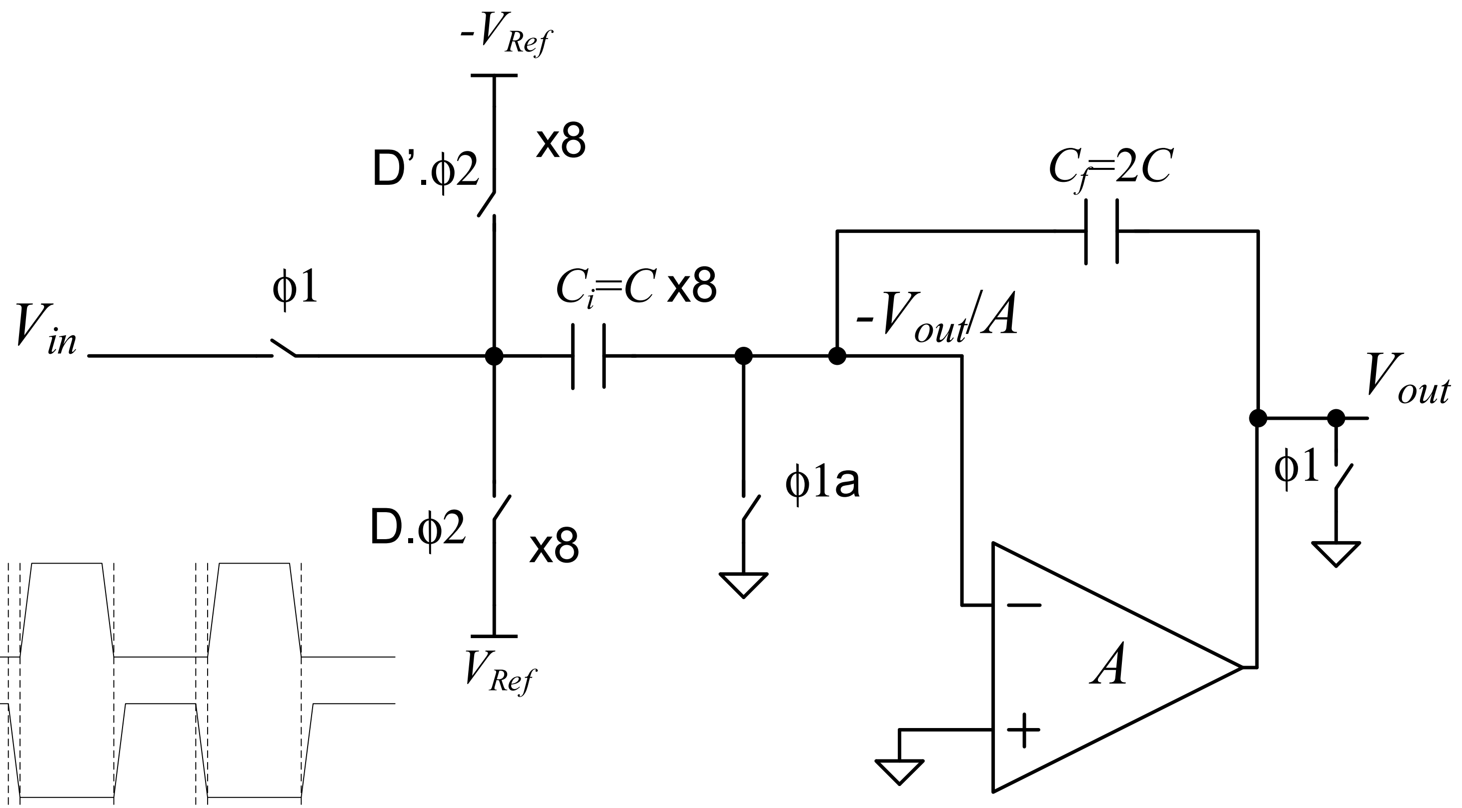


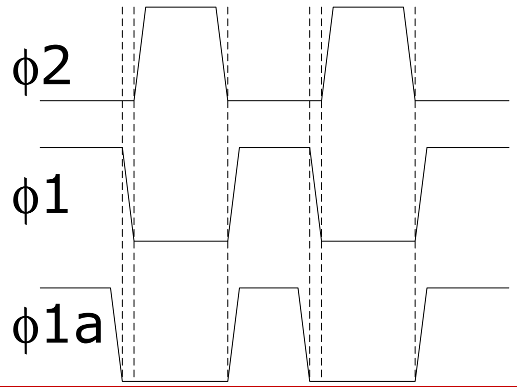
Correlation-Based Calibration



Simplified Multiplying DAC (MDAC)

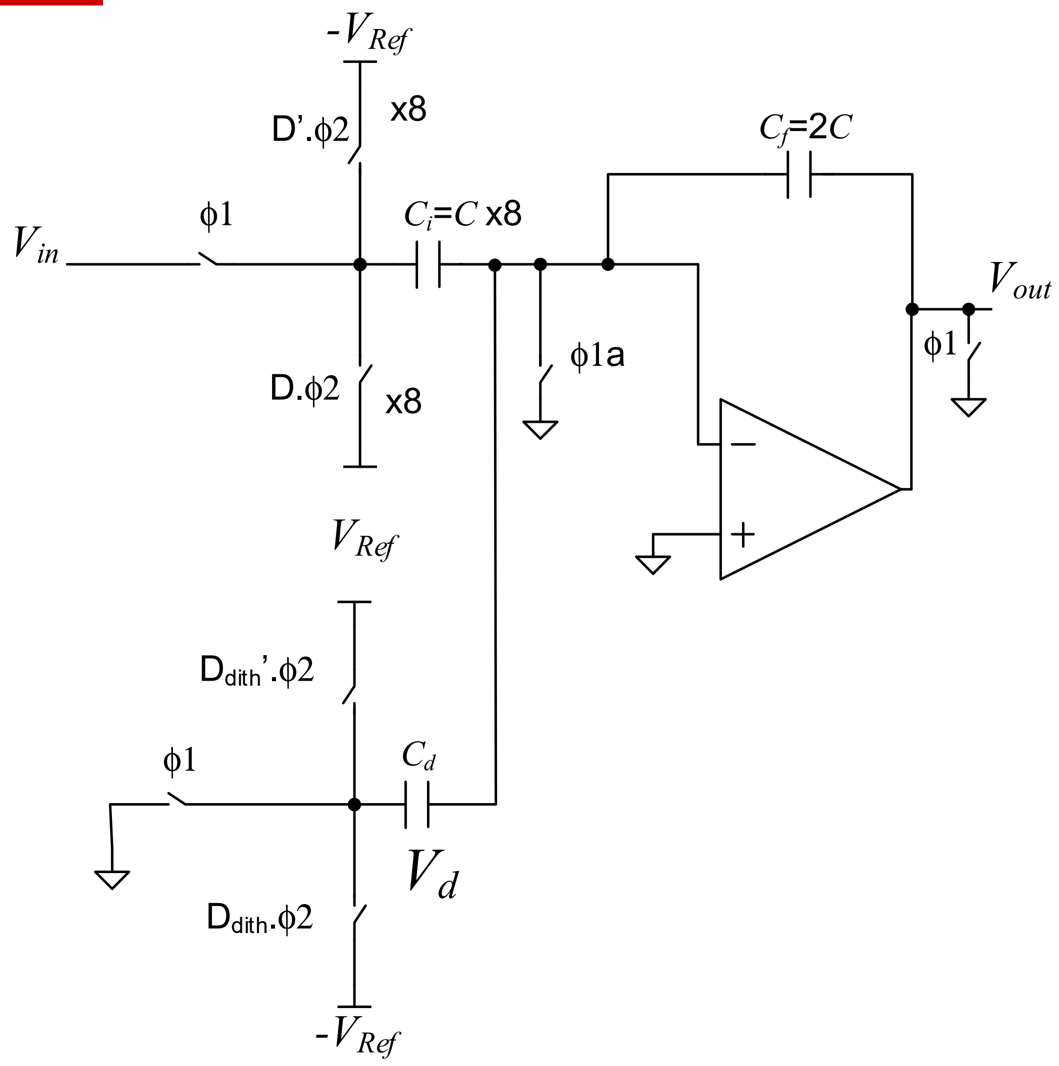
- The MDAC performs input sampling, DAC, subtraction, and inter-stage amplification
- Show is a 3-bit MDAC with shared capacitances





The IGE/IME Calibration [15, 2, 10, 11]

- Dither is injected in the MDAC
- It encounters the IGE and IME errors
- Correlation is used in the digital domain to estimate the errors
- Mismatches between the dither path and the signal path can limit accuracy
- Long convergence time
- Can be relatively input signal independent



The IGE/IME Calibration [15, 2, 10, 11]

- IGE: k=0, IME: k>0
- Estimation (for each k separately):

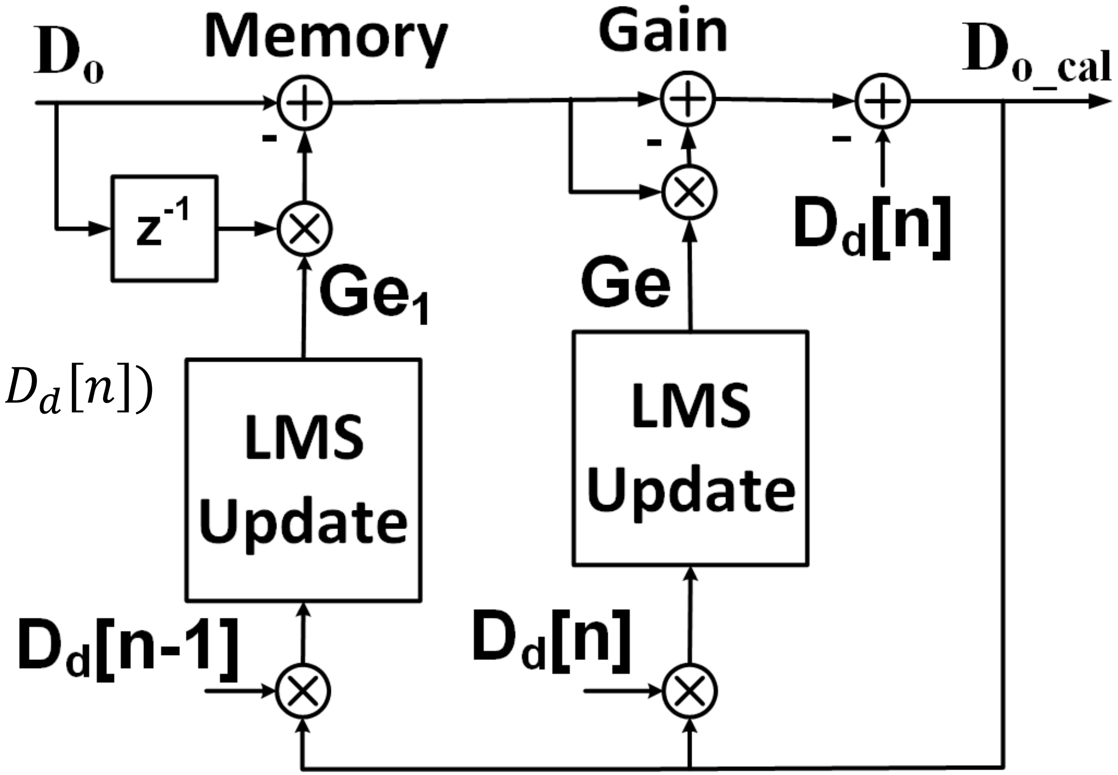
$$Ge_k[n+1] = Ge_k[n] + \mu \times D_d[n-k] \times \left(D_o[n] - \sum_{k=0}^{1}(D_o[n-k] \times Ge_k) - D_d[n]\right)$$

- BG Correction:

$$D_{o\_cal}[n] = D_o[n] - \sum_{k=0}^{1}(D_o[n-k] \times Ge_k) - D_d[n]$$

- FG Correction:

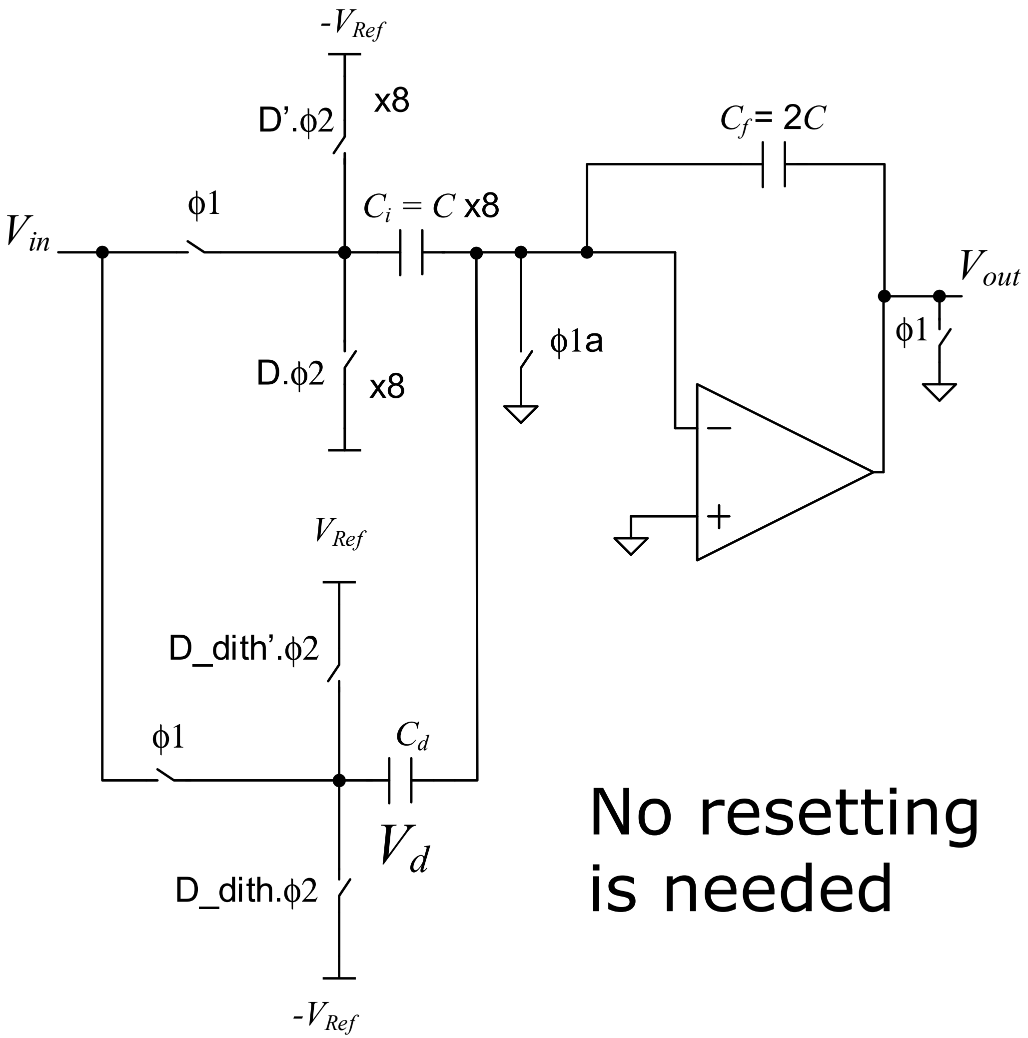
$$D_{o\_cal\_final}[n] = D_{o\_cal}[n] \times Ge_{FG}$$



LMS: Least Mean Square Algorithm

Kick-back Background Calibration [1, 2]

- The kick-back dither caps kick the input similar to the sampling capacitances' kick
- The dither's kick is sampled on the total capacitances and propagates down the pipeline



No resetting is needed

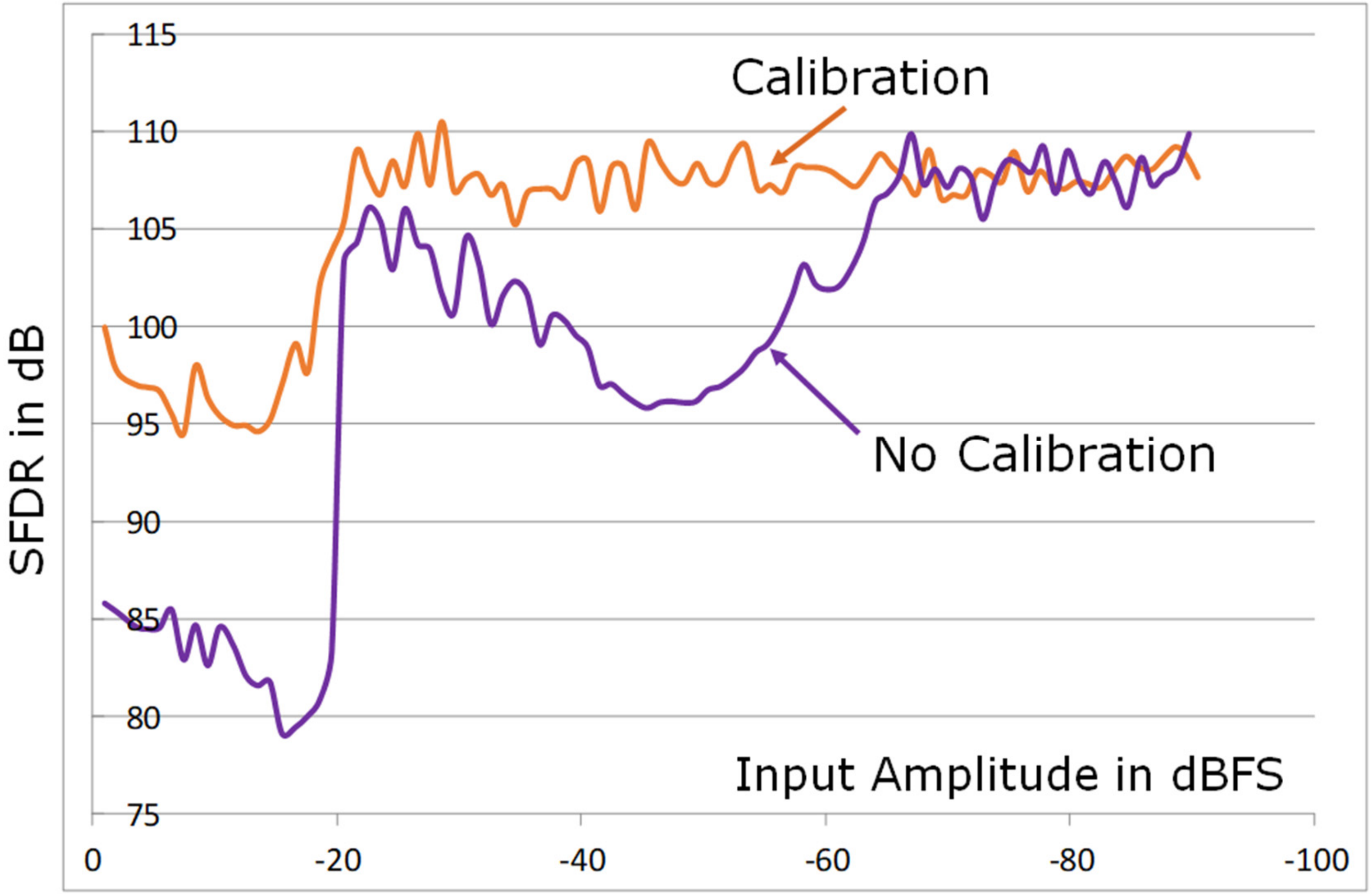
Kick-back Background Calibration [1, 2]

- The LMS algorithm is used to estimate the gain/correction coefficient *Gkb* of the dither's kick of the previous sample(s)
- The correction coefficient *Gkb* is applied to the previous stage-1 flash bits
- Conceptually:

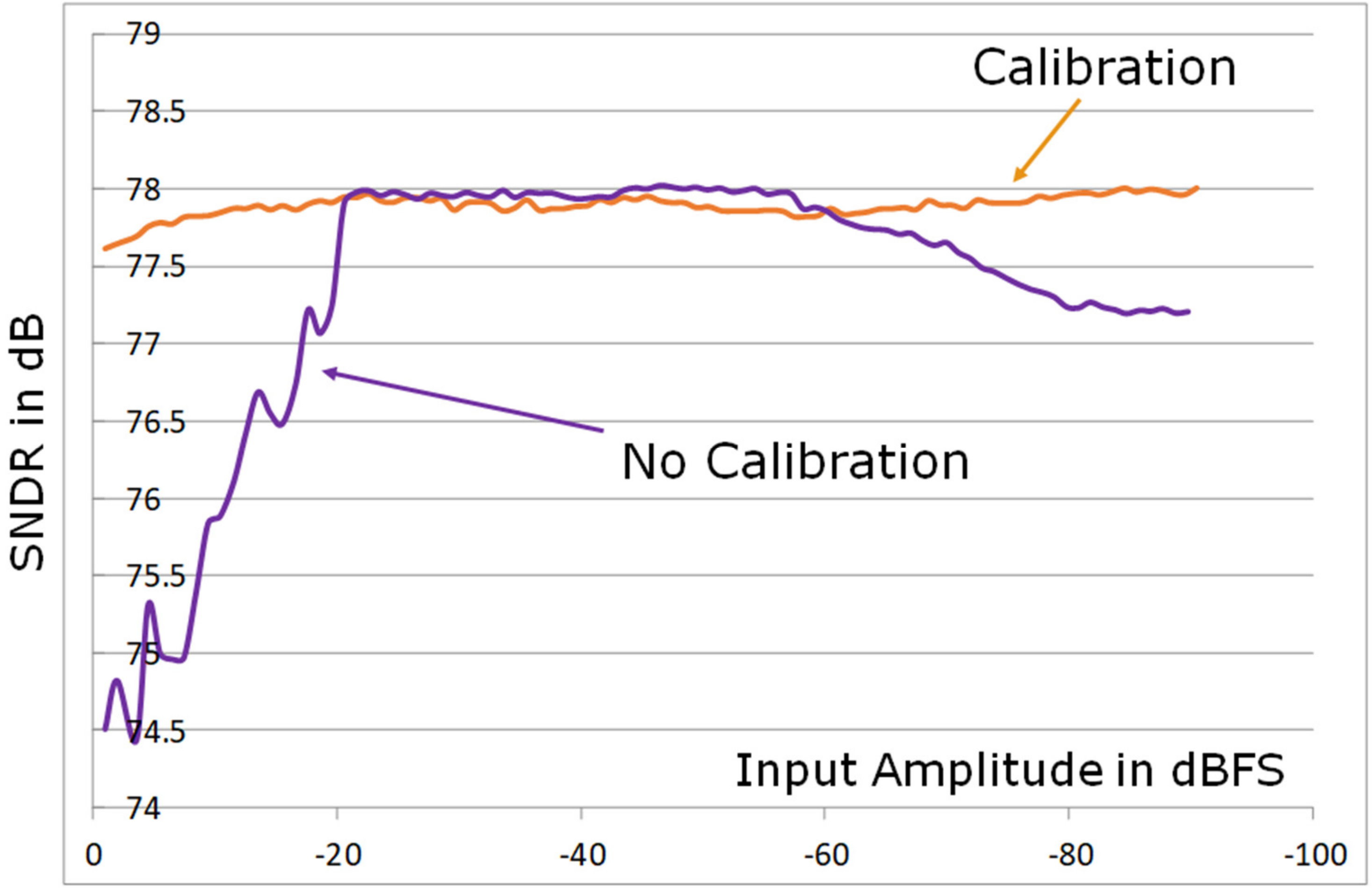
$$Gkb_k[n+1] = Gkb_k[n] + \mu \times D_d\,[n-k] \times (D_{out}[n] - D_d\,[n-k] \times Gkb_k[n])$$

$$D_{out\_kbcal}[n] = D_{out}[n] + \sum_{k=1}^{M_{kb}} D_1[n-k] \times Gkb'_k - Dd[n-k] \times Gkb_k$$

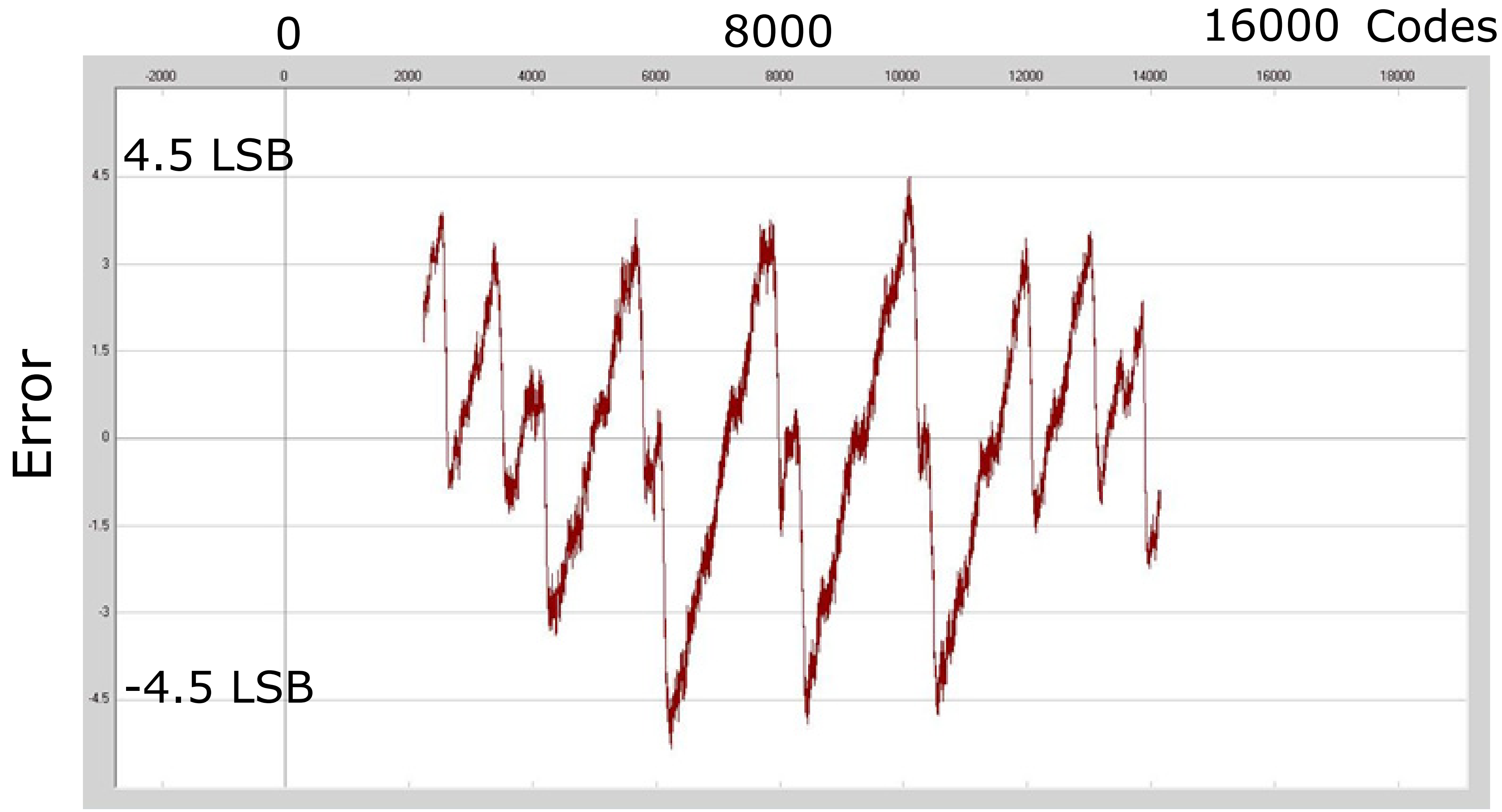
Input Amplitude Sweep with IGE (SFDR)



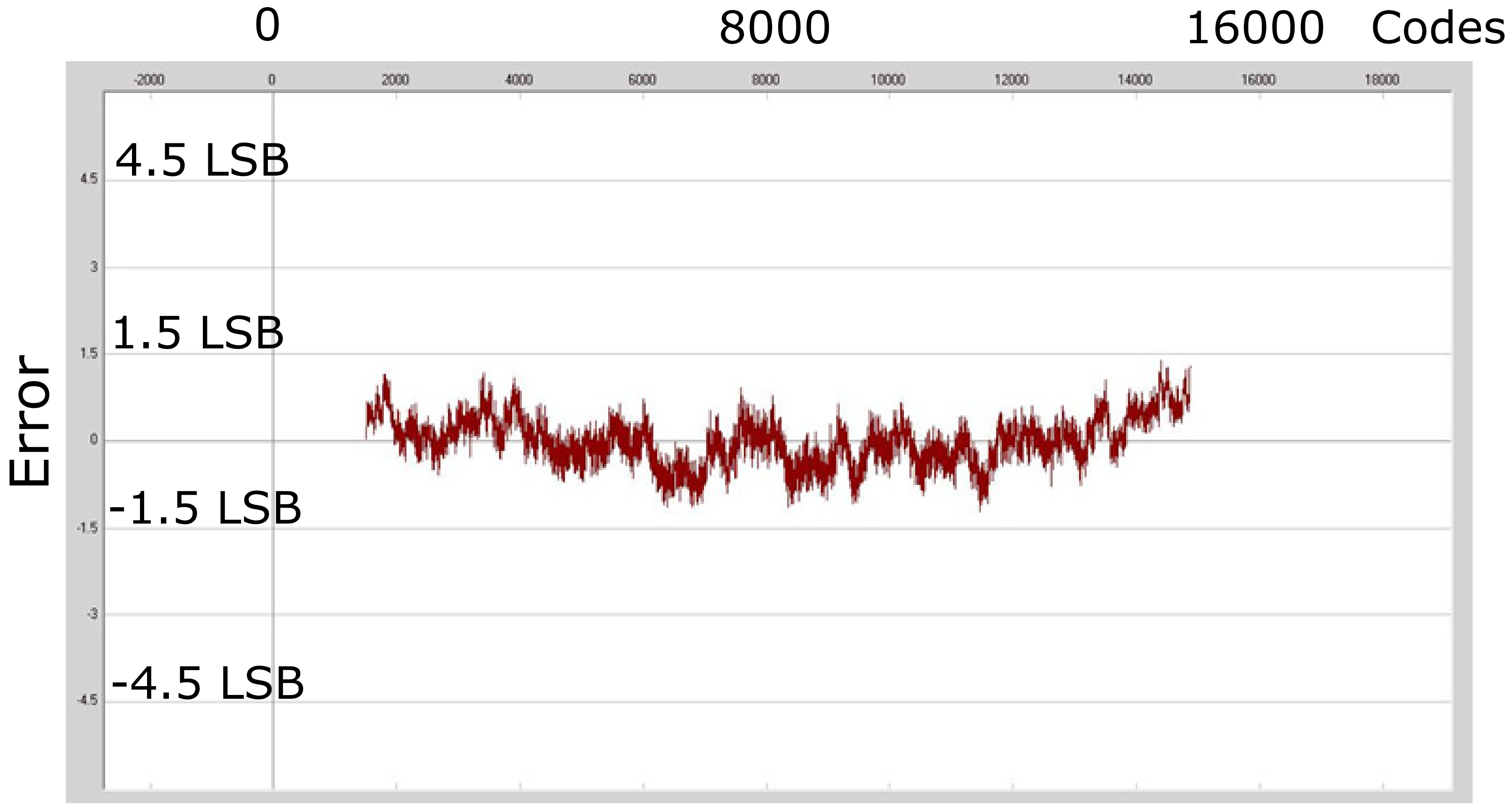
Input Amplitude Sweep with IGE (SNDR)



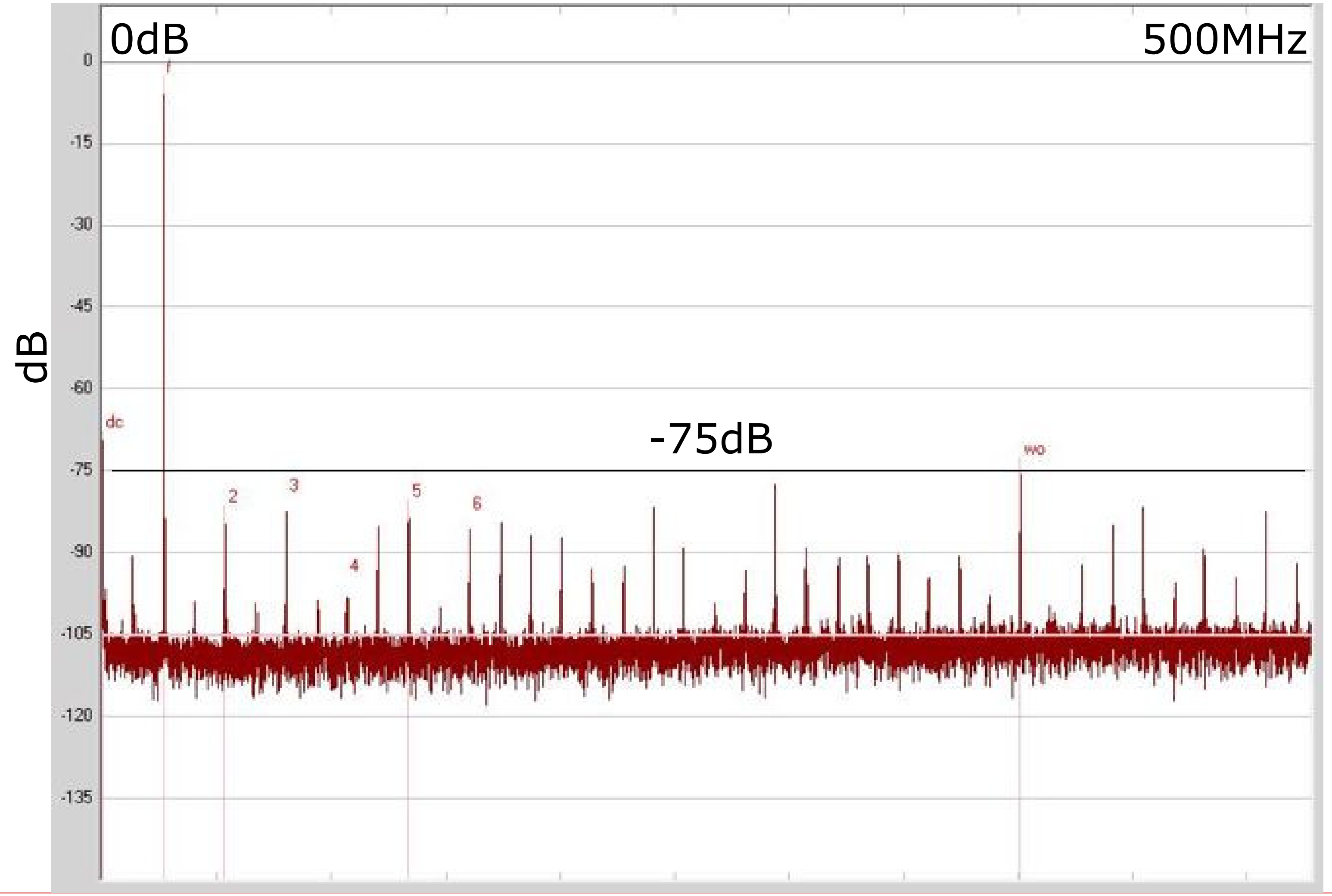
INL without Kick-back Calibration [1, 2]



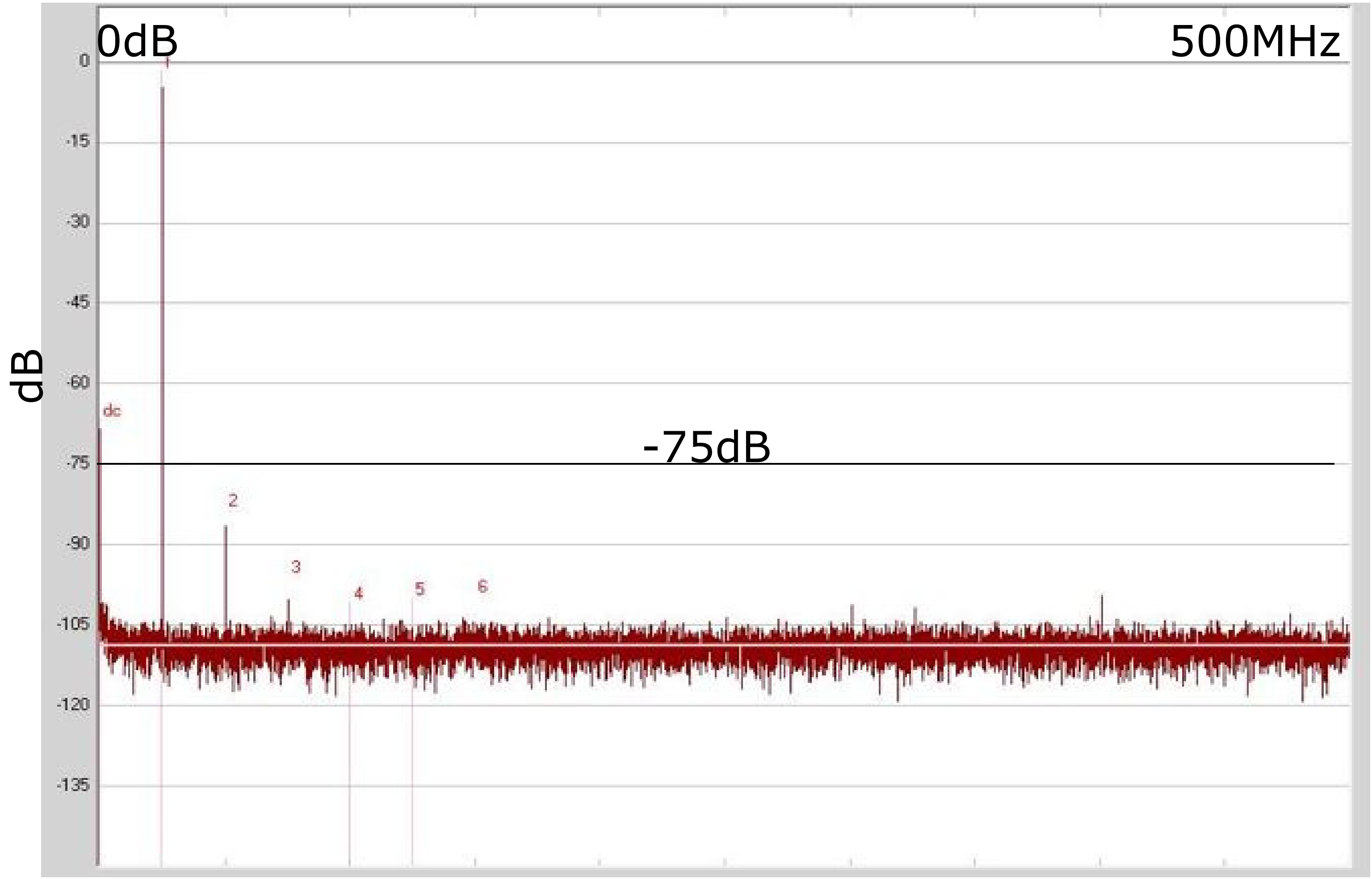
INL with Kick-back Calibration [1, 2]



FFT without kick-back calibration

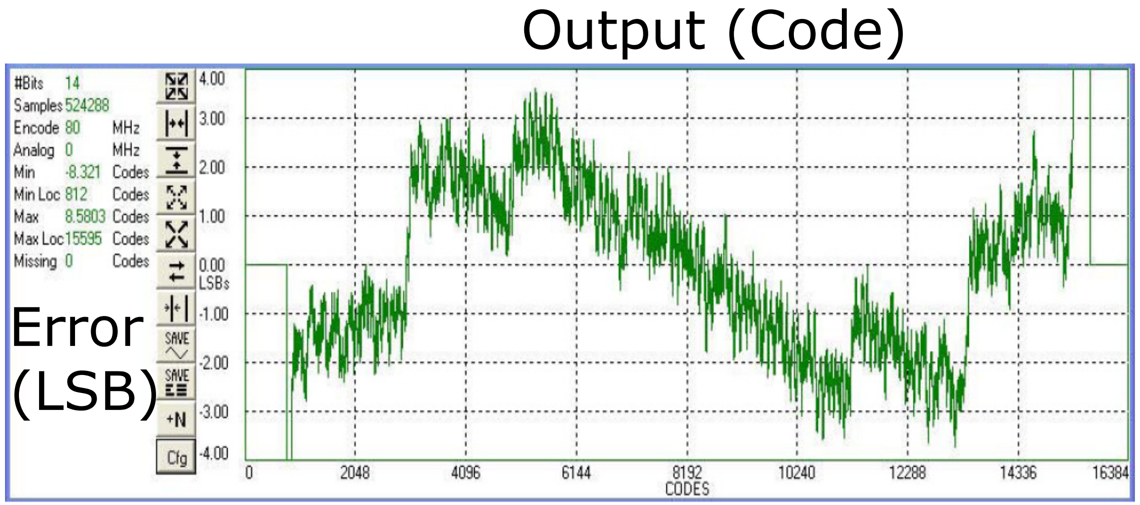


FFT with kick-back calibration



Calibration of ADC Impairments [8, 5]

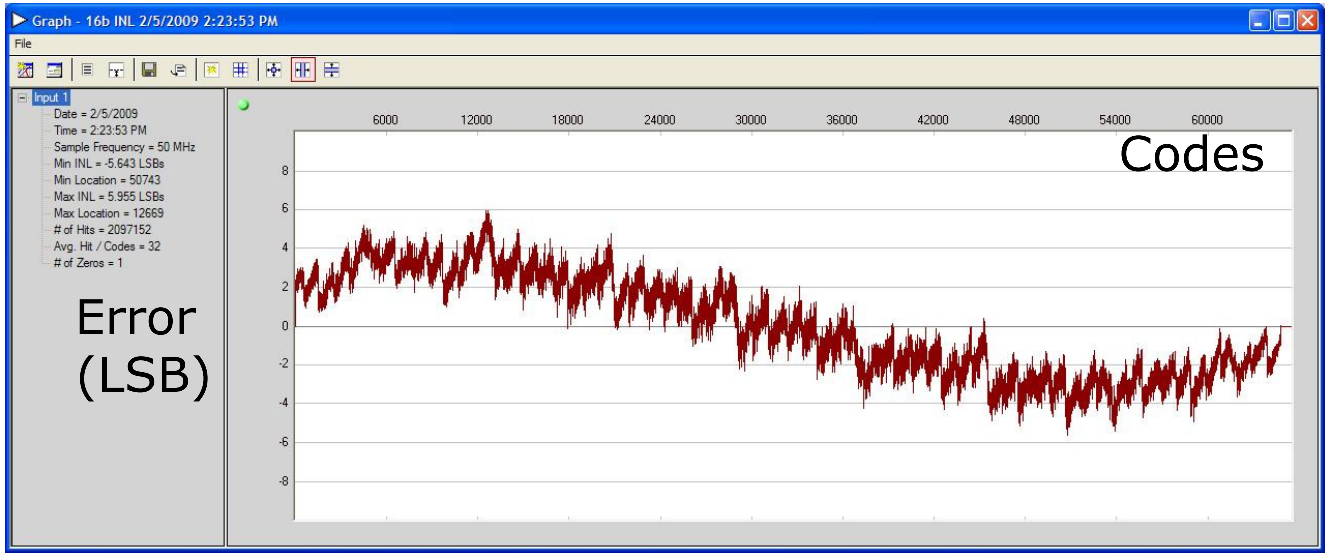
- Quantizer impairments:
  - Inter-stage gain and settling errors (IGE)
  - Inter-stage memory errors (IME)
  - DAC errors
  - Reference errors
  - MDAC amplifier non-linearity
- Sample-and-hold impairments:
  - Kick-back errors
  - Front-end non-linearity
- Interleaving impairments:
  - Offset and gain mismatch errors
  - BW/timing mismatch errors



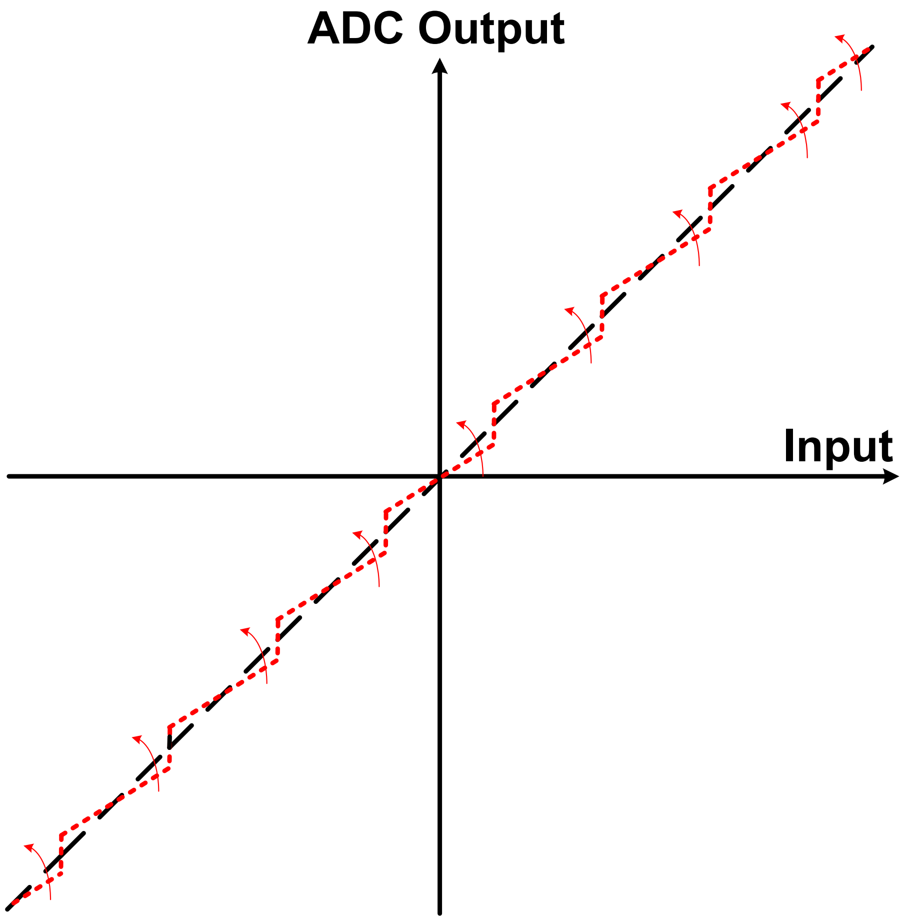
INL Plot

Calibration of ADC Impairments [20, 8, 9, 5]

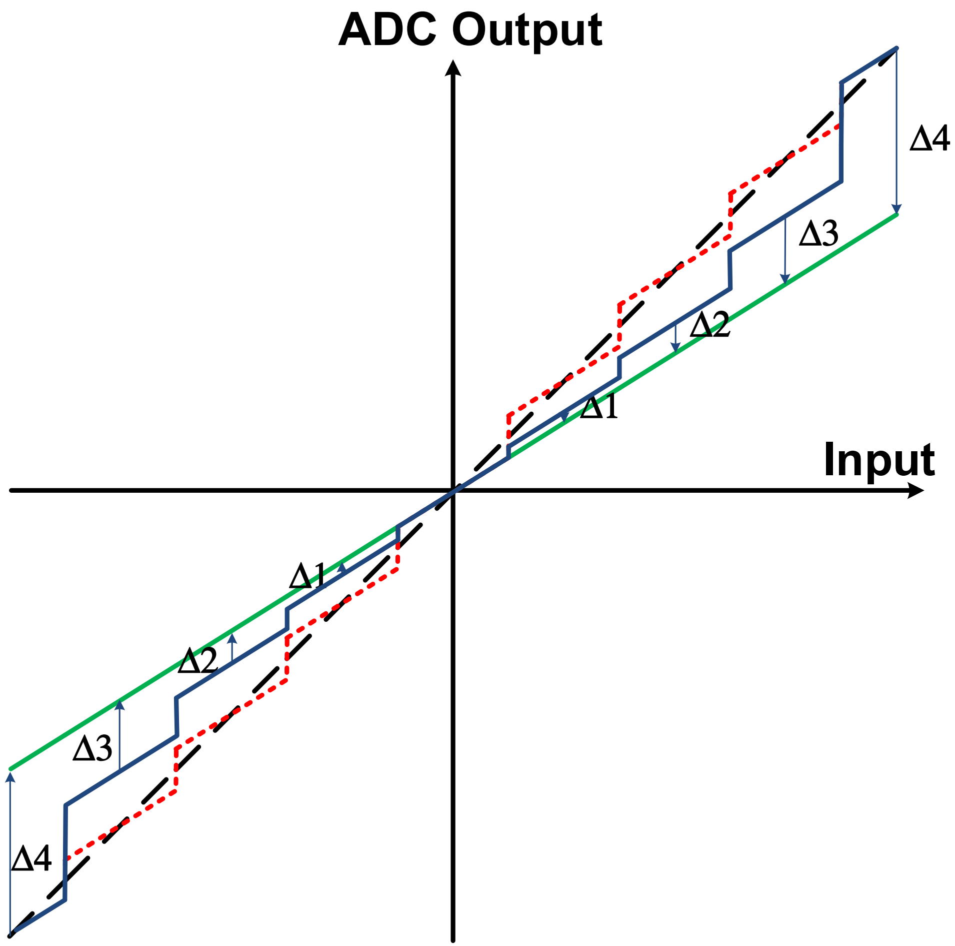
- Quantizer impairments:
  - Inter-stage gain and settling errors (IGE)
  - Inter-stage memory errors (IME)
  - DAC errors
  - Reference errors
  - MDAC amplifier non-linearity
- Sample-and-hold impairments:
  - Kick-back errors
  - Front-end non-linearity
- Interleaving impairments:
  - Offset and gain mismatch errors
  - BW/timing mismatch errors



Quantization Non-linearity (INL Breaks)

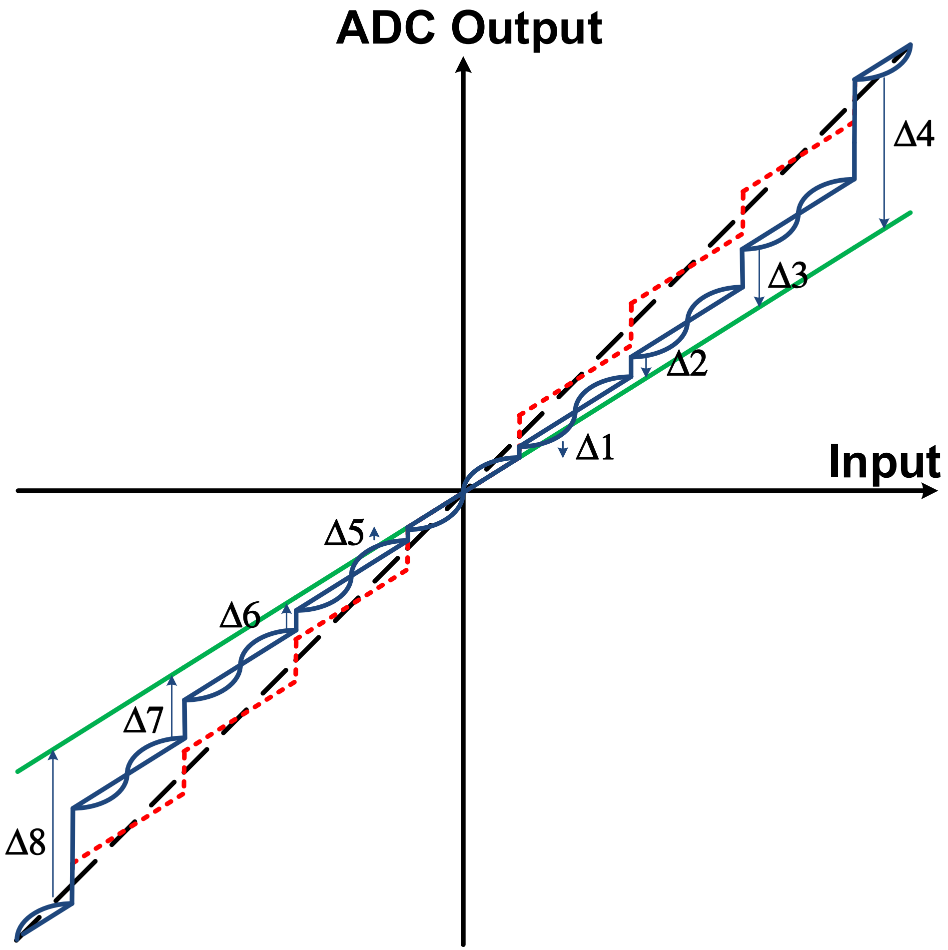


Inter-stage Gain Error (IGE)

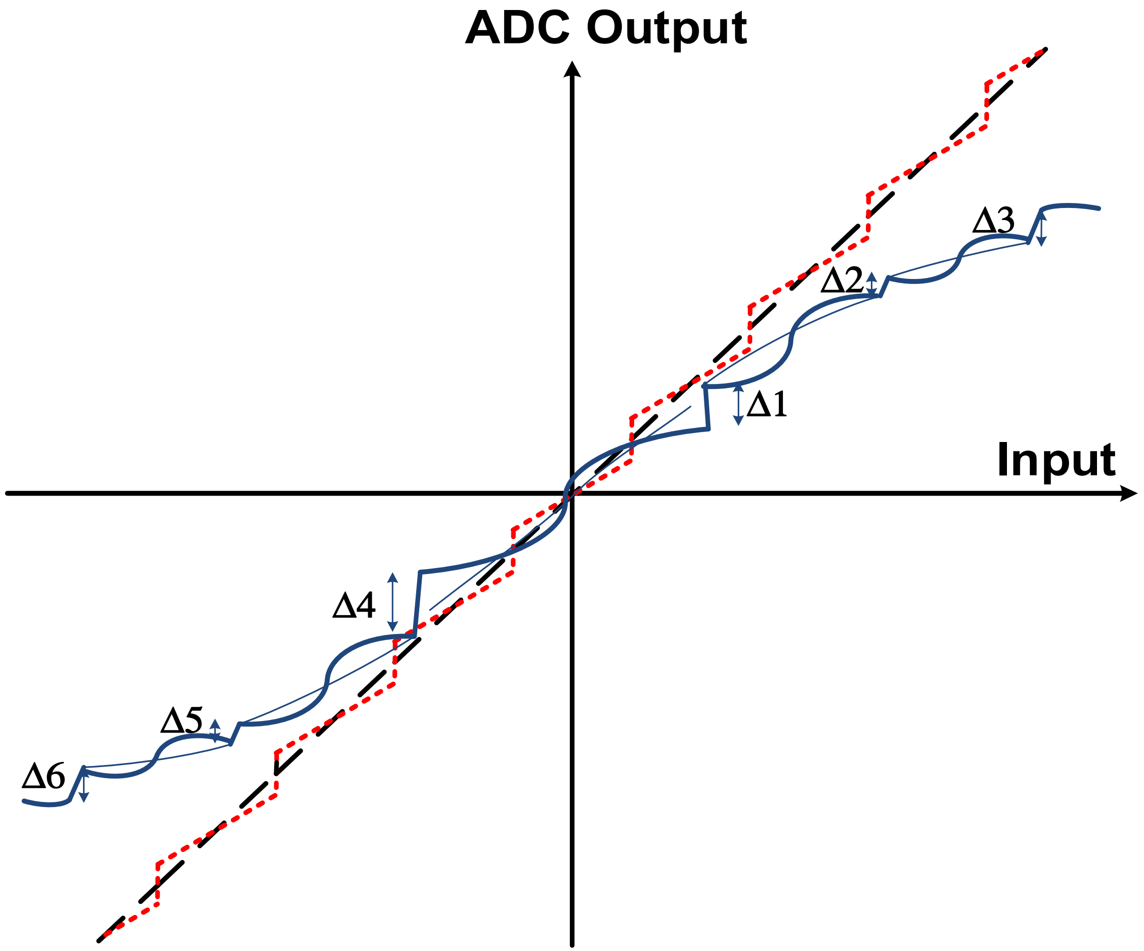


DAC/Reference Errors

INL Breaks and Harmonic Distortion (HD)



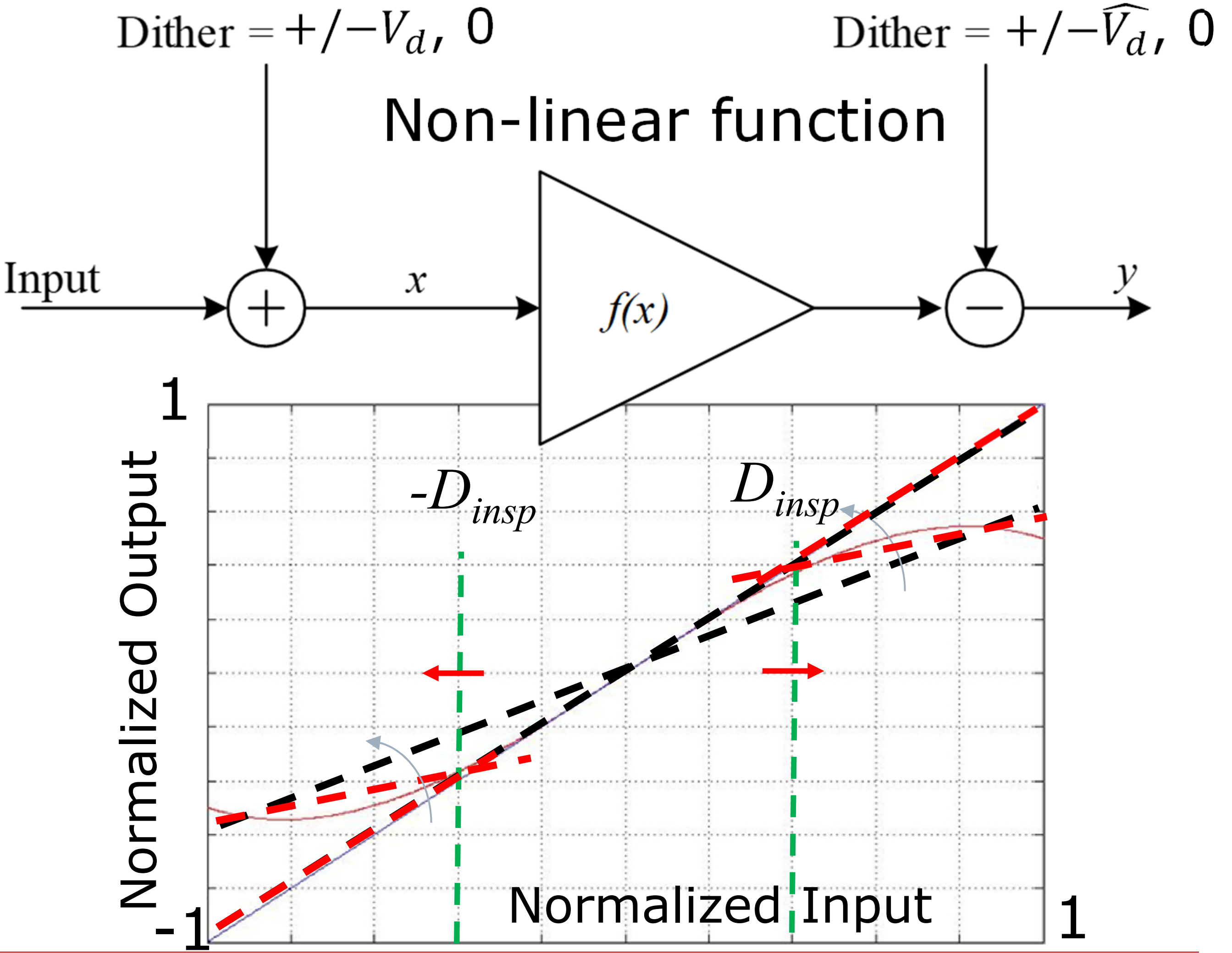
INL breaks and inter-stage HD



INL breaks, inter-stage and overall HD

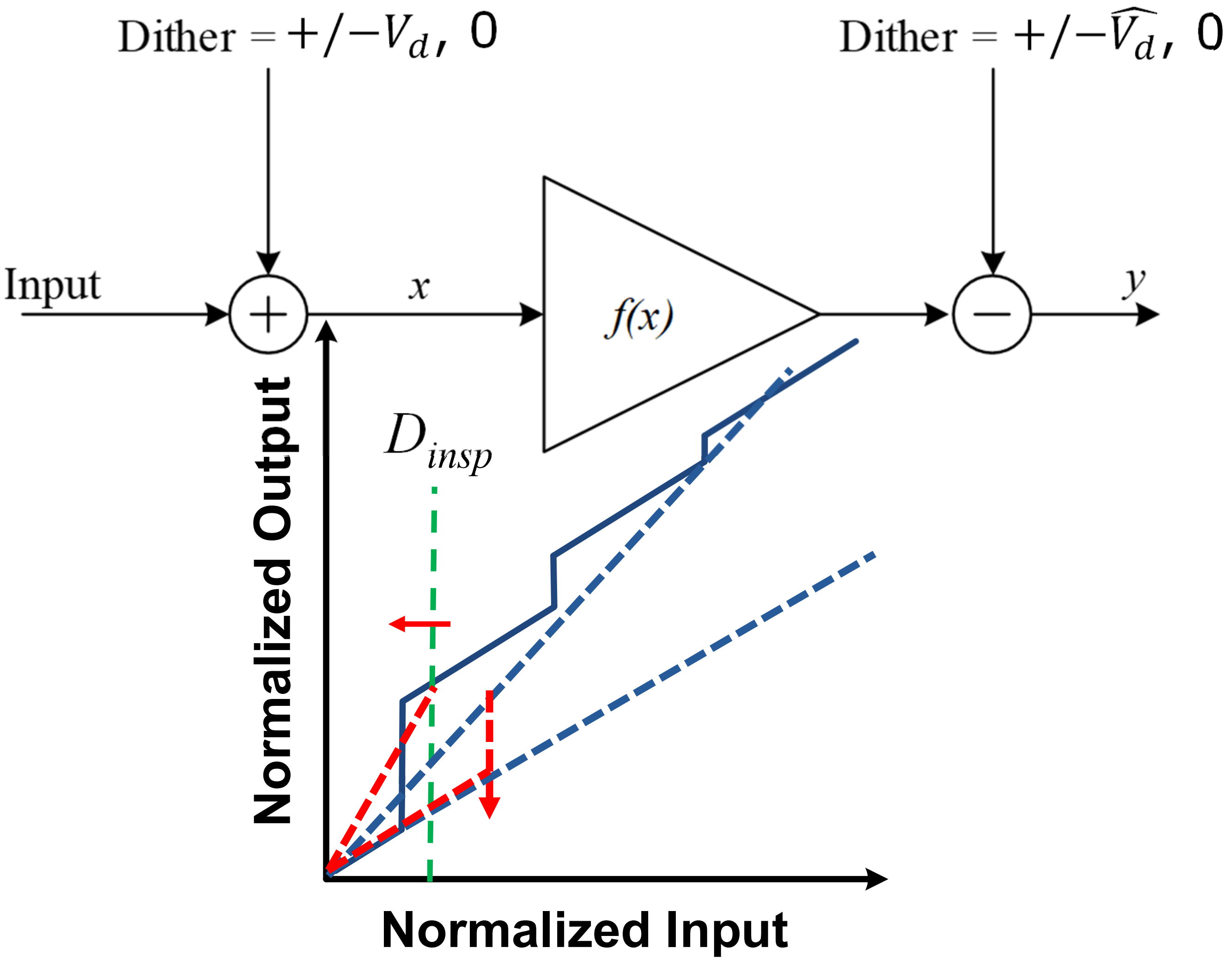
Dither-based Non-linearity Calibration [20,8,9,5]

- $y_1 = f(x + V_d) - \widehat{V_d}$
- $y_2 = f(x - V_d) + \widehat{V_d} \neq y_1$
- Error = $y_1 - y_2$
- Use thresholded LMS-like counting/correlation over half-bounded open intervals to estimate the error
- Calibrates harmonic distortion

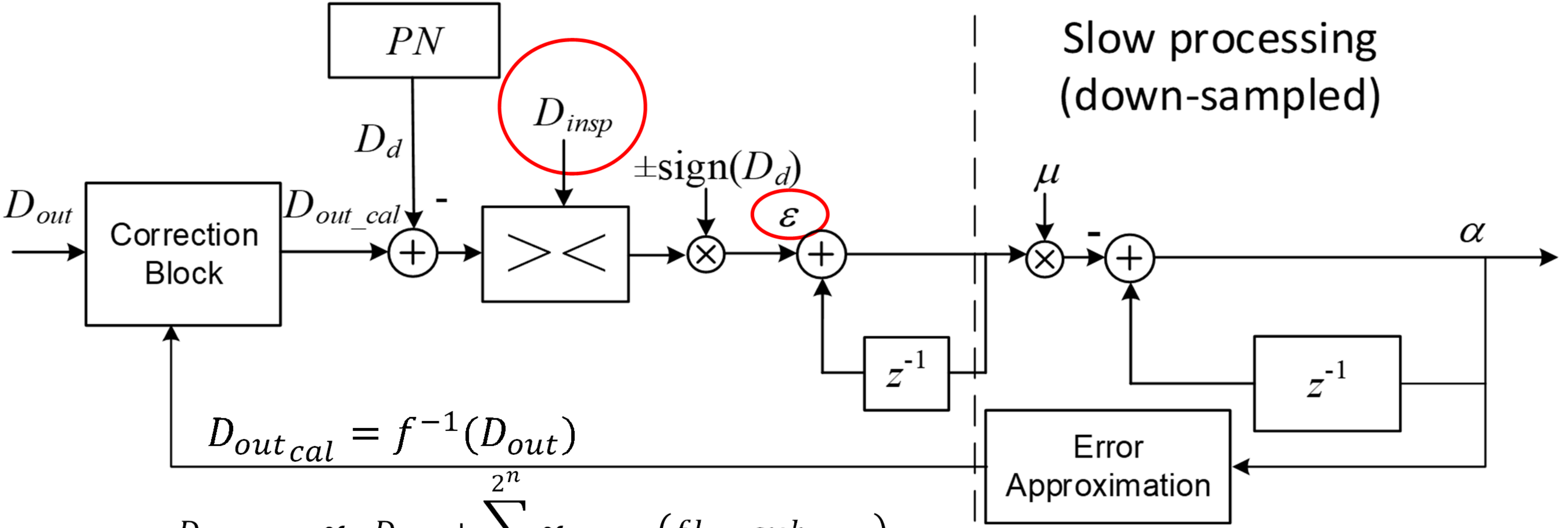


Dither-based Non-linearity Calibration [5]

- $y_1 = f(x + V_d) - \widehat{V_d}$
- $y_2 = f(x - V_d) + \widehat{V_d} \neq y_1$
- Error = $y_1 - y_2$
- Use thresholded LMS-like counting/correlation over half-bounded open intervals to estimate the error
- Calibrates INL breaks



Estimation of Non-linear Coefficients [5]



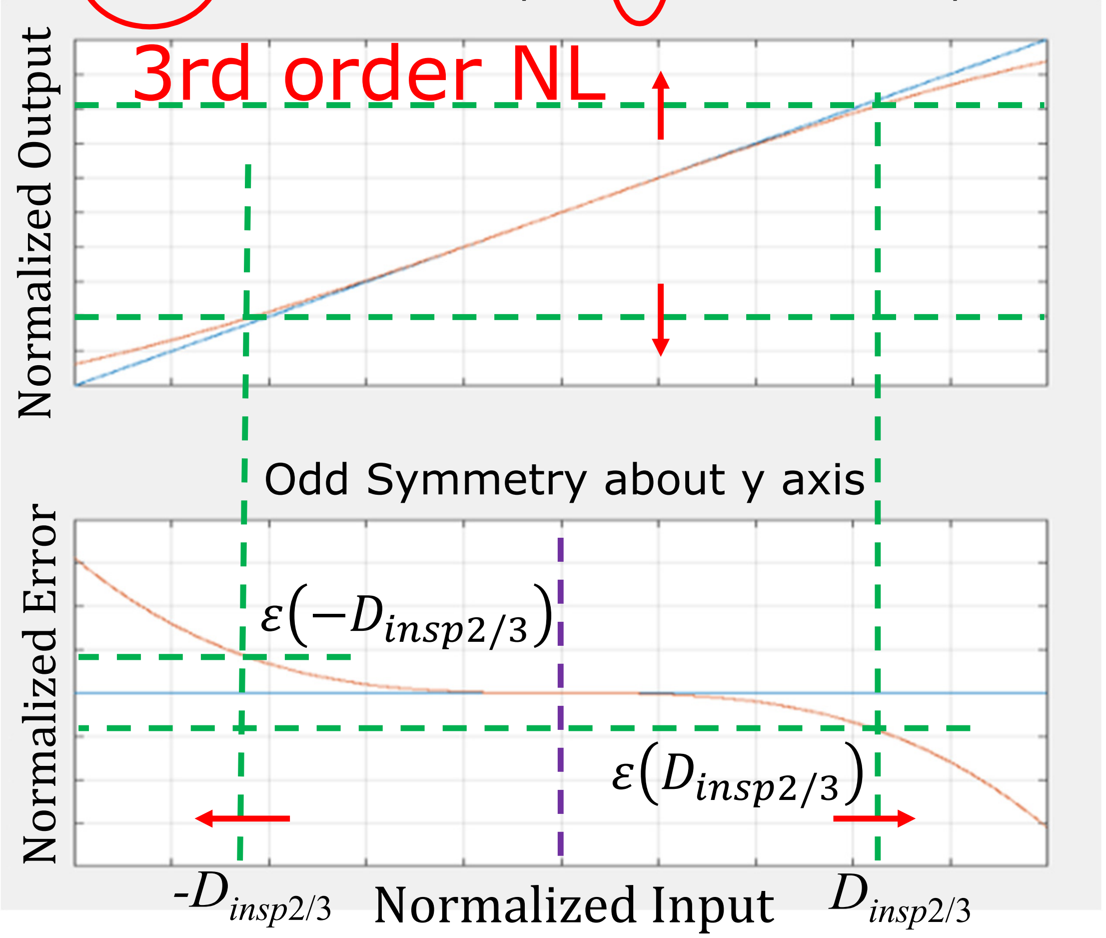
$$D_{out\,cal} = \propto_1 D_{out} + \sum_{i=1}^{2^n} \propto_{DAC\_i} \cdot \left(fl = sub_{(i+1)}\right)$$

$$\propto(n+1) = \propto(n) - \mu \times \varepsilon$$

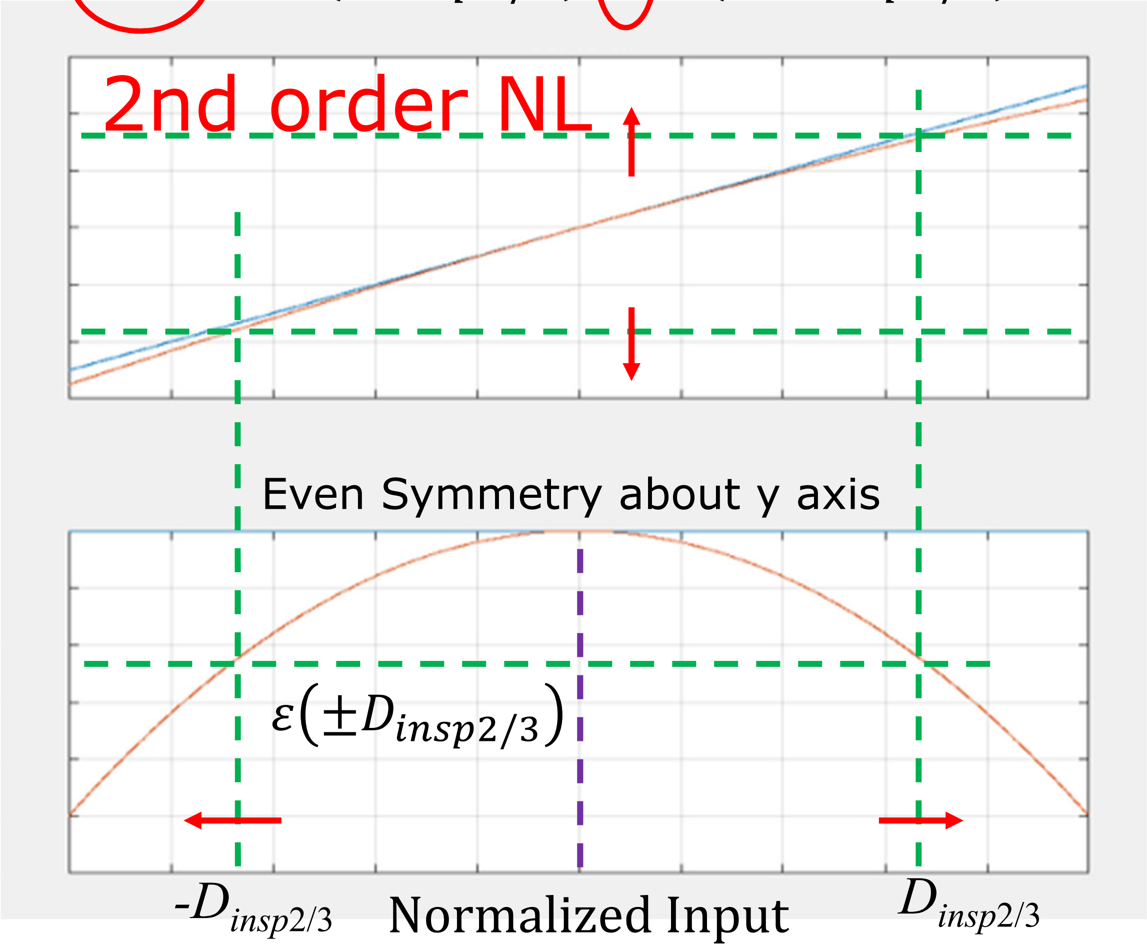
$$D_{out\,cal} = \propto_1 D_{out} + PWL\left(\sum_{i=2}^{j} \propto_i D_{out}^i + \text{higher order terms}\right)$$

Harmonic Distortion Inspection Points [20, 5]

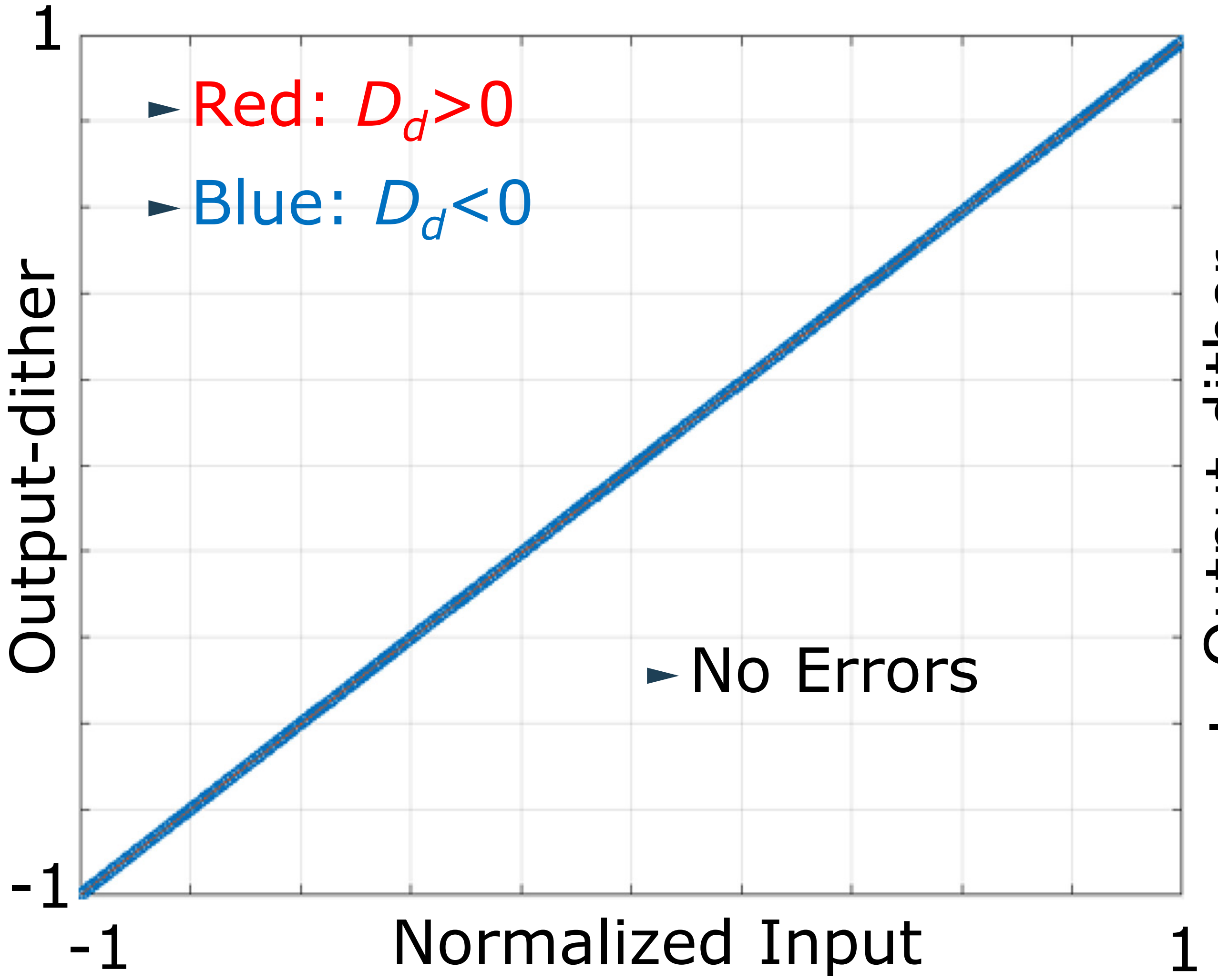
$$\varepsilon_{HD3} = \varepsilon(D_{insp2/3}) - \varepsilon(-D_{insp2/3})$$

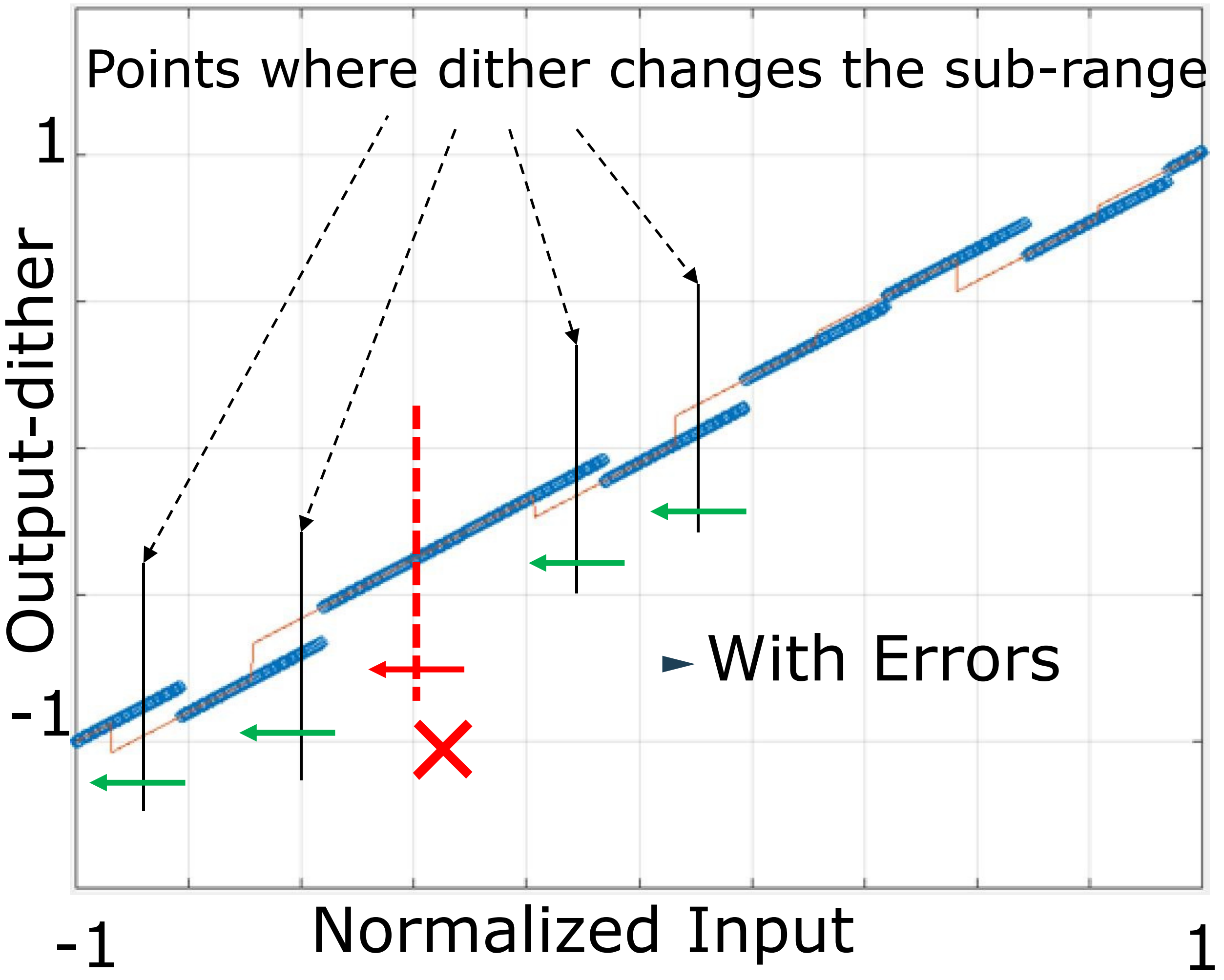


$$\varepsilon_{HD2} = \varepsilon(D_{insp2/3}) + \varepsilon(-D_{insp2/3})$$

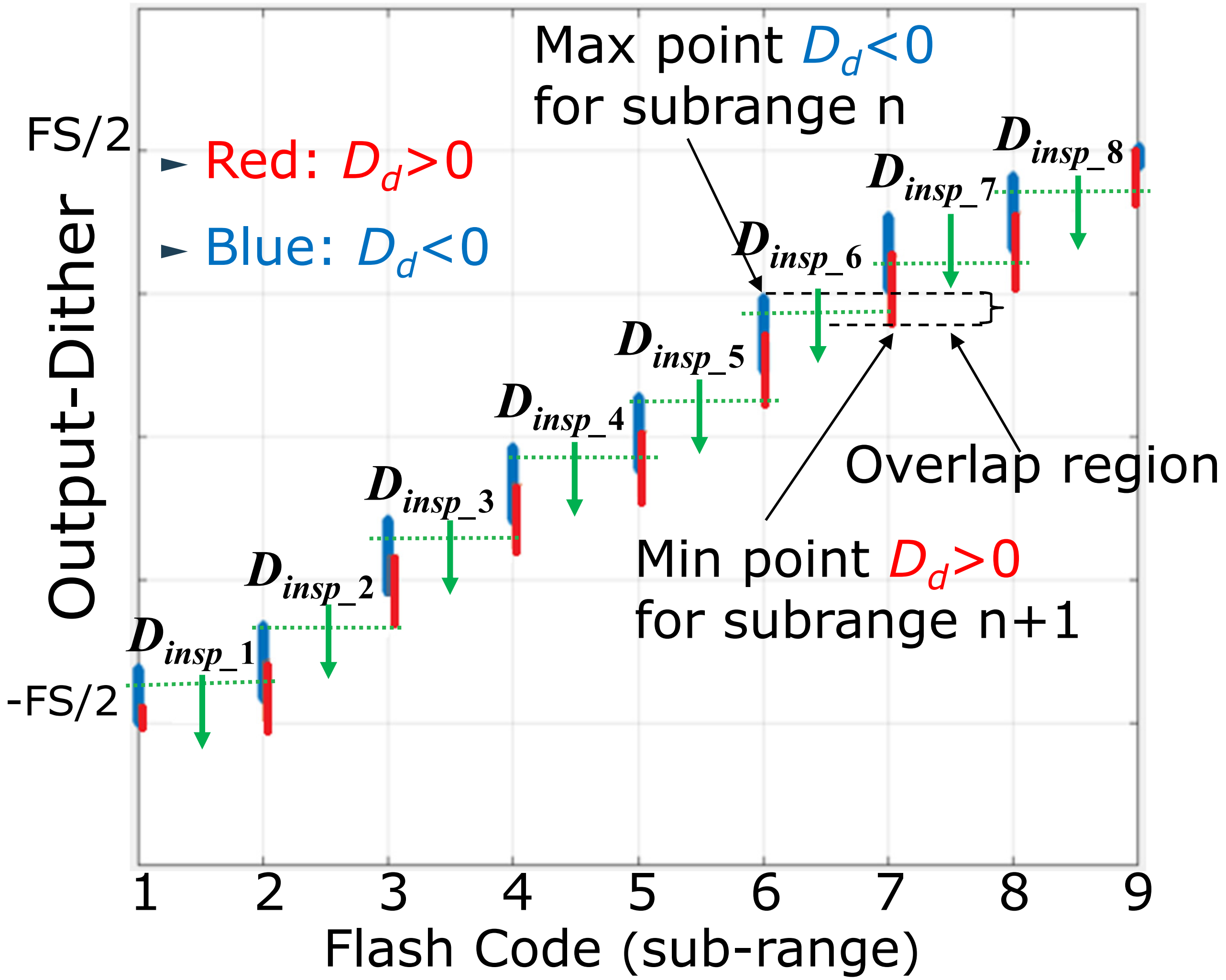


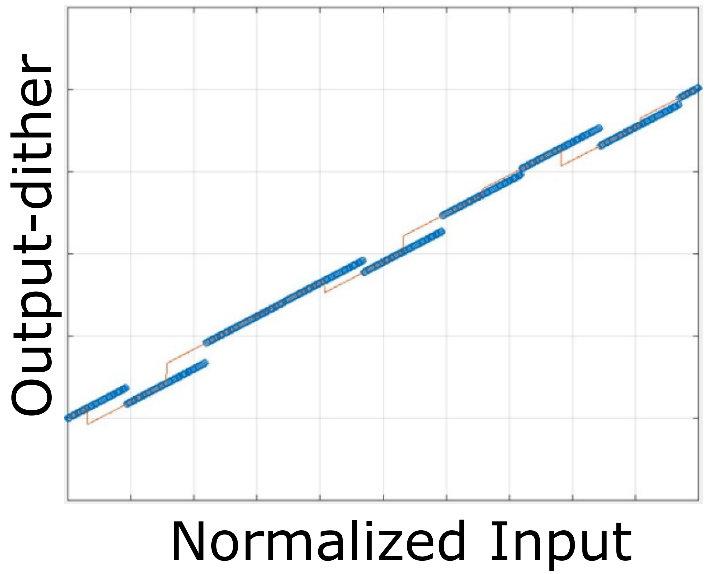
Dither Added with and without INL Breaks Inspection Points for INL Breaks





Locating Inspection Points in Real Time [5,4]

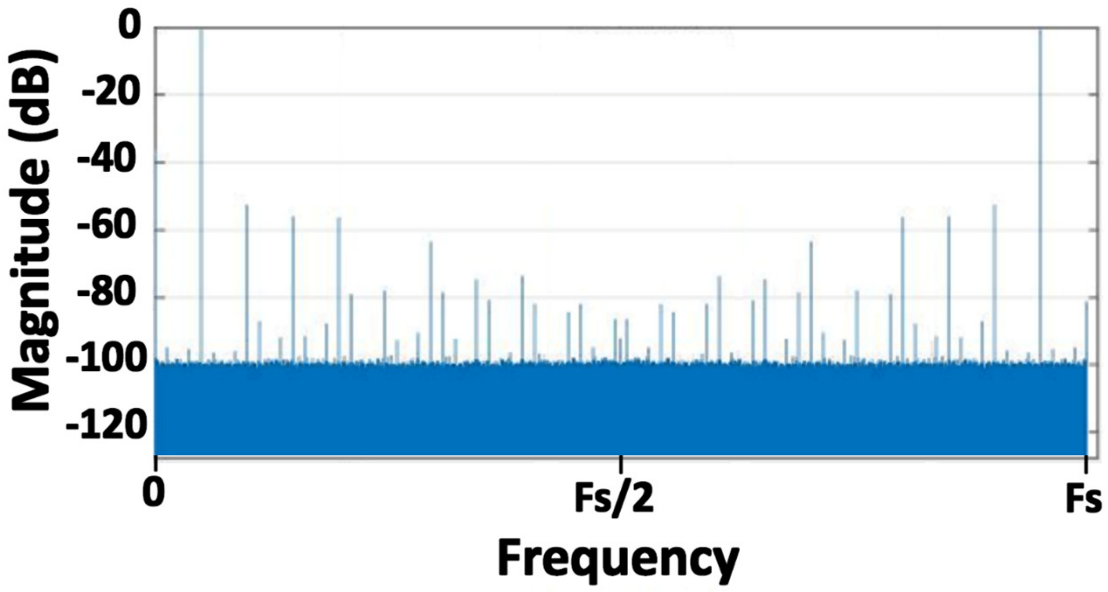




- With Errors

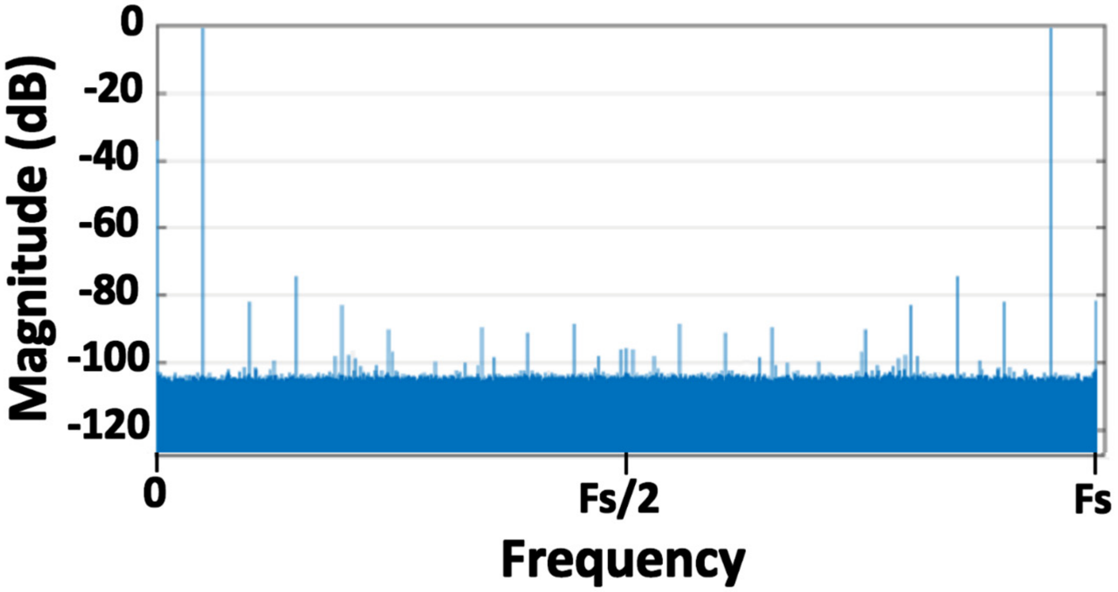
Example of DAC/Ref Non-linearity Calibration

Fs=3GS/s, SNR~53dB, SFDR~55dB



Without non-linearity calibration

Fs=3GS/s, SNR~60dB, SFDR~75dB



With non-linearity calibration

Papers to See This Year

- Paper 10.7: "A 64GS/s 4x-interpolated 1b Semi-Digital FIR DAC for Wideband Calibration and BIST of RF-Sampling A/D-Converters"
  - Wideband calibration of ADC non-linearity
- Paper 27.3: "A 13.8-ENOB 0.4pF-C_{IN} 3rd-Order Noise-Shaping SAR in a Single-Amplifier EF-CIFF Structure with Fully Dynamic Hardware-Reusing kT/C Noise Cancellation"
  - Foreground DAC calibration
- Paper 27.6: "A 25MHz-BW 75dB-SNDR Inherent Gain Error Tolerance Noise-Shaping SAR-Assisted Pipeline ADC with Background Offset Calibration"
  - Background offset calibration
- Paper 27.2: "14.1 ENOB 184.9 dB FoM Capacitor Array-Assisted Cascaded Charge-Injection SAR ADC"
  - DAC calibration
- Paper 27.7: "A 79dB-SNDR 167dB-FoM Bandpass ΔΣ ADC Combining N-Path Filter with Noise-Shaping SAR"
  - Interleaving and DAC calibration

Conclusion

- Data converters are ubiquitous and an essential building block in modern communication systems. The performance of the converter often decides the performance of the whole system

- Some converter performance metrics and non-idealities were discussed

- Calibration of the IGE, DAC, IME, kick-back, harmonic distortion and INL breaks are examples of using digital signal processing to improve the analog performance

- Digital assistance enables ADC designers to continue building efficient, accurate and fast ADCs as process geometry shrinks

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