Fundamentals of Fully-Integrated Voltage Regulators

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Live Q&A Session: Feb. 13, 2021, 8:00-8:20 am, PST

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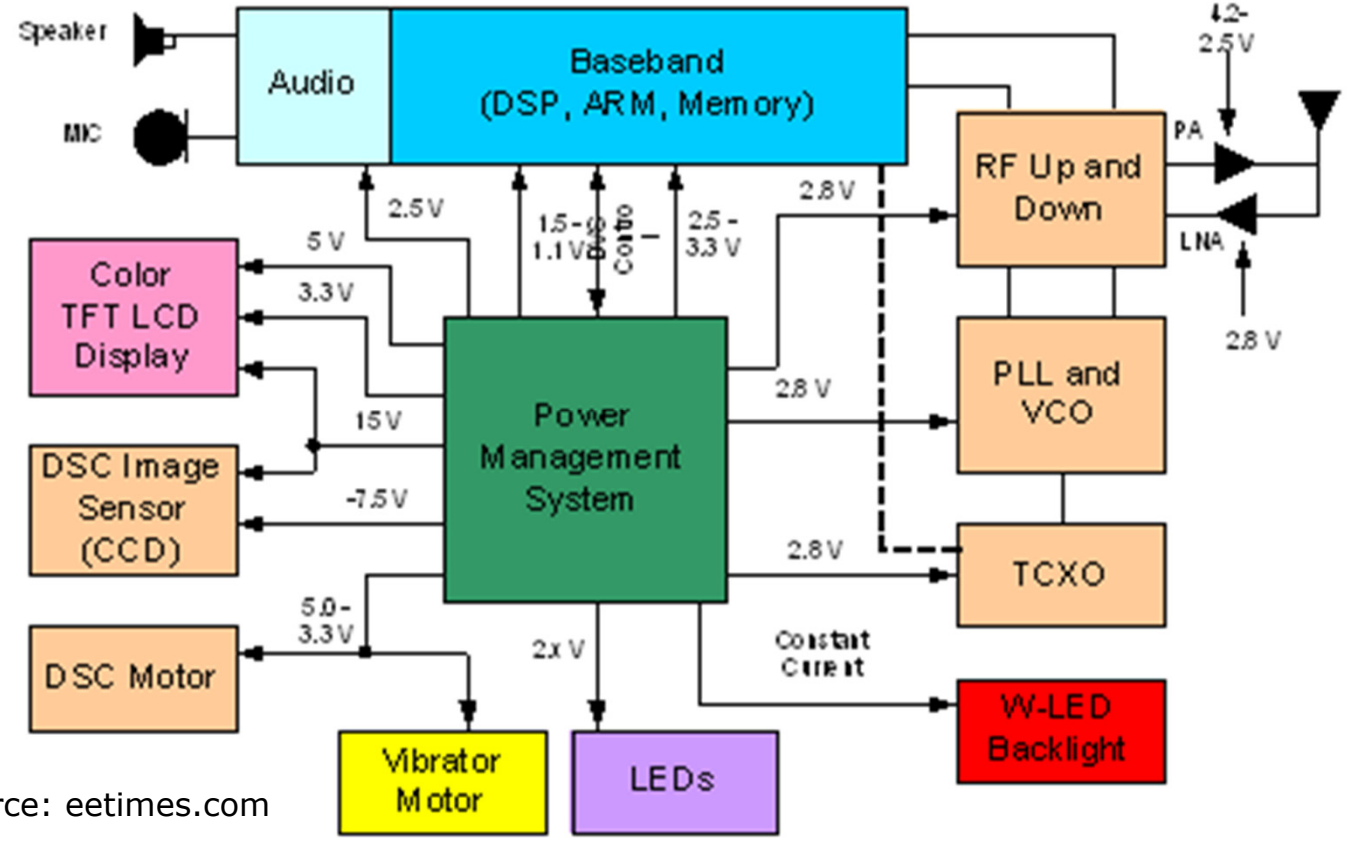
- Education
  - South China University of Technology, Guangzhou, BEng, MSc, ‘06 & ‘09
  - Hong Kong University of Science and Technology, Hong Kong, PhD, ‘13
- Experiences
  - Associate Professor, University of Macau, Macao, June 2020–
  - Assistant Professor, University of Macau, Macao, 2014–2020
  - Visiting Scholar, University of Twente, the Netherlands, 2013 Spring
- Research Interests
  - Fully-integrated voltage regulators
  - Wireless power transfer circuits and systems
- Awards
  - ISSCC 2017 Takuo Sugano Award for Outstanding Far-East Paper
  - IEEE Circuits and Systems Society Outstanding Young Author Award 2017
  - IEEE Solid-State Circuits Society Pre-doctoral Achievement Award 2013-14

What does power management do?

- "Cook" the (battery/line) energy for the customers (like processors).



Source: eetimes.com

Outline

- Introduction
- Basic Power Stage Selections
  - Linear Low-Dropout (LDO) Regulator
  - Switched-Capacitor Converter
  - Switched-Inductor Converter
- Control Loop Designs
  - PID Control
  - Hysteretic Control
- Advanced Topologies and Techniques
  - Resonant Switched-Capacitor Operation
  - Multiple Interleaving Phase
  - Switched-Capacitor-Inductor Hybrid Topologies
  - Distributed Integrated Voltage Regulators
- Summary

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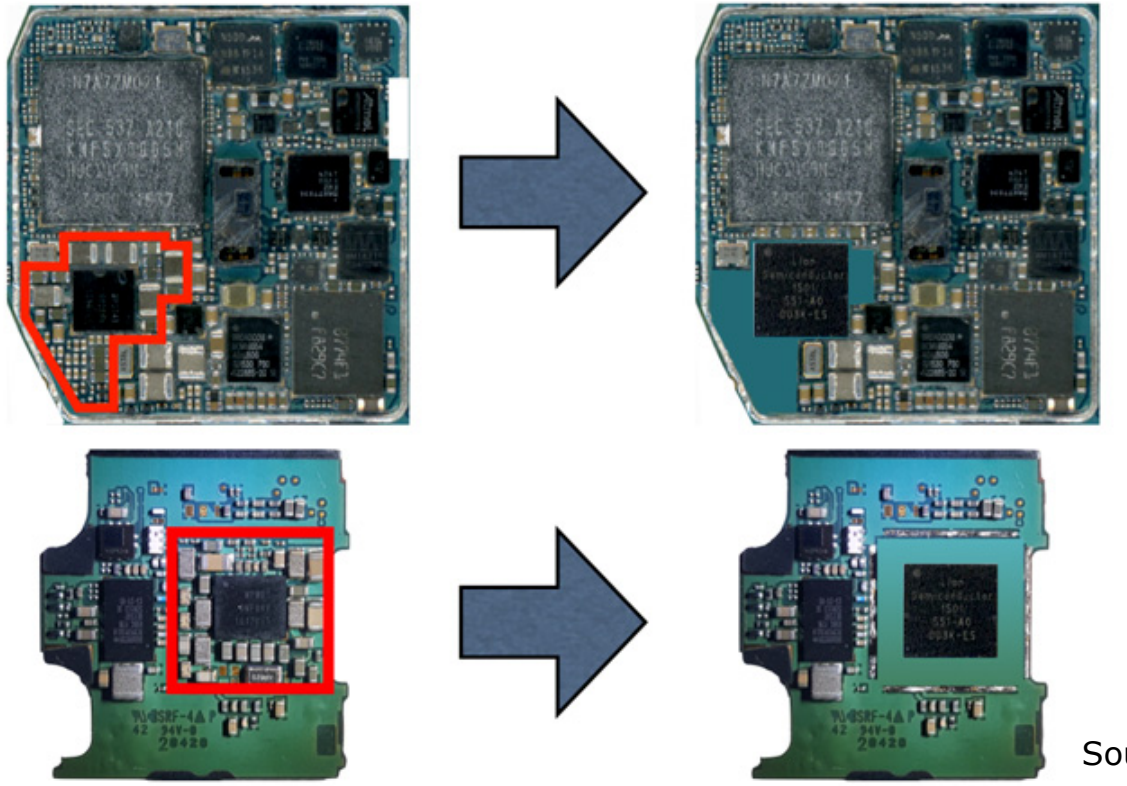
Fully Integrated Voltage Regulator (FIVR)

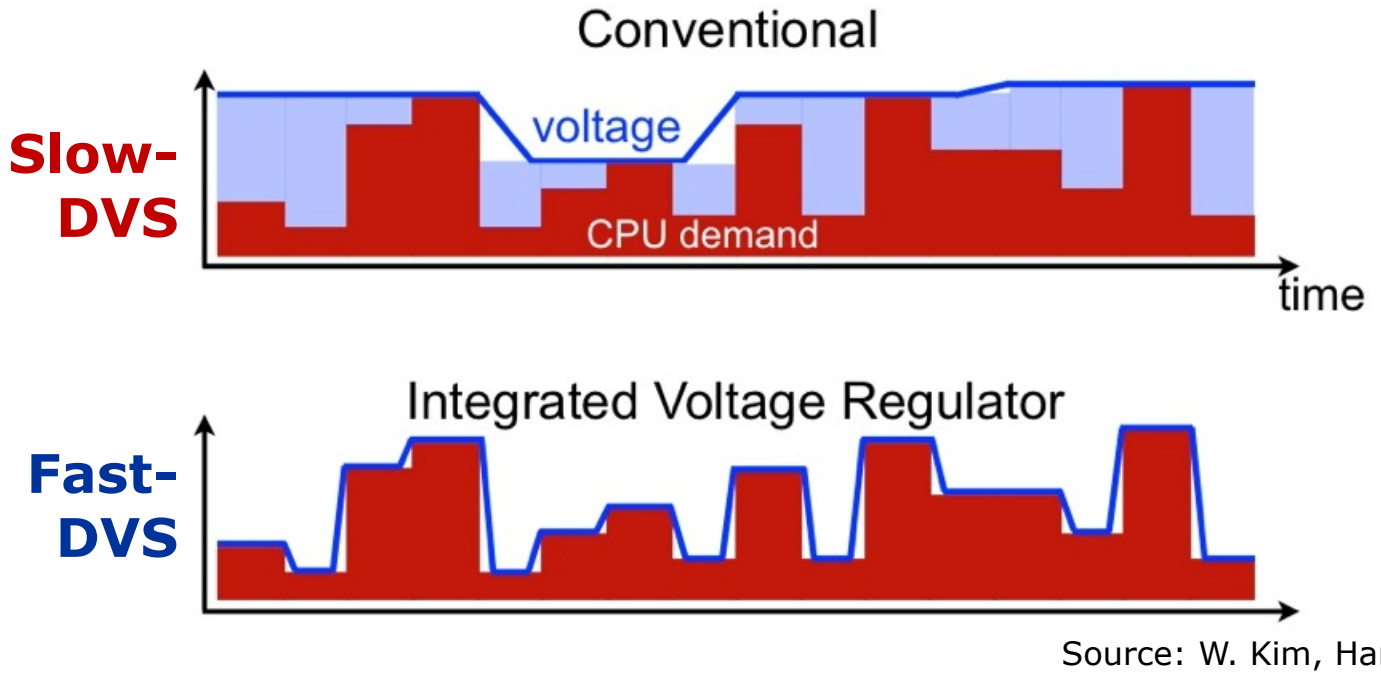


Source: Lion Semi

- Compact size, reduce number of pads, faster transient response, reduce IR drop, fine-grained voltage domains.

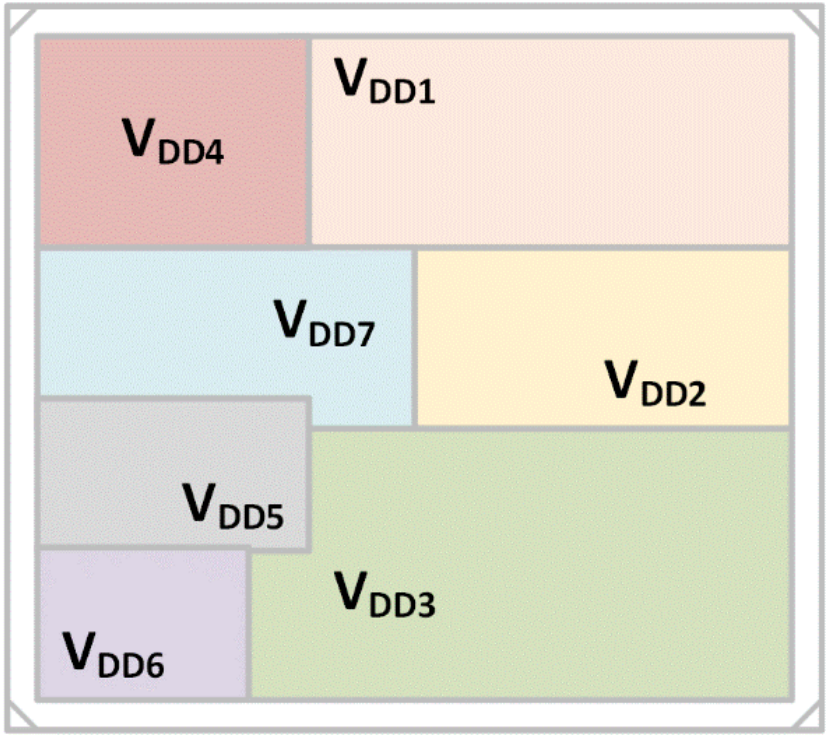
Dynamic Voltage and Frequency Scaling (DVFS)

- Decrease V_{DD} and F_{CLK} when the CPU is idle.
- Increase V_{DD} and F_{CLK} when the CPU needs high performance.
- Transition time is also considered as wasting power.
- **Fast-DVS can significantly save power.**



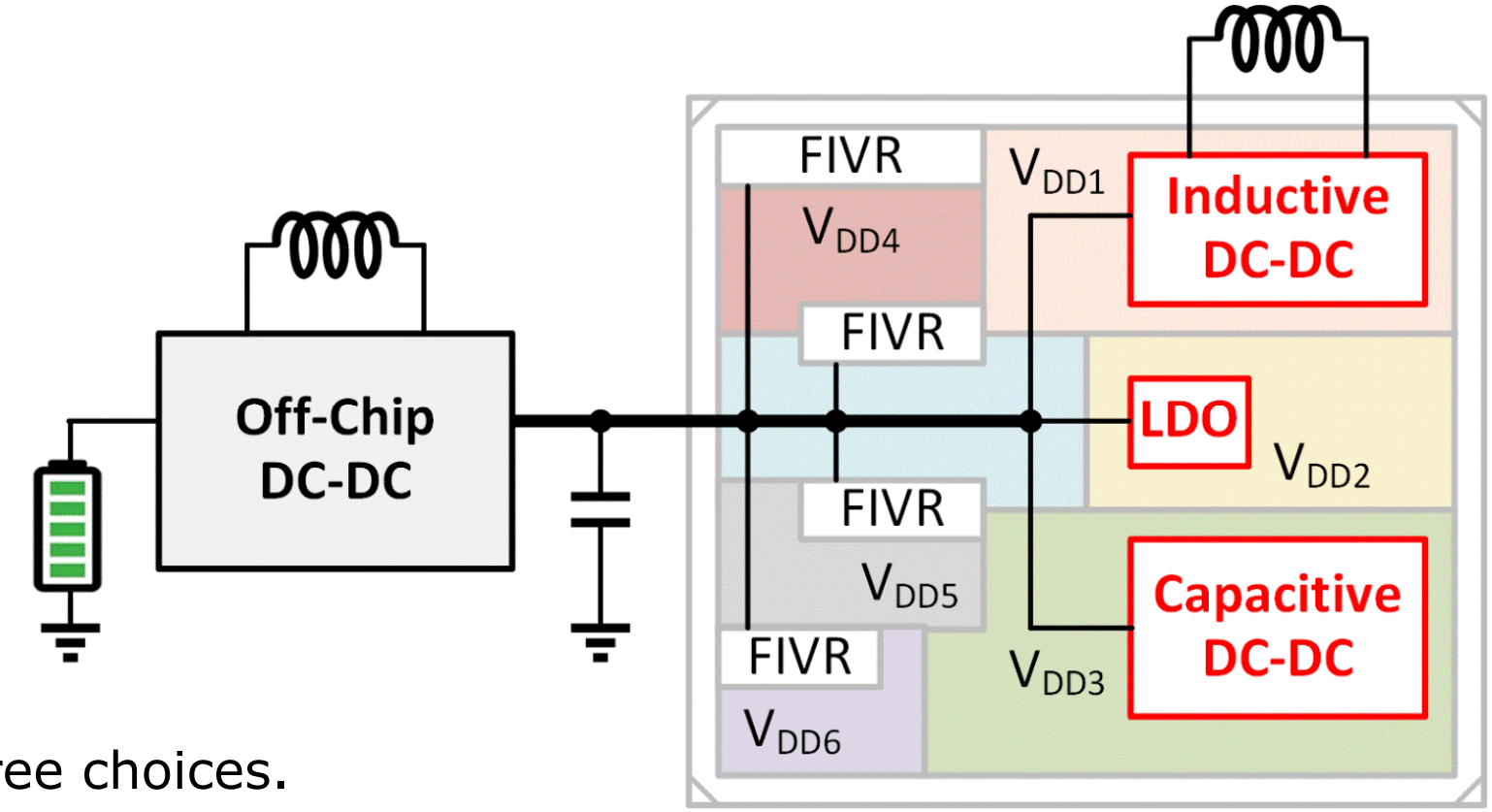
Source: W. Kim, Harvard

Fine-Grained Power Domains (Granular power)



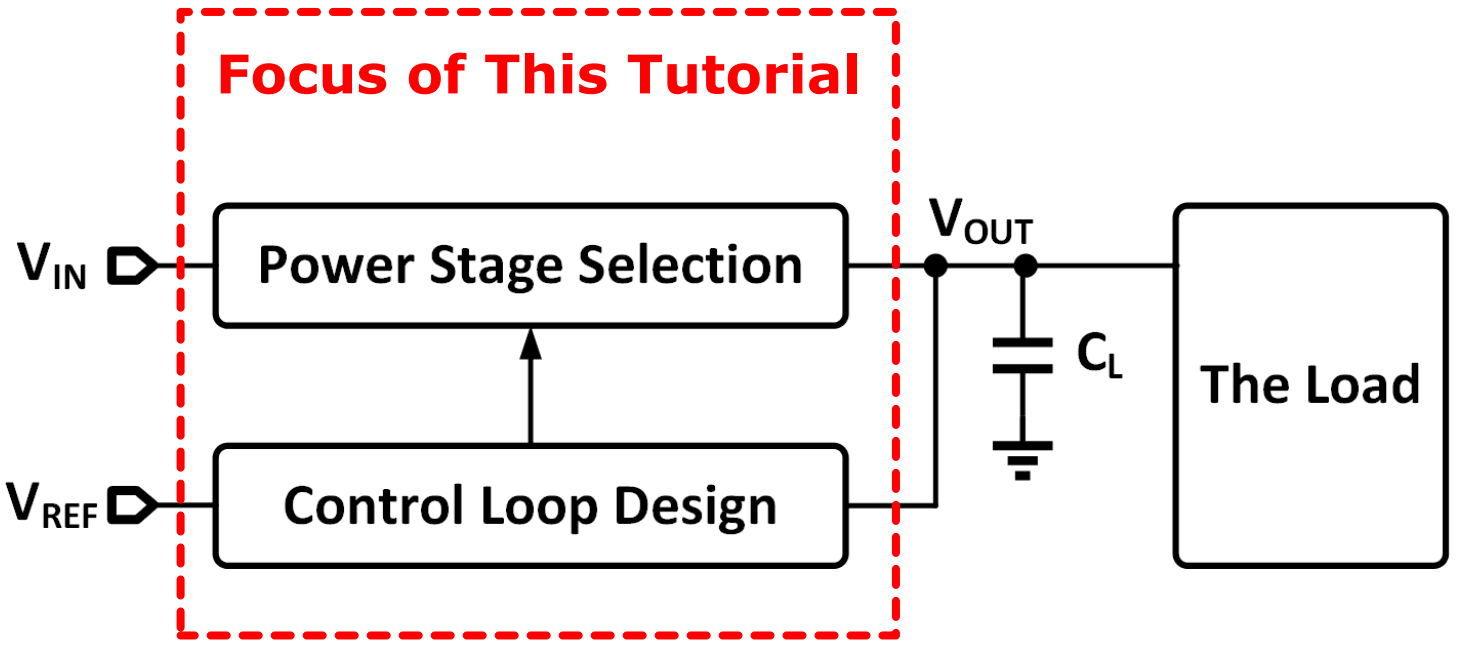
- Energy-efficient computing.
- Granular power needs FIVRs with small area and fast response.

FIVR Candidates



- Basically three choices.
  - Low dropout (LDO) regulator
  - Switched-capacitor (capacitive) DC-DC converter
  - Switched-inductor (inductive) DC-DC converter

What we will cover in this tutorial.



Power stage selection + Control loop design
for fully-integrated voltage regulator (FIVR)

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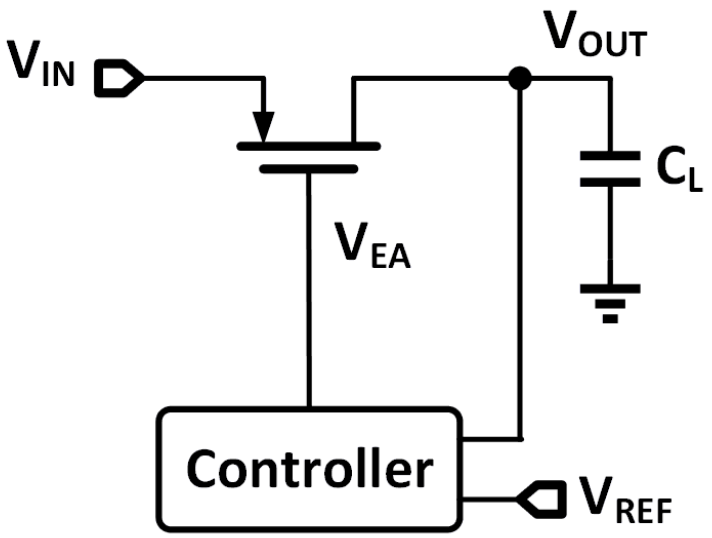
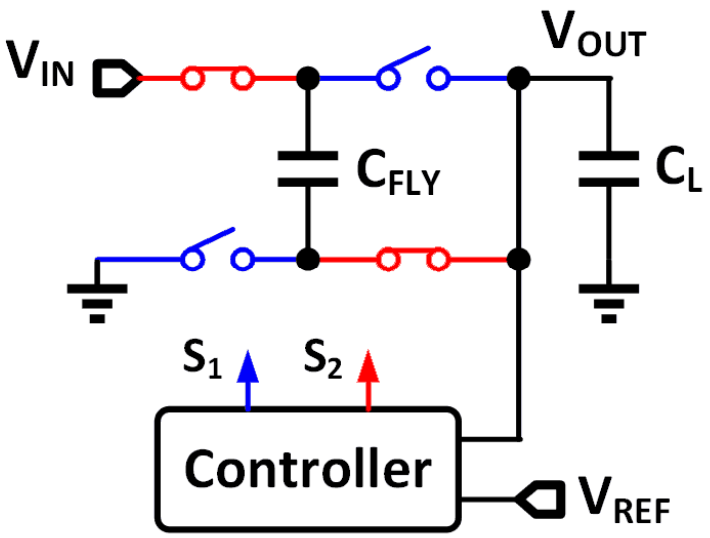
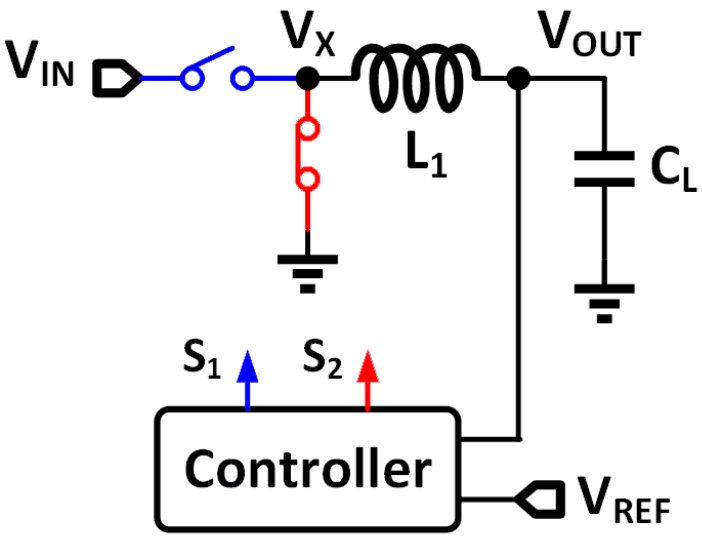
Basic Power Stage (Step-Down) Choices



LDO Regulator



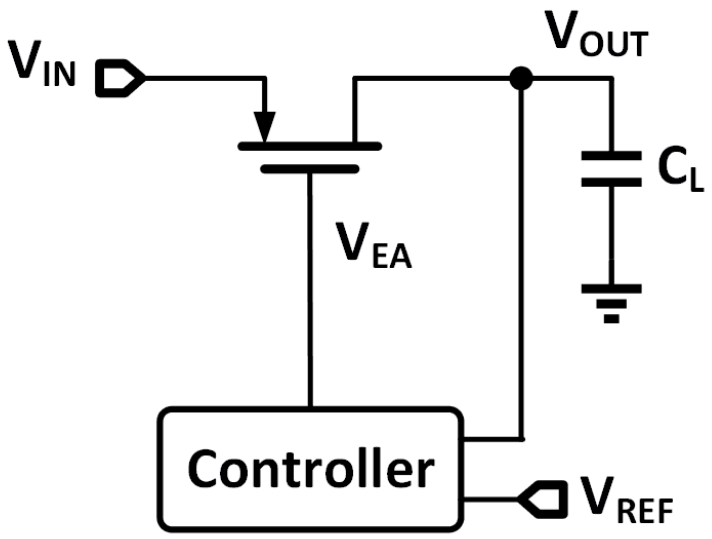
Switched-Capacitor (SC) or Capacitive DC-DC (a.k.a. Charge Pump)



Switching-Mode or Inductive DC-DC

Step-down (Buck) Converter

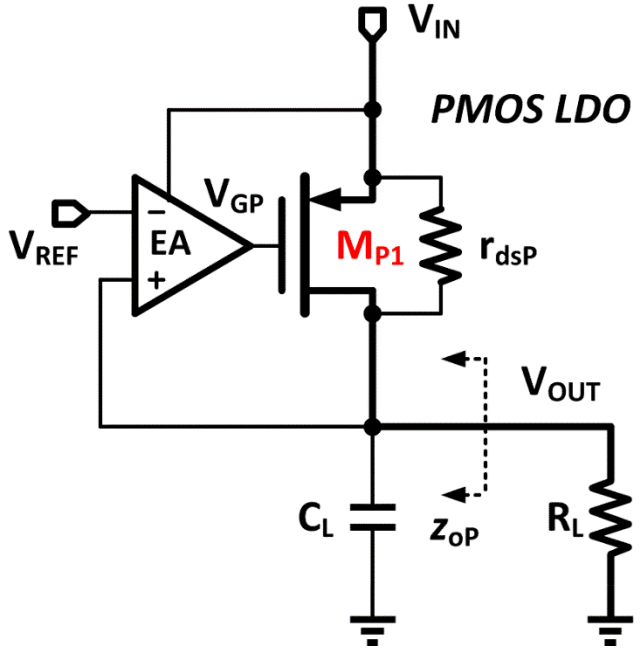
LDO Characteristics

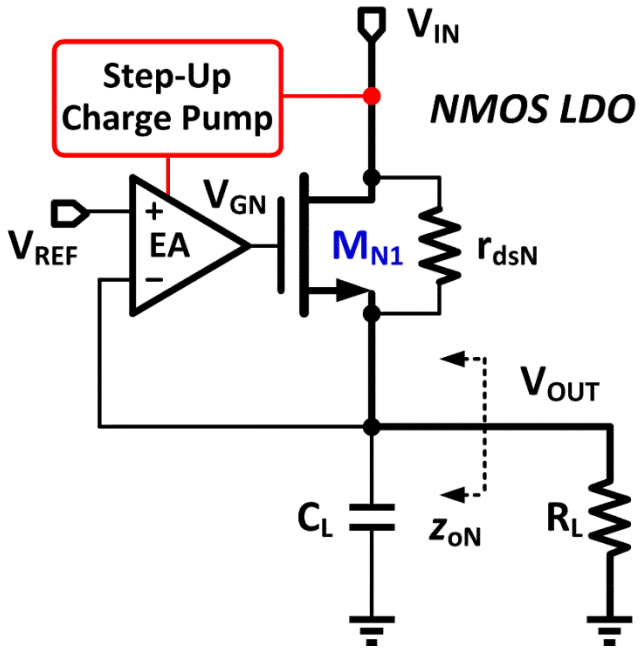


LDO Regulator

- Power transistor operates in linear or saturation region, acts as a tunable resistor.
- Low efficiency. Efficiency ≈ V_{OUT}/V_{IN}.
- Single pole power stage, easy to control.
- No energy storage components (C or L), tiny.
- Fast transient response.
- No switching activity (analog control), no ripple.

Output Impedances of the PMOS and NMOS LDOs





$$z_{oP} = r_{dsP} \parallel \frac{1}{sC_L} \parallel \frac{1}{A(s)\cdot g_{mP}}$$

$$z_{oP} = \frac{r_{dsP}}{1 + s\cdot r_{dsP}C_L + A(s)\cdot g_{mP}r_{dsP}}$$

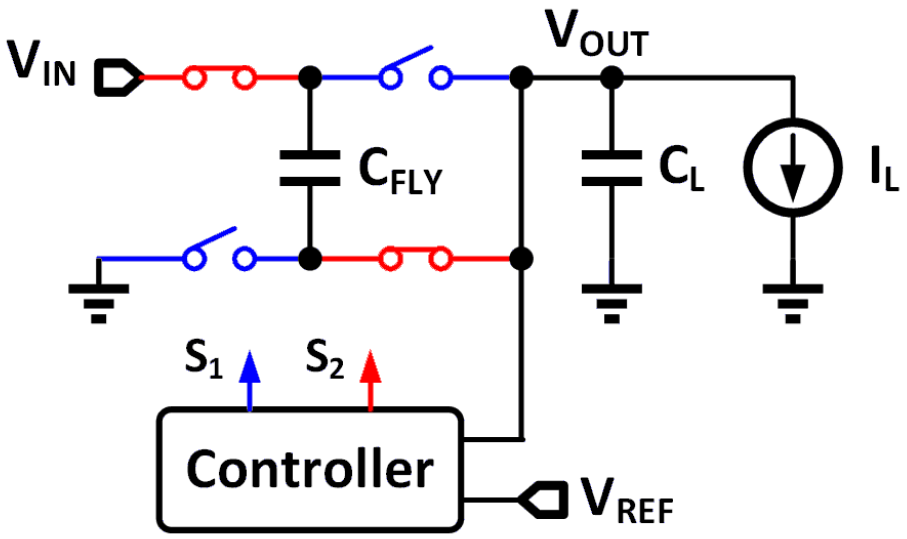
$$z_{oP,\,LF} \approx 1/A(s)\cdot g_{mP} \qquad z_{oP,\,HF} \approx 1/sC_L$$

$$z_{oN} = r_{dsN} \parallel \frac{1}{sC_L} \parallel \frac{1}{(1+A(s))\cdot g_{mN}}$$

$$z_{oN} = \frac{r_{dsN}}{1 + s\cdot r_{dsN}C_L + (1+A(s))\cdot g_{mN}r_{dsN}}$$

$$z_{oN,\,LF} \approx 1/A(s)\cdot g_{mN} \qquad z_{oN,\,HF} \approx 1/\left(sC_L + g_{mN}\right)$$

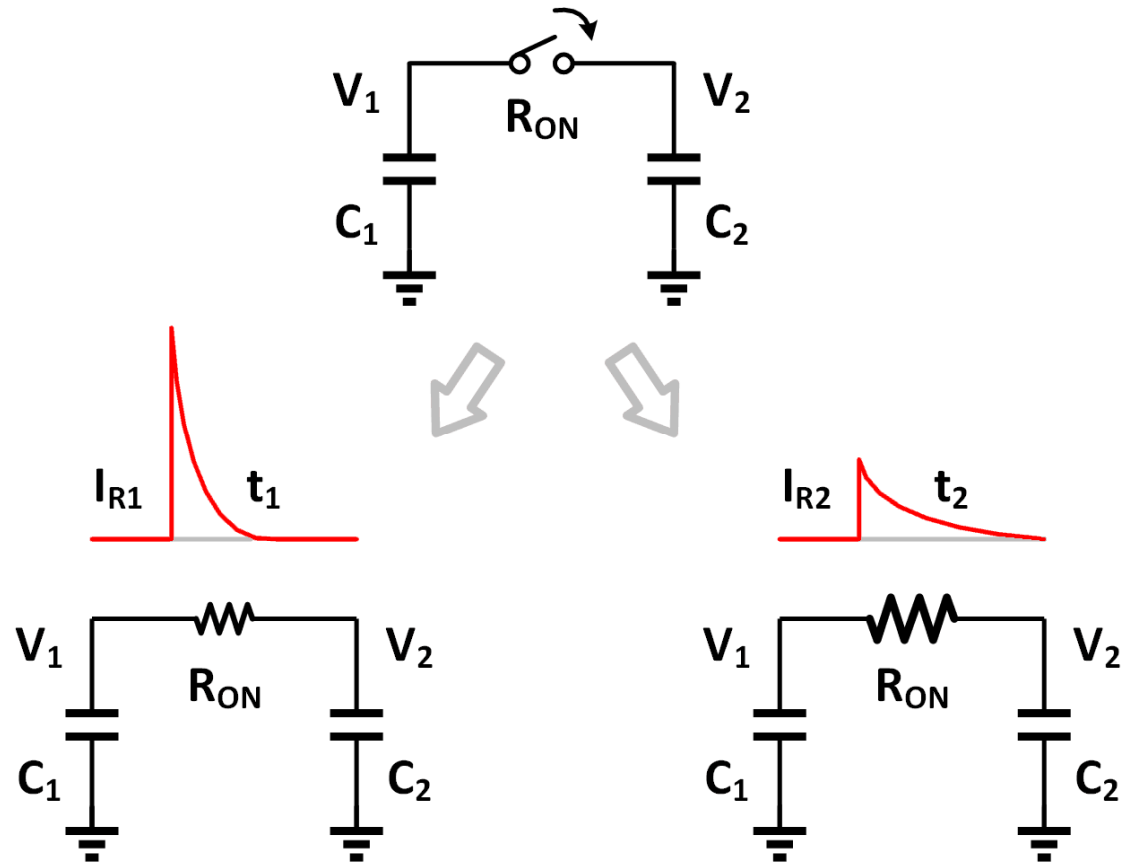
Analogue of Charge Pump



Bottleneck (Switch)

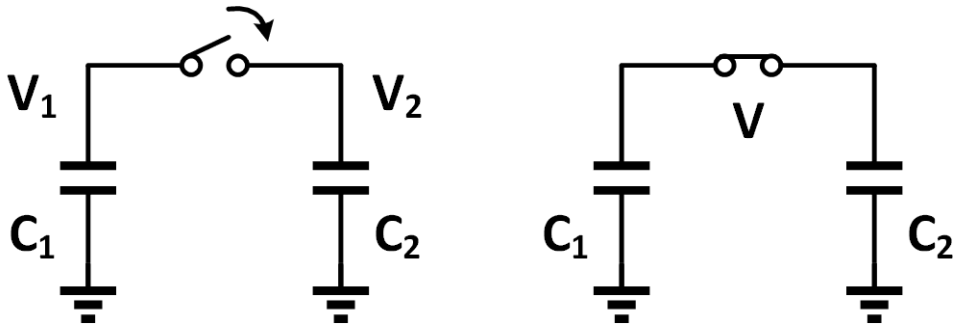
- Fly capacitor is the cup or bottle.
- The bucket is C_L.
- The load drain current from C_L.
- In fast switching, switch is the bottleneck.

Transfer Charge Between Capacitors



- To transfer charge between capacitors, the dissipation on the resistor (switch) is irrelevant to the resistance!

Charge Redistribution Loss (Hard Charging)



$$C_1V_1 + C_2V_2 = (C_1 + C_2)V \qquad V = \frac{C_1V_1 + C_2V_2}{C_1 + C_2}$$

$$E_{Cap} = \frac{1}{2}CV^2$$

$$E_{Initial} = \frac{1}{2}C_1V_1^2 + \frac{1}{2}C_2V_2^2$$

$$E_{Final} = \frac{1}{2}(C_1 + C_2)V^2$$

$$E_{Loss} = E_{Initial} - E_{Final} = \frac{1}{2}\left(\frac{C_1C_2}{C_1 + C_2}\right)(V_1 - V_2)^2$$

Assume

$$C_1 = C_2 = C$$

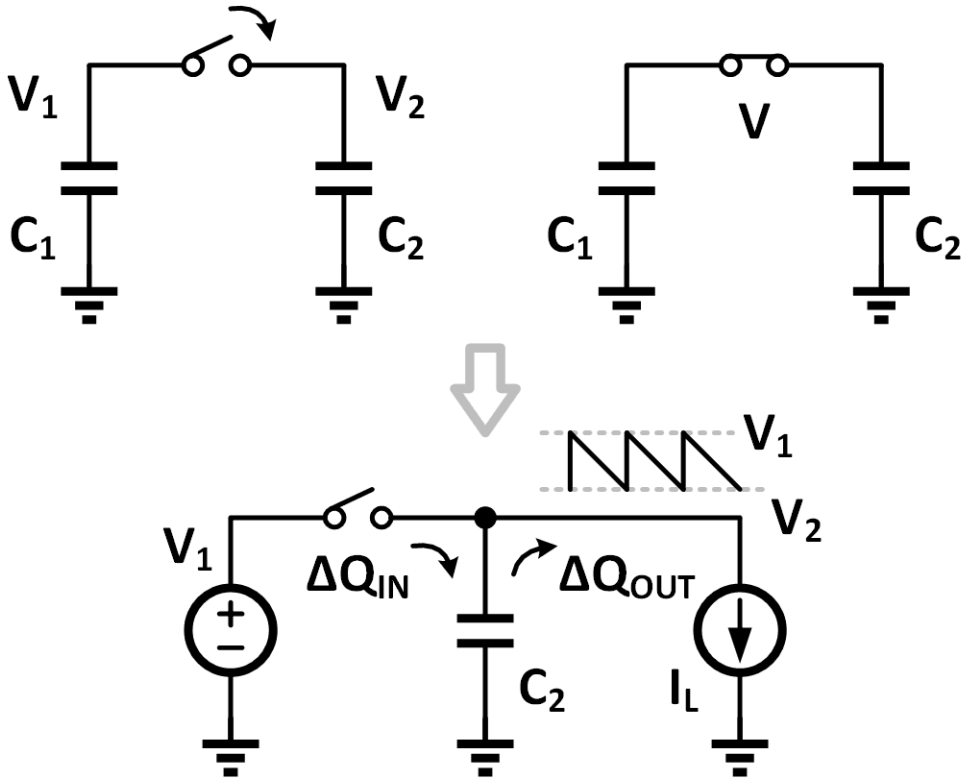
$$\Delta V = 0.5(V_1 - V_2)$$

We have

$$E_{Loss} = E_{Initial} - E_{Final}$$
$$= C\Delta V^2$$

E_{Loss} is proportional to ΔV^2.

Charge Redistribution Loss



$$E_{Loss} = \frac{1}{2}\left(\frac{C_1 C_2}{C_1 + C_2}\right)(V_1 - V_2)^2 = \frac{1}{2} C_2 (V_1 - V_2)^2$$

$$C_1 \to \infty \qquad = \frac{1}{2}(V_1 - V_2)\Delta Q_{IN}$$

Assume C_1 >> C_2, then, V_1 barely changes and C_1 can be considered as a voltage source.

A current source is connected to C_2 as a load, and V_1 refreshes C_2 periodically.

$$E_{Loss} = \frac{1}{2}(V_1 - V_2)\Delta Q_{IN}$$

$$E_{Load} = \frac{V_1 + V_2}{2}\Delta Q_{OUT}$$

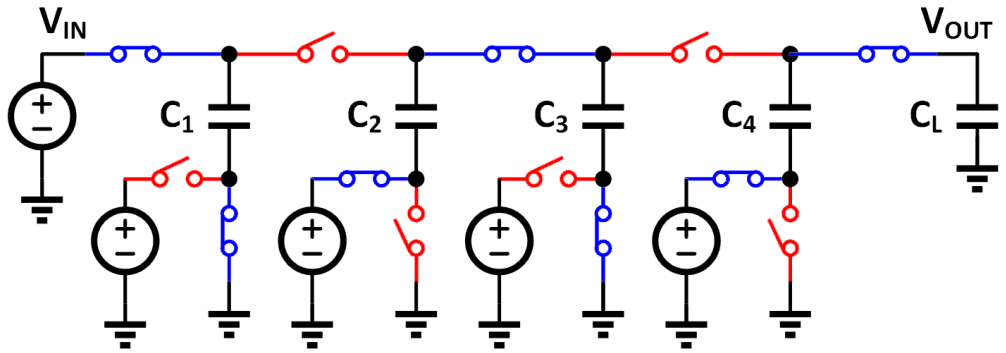
$\Delta Q_{IN} = \Delta Q_{OUT}$ In steady-state

$$\eta = \frac{E_{Load}}{E_{Loss} + E_{Load}}$$

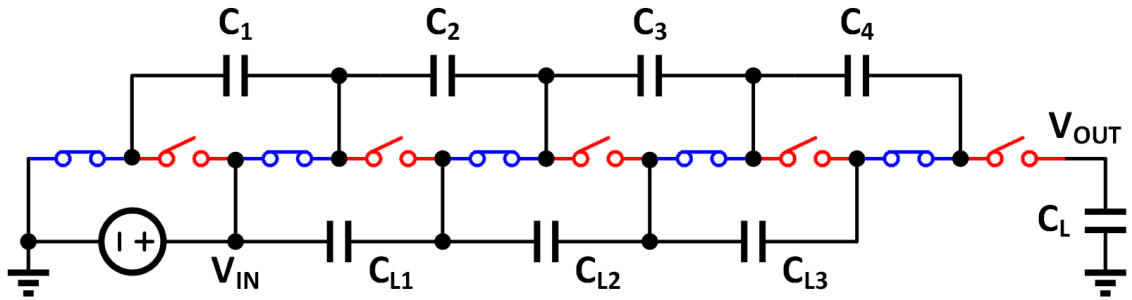
$$= \frac{(V_1 + V_2)/2}{V_1} = \frac{V_{2,AVG}}{V_1}$$

Linear-VCR Topologies and Fibonacci Topology

- Dickson

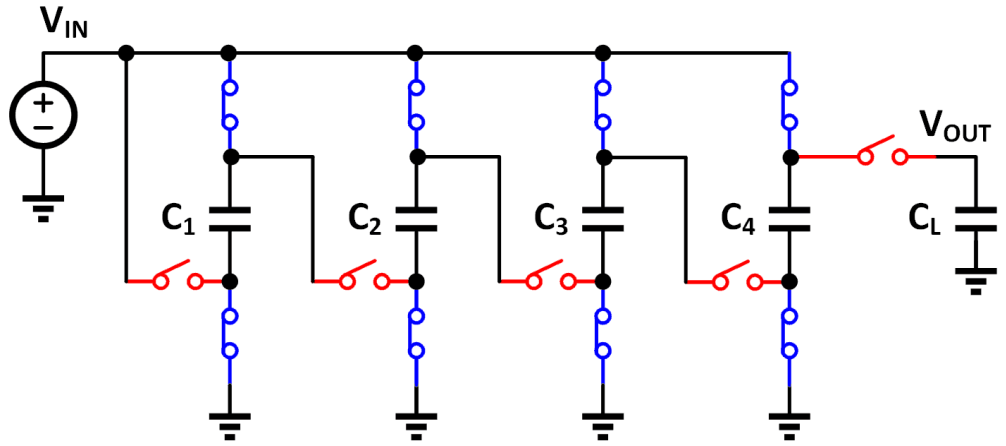


- Ladder

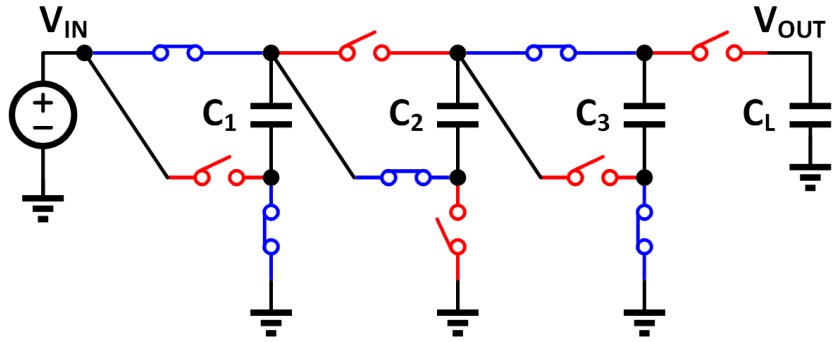


VCR=(N+1)V_{IN}, N: no. of flying capacitors

- Series-Parallel

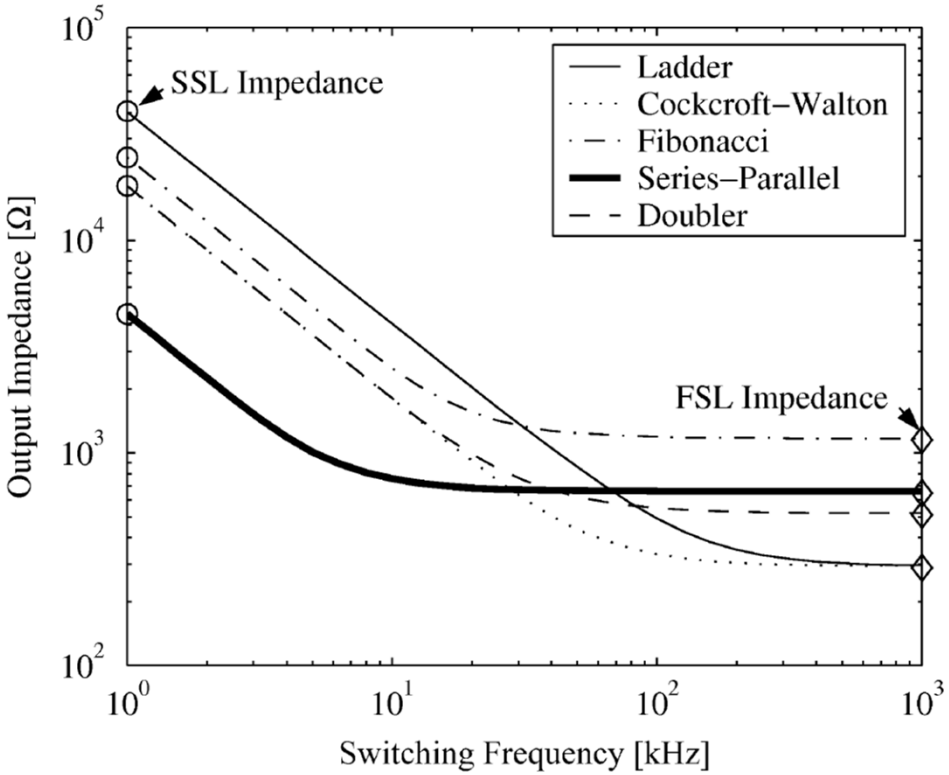


- Fibonacci (VCR = 2, 3, 5, 8, …)



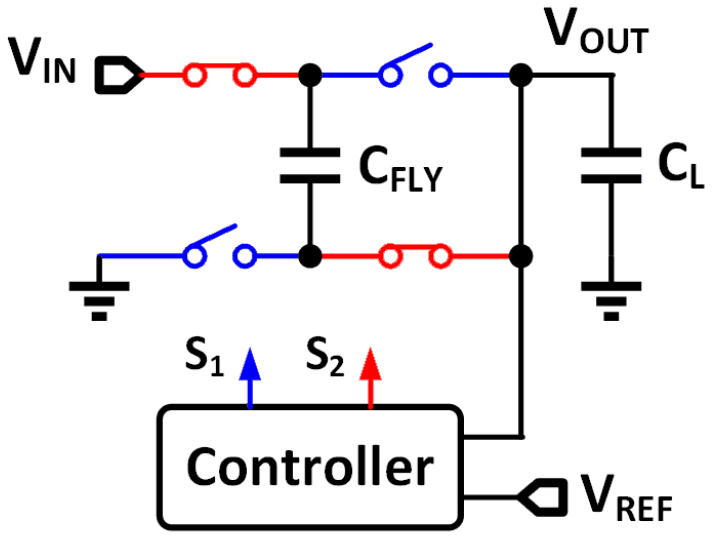
SC Topology Comparisons

- Series-Parallel (SP)
  - Using the capacitors more efficiently.
  - Large switch resistances in the series state.
  - Suitable for capacitor limited case, like in FIVR.
- Cockcroft-Walton (Dickson) and Ladder
  - Perform better at fast switching frequency.
  - Smaller equivalent capacitance compared to SP.
  - Suitable for solution with large capacitance.
- Fibonacci
  - Not good in both capacitor and switch usage.
  - Suitable for scenarios with limited number of discrete capacitors.



[M. D. Seeman, TPEL, 2008]

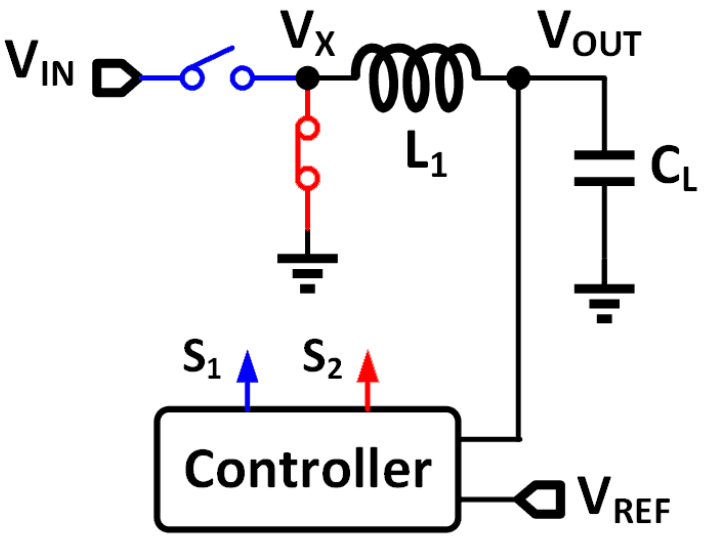
Switched-Capacitor (SC) Converter Characteristics



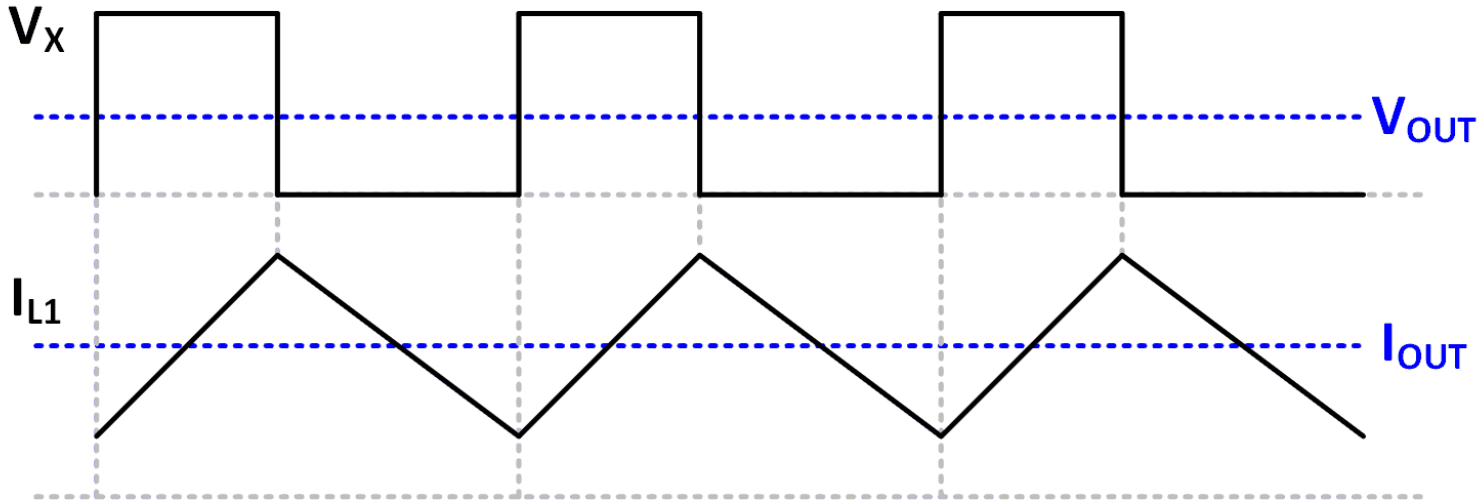
Capacitive DC-DC

- SC network acts as a tunable resistor, low efficiency.
- $V_{OUT}=VCR\times V_{IN}-I_{OUT}\times T/\alpha C_{FLY}$, where α is a topology related factor.
- Efficiency can be improved by having a proper voltage conversion ratio (VCR).
- More capacitors and switches for more VCRs.
- Single pole power stage, easy to control.
- Performances of both switches and capacitors improve with advanced processes, easy to integrate.
- Easy for multi-interleaving phase operation, reducing input and output ripples.

Operation of a Buck Converter

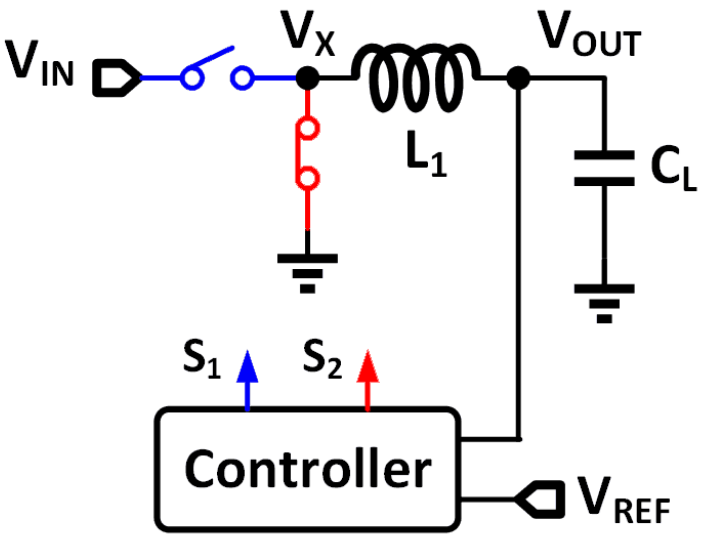


Inductive DC-DC



- $V_{OUT}=D\times V_{IN}$, where D is duty cycle of the switch S_1.
- V_{OUT} is an averaged value of V_X.
- I_{OUT} is an averaged value of I_{L1}.
- LC is a 2^{nd}-order filter.

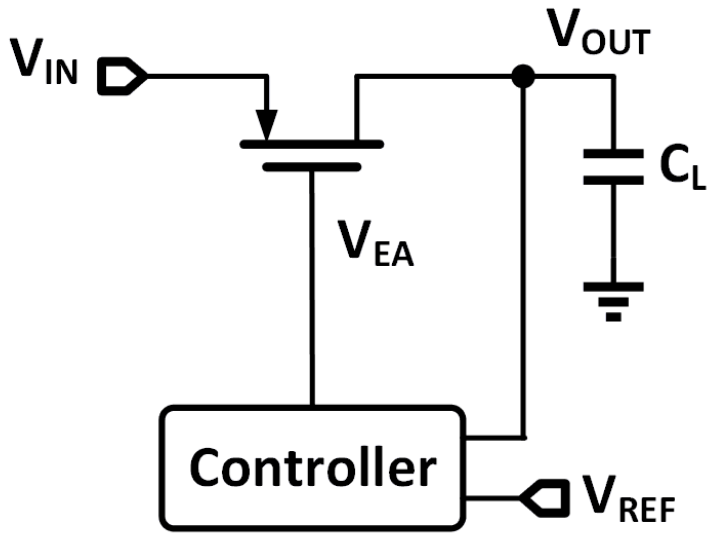
Switching-Mode Buck Converter Characteristics



Inductive DC-DC

- Energy transfer between L and C is ideally lossless, theoretically high efficiency.
- But, its efficiency heavily depends on the inductor Q.
- Inductor Q is limited by physical constrains.
- Inductor has intrinsically larger DCR than a capacitor, difficult to integrate.
- Switching noises can be large.
- High switching frequency (F_{SW}) for smaller passives, but with high switching losses.
- The LC filter forms a two-pole power stage, needs more complex compensation.

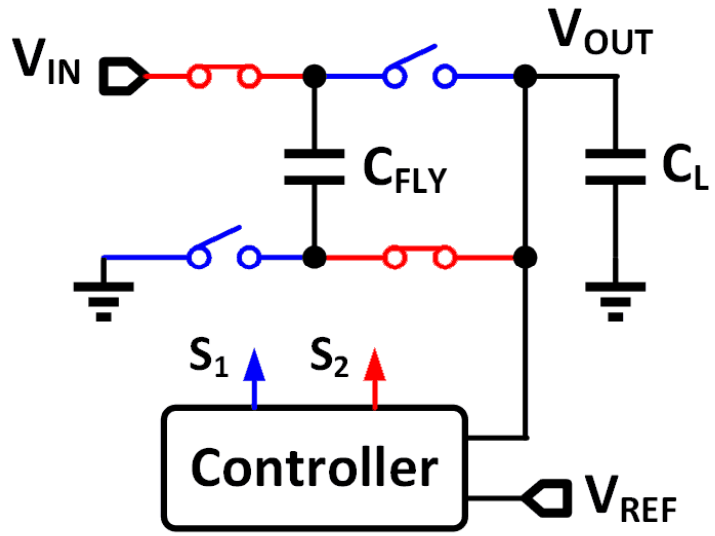
Power Stage Characteristics Brief Summary



LDO Regulator

Power transistor in linear region, acts as a tunable resistor, low efficiency.

No energy storage components (C or L), tiny.

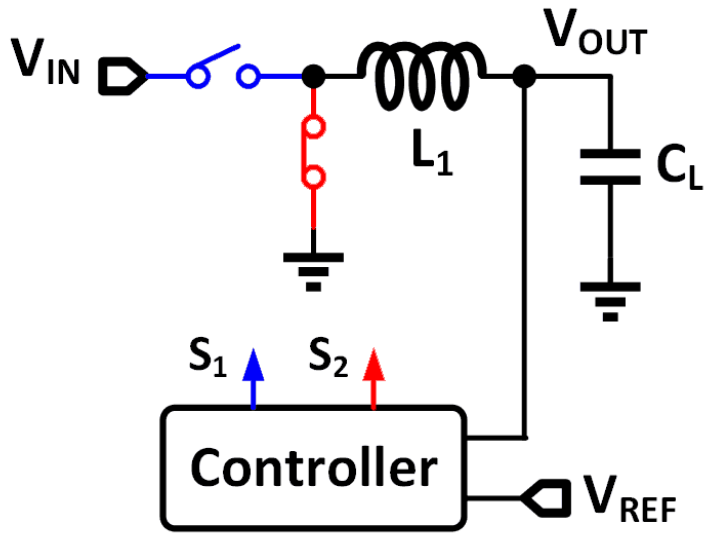


Capacitive DC-DC

SC network acts as a tunable resistor, low efficiency.

Discrete VCRs.

Efficiency can be improved by having a proper VCR.



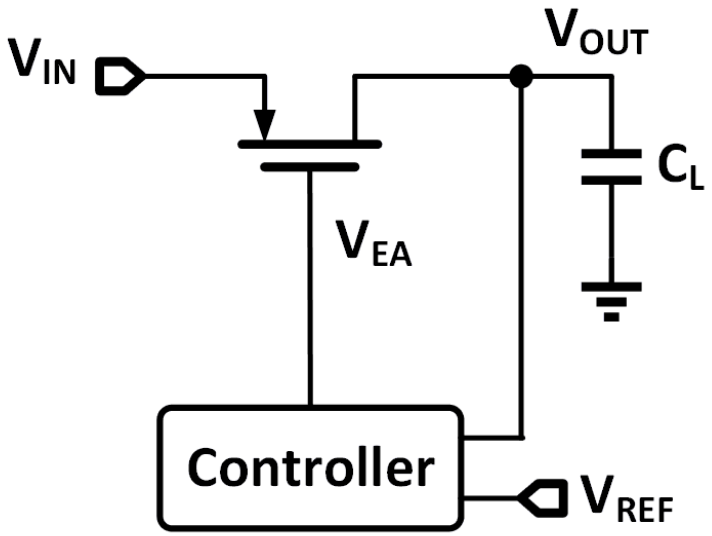
Inductive DC-DC

Continuous VCR.

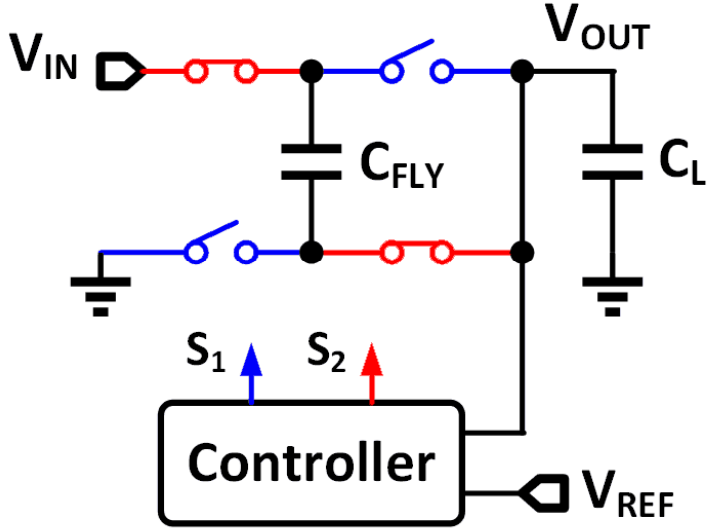
Efficiency heavily depends on the inductor Q.

Inductor has intrinsically larger DCR than a capacitor.

Advanced Power Stage Choices

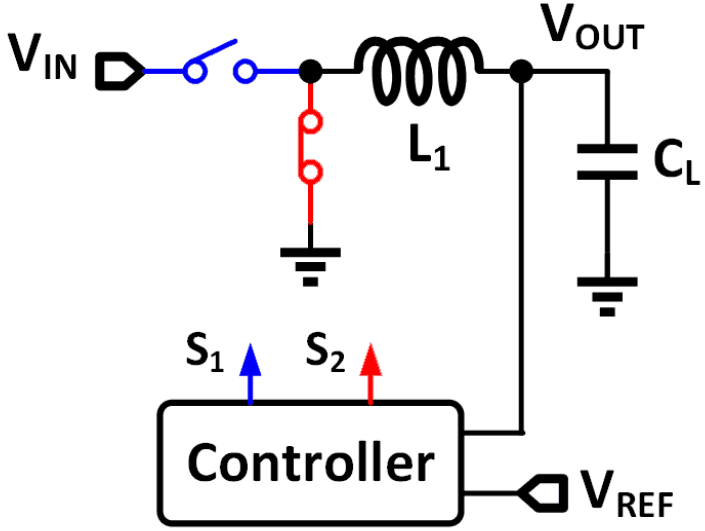


LDO Regulator



Capacitive DC-DC

More caps and switches for more voltage conversion ratios.



Inductive DC-DC

More caps and switches for hybrid operation with a smaller inductor.

Switched-Capacitor-Inductor Hybrid Topology!

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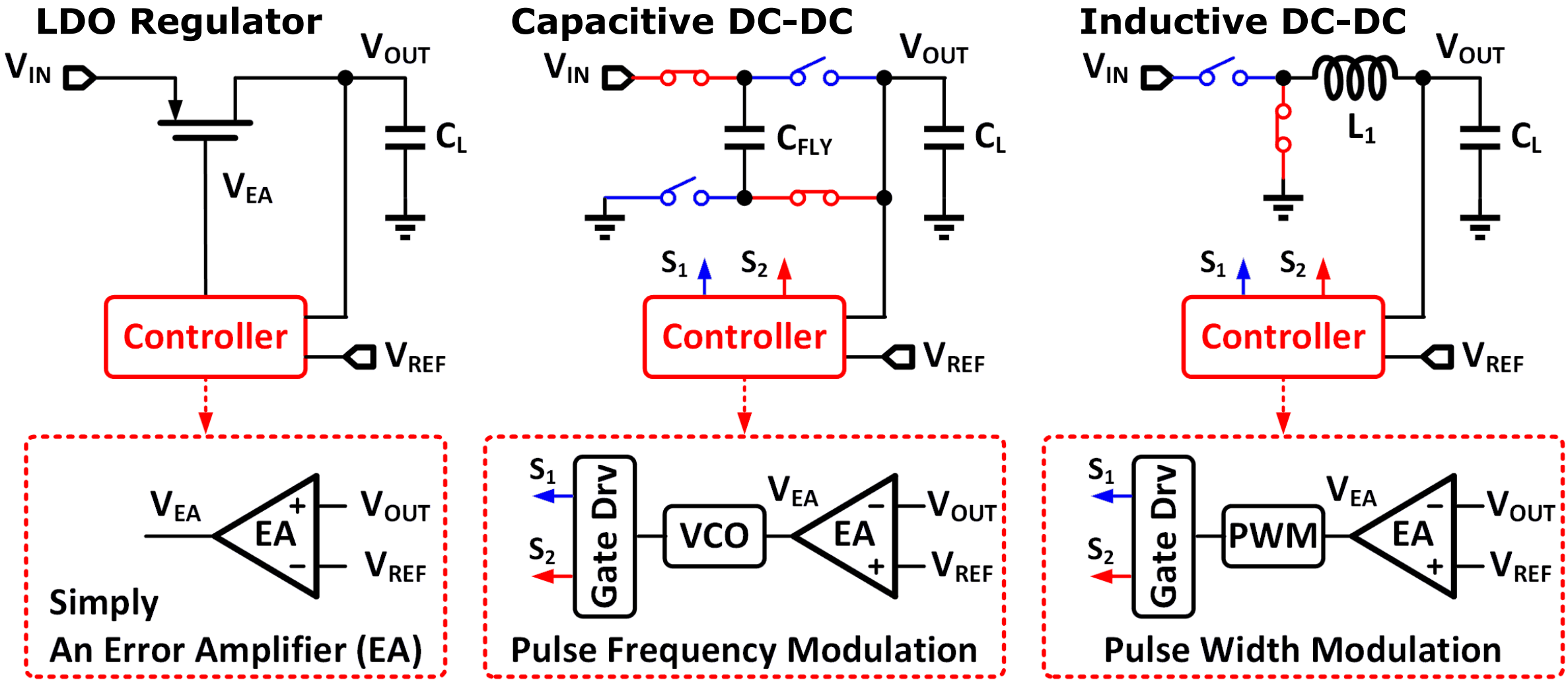
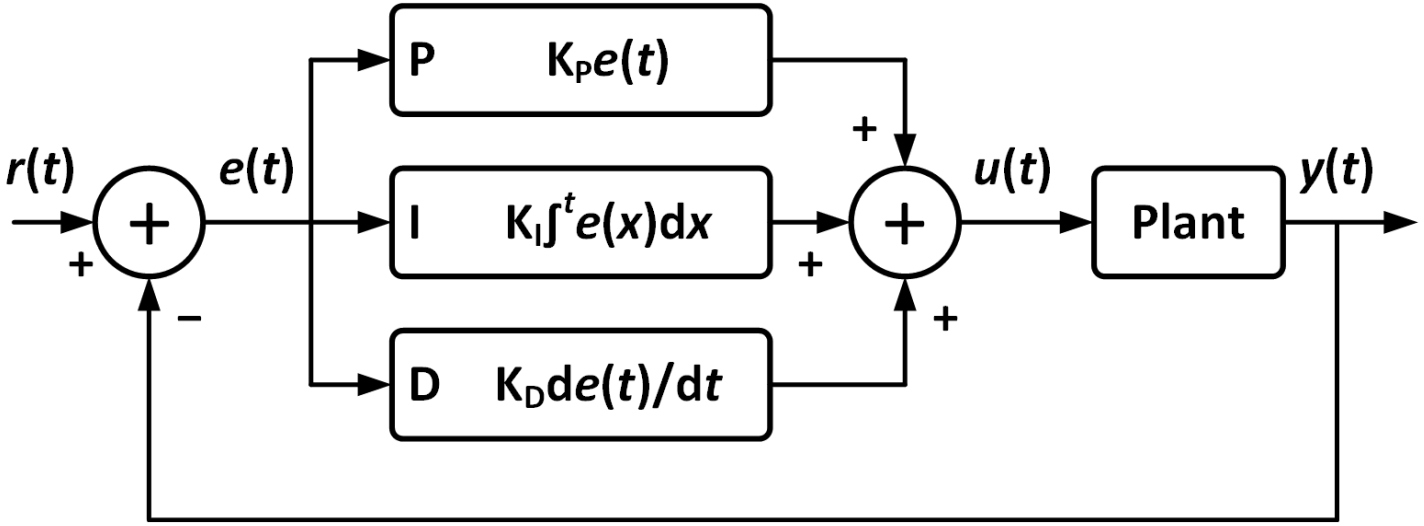
Basic Control Strategy for Each Selection



Proportional-Integral-Derivative (PID) Control

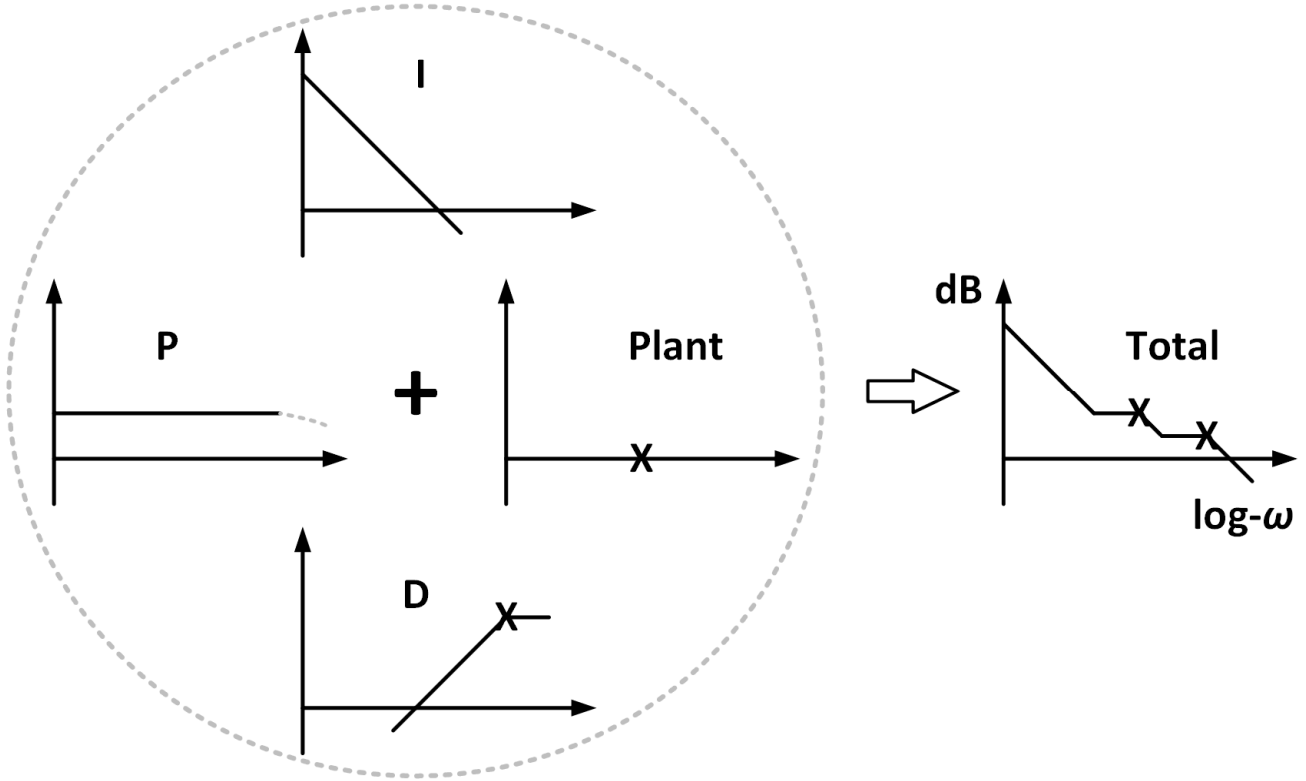


The plant is the power stage that being controlled.

$$u(t) = K_P e(t) + K_I \int_0^t e(x)dx + K_D \, de(t)/dt$$

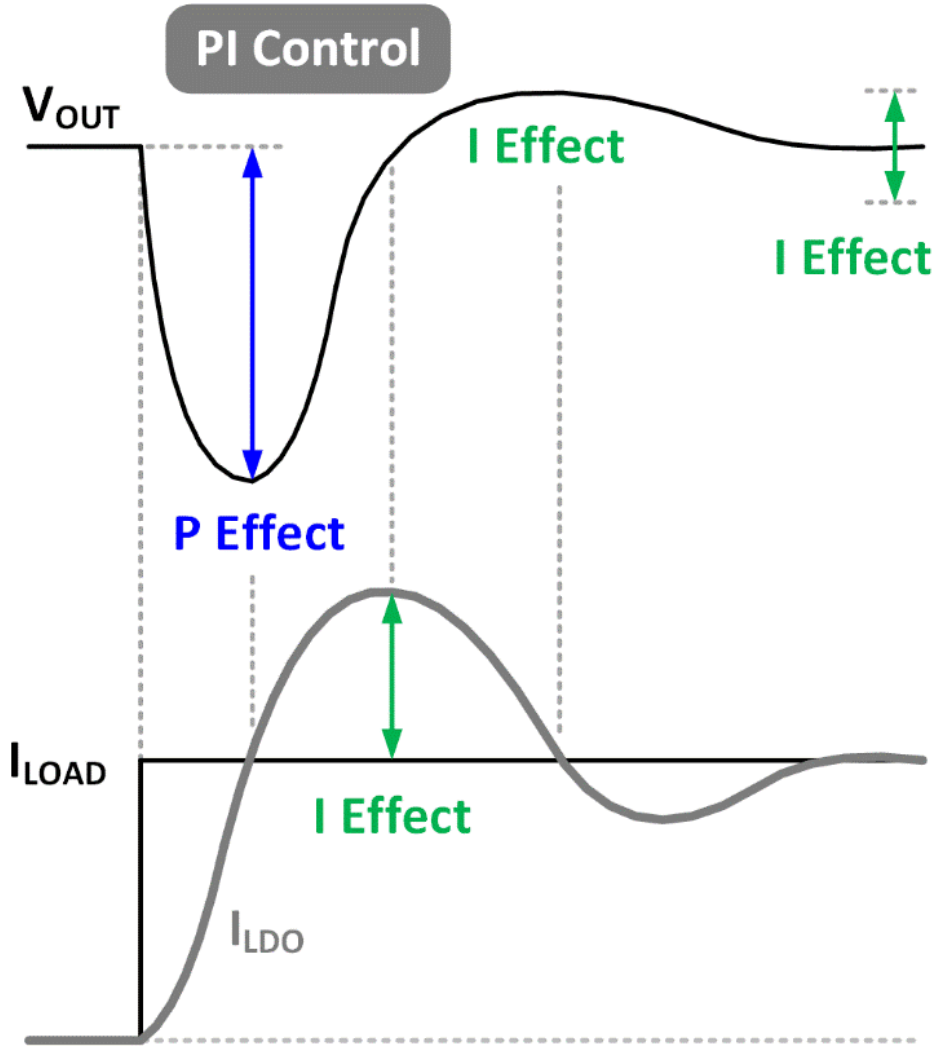
- The P path output is proportional to the **current** error.
- The I path integrates the **past** information.
- The D path predicts the **future** based on the rate of change.

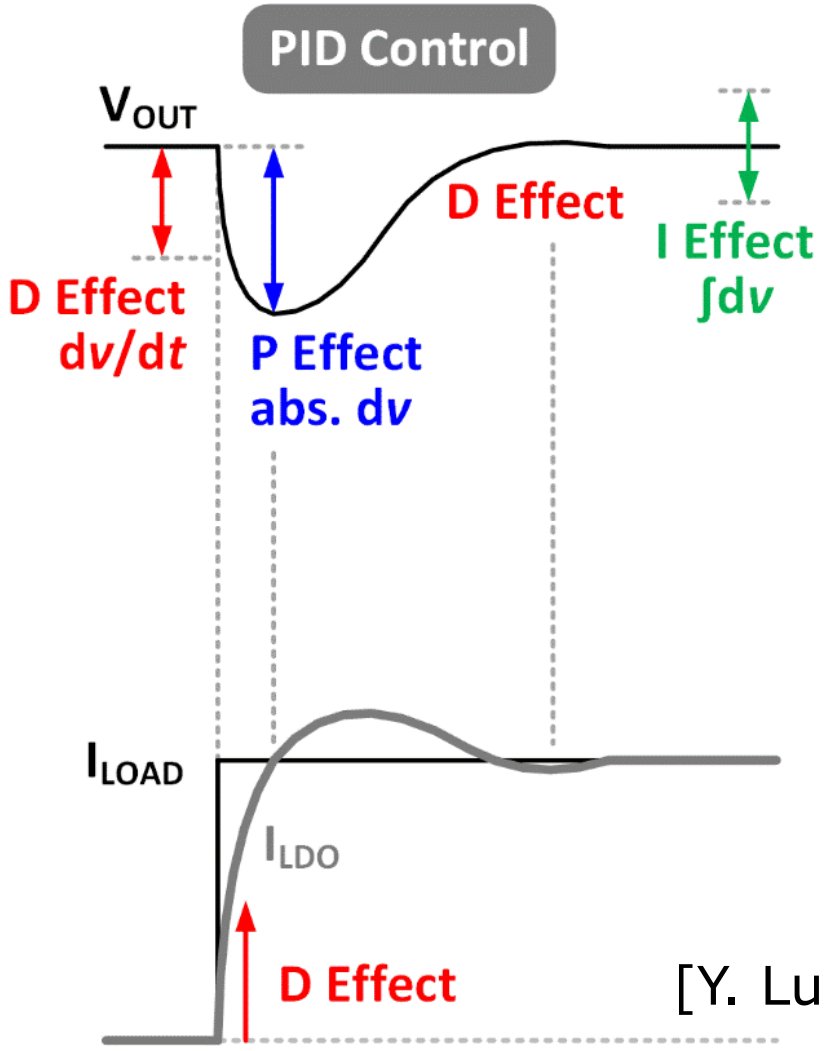
Bode Plots of PID Control Paths for an LDO



- The I path is a low pass filter.
- The P path may have poles beyond the frequency of interest.
- The D path processes high freq. (HF) signal, so is vulnerable to HF noise.

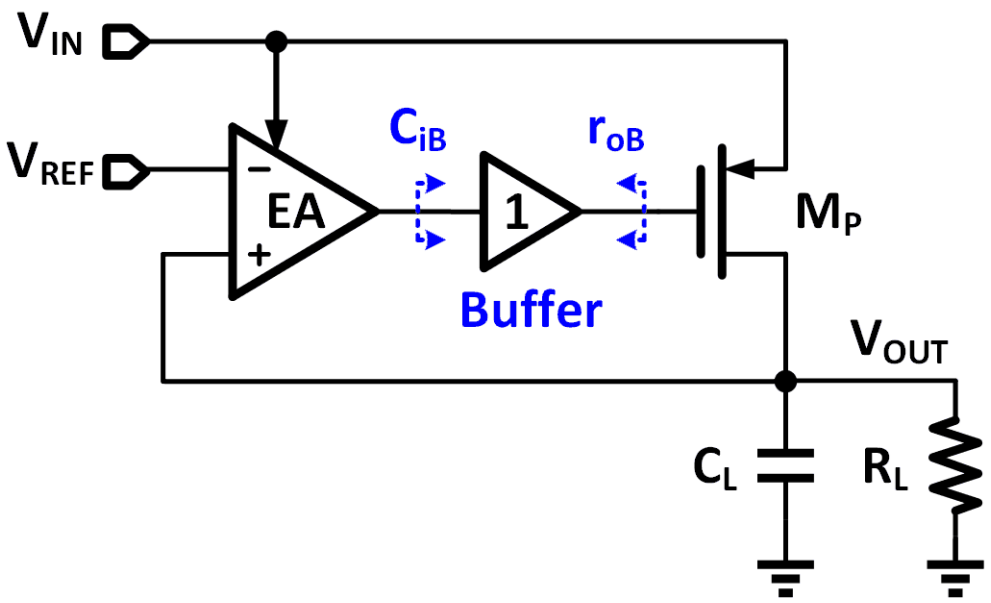
Load Transient Responses with PI or PID Controls

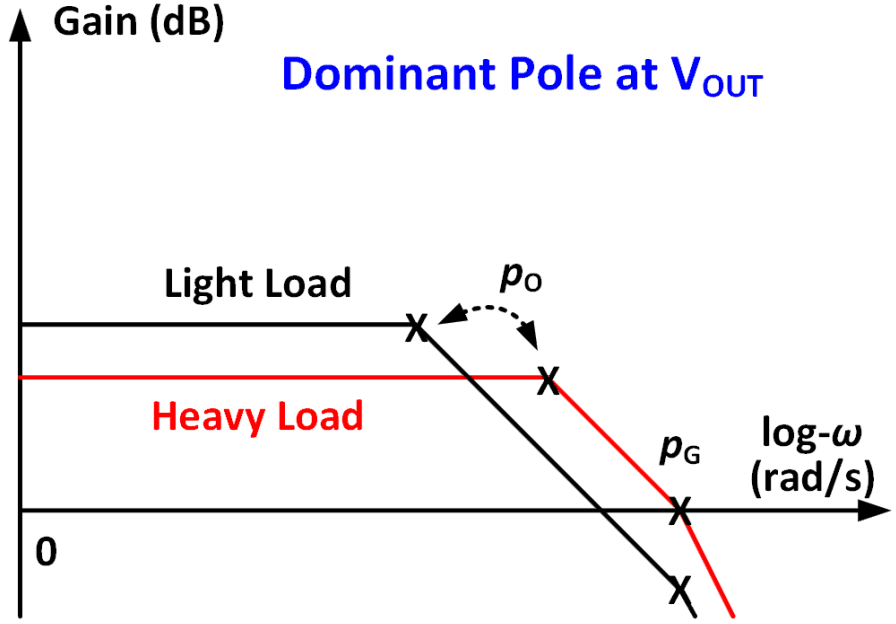




[Y. Lu, EDSSC, 2019]

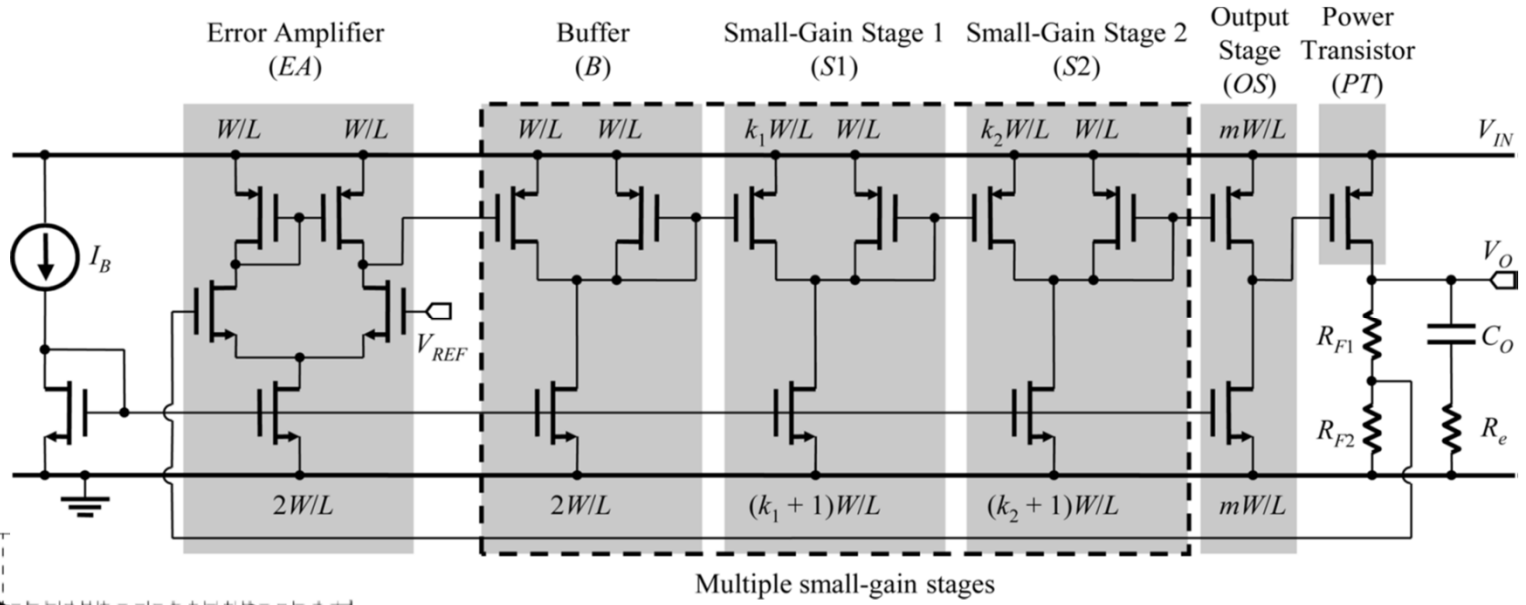
LDO with Proportional (P) Control

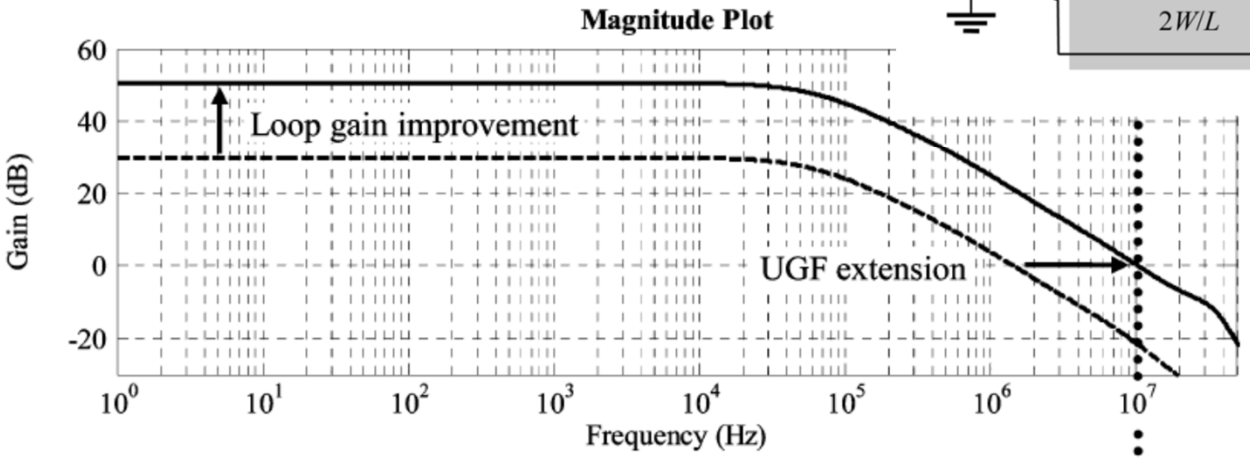




- Output pole dominant.
- Push internal poles to HF with buffer.
- Output current is proportional to the V_{OUT} error.
- **Fast, but poor accuracy.**

Example: LDO with Small-Gain Stages

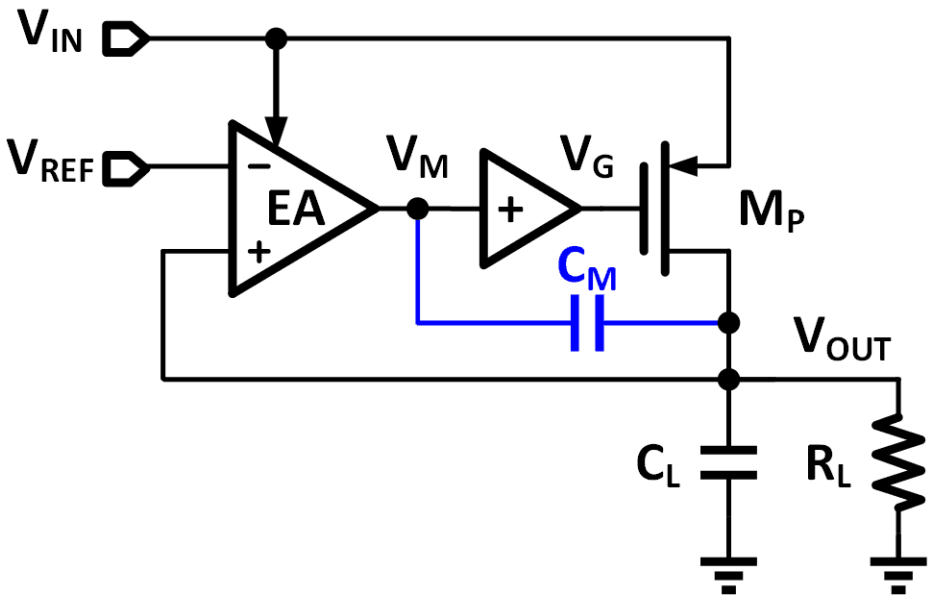


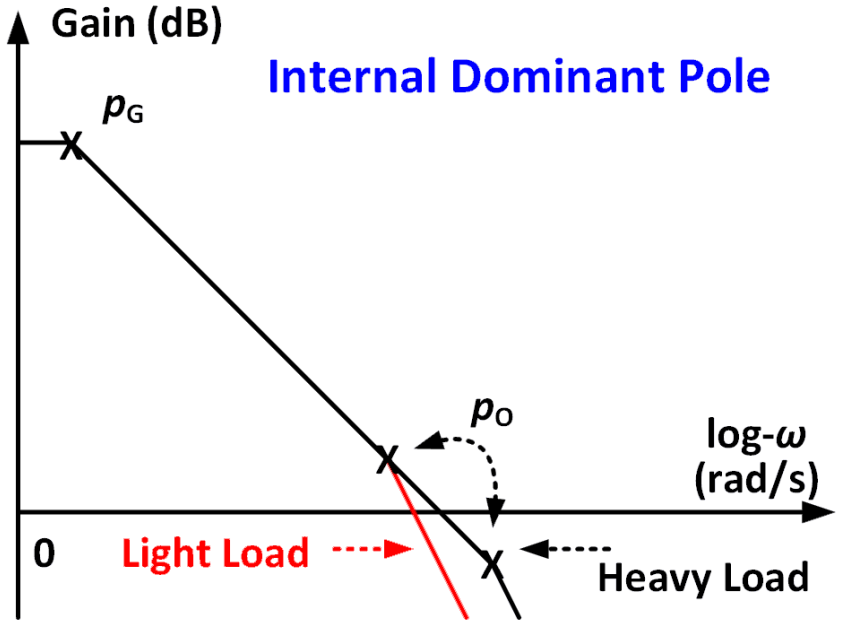


[M. Ho, JSSC, 2010]

- Increase the loop gain with multiple small-gain stages, advanced P control.

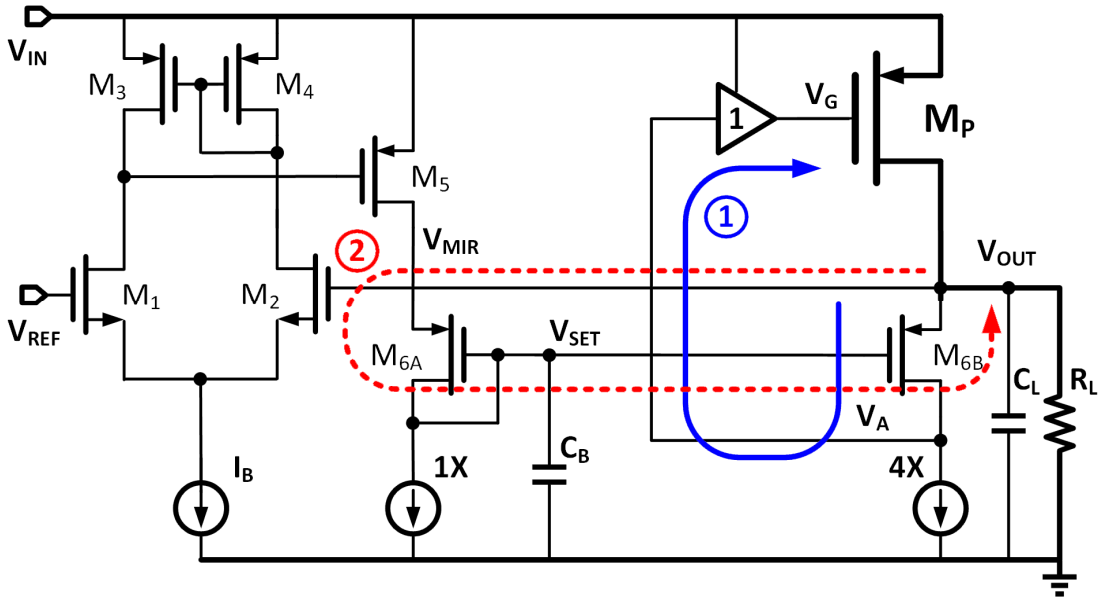
Integral (I) Control

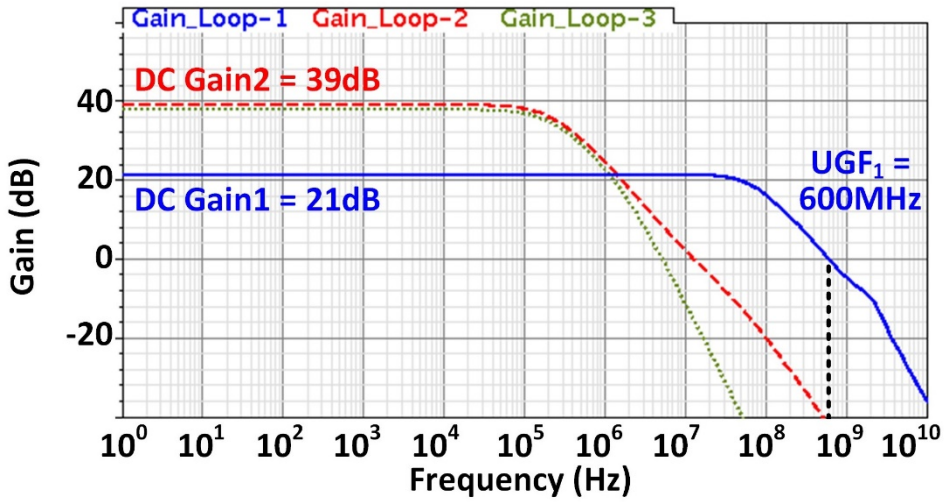




- Internal pole dominant.
- V_{OUT} error is integrated on an internal capacitor.
- Miller compensation lowers the dominant pole freq. with smaller capacitor.
- **Low power, accurate, but slow.**

Example: LDO with Dual-Loop (PI) Control

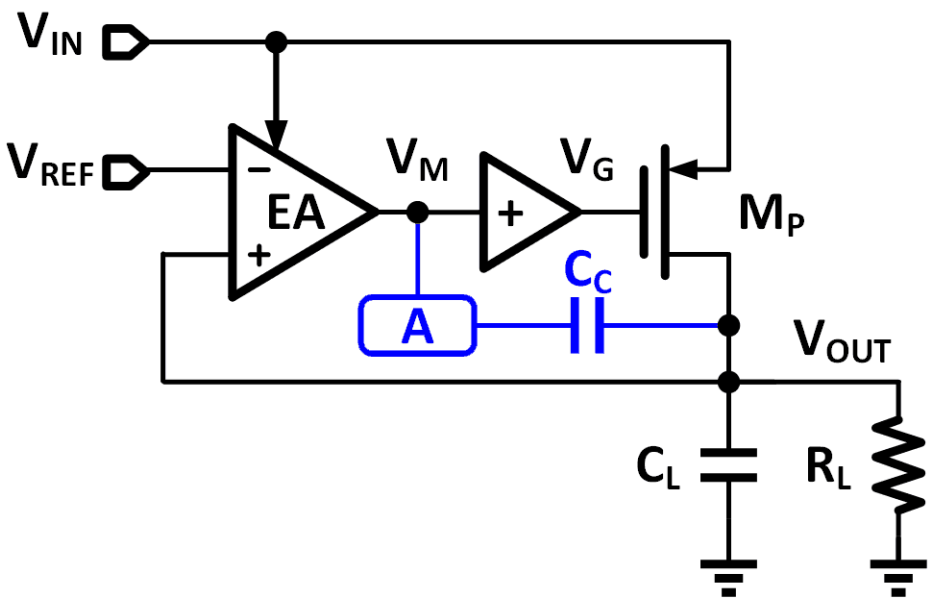


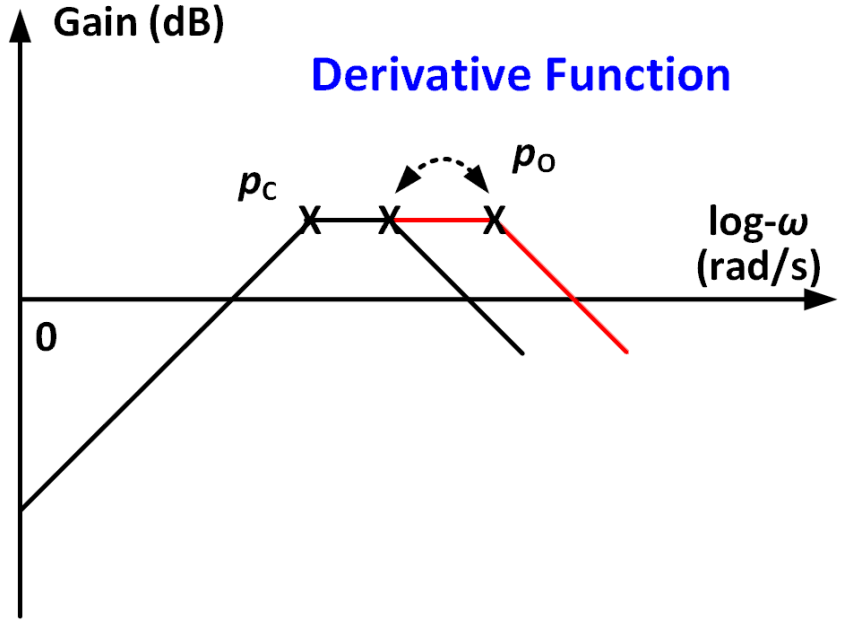


- Realize PI control with one fast (P) loop and one slow (I) loop.
- The flipped-voltage follower (FVF) forms the P path.
- C_B is an integrator.

[Y. Lu, ISSCC, 2014]

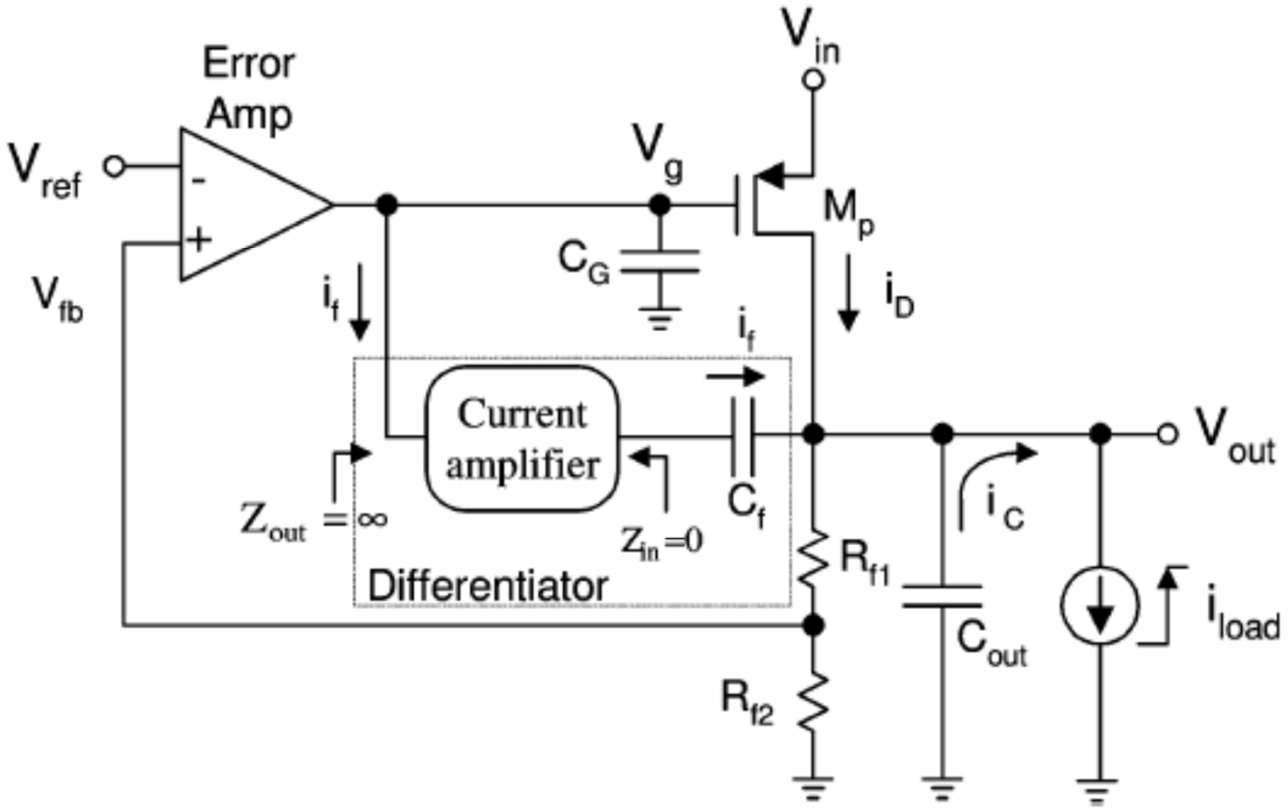
Derivative (D) Control

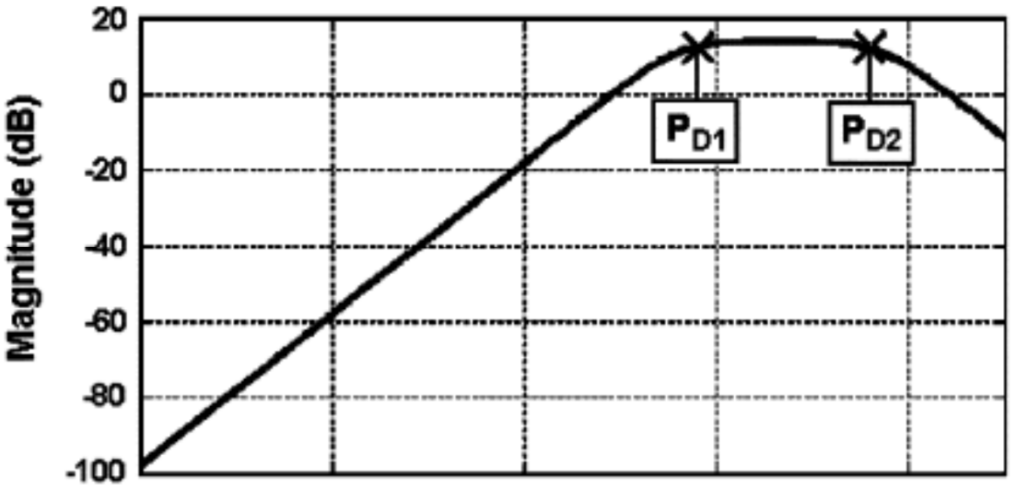




- A derivative path is a high-pass path, contributes a zero.
- The high frequency (HF) path is vulnerable to HF noise.
- Needs HF poles to attenuate the HF noise, then becomes a band-pass path.

Example: LDO with a Differentiator

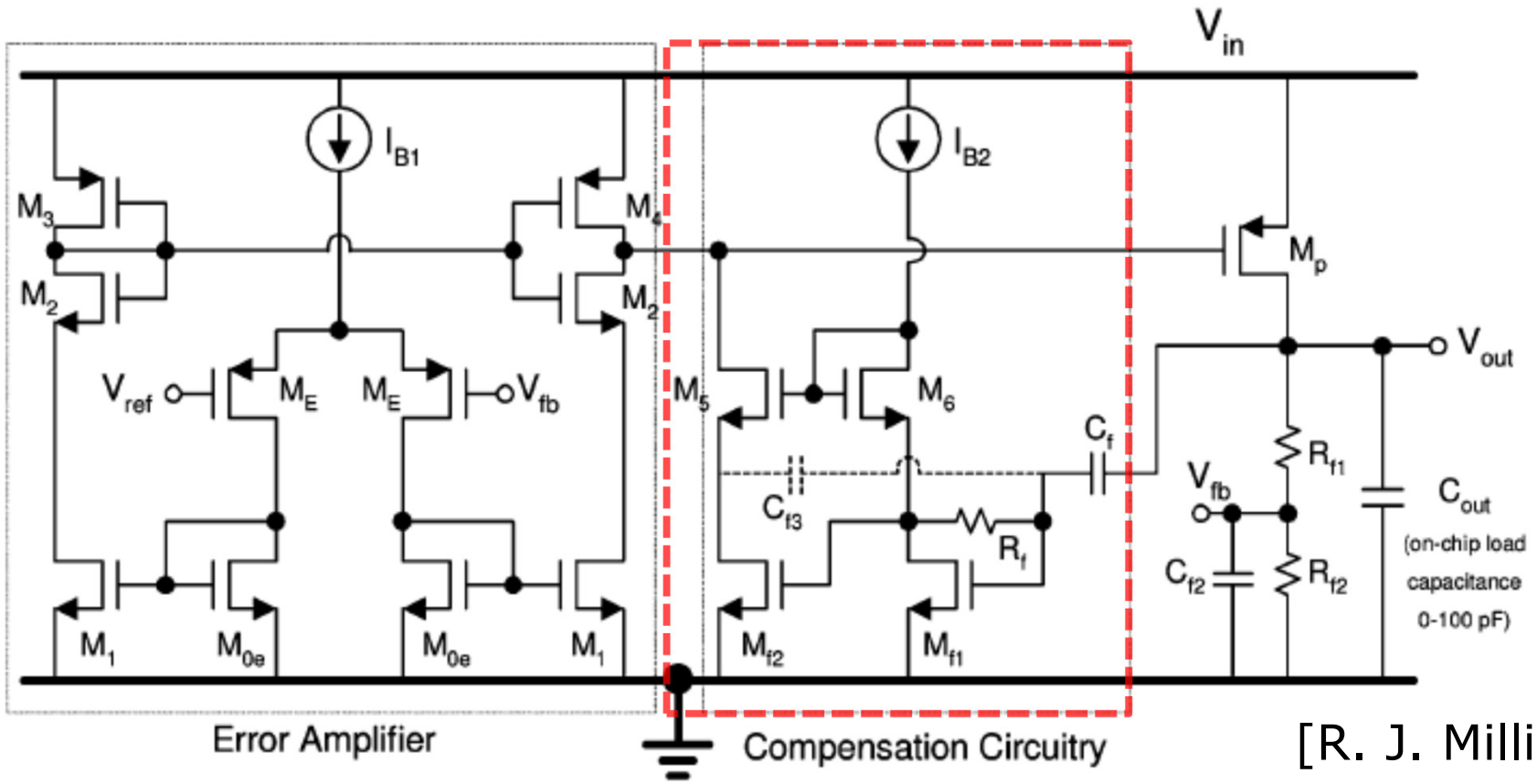




[R. J. Milliken, TCAS-I, 2007]

- C_f senses the slope of V_{OUT} changes.

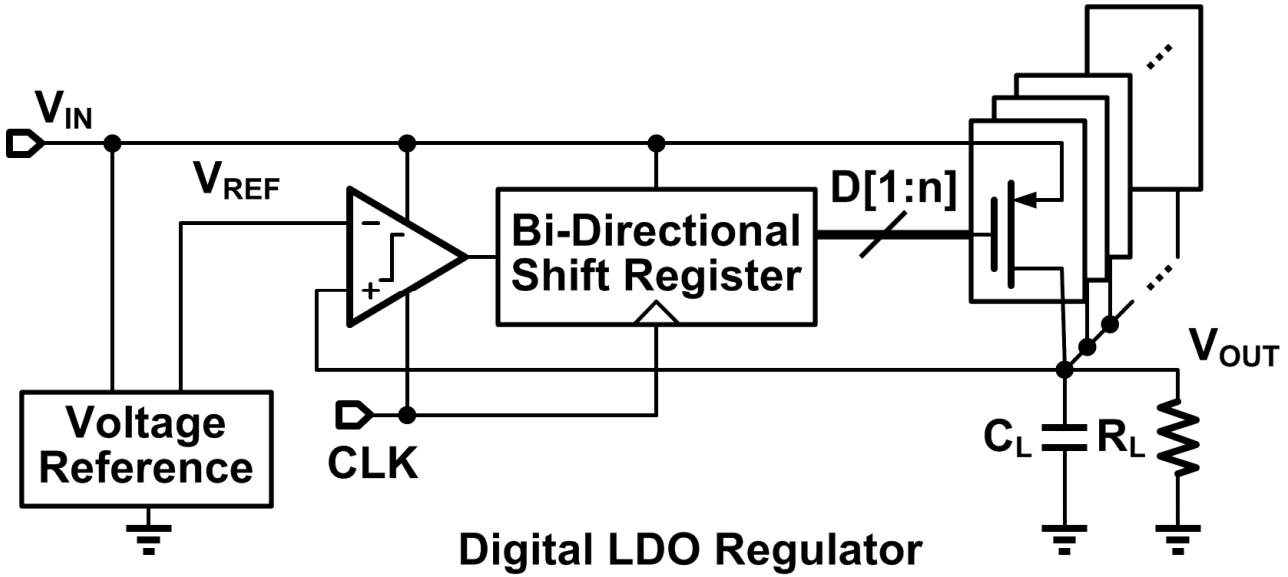
Transistor-Level Schematic of the LDO with Differentiator



[R. J. Milliken, TCAS-I, 2007]

- R_f transforms the C_f transient current into a voltage, helps to lower the differentiator's input impedance, pushing the added pole to higher frequency.

Digital Low Dropout Regulator (Digital LDO)

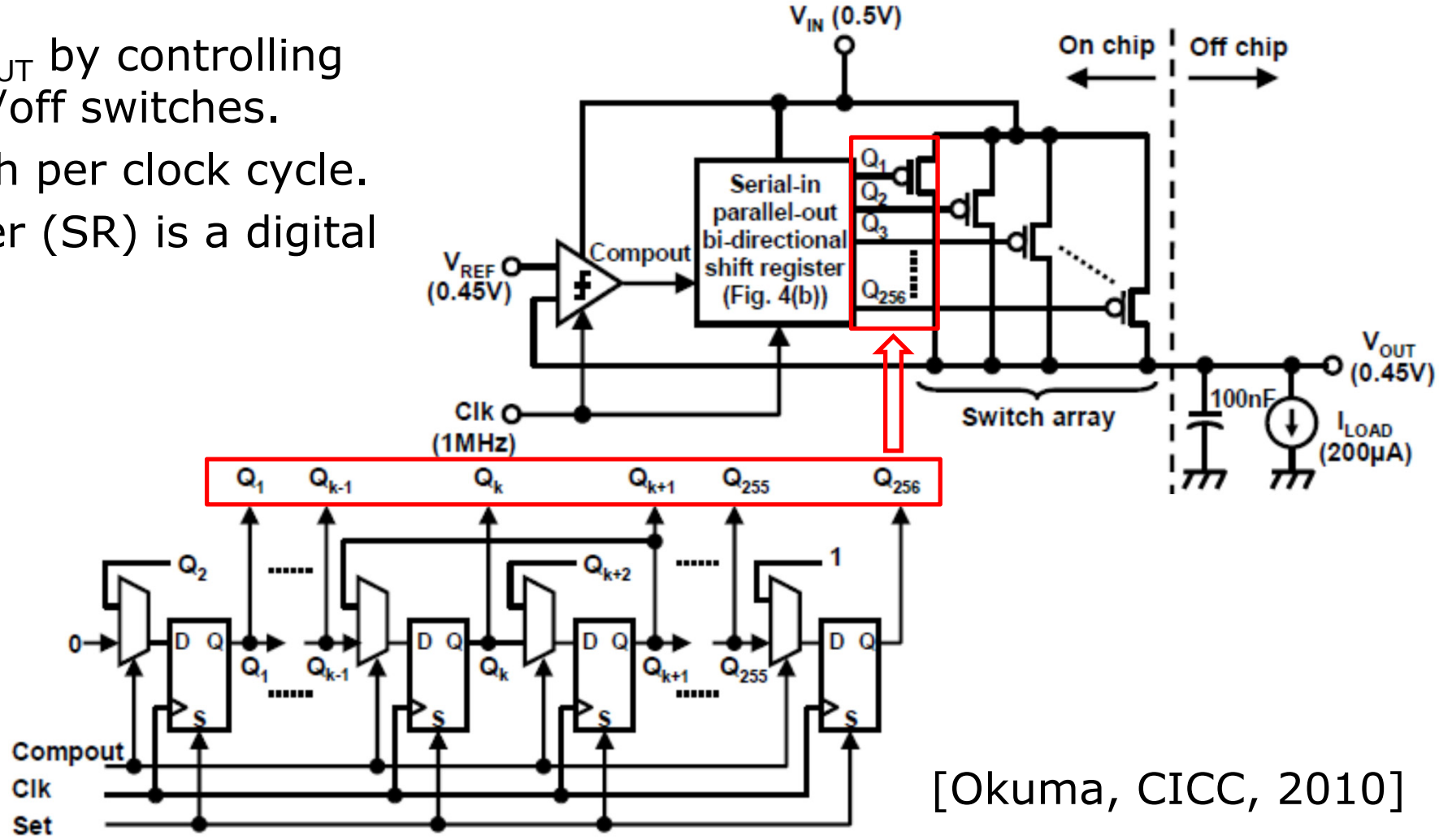


Digital LDO Regulator

- ✓ Low voltage operation (<0.6V)
- ✓ Benefit from process scaling
- ✓ Easy cooperation with digital loads
- x Not energy-efficient for the power-speed tradeoff
- x Limit cycle oscillation (LCO)

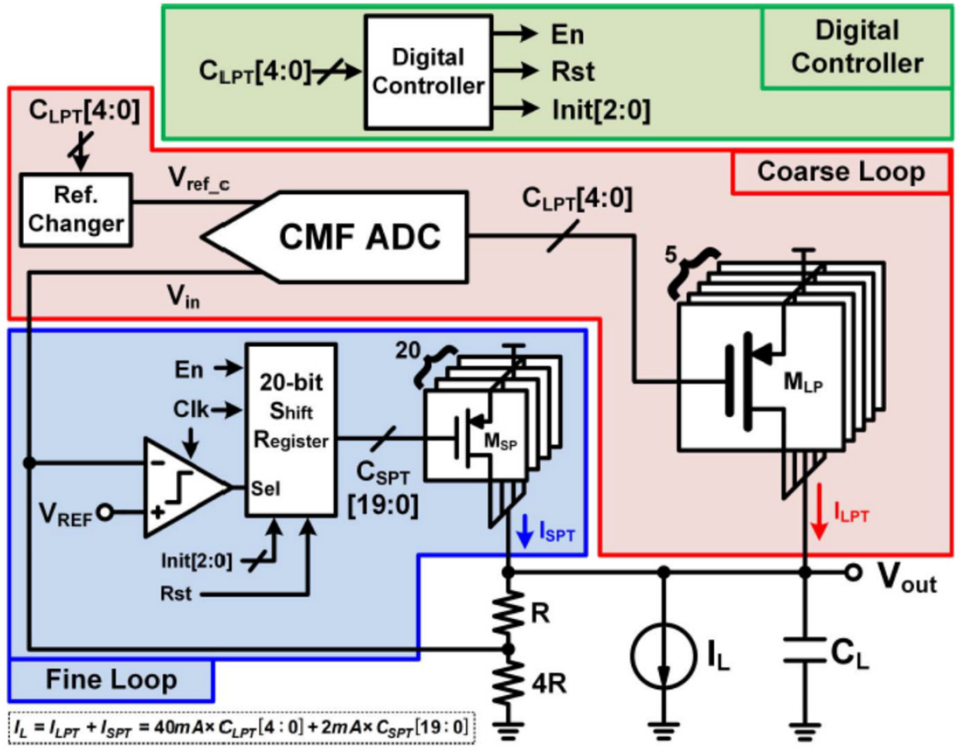
Shifter-Register-Based Digital LDO (I Control)

- Regulating the V_{OUT} by controlling the number of on/off switches.
- Change one switch per clock cycle.
- The shifter register (SR) is a digital integrator.



[Okuma, CICC, 2010]

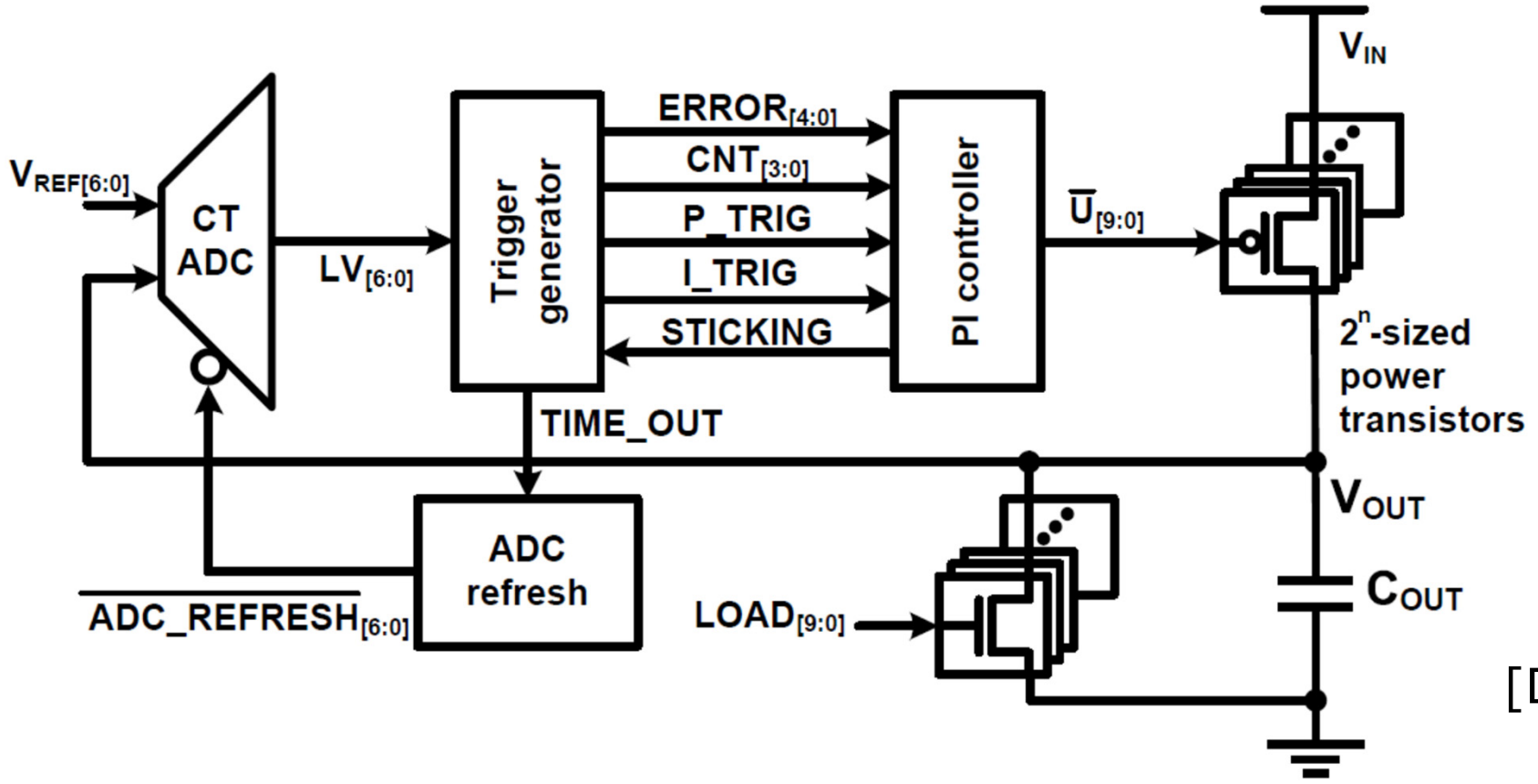
Example: DLDO with PI Control



[Y.-J. Lee, ISSCC, 2016]
[Y.-J. Lee, JSSC, 2017]

- Shift-register based loop for fine tuning (I control).
- Flash-ADC based loop for coarse tuning (P control).
- Reference changer compensates the V_{OUT} error that comes from the P control.

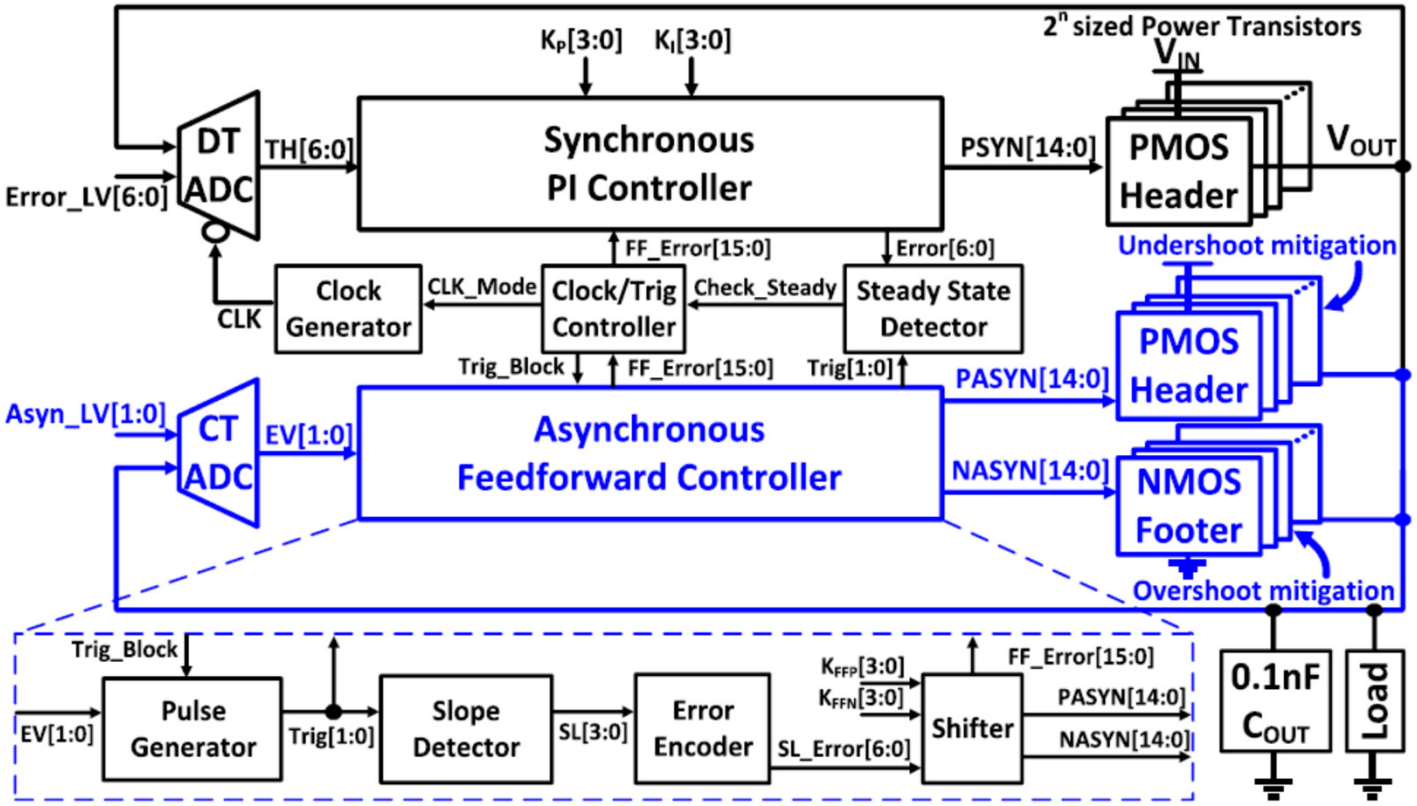
Example: DLDO with PI Control

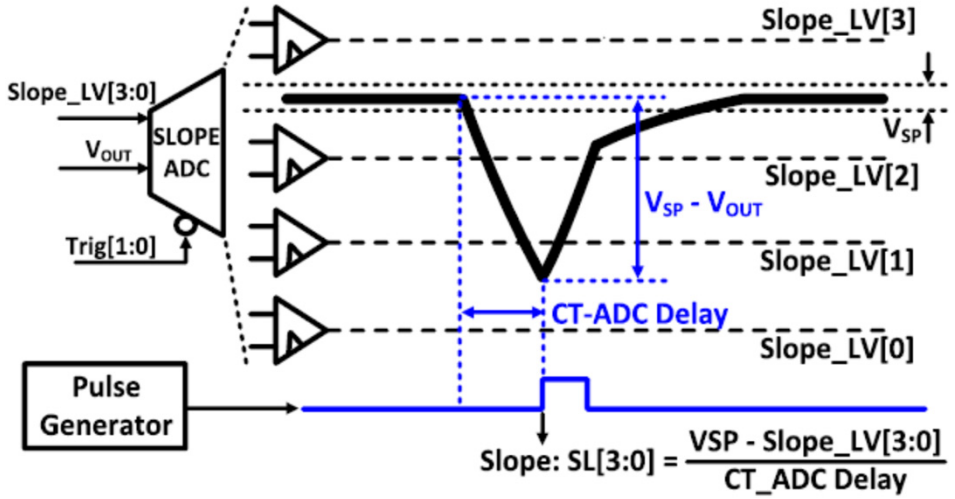


[D. Kim, ISSCC, 2016]
[D. Kim, JSSC, 2017]

- Continuous-time ADC: 7-bit thermometer-coded.

Example: DLDO with PID Control

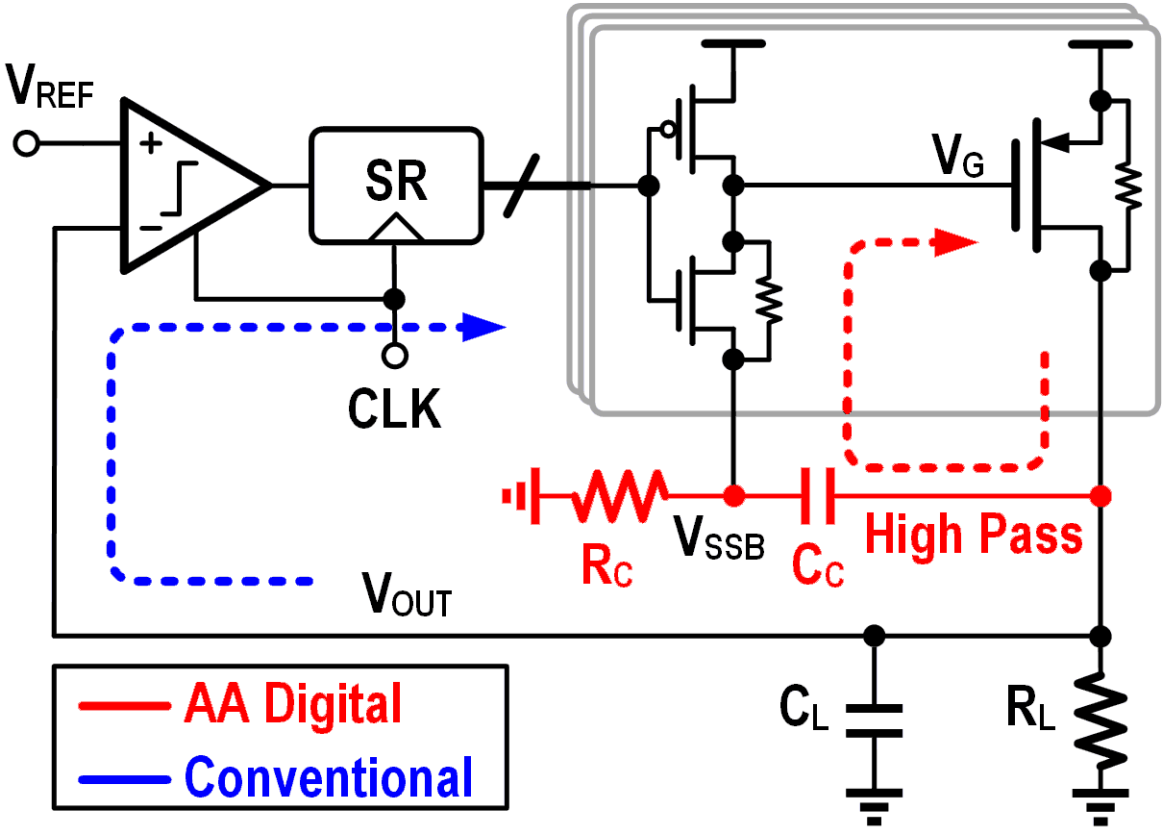


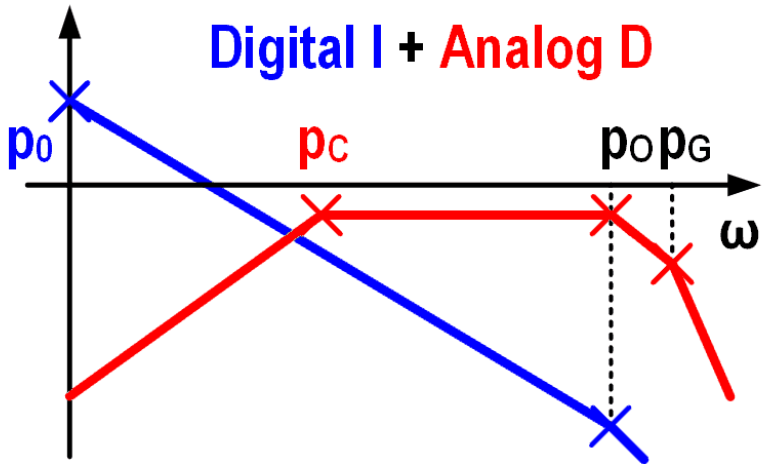


[S. J. Kim, SSC-L, 2018]

- Asynchronous slope detection (D).
- Synchronous PI control.

Control Loops: Analog, Digital, Hybrid

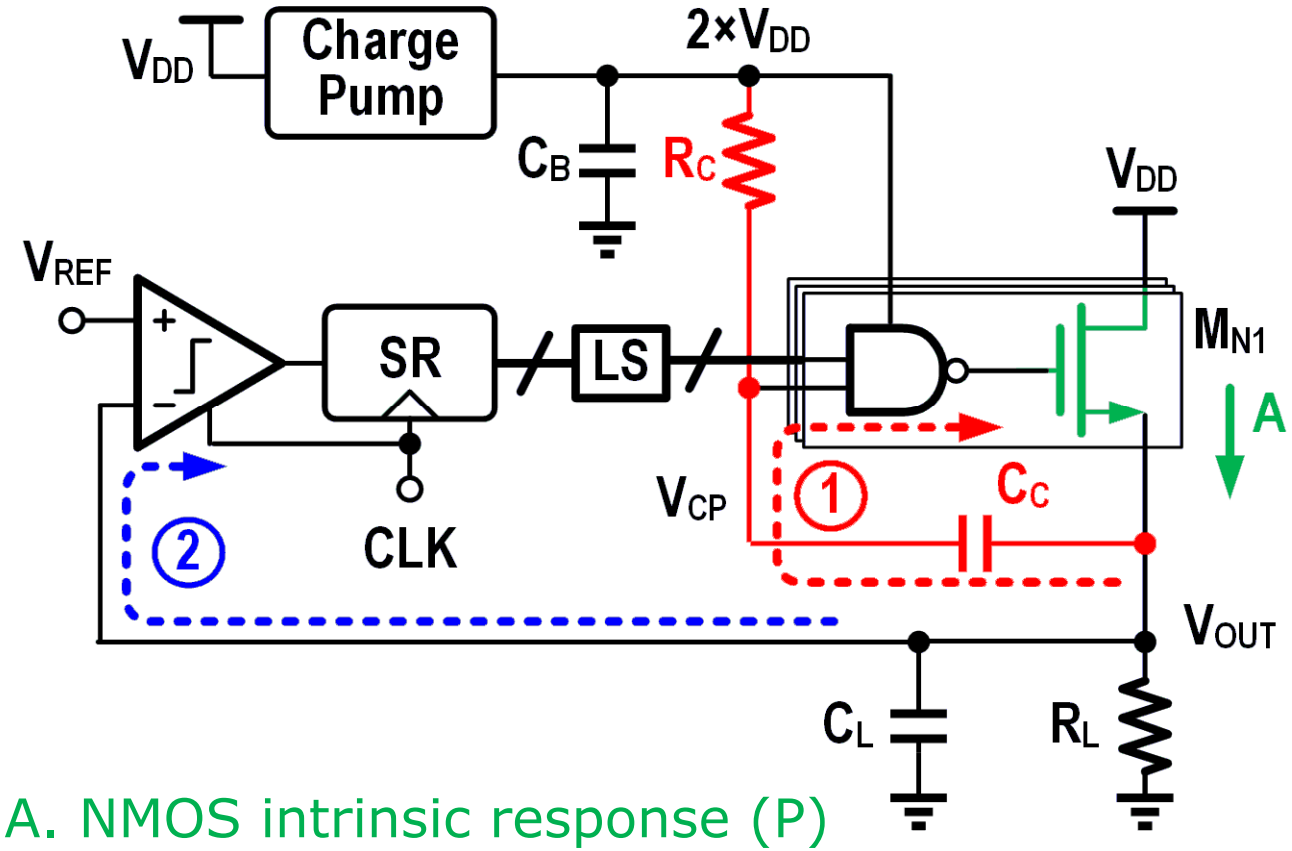


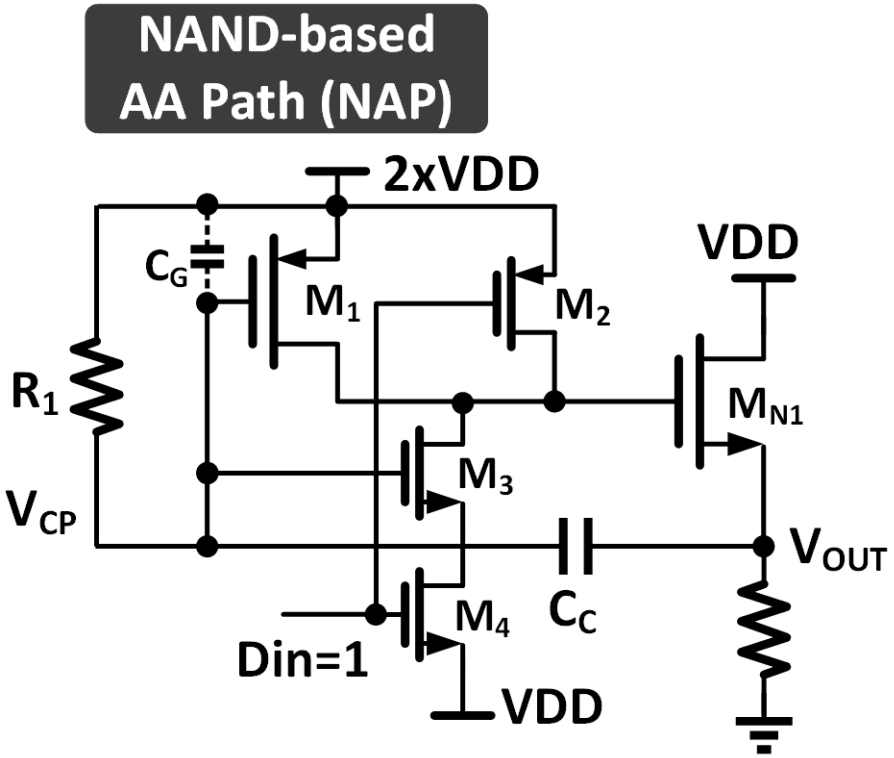


[M. Huang, ISSCC 2017]
[M. Huang, JSSC 2018]

- Using a high pass analog path to assist the slow digital loop.

Analog-Assisted (AA) NMOS Digital LDO

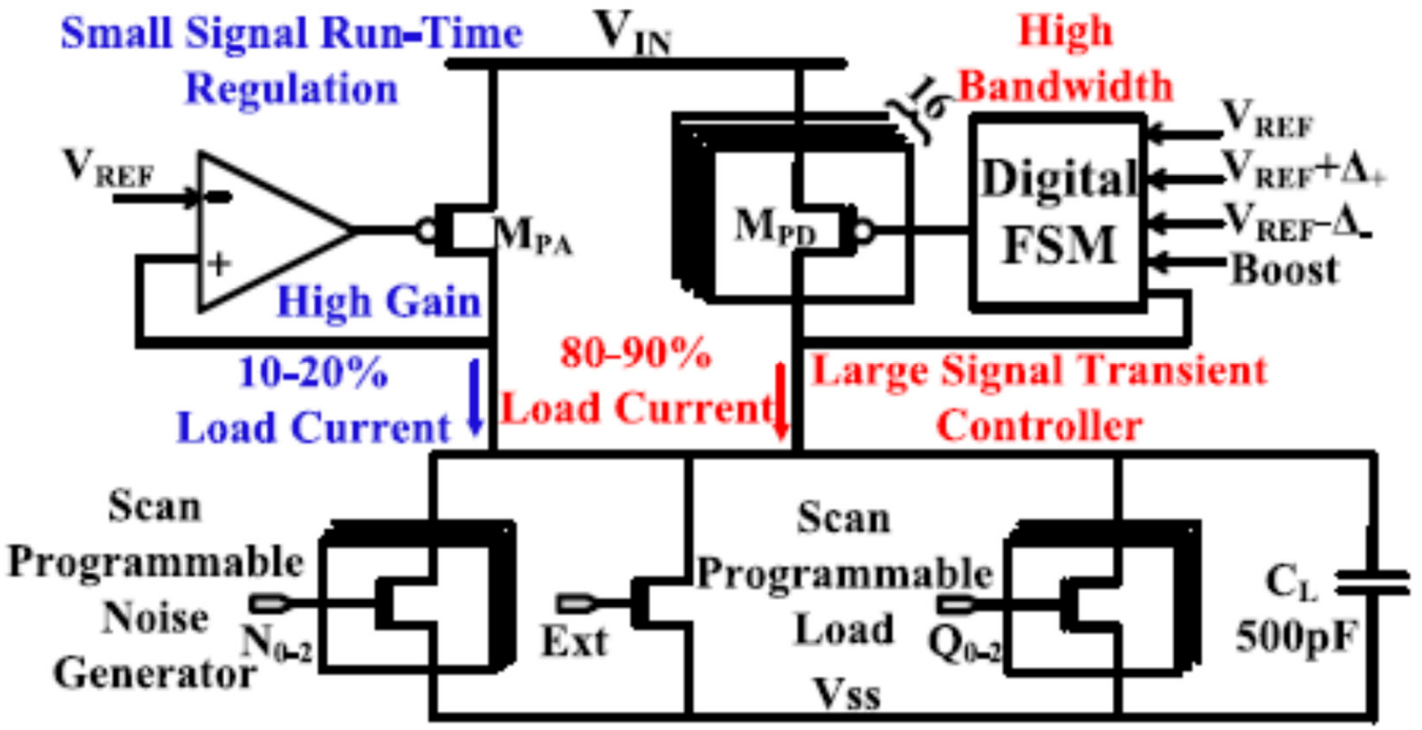




- A. NMOS intrinsic response (P)
- 1. NAND-based AA path (D)
- 2. Digital control loop (I)

[X. Ma, ISSCC 2018]

Example: Analog-Digital Hybrid LDO



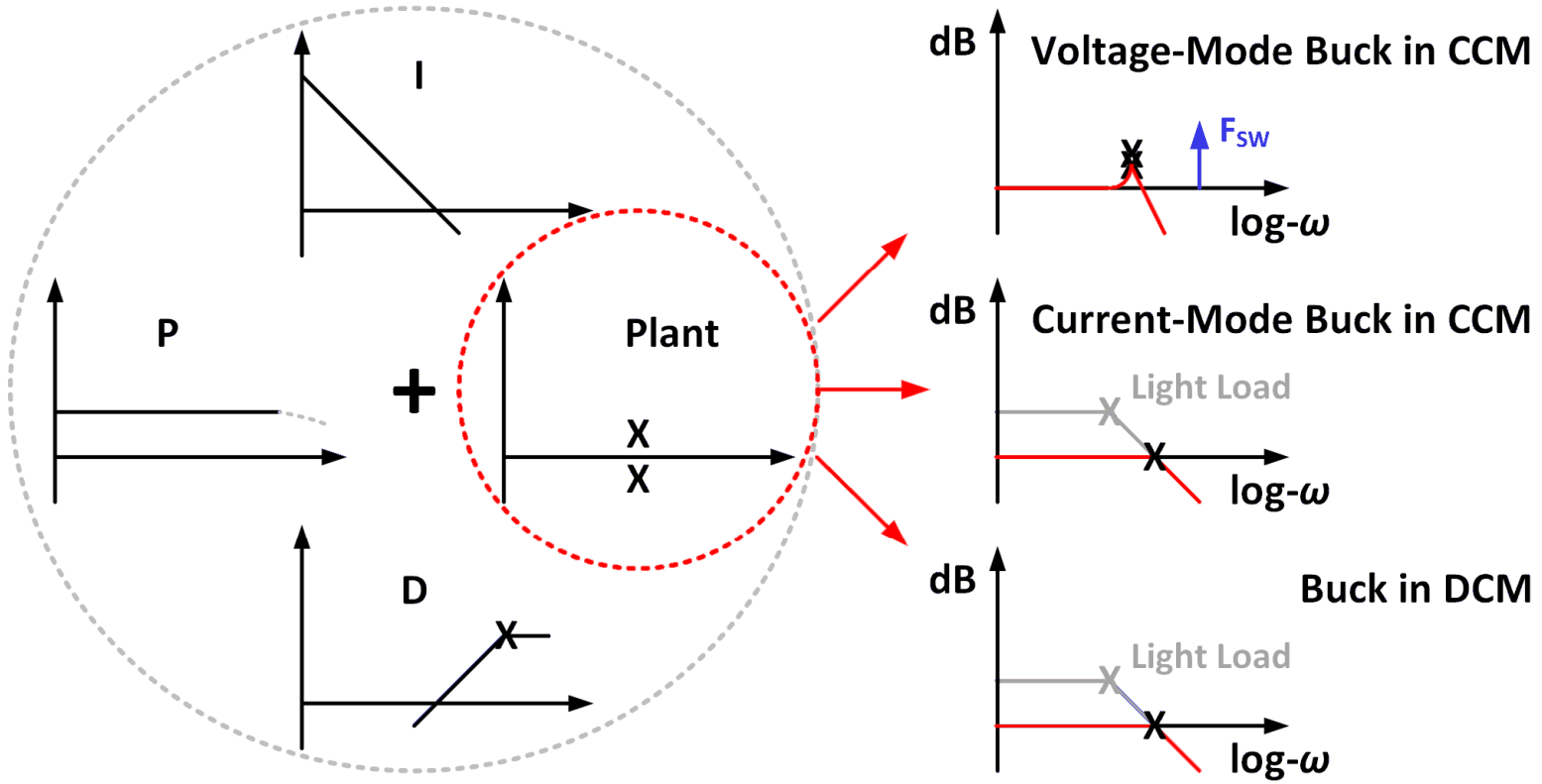
[S. B. Nasir, ESSCIRC, 2016]
[S. B. Nasir, JSSC, 2018]

- Small-signal analog.
- Large-signal digital.

Example Summary of LDO Control Techniques

Category	Publications	Techniques
Analog P	Ho, JSSC 2010	Small-gain stages
Analog PI	Lu, TCAS-I 2015	Dual-loop with fast FVF
Analog PID	Milliken, TCAS-I 2007	Differentiator
Digital I	Okuma, CICC 2010	Shift-register based
Digital PI	Lee, ISSCC 2016 Kim, ISSCC 2016	Flash ADC with reference changer Multi-bit ADC and digital PI
Digital PID	Kim, SSC-L 2018	Slope detector
Digital I + Analog P	Nasir JSSC 2018 Huang, CICC 2019	Small-signal analog Fast and adaptive analog
Digital I + Analog D	Huang, ISSCC 2017	Analog-assisted (AA) digital
Digital I + Analog PD	Ma, ISSCC 2018	NAND-based AA NMOS LDO

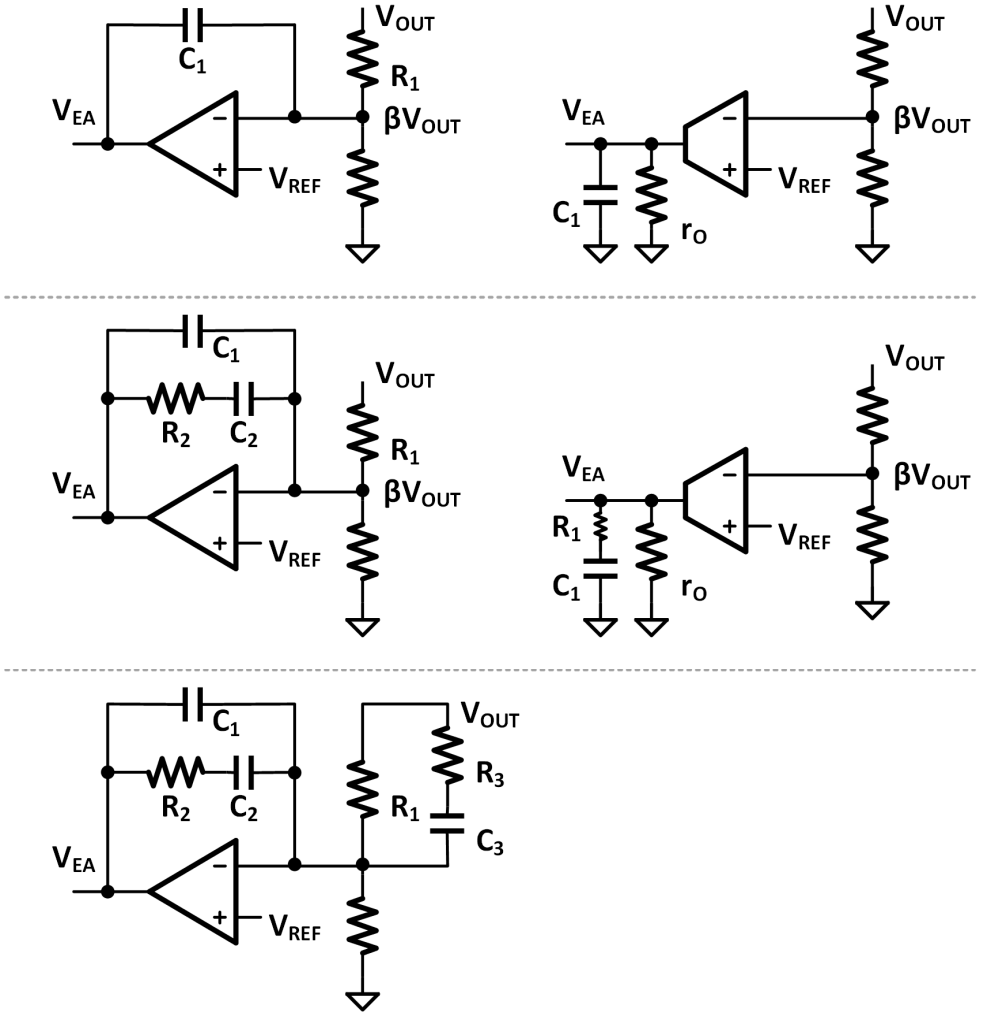
Bode Plots of PID Control for Buck Converter



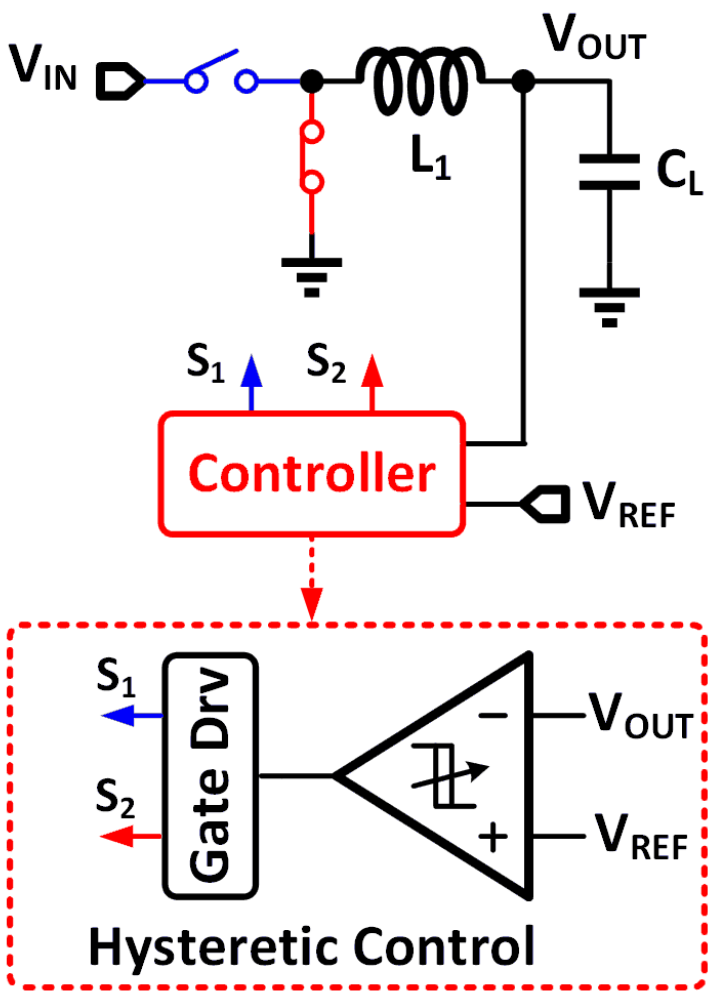
- The LC filter in continuous-conduction mode (CCM) has a pair of complex poles.
- Current-mode control uses the inductor current information, complex pole pair turns into two separated real poles, one related to R_L.
- Discontinuous-conduction mode (DCM) operation only has a small inductor, of which the dynamics occur at HF, above or just below F_{SW}.

Loop Compensation for Buck Converter

- Type-I: I Control
  - Simple, slow.
  - Need large compensation cap.
  - Unity-gain freq. (UGF) limited to ~10x < $F_{RES,LC}$.
- Type-II: PI Control
  - 1 zero compensates 1 pole.
  - Used for current mode or DCM.
  - Not for voltage mode CCM.
- Type-III: PID Control
  - 2 zeros compensate complex pole pair.
  - For voltage mode, extend the UGF > $F_{RES,LC}$.



Hysteretic Control (Bang-Bang Control)



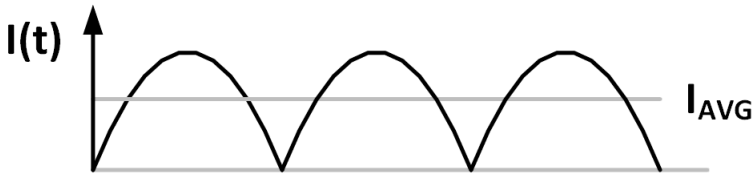
- Replace the compensator and PWM generator with simply a hysteresis comparator. React immediately when $V_{OUT} < V_{REF}-\Delta$, or $> V_{REF}+\Delta$.
- Pros:
  - Extremely simple, and extremely fast.
  - Low quiescent current.
- Cons:
  - F_{SW} varies with V_{IN} and I_{OUT}, EMI issue.
- Solutions:
  - Adaptive hysteresis window tuning.
  - Constant on-time control, $D=T_{ON}/T=V_{OUT}/V_{IN}$.

Outline

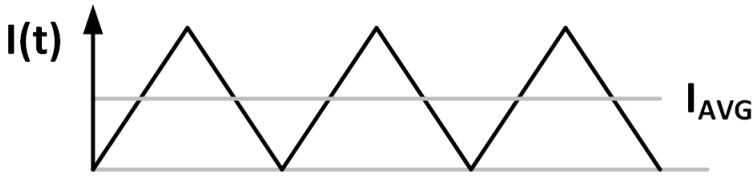
- Introduction
- Basic Power Stage Selections
  - Linear Low-Dropout (LDO) Regulator
  - Switched-Capacitor Converter
  - Switched-Inductor Converter
- Control Loop Designs
  - PID Control
  - Hysteretic Control
- Advanced Topologies and Techniques
  - Resonant Switched-Capacitor Operation
  - Multiple Interleaving Phase
  - Switched-Capacitor-Inductor Hybrid Topologies
  - Distributed Integrated Voltage Regulators
- Summary

Root-Mean-Square (RMS) Current

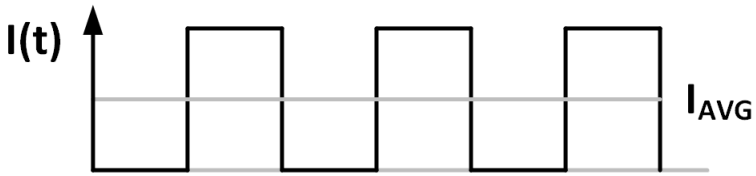
- Sinusoidal current
  - $I_{RMS,S} = I_{AVG} \times 1.11$



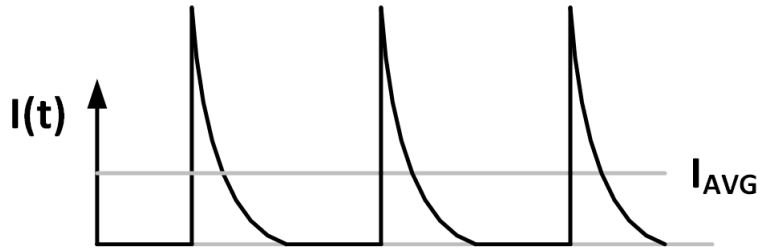
- Triangular current
  - $I_{RMS,T} = I_{AVG} \times 1.155$



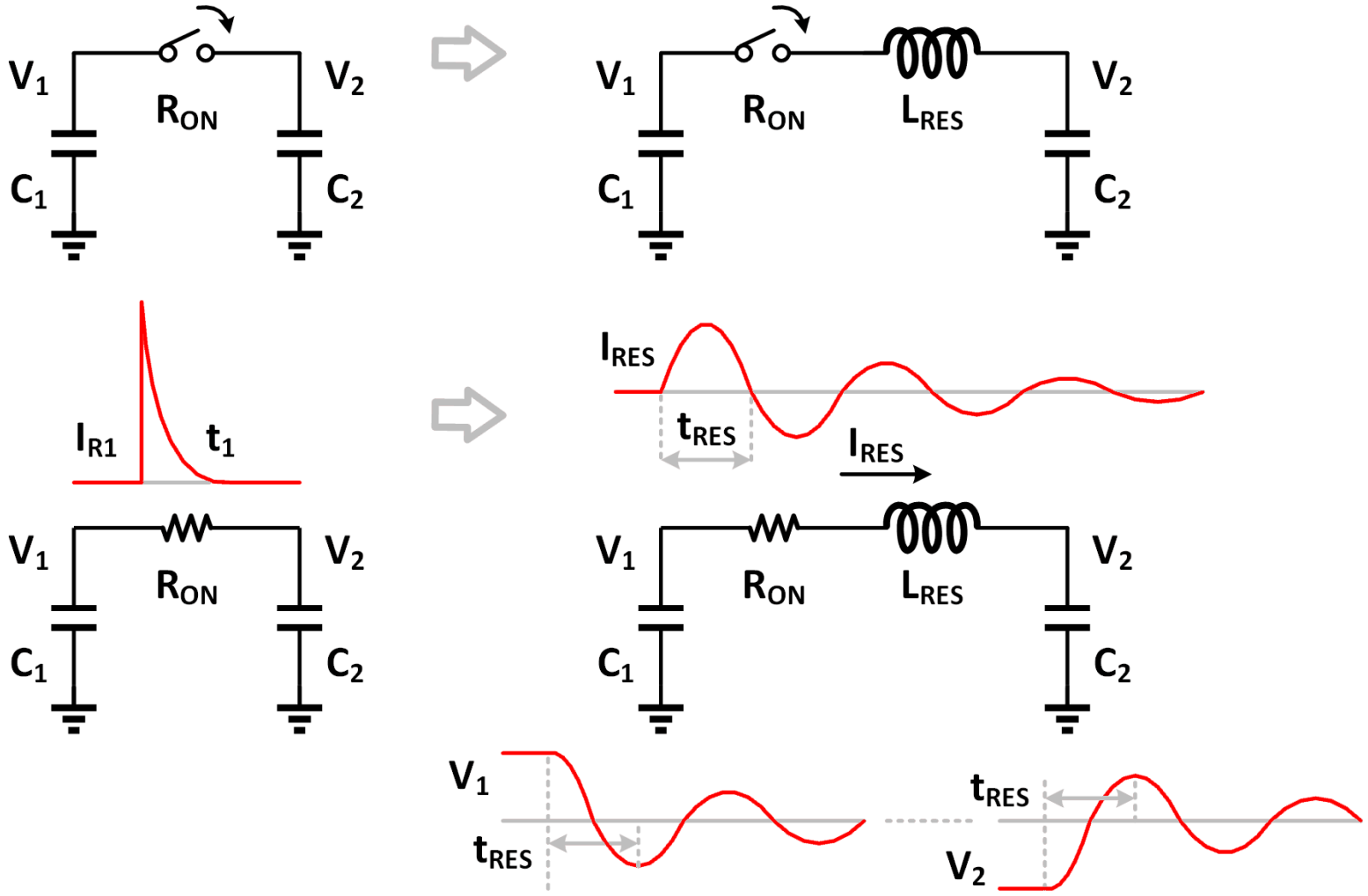
- Duty-cycled (D) current
  - $I_{RMS,D} = I_{AVG} / D^{1/2}$



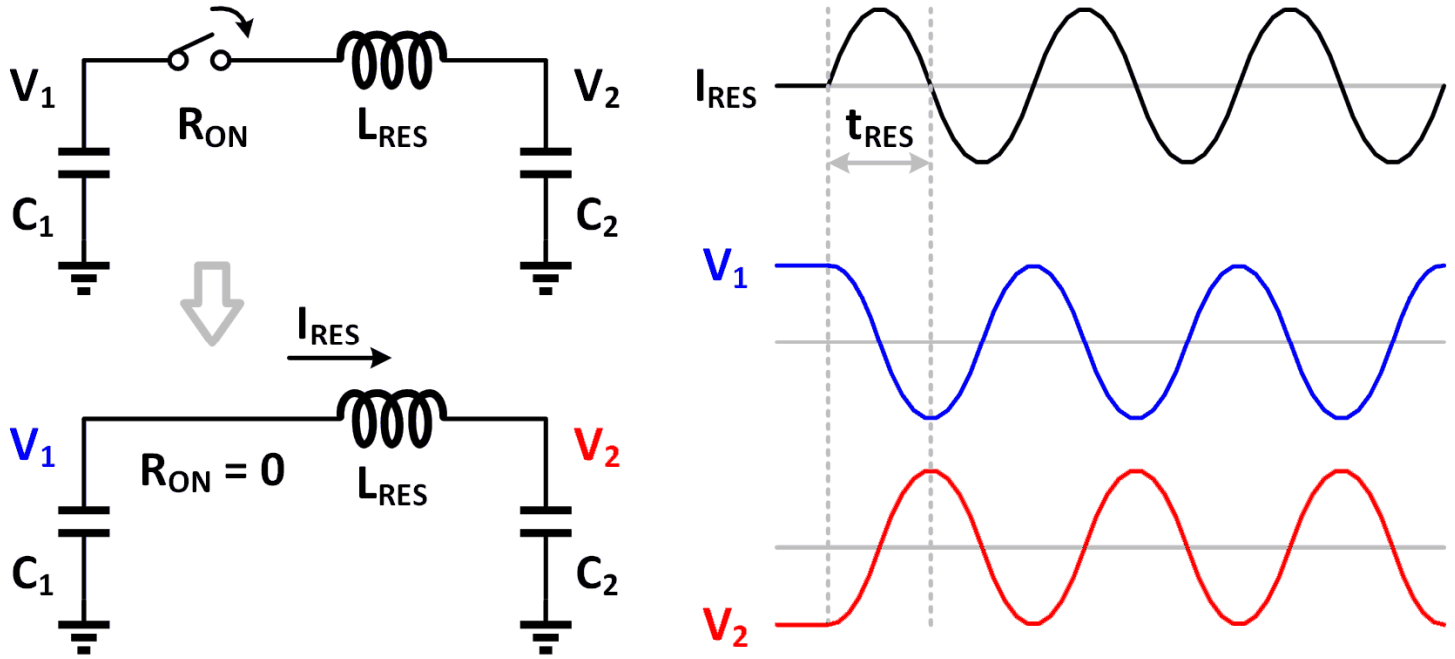
- Conduction loss = $I_{RMS}^2 R$
  - $1.11^2 = 1.232$ (Sinusoidal)
  - $1.155^2 = 1.334$ (Triangular)
  - $1.414^2 = 2$ (Pulse D=0.5)



Charge Redistribution with a Resonant Inductor

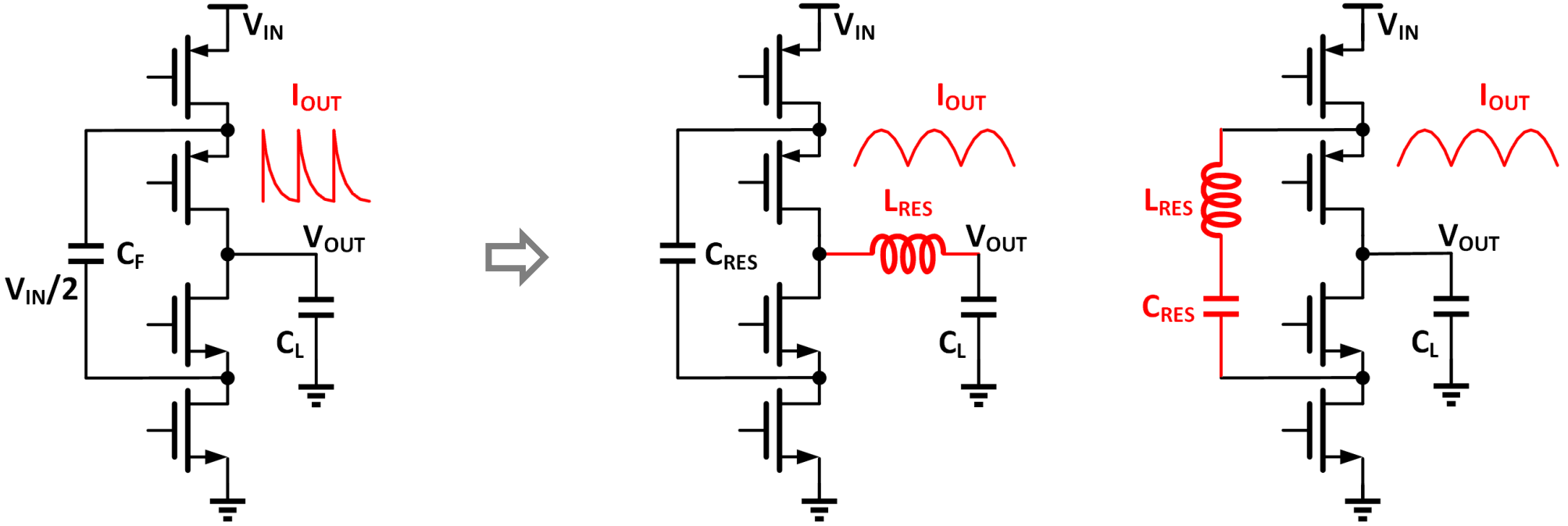


Charge Redistribution with a Resonant Inductor



- No hard charging and no loss in the ideal resonant case.
- Soft charging.

Resonant SC (ReSC) Converter

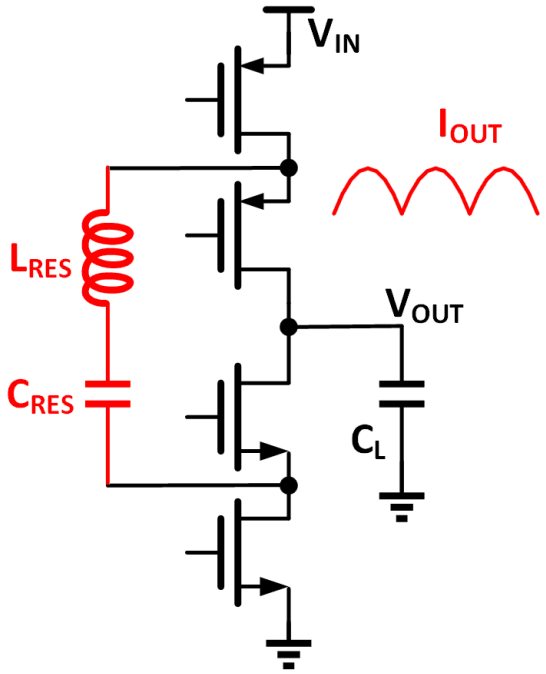


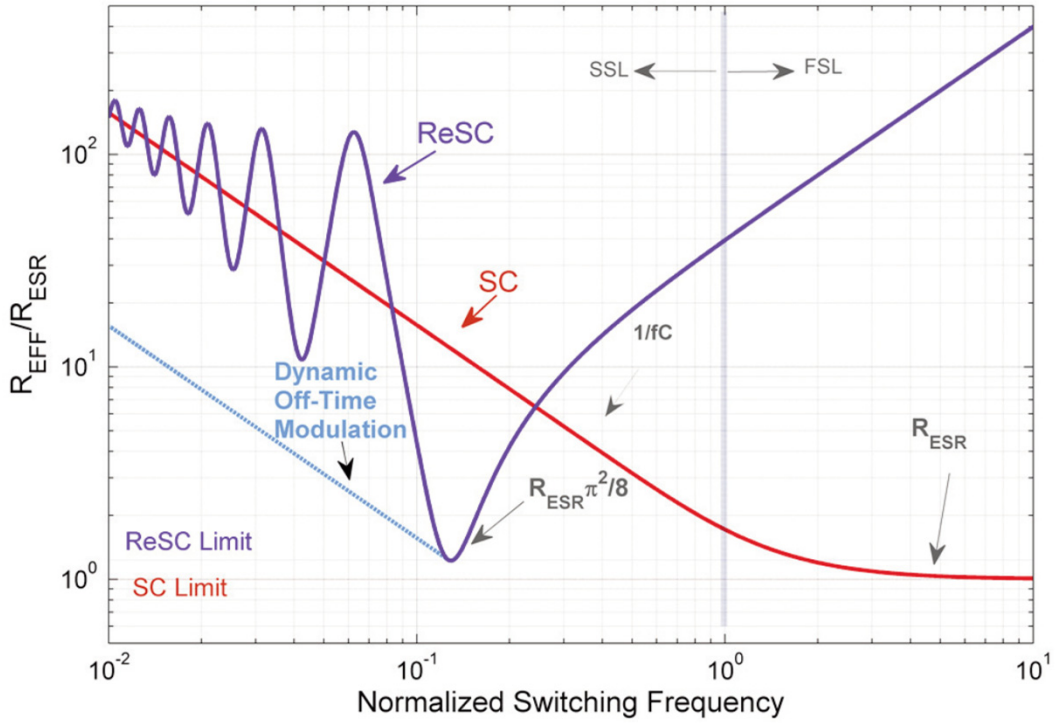
- 2:1 SC Converter
- Hard charging

- 2:1 Resonant SC Converters
- Soft charging

Output Impedance of a Resonant SC Converter

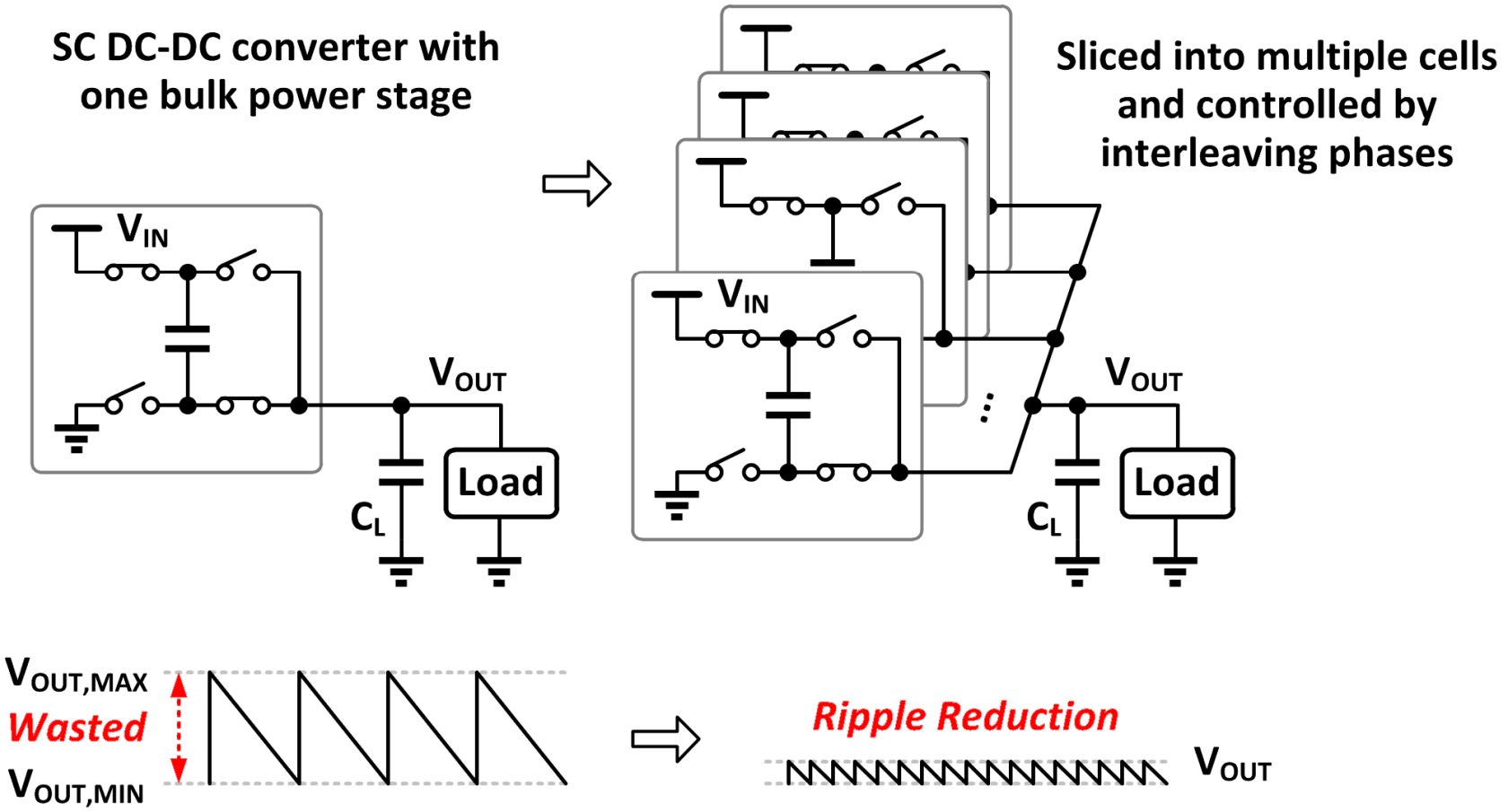
[K. Kesarwani, ISSCC, 2014]





- ReSC converter achieves the same R_{OUT} as SC converter at much lower F_{SW}.
- Resonant operation allows C_{RES} to have much larger ΔV, compared to C_F in SC.
- But, the maximum output capability is limited by L_{RES}.

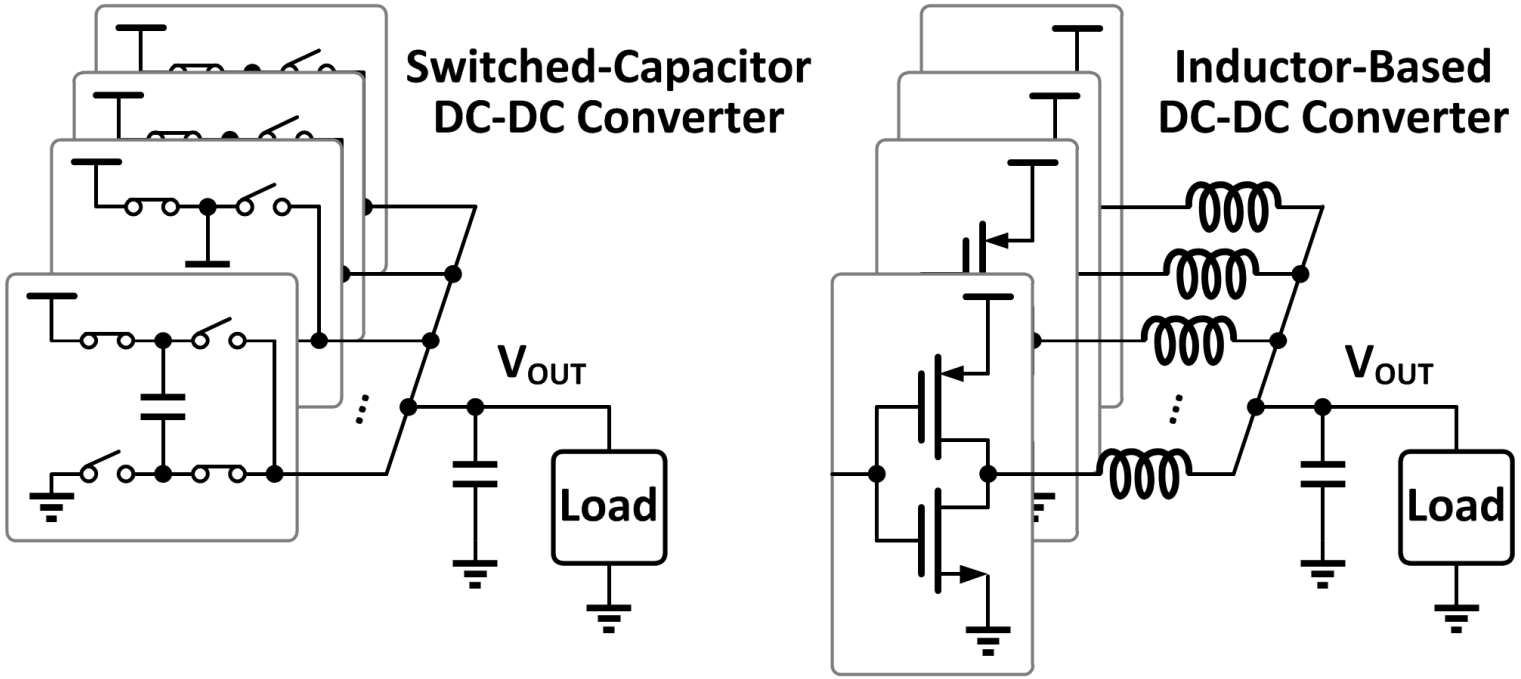
Ripple Effect



- Any voltage higher than $V_{OUT,MIN}$ is wasted.

Multiphase-Interleaving DC-DC Converters

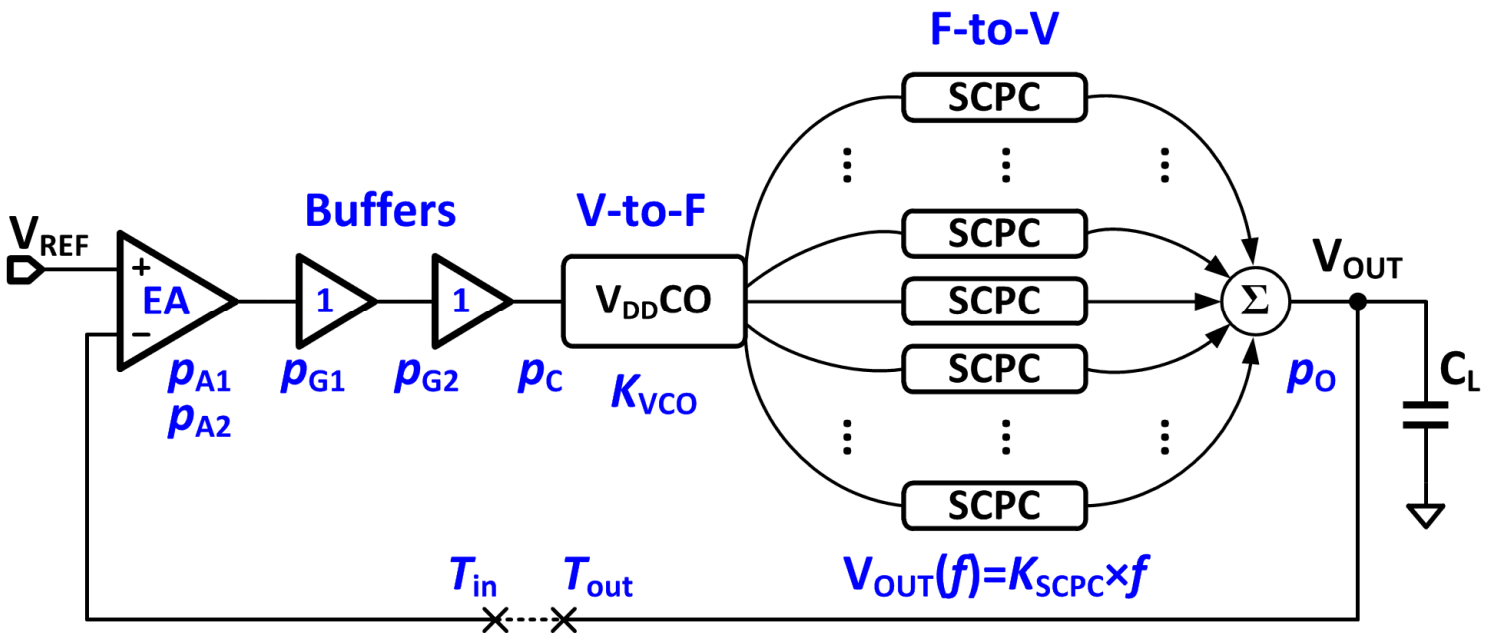
- Reduce output voltage and input current ripples.



- ✓ Fully-on-chip, multi-phase
- x Efficiency (like linear regulator)
- ✓ First-order power stage (Potential for fast control loop)

- x One *L* for each phase
- – Efficiency (ideally 100%, but need high *Q*)
- – *LC* second-order filter (Complex compensator)

Extending the Loop Bandwidth Beyond F_{SW}

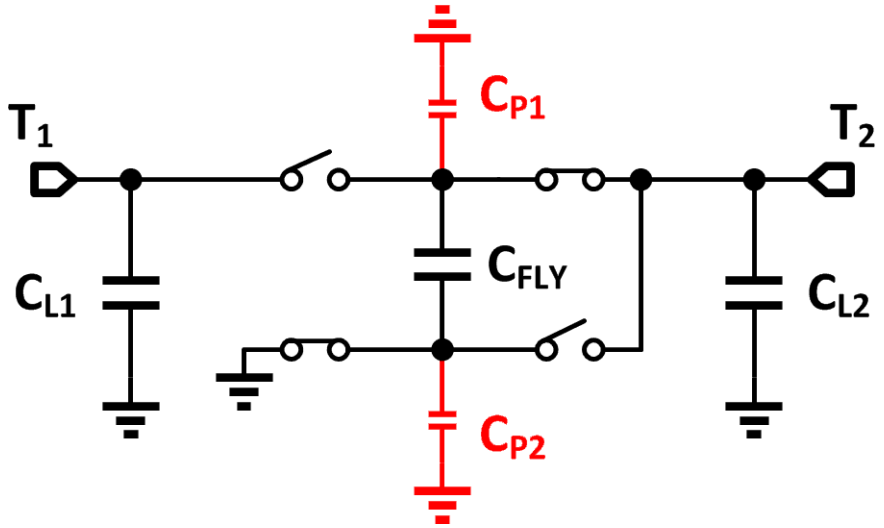


- The control loop bandwidth can be extended beyond FSW with multi-interleaving phase operation.

[Y. Lu, ISSCC, 2015]
[Y. Lu, JSSC, 2017]

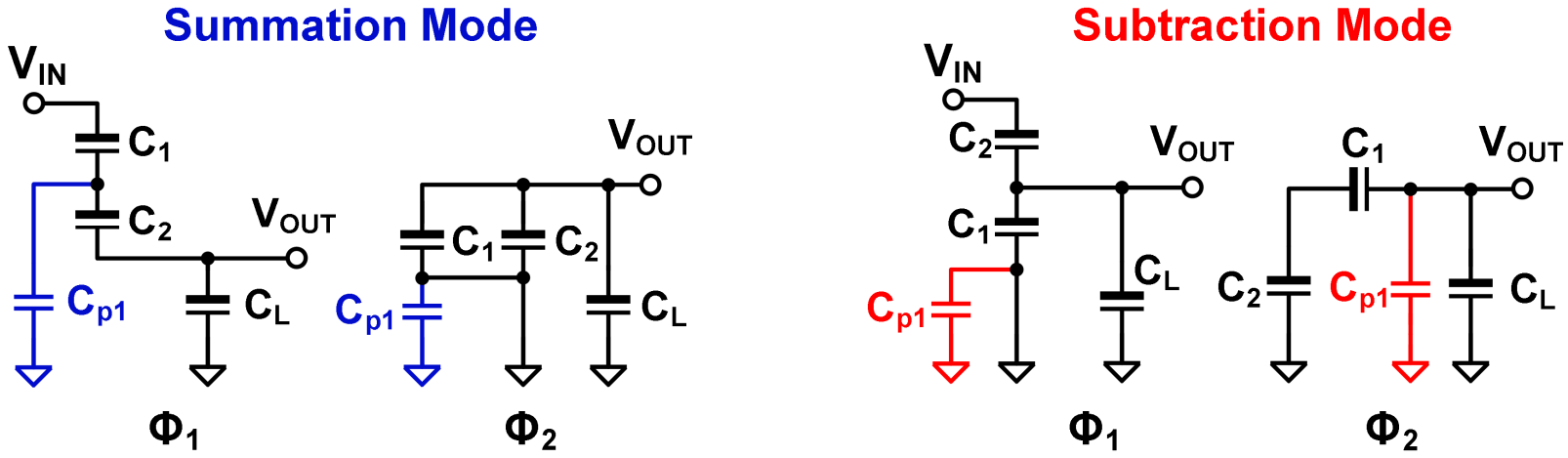
*SCPC: Switched-Capacitor Power Converter

Non-Ideal Effects of the Fully-Integrated SC



- Parasitic loss
  - Parasitic capacitor of the on-chip capacitors is about 5% of the main capacitor.
  - High density capacitor helps.
  - Topology dependent.

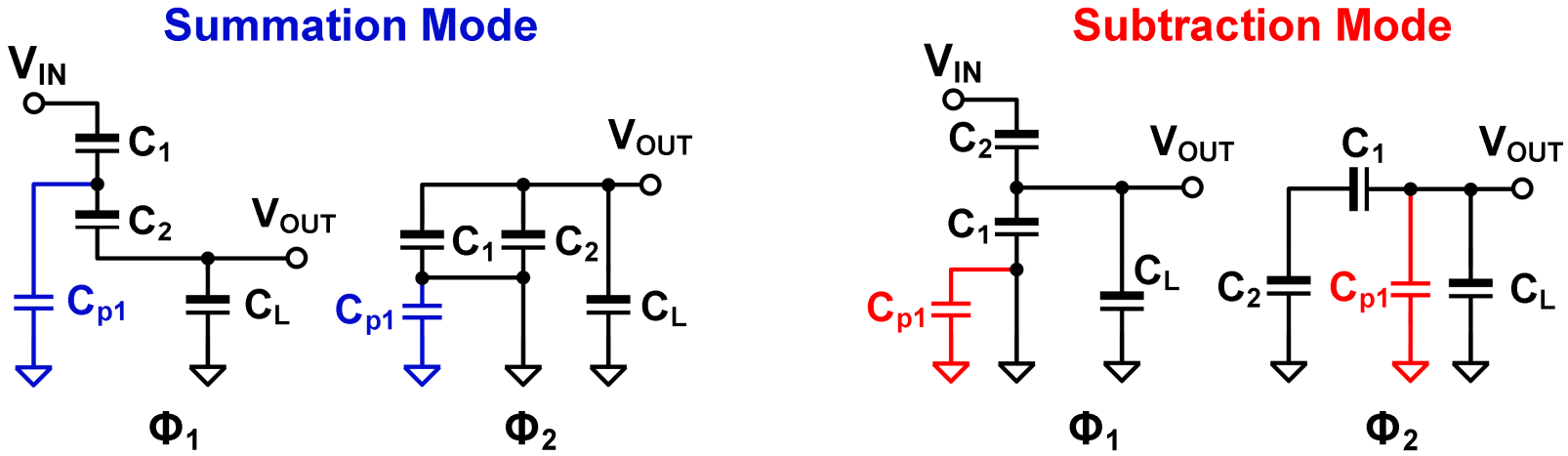
Parasitic Insensitive Topology



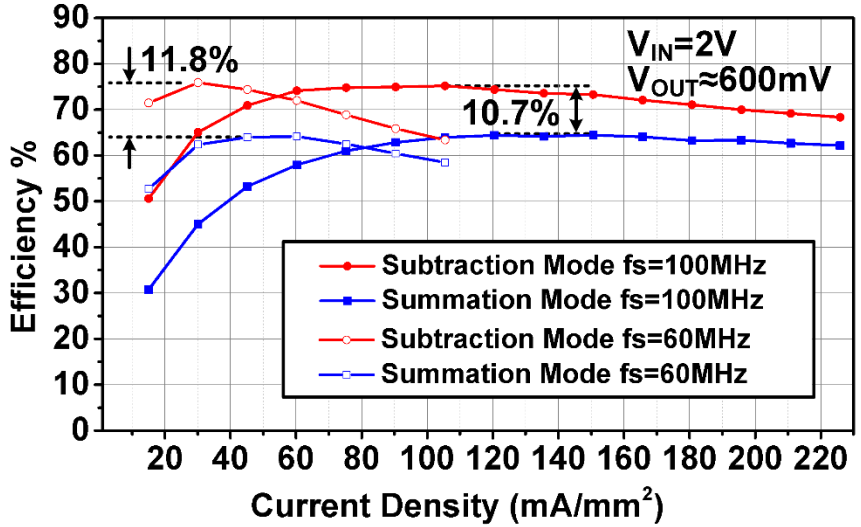
[J. Jiang, ISSCC, 2015]

CAP	Sum Φ_1	Sum Φ_2	Voltage Swing	Sub Φ_1	Sub Φ_2	Voltage Swing
$C_{p1(+)}$	V_{IN}	$1/3V_{IN}$	**$2/3V_{IN}$**	$1/3V_{IN}$	$2/3V_{IN}$	**$1/3V_{IN}$**
$C_{p1(-)}$	$2/3V_{IN}$	GND	**$2/3V_{IN}$**	GND	$1/3V_{IN}$	**$1/3V_{IN}$**
$C_{p2(+)}$	$2/3V_{IN}$	$1/3V_{IN}$	$1/3V_{IN}$	V_{IN}	$2/3V_{IN}$	$1/3V_{IN}$
$C_{p2(-)}$	$1/3V_{IN}$	GND	$1/3V_{IN}$	$1/3V_{IN}$	GND	$1/3V_{IN}$

Parasitic Insensitive Topology

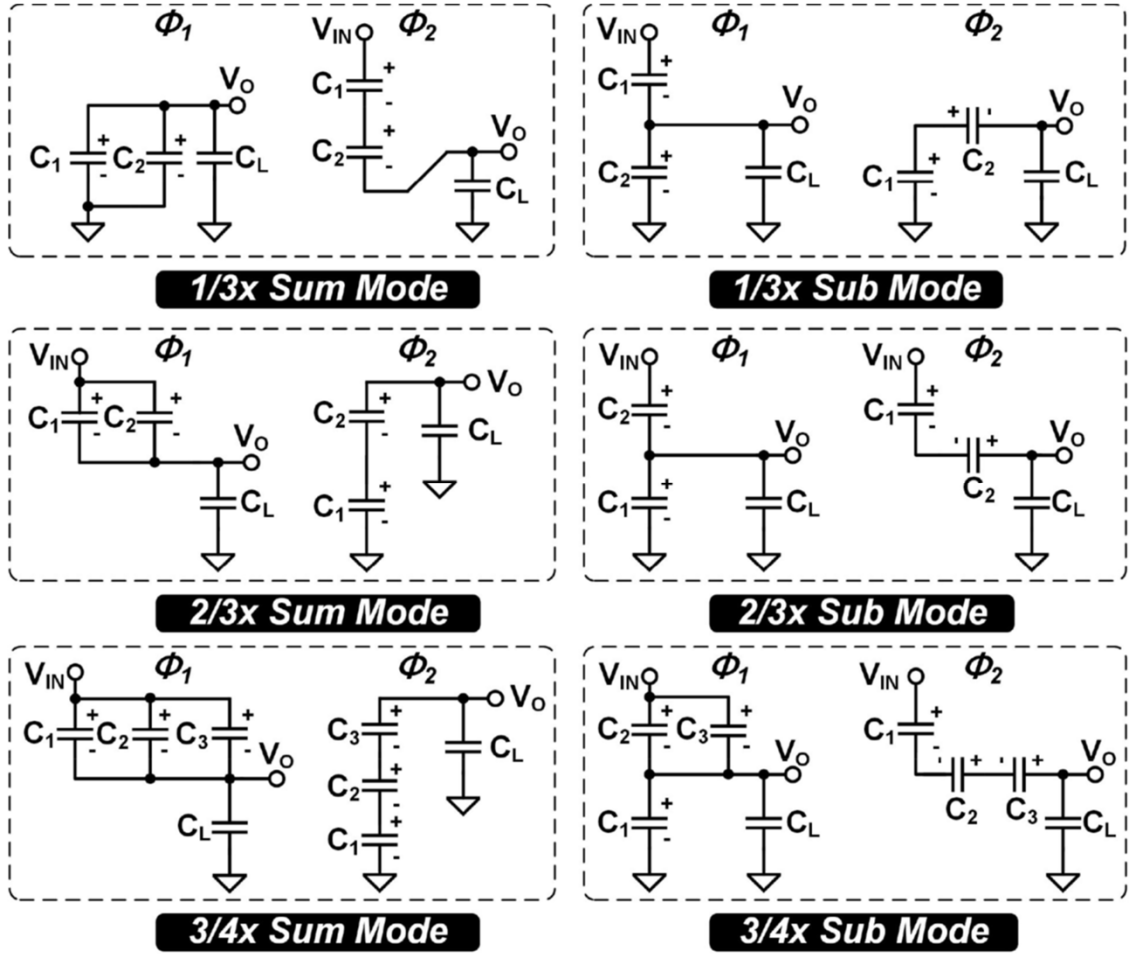


[J. Jiang, ISSCC, 2015]



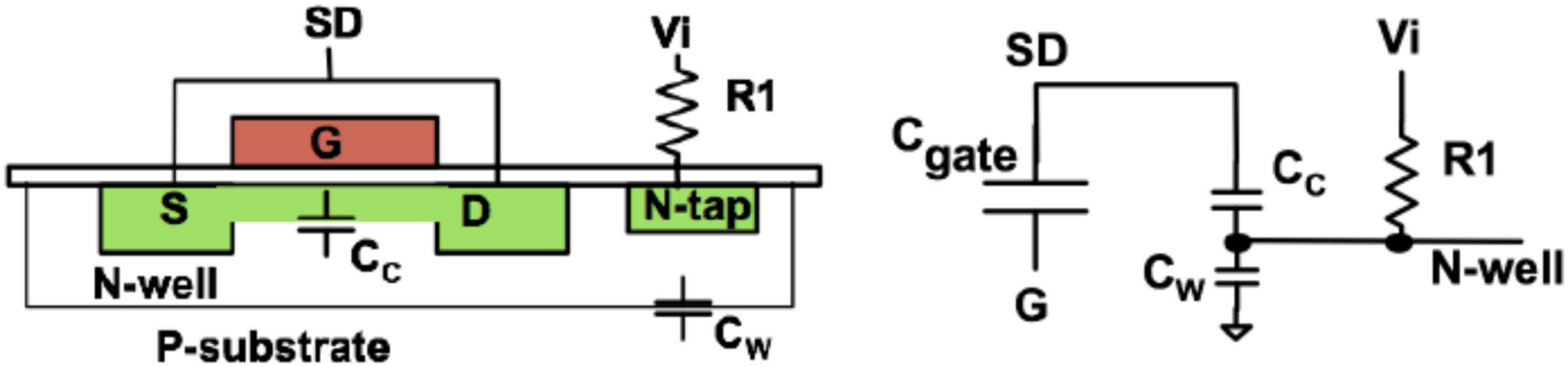
Subtraction-Mode SC

- Modified series-parallel topology.
- Subtraction-mode SC converters with parasitic loss reduction.
- Different capacitor voltages on each C_{FLY}.



[J. Jiang, TPEL, 2020]

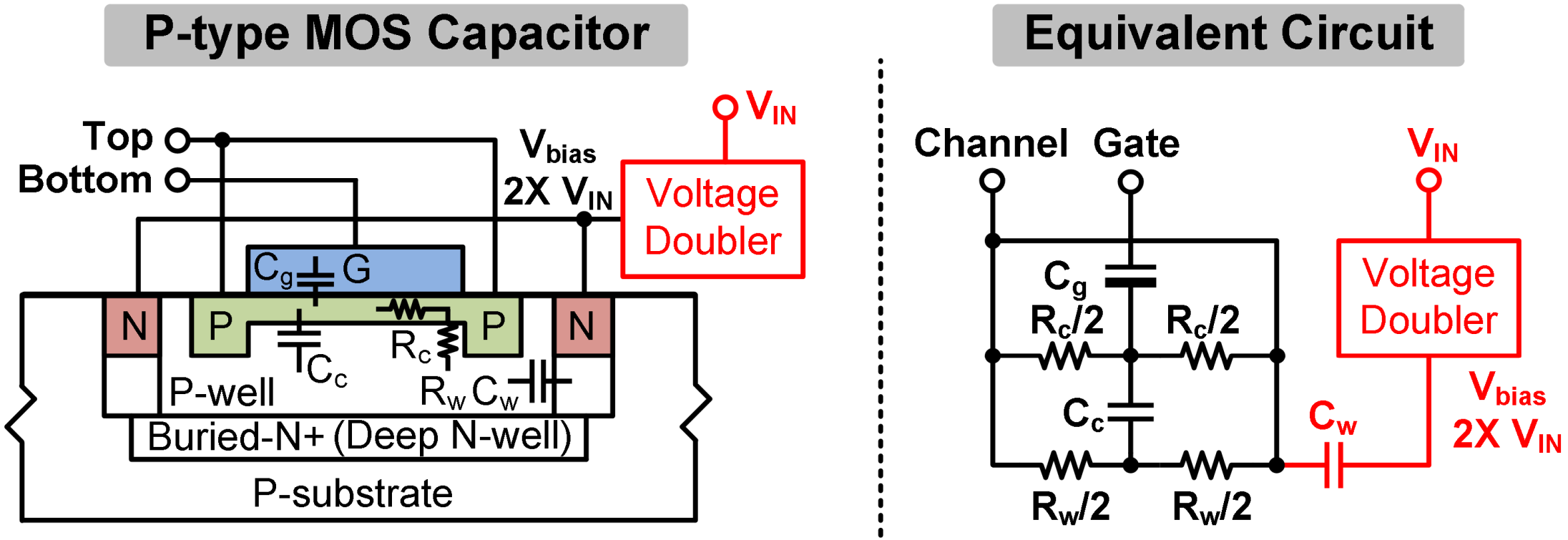
Parasitic Reduction Techniques (1/3)



- Use a large resistor R1 to bias the N-well, making the N-well "floating".
- Then, parasitic cap is dominated by C_W ($<<C_C$).

[H.-P. Le, ISSCC 2013]

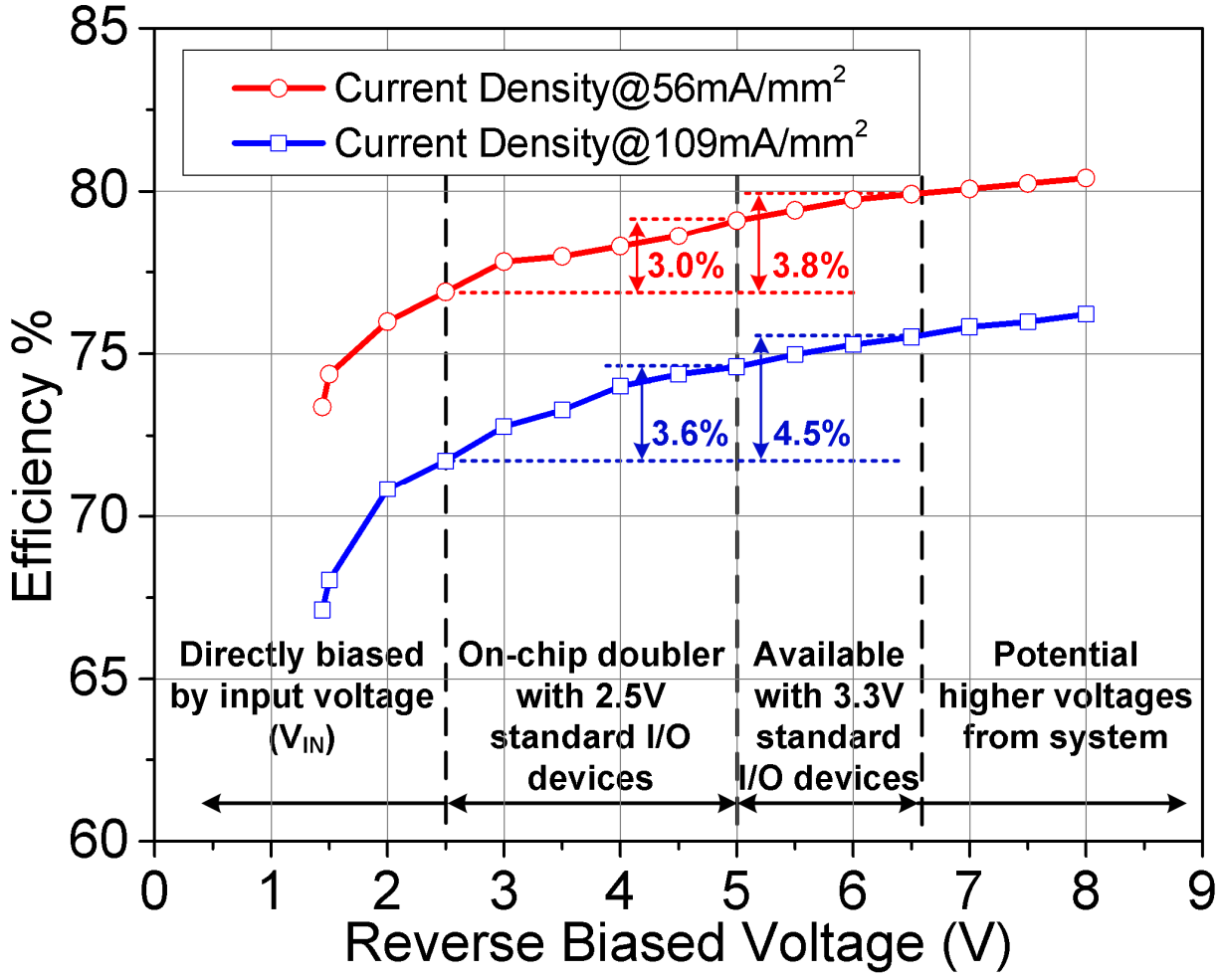
Parasitic Reduction Techniques (2/3)



- C_W: Reduced by on-chip voltage doubler.

[J. Jiang, ISSCC, 2015]

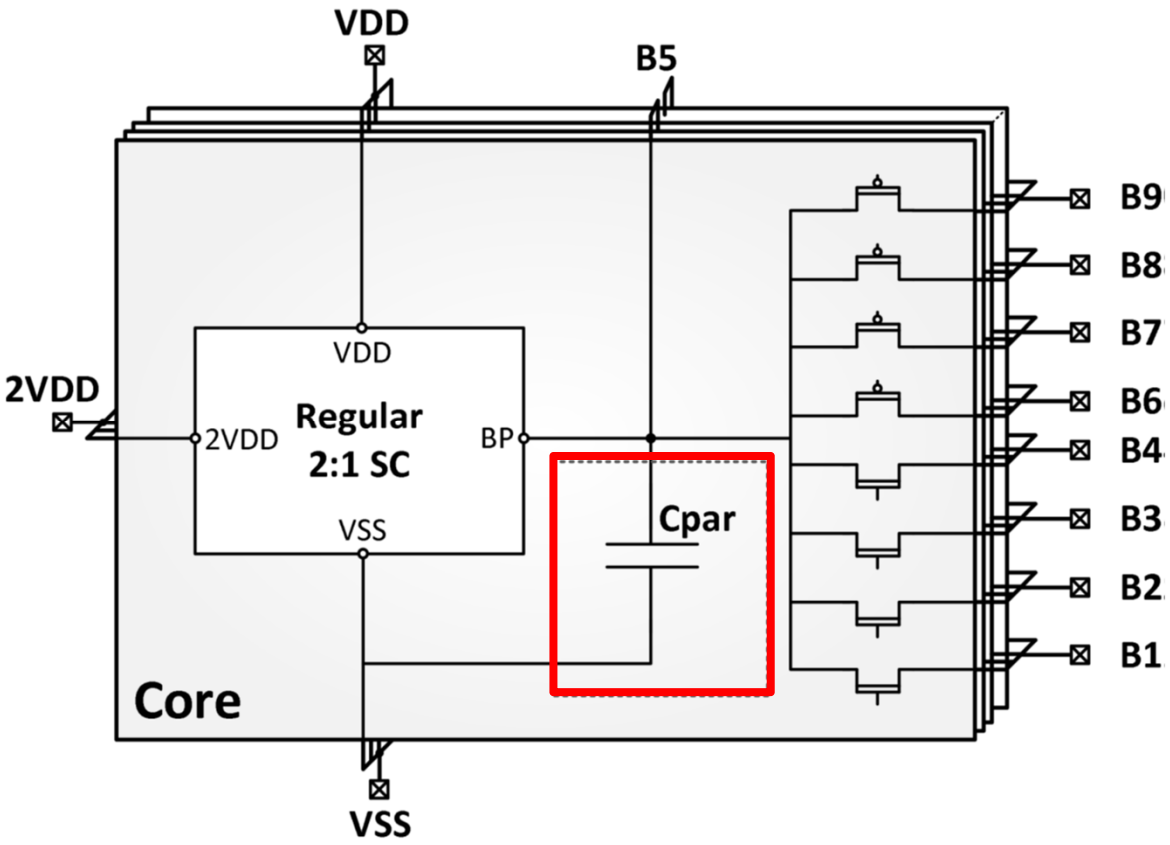
Efficiency Improvements with Reverse Bias Voltage

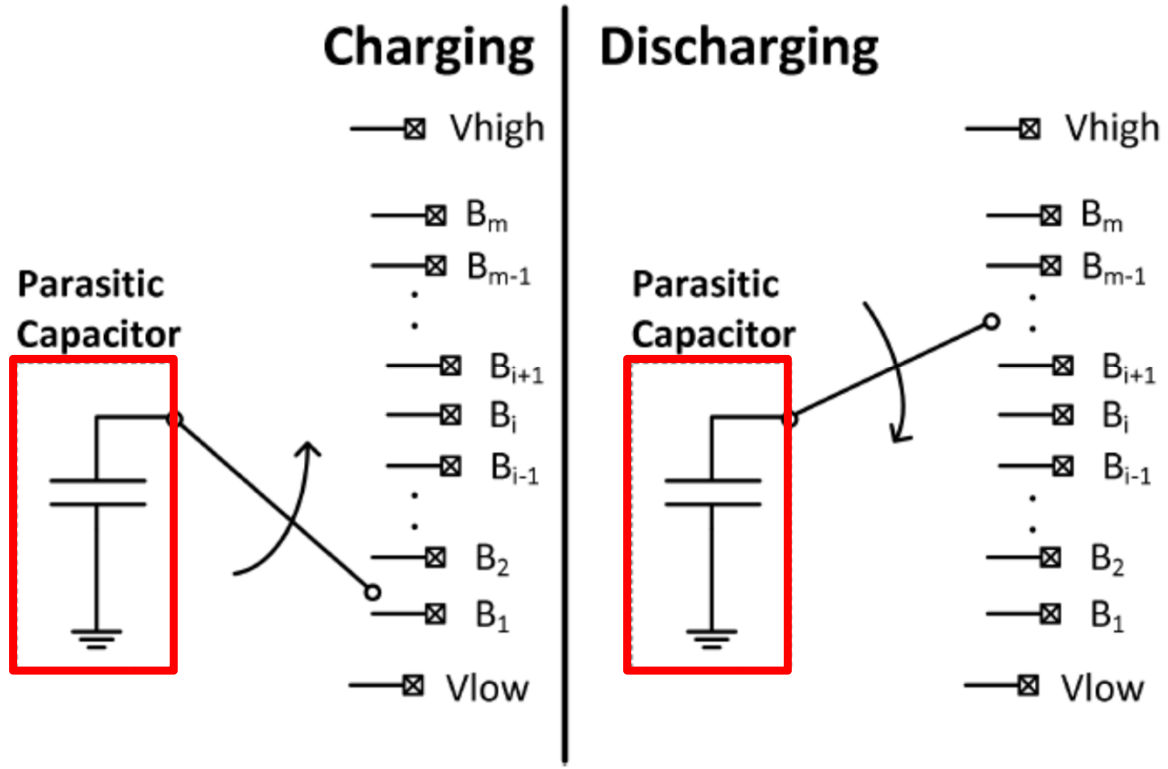


- >3% efficiency improvement for reverse bias voltage changes from 2.5V to 5V.
- Another >3% improvement for voltage changes from 5V to 6.6V.

[J. Jiang, ISSCC, 2015]

Parasitic Reduction Techniques (3/3)





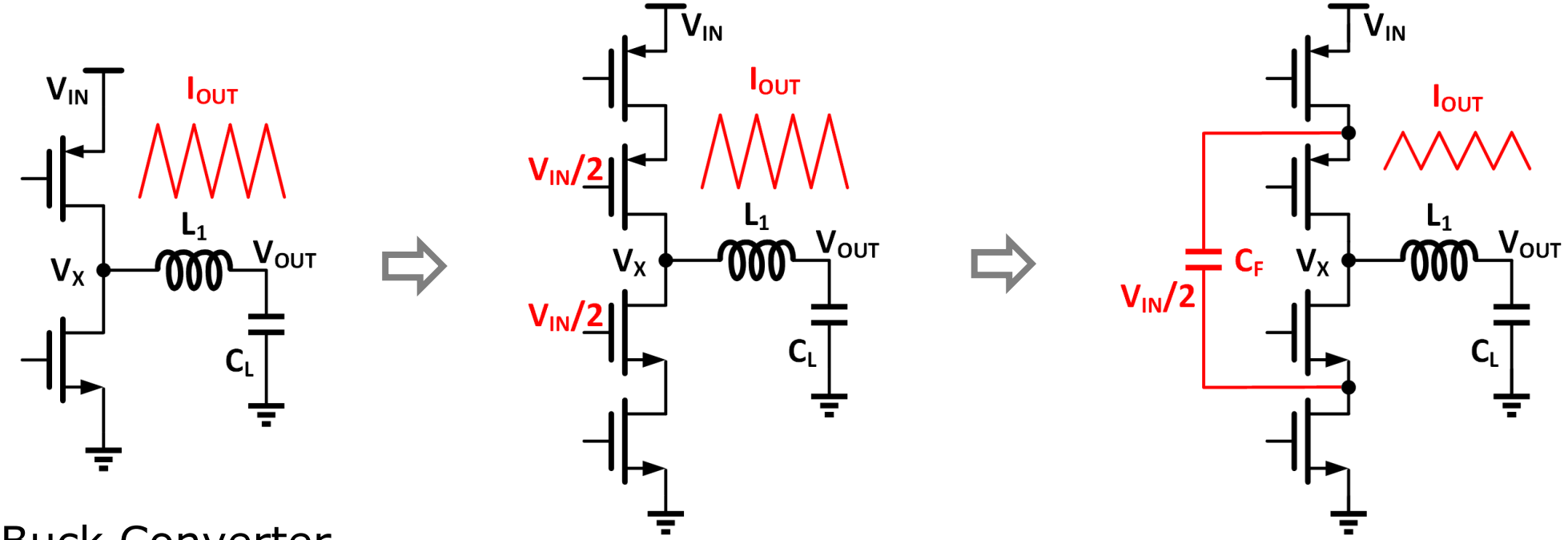
- Recycle parasitic charge between multiple phases. [N. Butzen, JSSC 2017]

Fully-Integrated SC Converter Considerations

- For efficiency
  - More VCR means high efficiencies across a wide input/output range.
  - Choose parasitic-insensitive conversion topologies.
  - Use parasitic reduction circuit techniques.

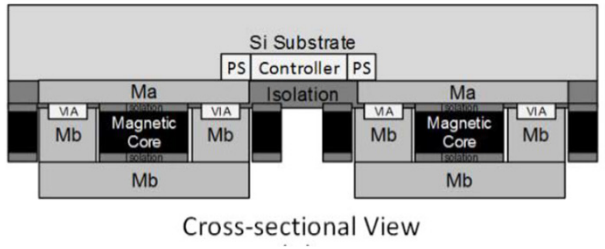
- For output accuracy and efficiency
  - Pulse-frequency modulation (PFM)
  - Adaptive switch size for optimum efficiency and smaller ripple.
  - Tuning the gate-drive voltage of the switches

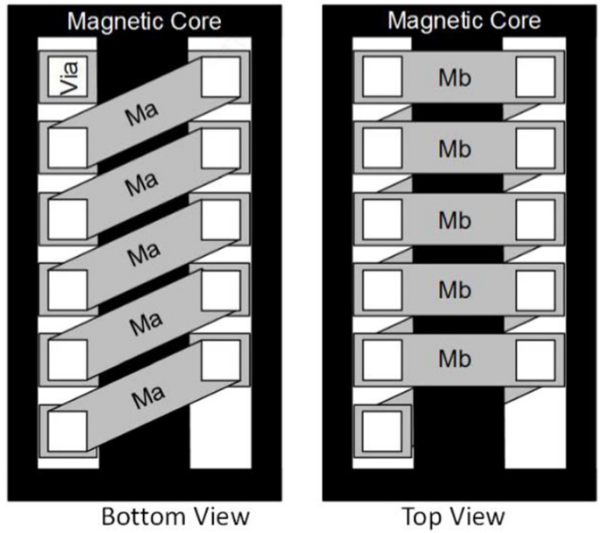
Multi-Level Hybrid DC-DC Converter



- Buck Converter
  - Buck with Stacked Switches
  - Use low-voltage devices for less switching losses
  - 3-Level Buck
  - Smaller voltage swing on V_X
  - Smaller ΔI_L

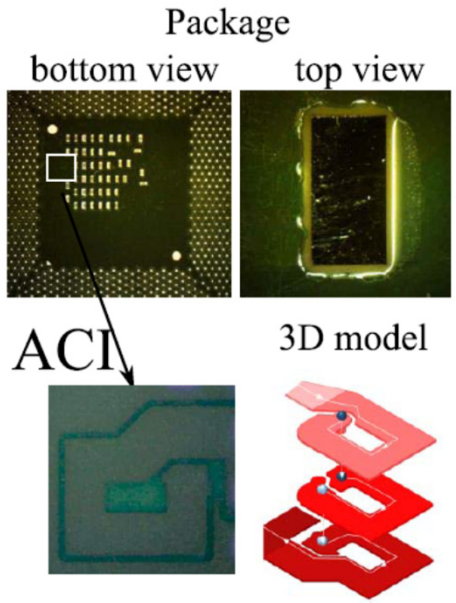
Integrated Inductors





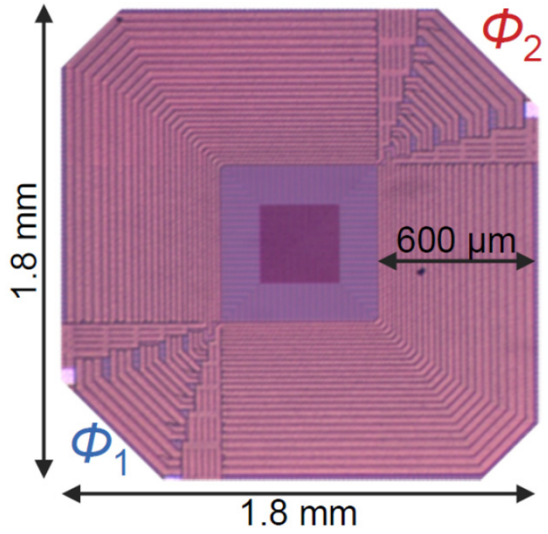
- On-chip magnetic inductor
- 1.5nH, Q≈3.8 @100MHz

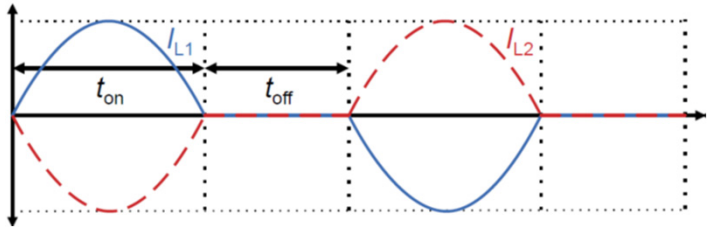
[H. K. Krishnamurthy, ISSCC 2017]



- In-package air-core inductor
- 2.5nH, Q≈7.8 @70MHz

[C. Schaef, ISSCC 2019]

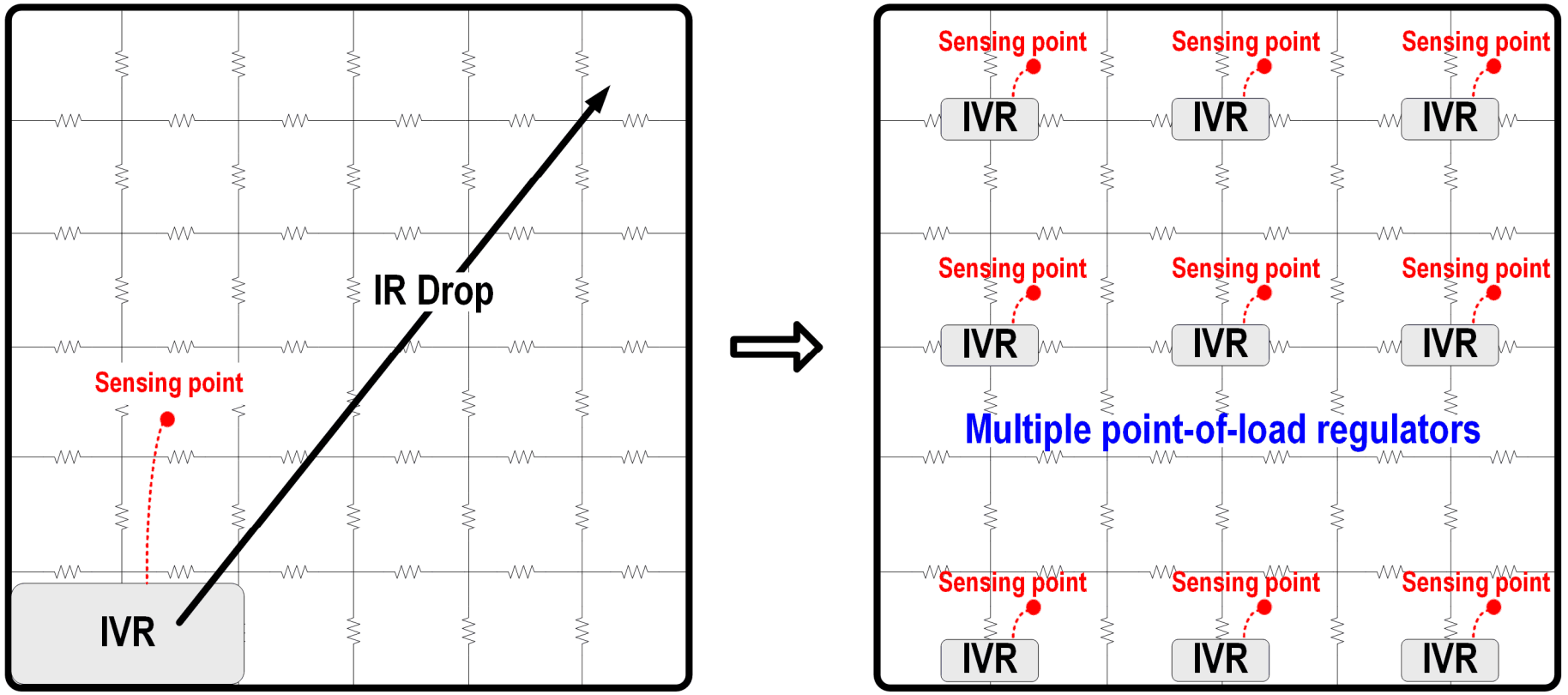




- On-chip coupled LC resonator
- 7.7nH @47.5MHz

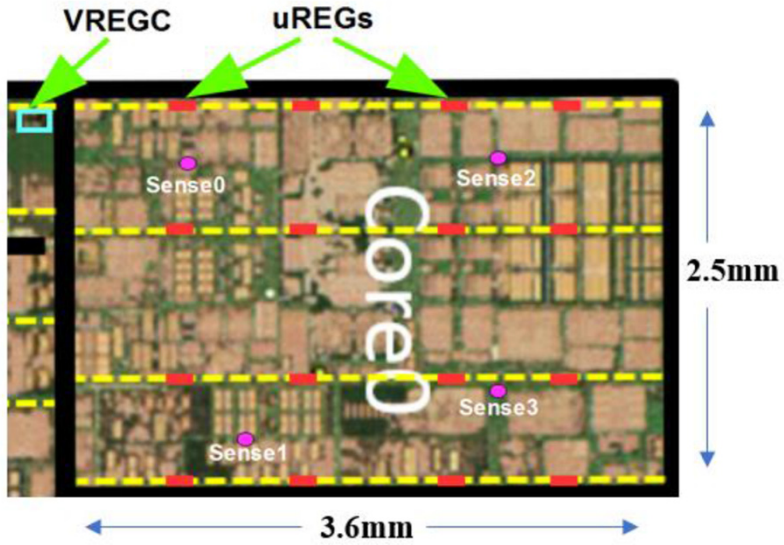
[P. H. McLaughlin, ISSCC 2020]

Distributed FIVR



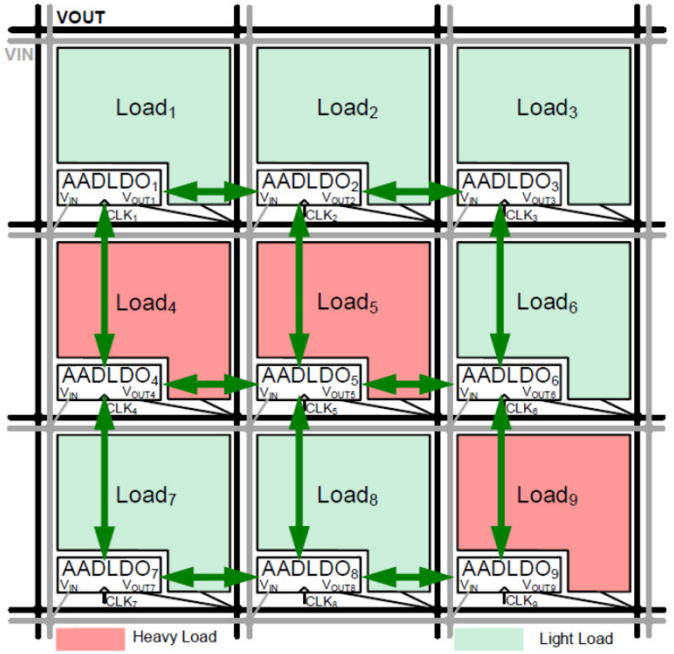
- Reducing the IR drop across a large area chip (>1mm).
- Improving the droop during transient response.

Distributed FIVR Examples



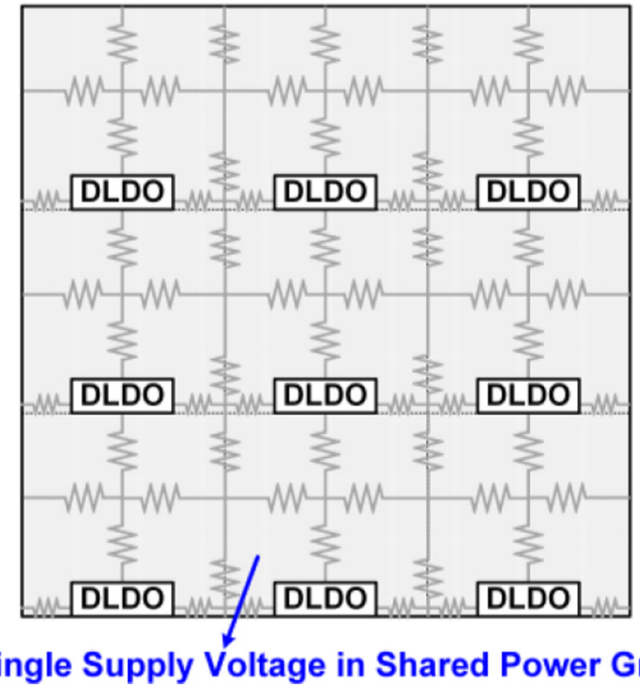
- Global + Distributed local
- Switching linear regulator

[M. E. Perez, CICC, 2019]



- Neighboring cooperation
- Analog-assisted DLDO

[Y. Lu, ISSCC, 2018]



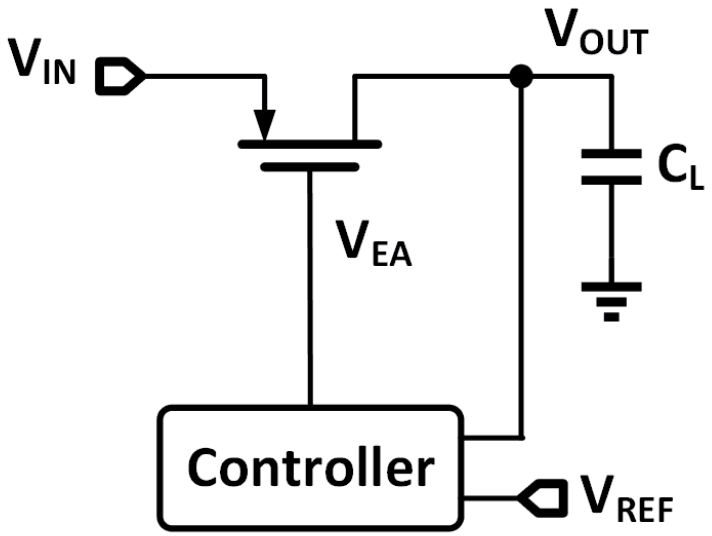
- Each works independently
- Synthesizable DLDO

[S. Bang, ISSCC, 2020]

Outline

- Introduction
- Basic Power Stage Selections
  - Linear Low-Dropout (LDO) Regulator
  - Switched-Capacitor Converter
  - Switched-Inductor Converter
- Control Loop Designs
  - PID Control
  - Hysteretic Control
- Advanced Topologies and Techniques
  - Resonant Switched-Capacitor Operation
  - Multiple Interleaving Phase
  - Switched-Capacitor-Inductor Hybrid Topologies
  - Distributed Integrated Voltage Regulators
- Summary

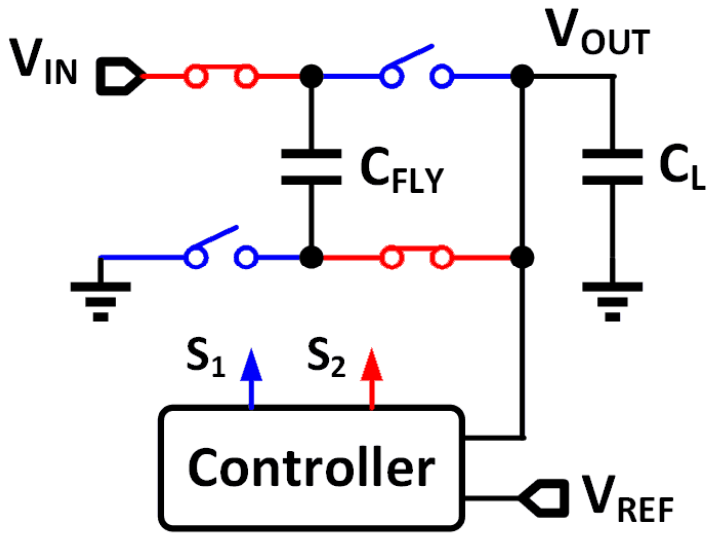
Power Stage Characteristics Summary



LDO Regulator

Power transistor in linear region, acts as a tunable resistor, low efficiency.

No energy storage components (C or L), tiny.

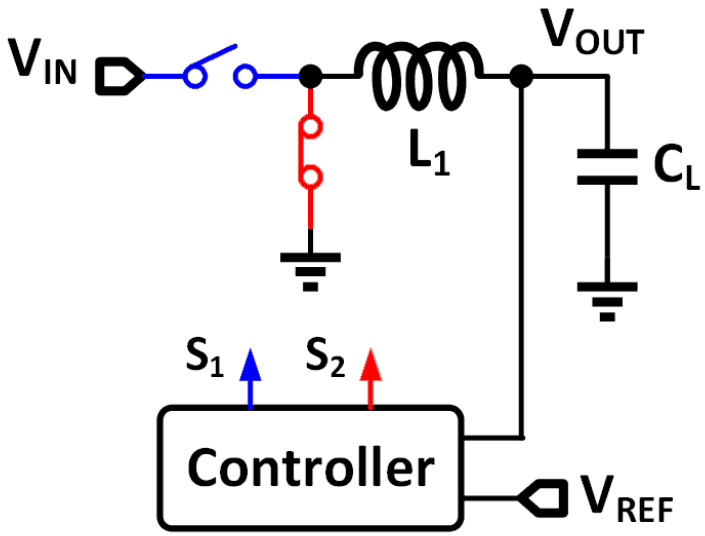


Capacitive DC-DC

SC network acts as a tunable resistor, low efficiency.

Discrete VCR.

Efficiency can be improved by having a proper VCR.



Inductive DC-DC

Continuous VCR.

Efficiency heavily depends on the inductor Q.

Inductor has intrinsically larger DCR than a capacitor.

Summary

- For power stage selection between LDO, SC, and Buck converters, and their control strategies.
  - LDO and SC converter have a single pole power stage.
  - Buck converter in CCM has a complex pole-pair, needs two zeros (PID, Type-III) to cancel out the pole-pair, extending the bandwidth beyond the LC F_{RES}.
  - Buck converter in DCM, or with current-mode control, can ignore the pole associated with the power inductor, being like a single pole power stage.
  - Hysteretic control is extremely fast, but has a varying F_{SW}.
  - Multiple-interleaving-phase power stage helps to extend the loop bandwidth.
- For full integration:
  - LDO is fast, tiny, and hot.
  - SC converter is friendly to process scaling, suffers from parasitic losses.
  - Inductor-based DC-DC needs a good inductor (a luxury for FIVR).
  - Switched-capacitor-inductor hybrid topologies alleviate the burden on inductor.
  - System-in-package solutions provide high Q passives.

Knowledge Required for PMIC

- Analog IC
- Digital IC
- Power Electronics
- Power Device
- Magnetics/Electromagnetics
- Control theory

- **A multi-disciplinary area.**

Papers to See This Year

- **Session 17 "DC-DC Converters"** Relevant Papers:

- **17.1** A Two-Stage Cascaded Hybrid Switched Capacitor DC-DC Converter With 96.9% Peak Efficiency Tolerating 0.6V/μs Input Slew Rate during Startup
- **17.3** A 1.25GHz Fully Integrated DC-DC Converter Using Electromagnetically Coupled Class-D LC Oscillators
- **17.4** Peak-Current-Controlled Ganged Integrated High-Frequency Buck Voltage Regulators in 22nm CMOS for Robust Cross-Tile Current Sharing
- **17.5** A 98.2%-Efficiency Reciprocal Direct Charge Recycling Inductor-First DC-DC Converter

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Acknowledgements

- I would like to thank my (Current and Previous) Colleagues for their significant contributions to this tutorial.
  - Mo Huang, Junmin Jiang, Xiaofei Ma, Chuang Wang, Xiangyu Mao, Lin Cheng, Wing-Hung Ki, Patrick Yue, and Rui Martins.
- And also thank the Tutorial Chair Ali Sheikholeslami (U. of Toronto) and Coordinator Harish Krishnamurthy (Intel) for their inputs and suggestions.

- Funding supports:

科學技術發展基金 FDCT

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Questions?

Live Q&A Session:

Feb. 13, 2021, 8:00-8:20 am, PST

Email: yanlu@um.edu.mo