Basics of Digital Low-Dropout (LDO) Integrated Voltage Regulator

Mingoo Seok
mgseok@ee.columbia.edu

February 16, 2020

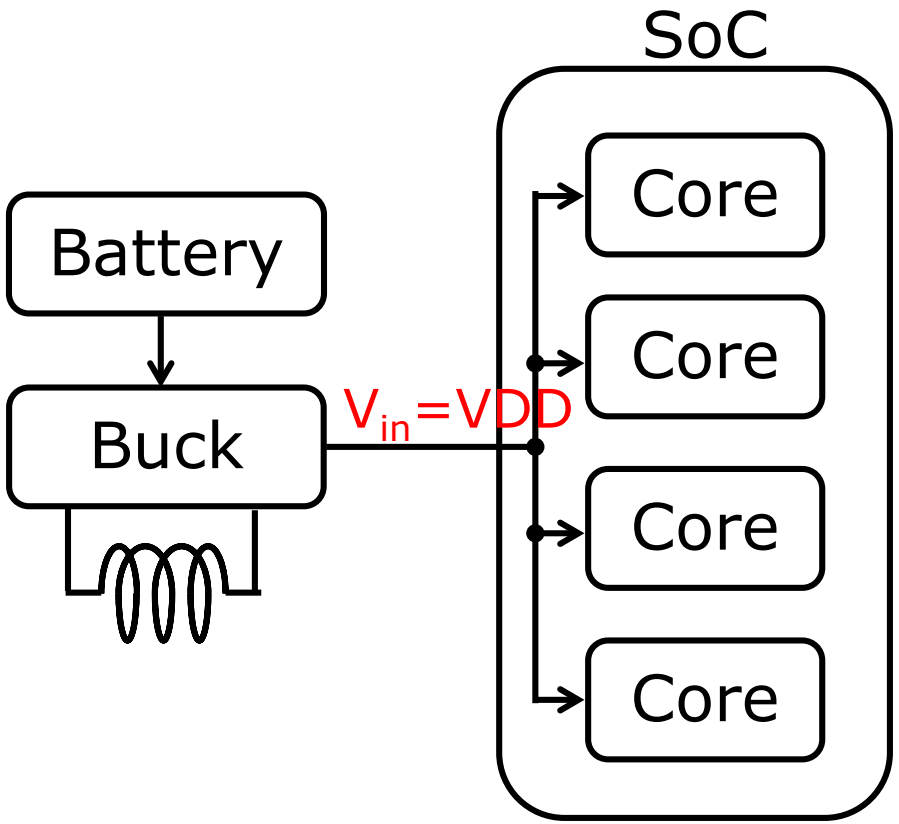
Outline

- Motivation
- Digital vs. Analog LDOs
- Key Specifications
- Interim Q/A
- State-of-the-Art Digital LDO Architectures
- Stability Analysis
- Concluding Remarks

Outline

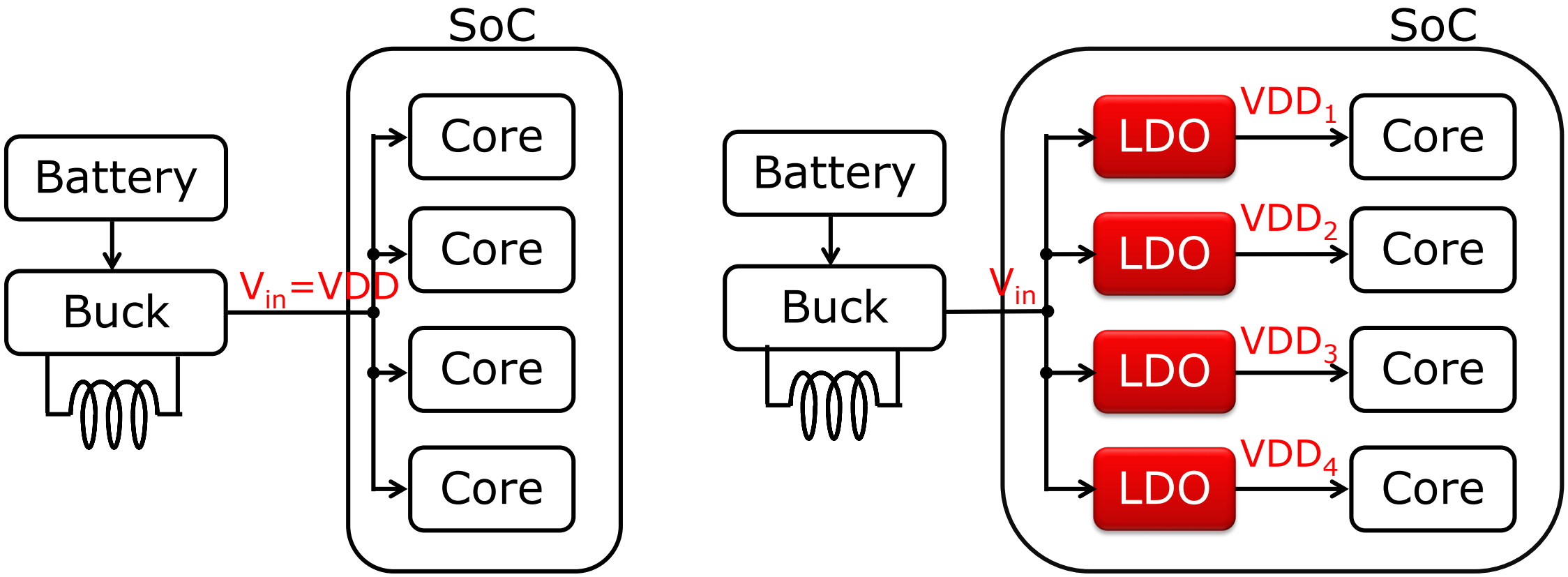
- **Motivation**
- Digital vs. Analog LDOs
- Key Specifications
- Interim Q/A
- State-of-the-Art Digital LDO Architectures
- Stability Analysis
- Concluding Remarks

Conventional Architecture



- Hard to integrate a buck on a chip
- Cores share a single voltage

Integrated Low-Dropout (LDO) Voltage Regulators

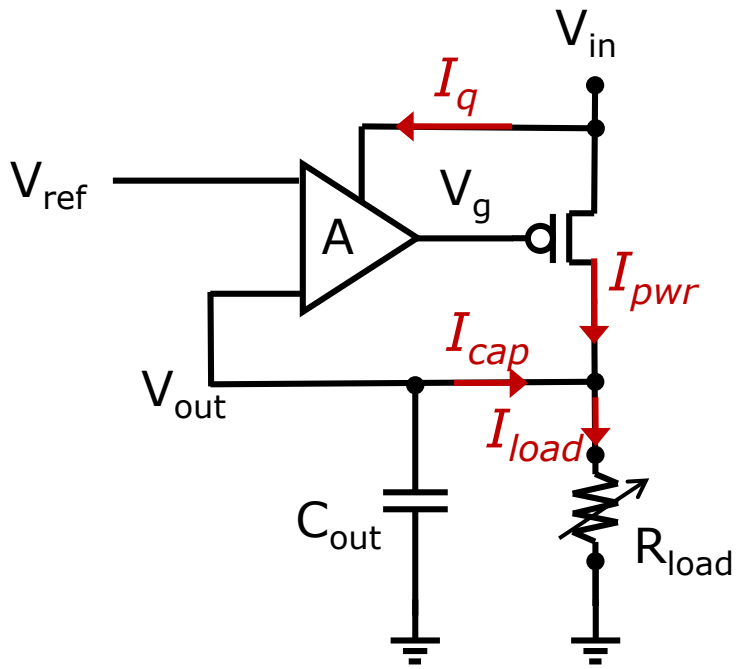


- Hard to integrate a buck on a chip
- Cores share a single voltage
- LDO easy to integrate; no large passives
- LDO can enable per-core voltage domain

Outline

- Motivation
- **Digital vs. Analog LDOs**
- Key Specifications
- Interim Q/A
- State-of-the-Art Digital LDO Architectures
- Stability Analysis
- Concluding Remarks

Analog LDO

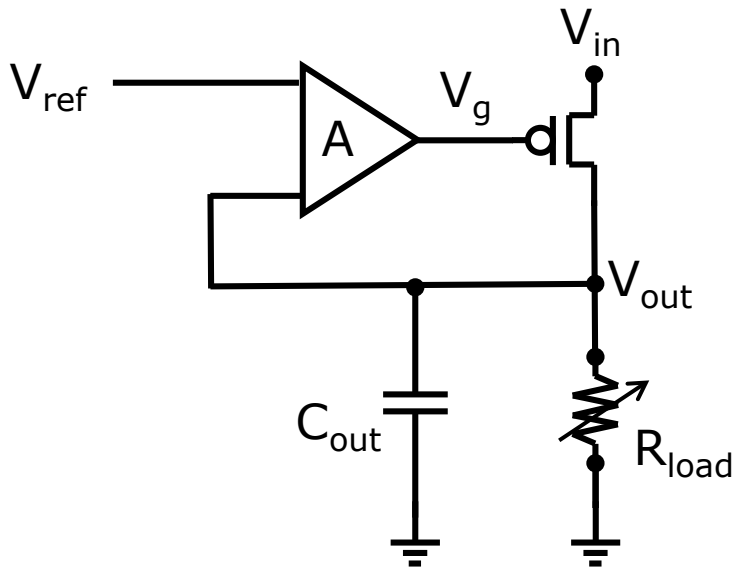


- Analog circuit-based feedback

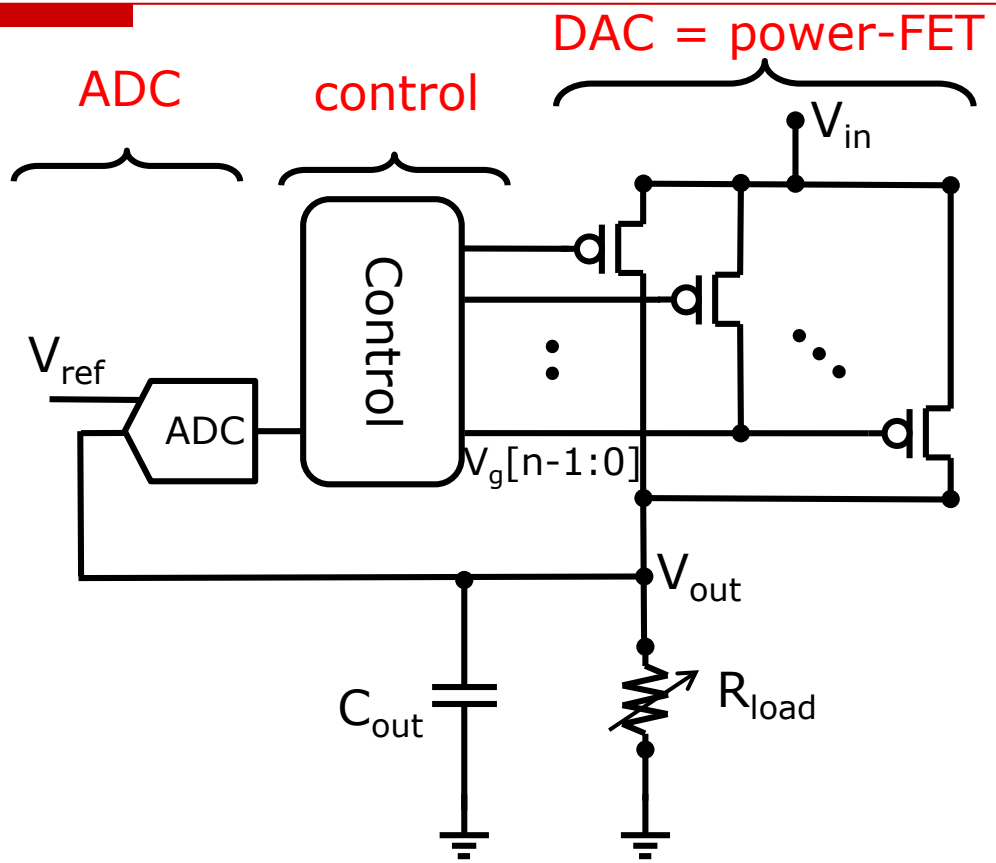
V_g: gate voltage
V_{in}: input voltage
V_{out}: output voltage
V_{ref}: reference voltage
R_{load}: load resistance
C_{out}: output capacitance

I_{load}: load current
I_{pwr}: power-FET current
I_q: quiescent current
I_{cap}: capacitor current

Digital LDO



- Analog circuit-based feedback



- Digital control, sandwiched by ADC and DAC
- ADC: analog to digital converter, DAC: digital to analog converter

Analog vs Digital LDOs

Analog LDO

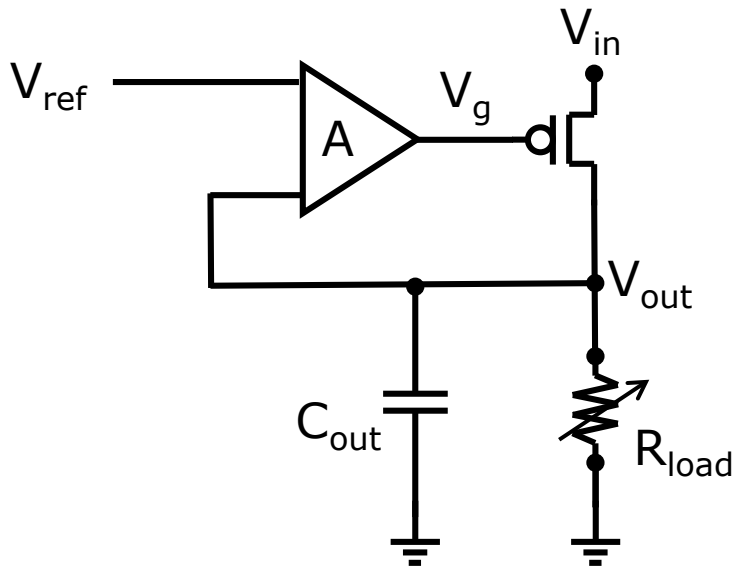
- Pros
  - High bandwidth for fast transient response
  - High power supply rejection ratio (PSRR)
  - Small output ripple
- Cons
  - Complex/bulky analog design
  - Limited scalability to low voltage
  - Loop gain depends on operating voltage

Digital LDO

- Pros
  - No major analog components and synthesizable control
  - Scales well for low-voltage operation
  - Decouples loop gain from operating voltage
- Cons
  - Low bandwidth
  - Low PSRR
  - Large output ripple

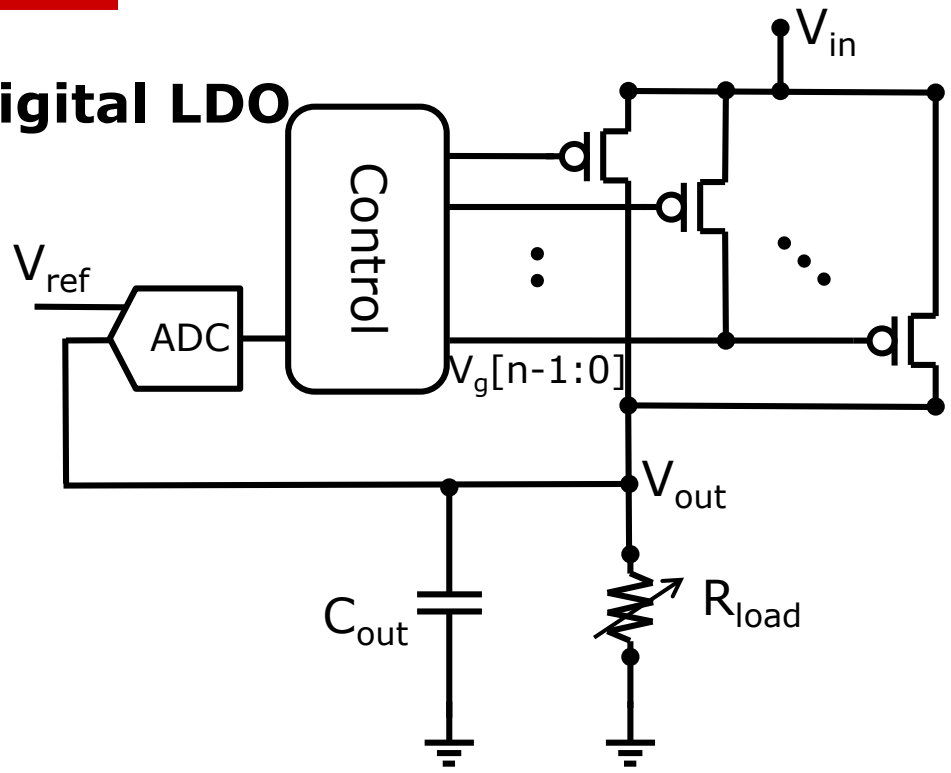
Input Voltage

Analog LDO



- Limited V_{in} scalability
- Typically, V_{in} > 0.6-0.7V
- A high-speed OP amplifier

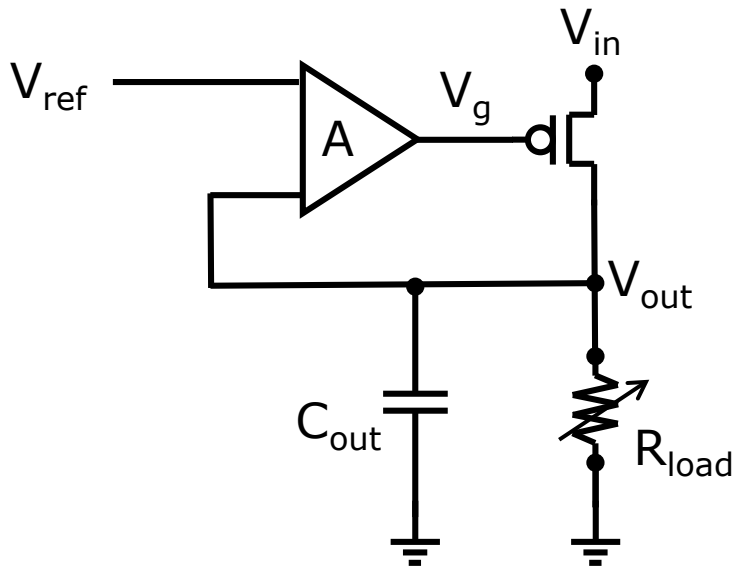
Digital LDO



- Better V_{in} scalability
- 0.5V or less

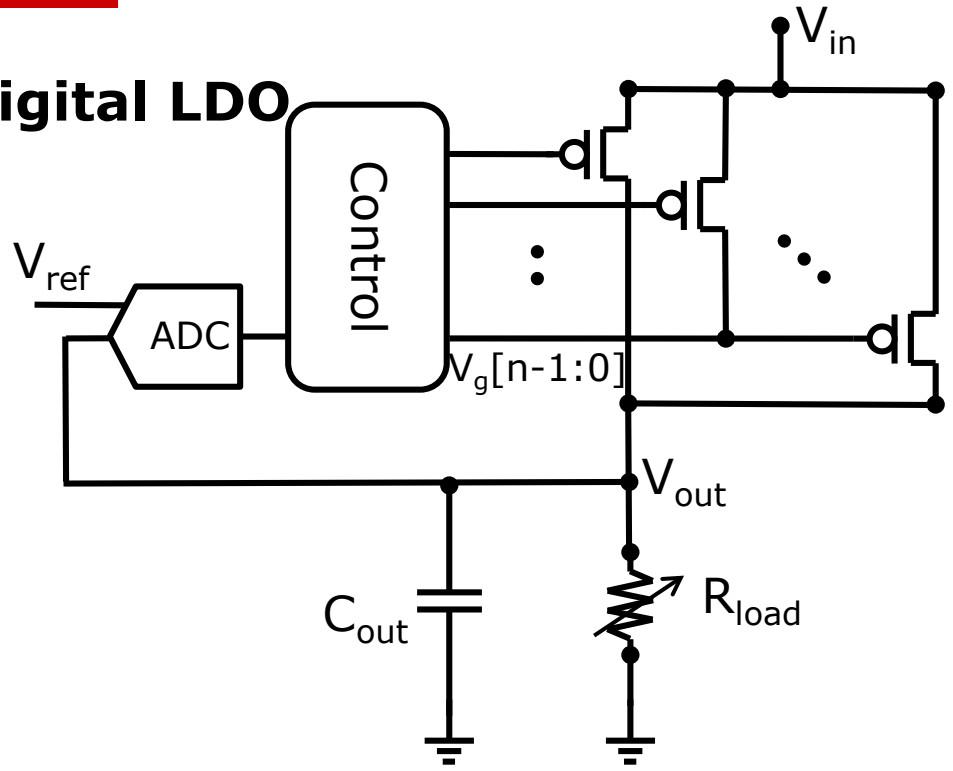
Power-FET's Source-Gate Voltage (V_{sg})

Analog LDO



- $V_{sg}=V_{in}-V_g$ ***between*** $V_{in}-V_{th}$ and 0V
- i.e., V_g is analog voltage

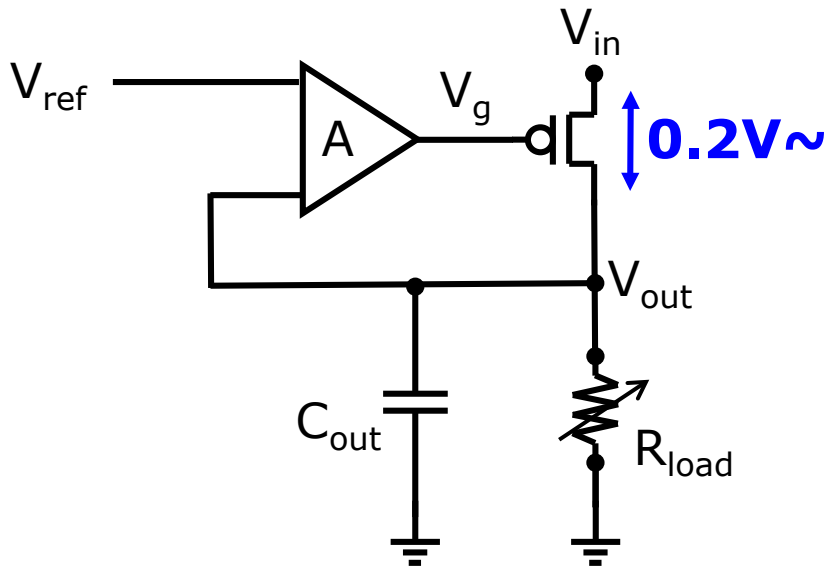
Digital LDO



- $V_{sg}=V_{in}-V_g$: ***either*** 0V or V_{in}
- i.e., V_g is digital voltage

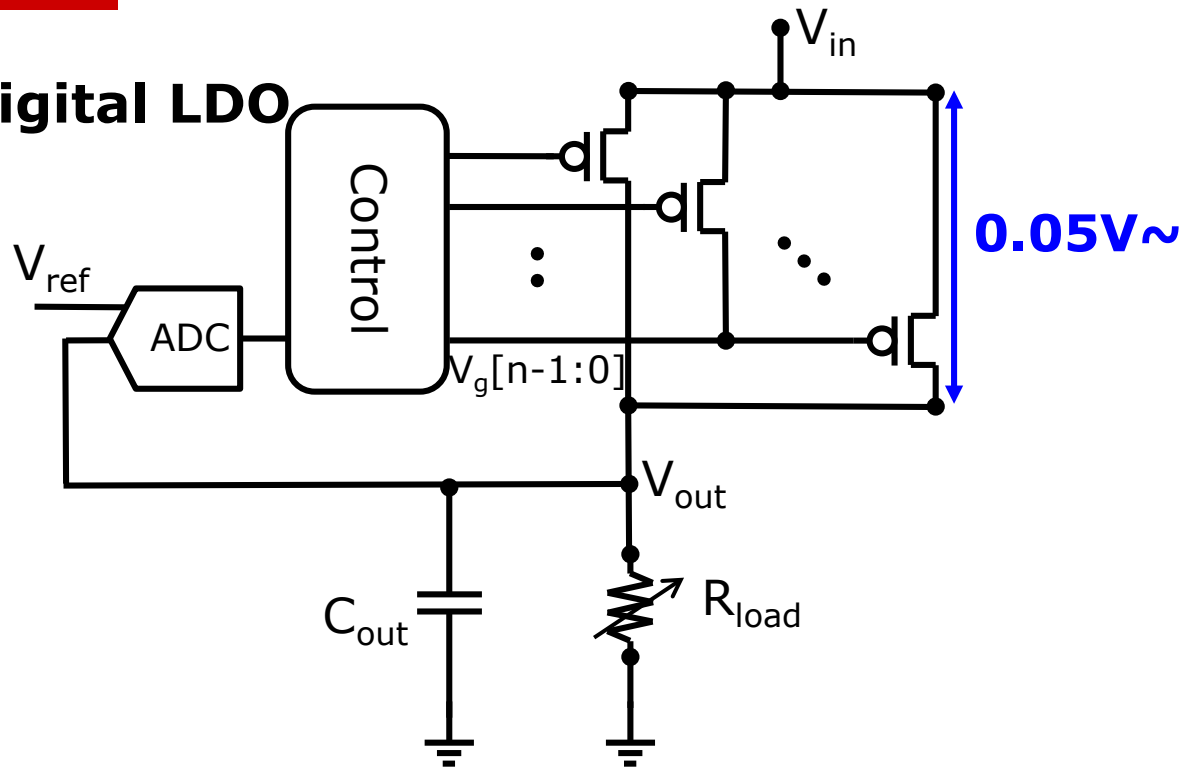
Output Voltage

Analog LDO



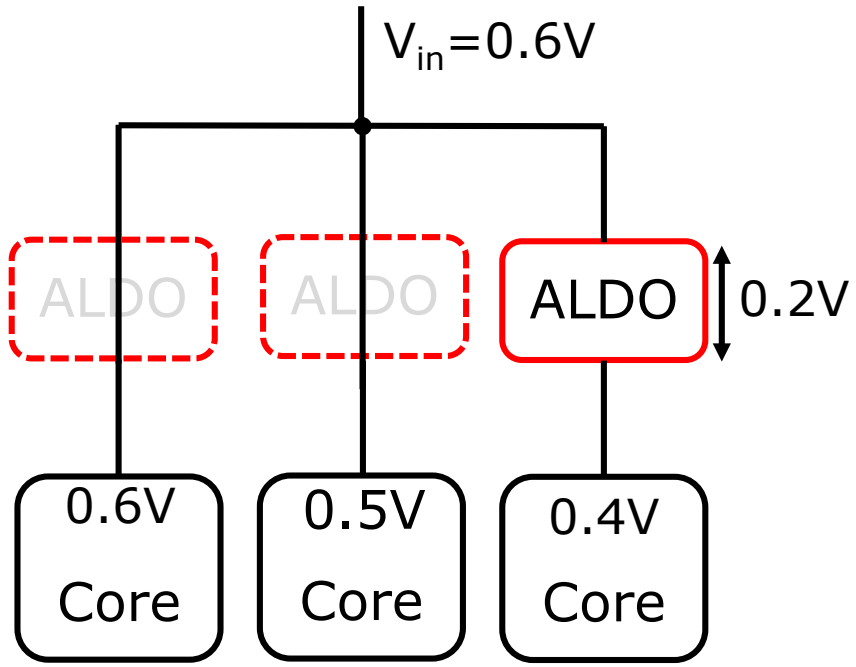
- **V_{out} = V_{in}–0.2V to ~0V**
- Power FET is typically in saturation
- If a load needs V_{in}-0.1V, we supply V_{in}

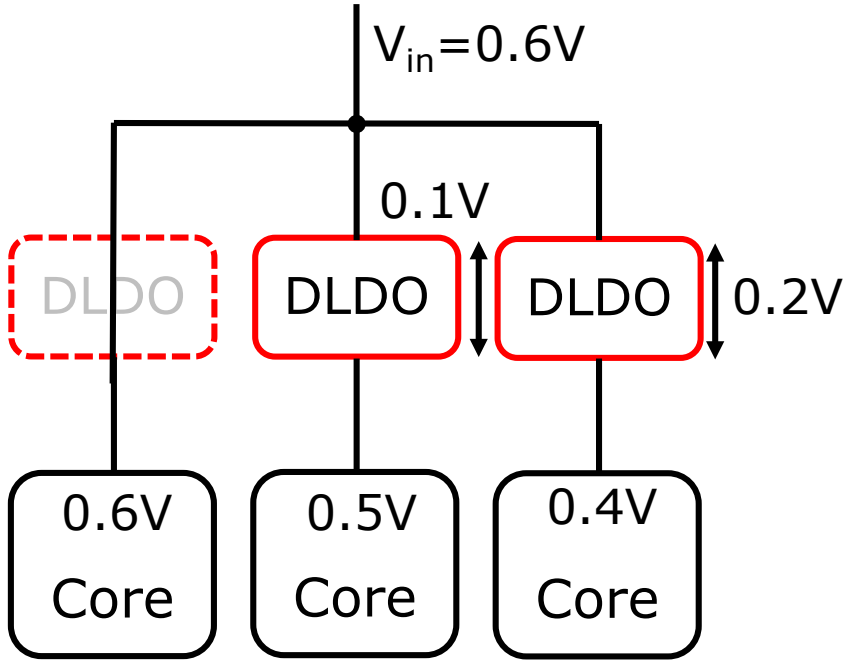
Digital LDO



- **V_{out} = V_{in}–0.05V to ~0V**
- Power FET is in linear to saturation
- Wider output voltage range

Dropout Voltage Requirement





- V_{in} set to the highest VDD requirement
- An LDO can be bypassed

- Less dropout voltage requirement
- Support wider output voltage

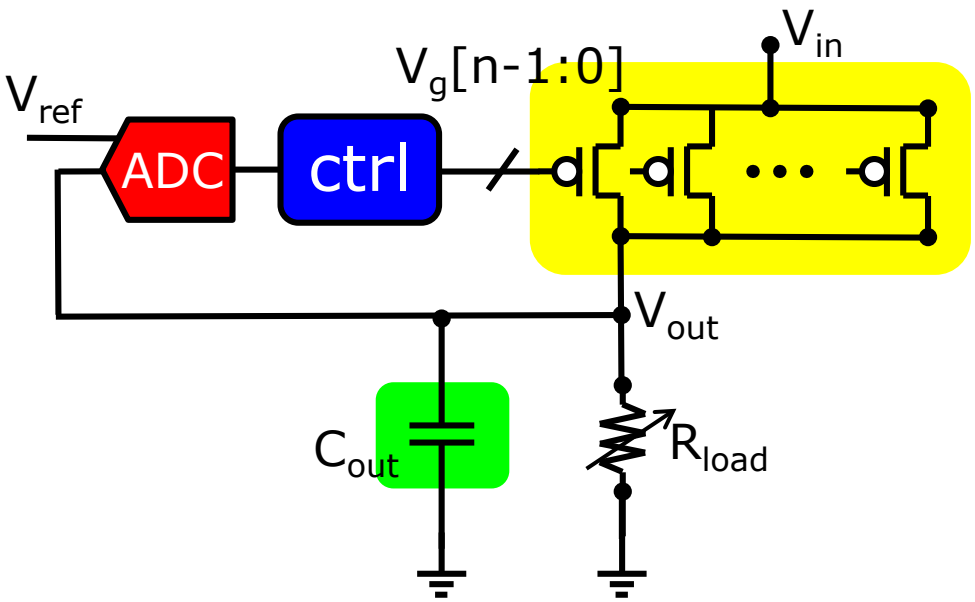
Outline

- Motivation
- Digital vs. Analog LDOs
- **Key Specifications**
- Interim Q/A
- State-of-the-Art Digital LDO Architectures
- Stability Analysis
- Concluding Remarks

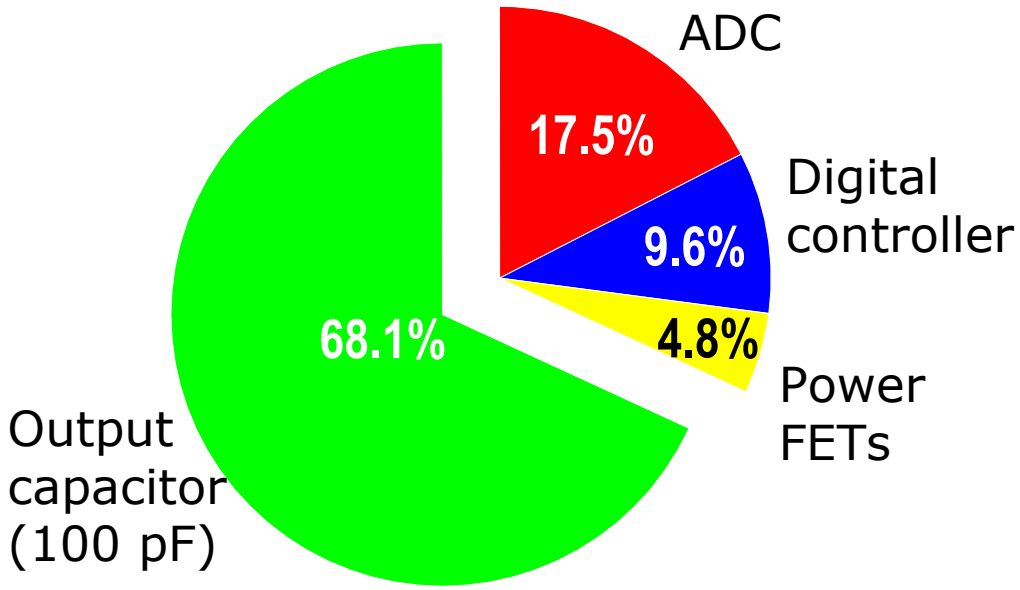
Key Specifications

- Silicon area
- Input, reference, and output voltage (V_{in}, V_{ref}, V_{out})
- Edge time (t_{edge})
- Voltage droop and overshoot (V_{droop}, $V_{overshoot}$)
- Response and settling time ($t_{response,}$ t_{settle})
- Load, quiescent, power-FET, and capacitor current (I_{load}, I_q, I_{pwr}, I_{cap})
- Peak current and power efficiency ($CE_{peak,}$ PE_{peak})
- Dropout voltage ($V_{dropout}$)
- Power supply rejection ratio (PSRR)
- Load regulation performance FoMs: ps FoM and pF FoM
- Maximum and minimum load current ($I_{load,max}$, $I_{load,min}$)
- DAC and ADC number of bits (N_{DAC},N_{ADC})
- Dead-zone voltage (V_{dz})
- DAC step size ($V_{DAC,ss}$)
- IR drop voltage (V_{IR})

Silicon Area

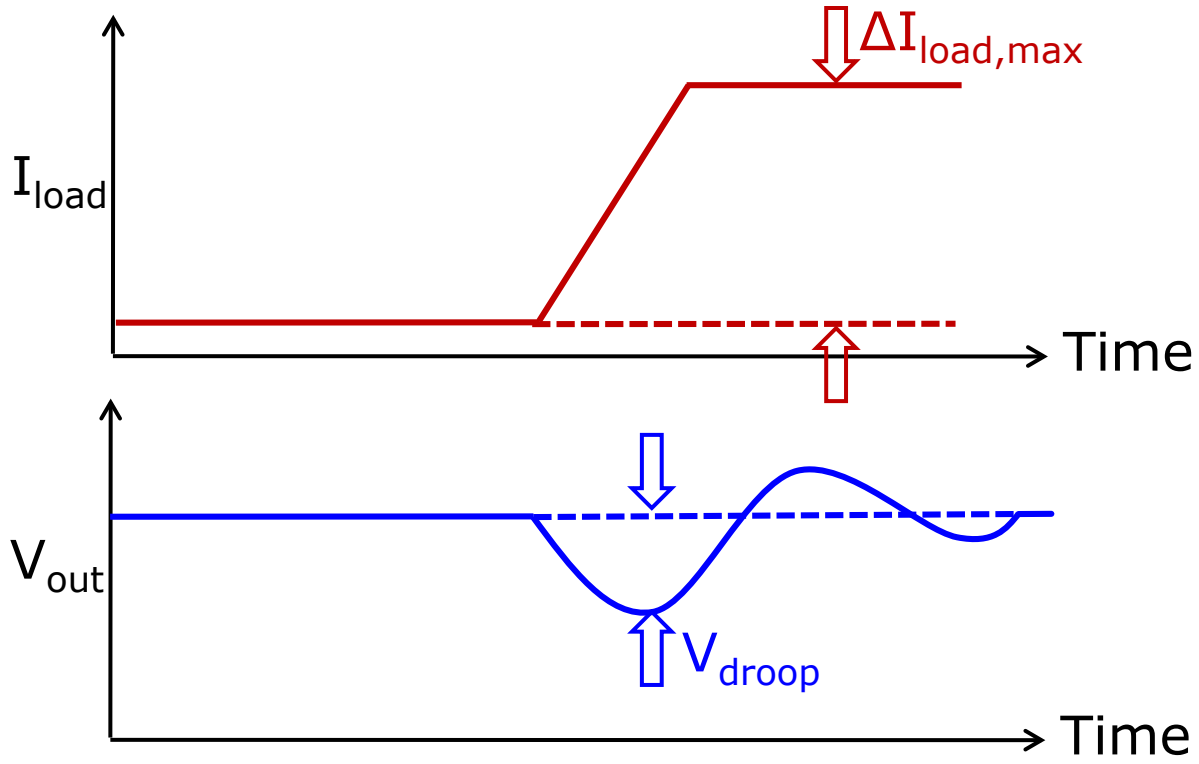


65-nm example [Kim-VLSI19]



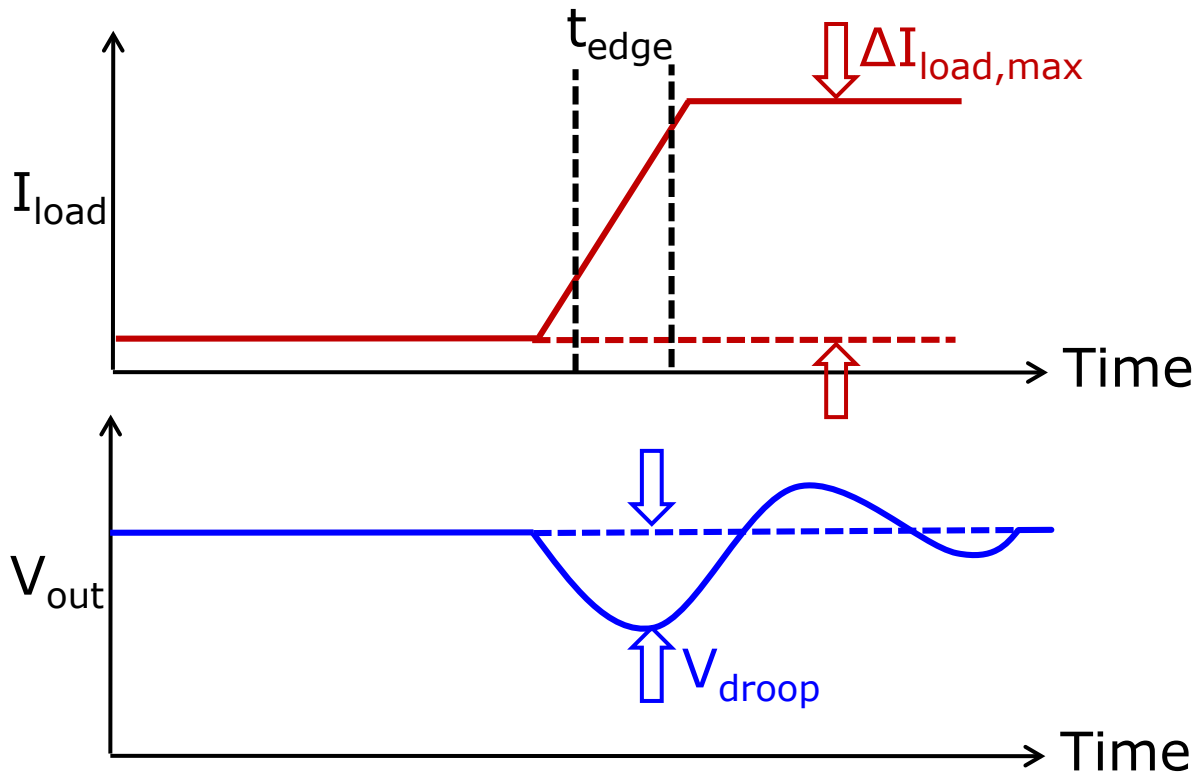
- Active components scale better than passive with technology scaling

Voltage Droop (V_{droop})



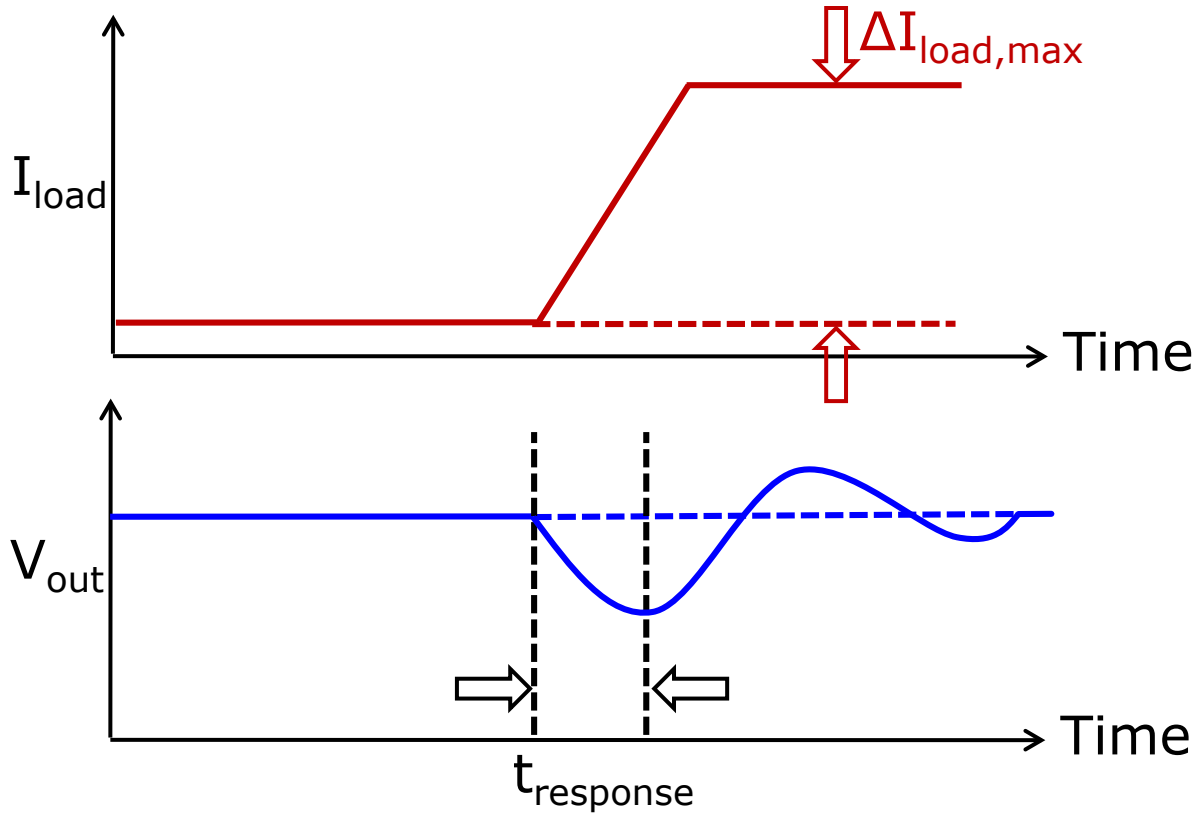
- V_{out}'s maximum *downward* deviation from V_{ref}
- V_{droop} is typically targeted to less than 10% of V_{out}
- $\Delta I_{load,max}$ can be different from $I_{load,max}$

Edge Time (t_{edge})



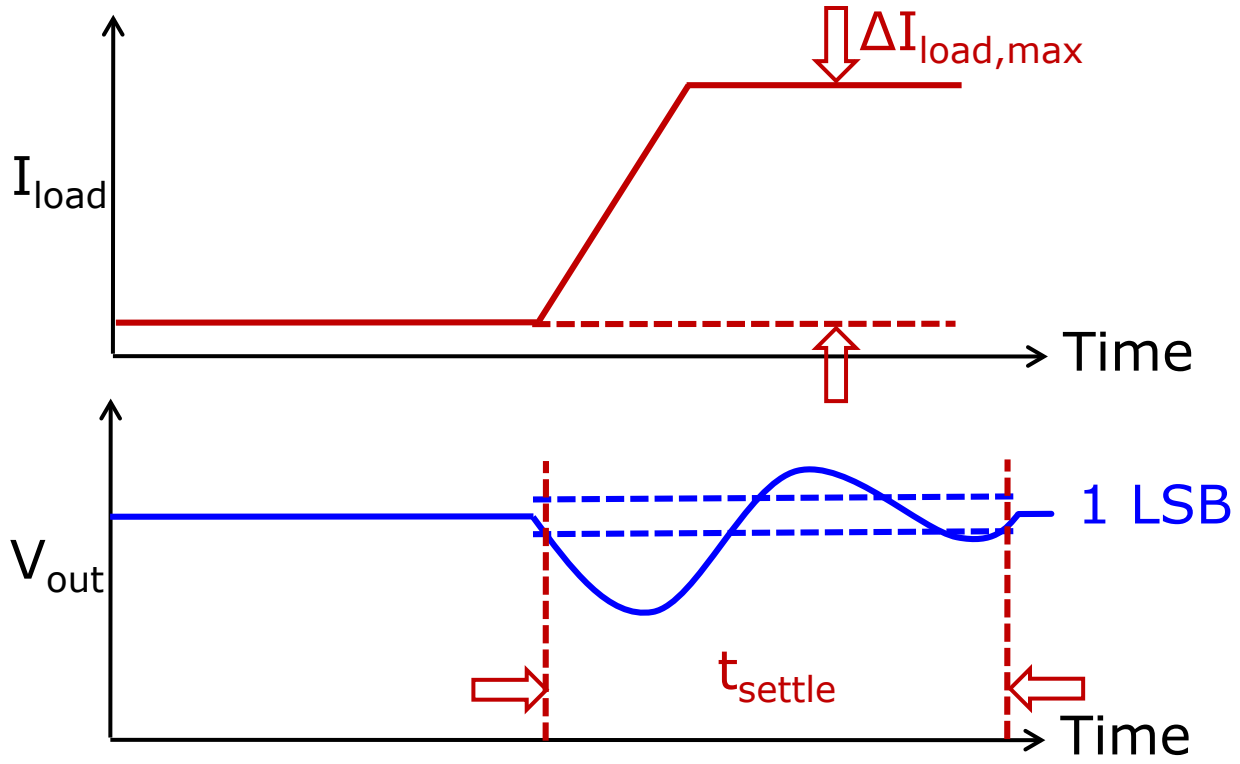
- t_{edge} is a function of the clock period of a load
- 1 GHz core → 1-ns t_{edge}
- 2 GHz core → 0.5-ns t_{edge}

Response Time ($t_{response}$)



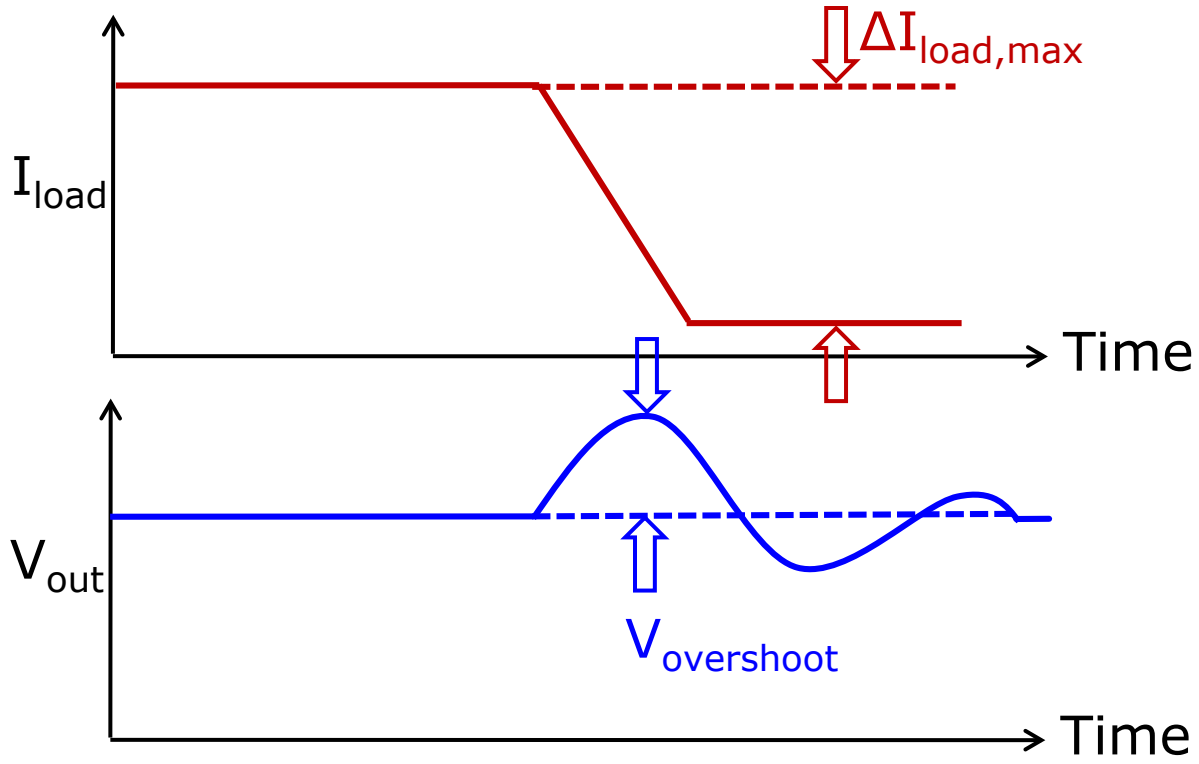
- It is roughly proportional to feedback latency
- In synchronous control, it is proportional to t_{clk}
- In asynchronous control, it is proportional to circuit latency/delay

Settling Time (t_{settle})



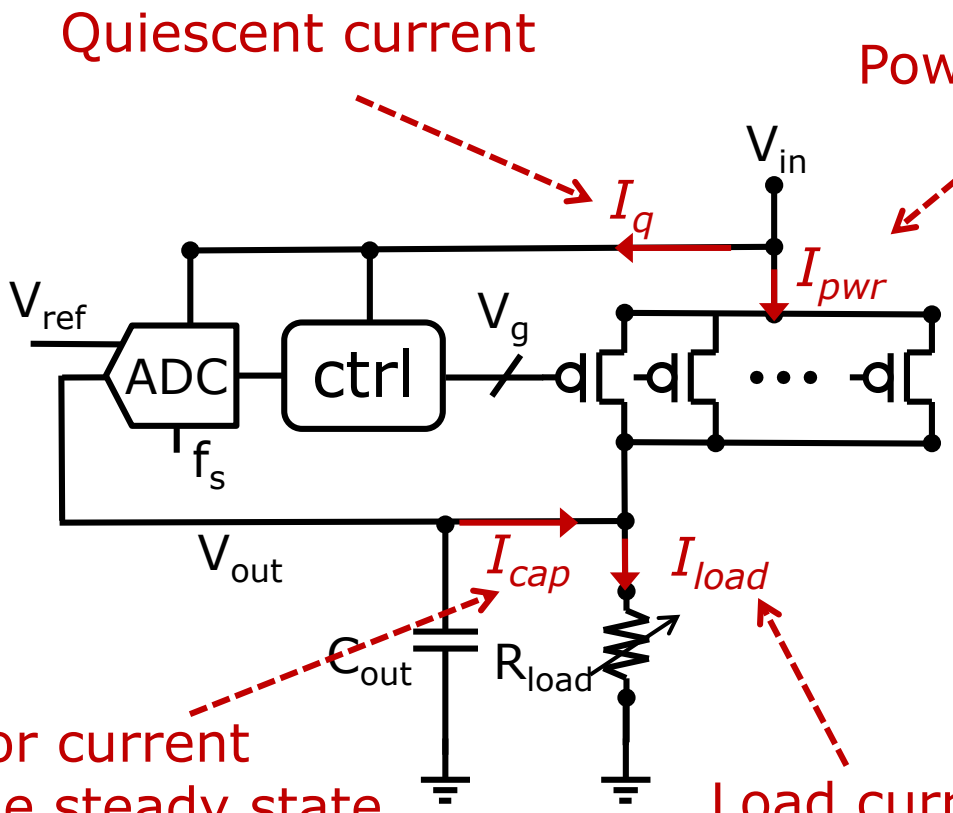
- Time to take for V_{out} to settle within less than a small % of V_{ref} (e.g., +/- 0.5%)
- The output can have a ripple

Voltage Overshoot ($V_{overshoot}$)



- V_{out}'s maximum *upward* deviation from V_{ref}
- $V_{overshoot}$ is typically targeted to less than 10% of V_{out}
- $\Delta I_{load,max}$ is different from $I_{load,max}$

Current and Power Efficiency (CE, PE)



$$CE = \frac{I_{load}}{I_q + I_{load}}$$

Total current

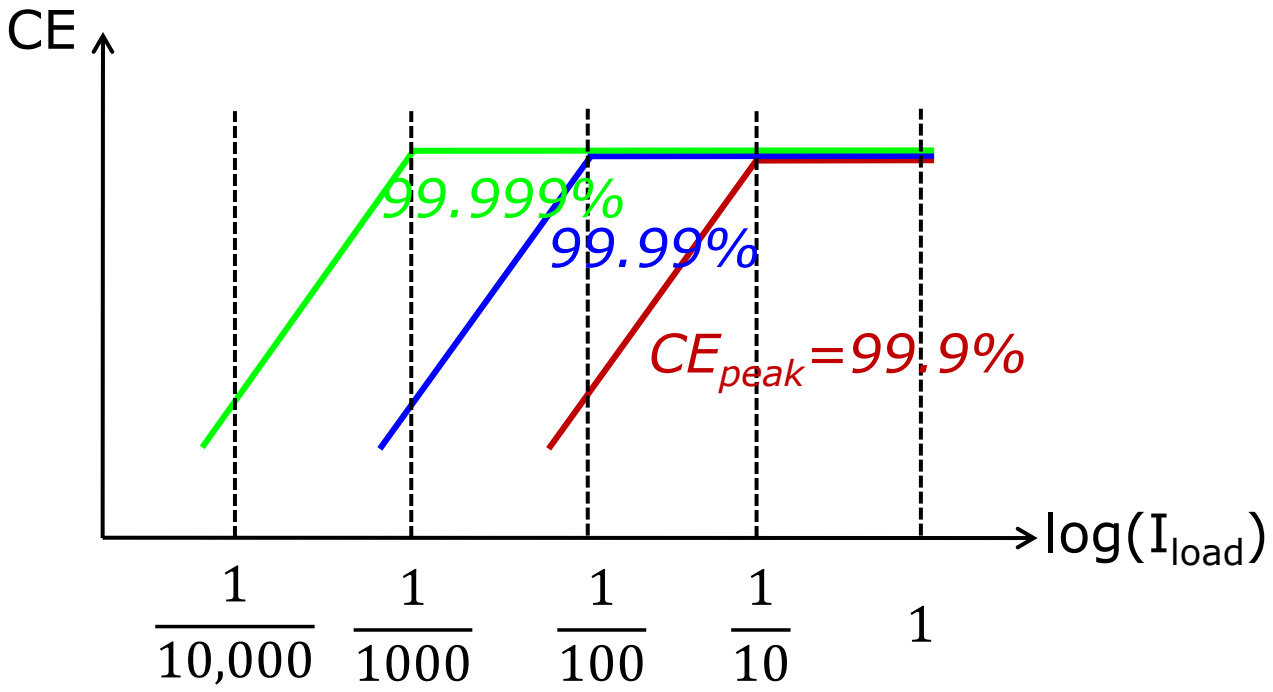
$$PE = \frac{V_{out} \cdot I_{load}}{V_{in} \cdot (I_q + I_{load})} \approx \frac{V_{out}}{V_{in}}$$

If: $I_q << I_{load}$

Current Efficiency vs. *Peak* Current Efficiency

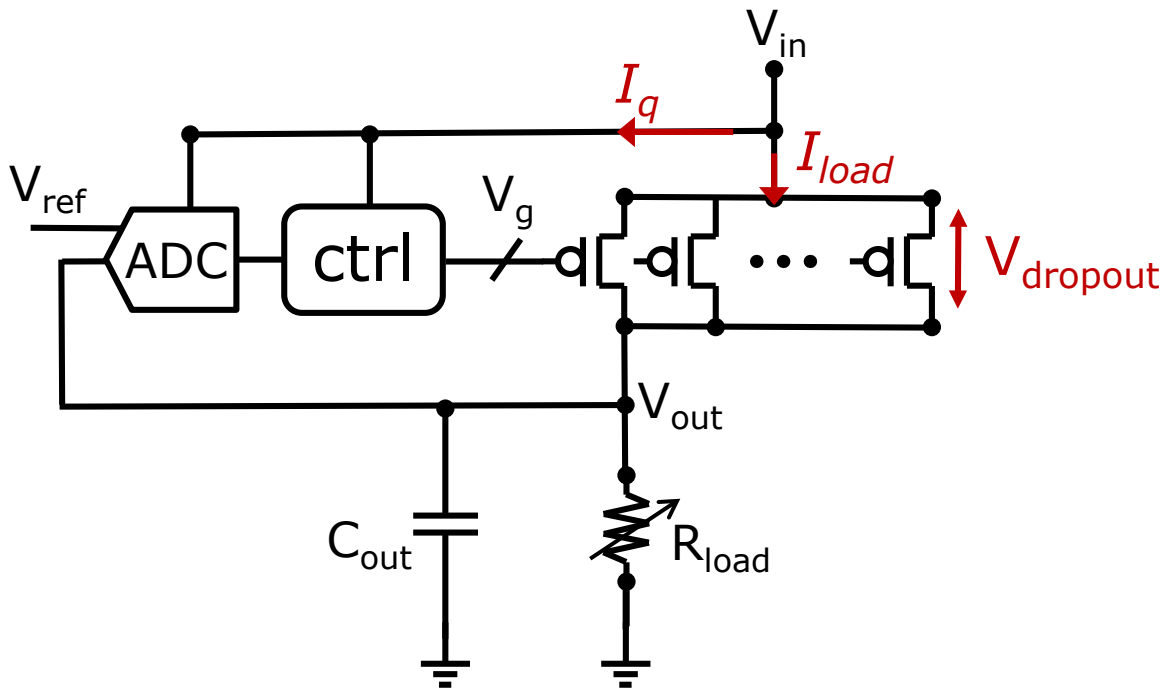
$$CE = \frac{I_{load}}{I_q + I_{load}}$$

$$CE_{peak} = \frac{I_{load,\,max}}{I_q + I_{load,max}}$$



- 99.9% CE_{peak} → 1% or less loss for I_{load} = **$0.1 \cdot I_{load,max}$** to $I_{load,max}$
- 99.999% CE_{peak} → 1% or less loss for I_{load} = **$0.001 \cdot I_{load,max}$** to $I_{load,max}$

Dropout Voltage ($V_{dropout}$)



$$CE = \frac{I_{load}}{I_q + I_{load}}$$

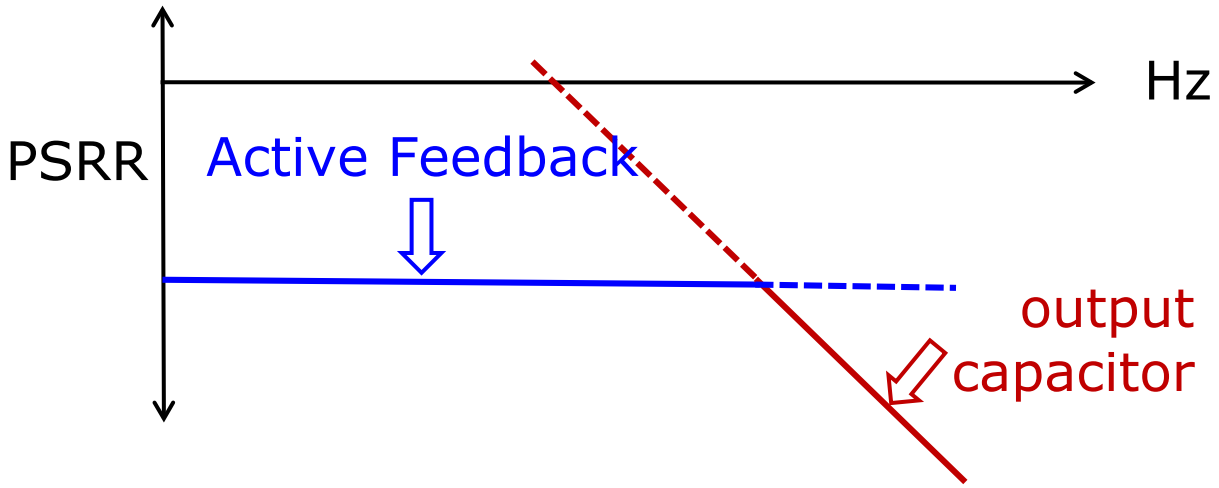
$$PE = \frac{V_{out} \cdot I_{load}}{V_{in} \cdot (I_q + I_{load})} \approx \frac{V_{out}}{V_{in}}$$

$$= \frac{V_{in} - V_{dropout}}{V_{in}} = 1 - \underbrace{\frac{\boldsymbol{V_{dropout}}}{\boldsymbol{V_{in}}}}$$

The larger dropout voltage, the lower PE

Power Supply Rejection Ratio (PSRR)

$$PSRR = 20 \cdot \log \frac{\Delta V_{out}}{\Delta V_{in}} \quad [dB]$$



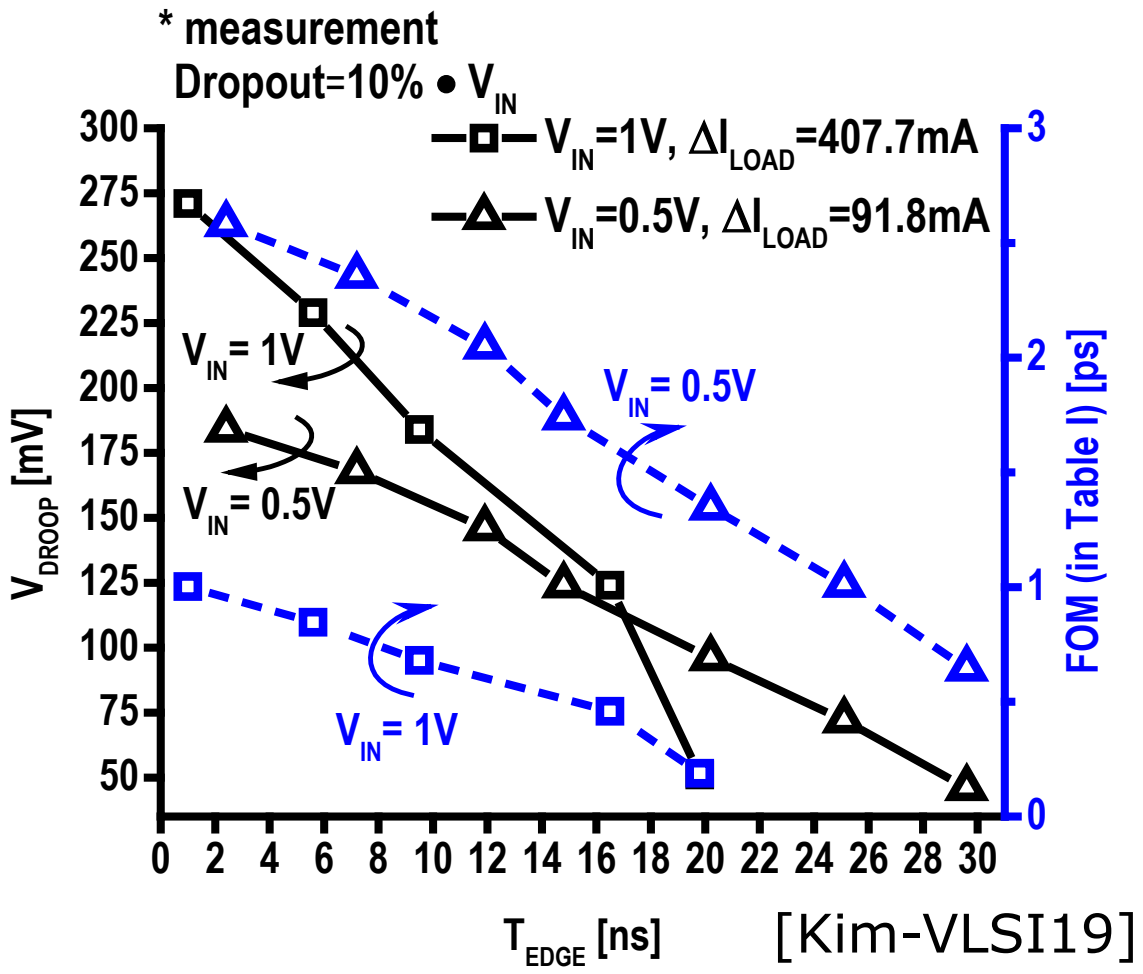
ps Figure of Merit (ps-FoM)

$$ps\ FoM = t_{response} \cdot \widehat{I_q} = \underbrace{\left(\frac{C_{out} \cdot \Delta V_{out}}{\Delta I_{load,\,max}}\right)}_{\text{Pseudo response time}} \cdot \underbrace{\left(\frac{I_q}{\Delta I_{load,\,max}}\right)}_{\text{Pseudo current efficiency}}$$

- Dynamic load regulation performance
- *This FoM aims to capture the product of the LDO response time and current efficiency*
- Smaller is better

[Hazucha-JSSC05]

Caveats for the ps-FoM



[Kim-VLSI19]

- V_{in}, $t_{edge,}$ and $\Delta I_{load,max}$ have a strong impact on FoM.
- ps FoM favors large $\Delta I_{load,max}$ ($\because ps\ FoM \propto \Delta V_{out}/\Delta I_{load,max}^2$)
- Using a large output capacitor and proportionally increasing $\Delta I_{load,max}$ improves ps FoM in a same design
- Note $\Delta I_{load,max}$, not $I_{load,max}$
- Ideal to compare designs having similar V_{in}, t_{edge}, and $\Delta I_{load,max}$

pF Figure of Merit (pF-FoM)

$$pF\ FoM = I_q \underbrace{\left(\frac{\Delta V_{out}}{\Delta I_{load,\ max} \cdot V_{out}} \right)}_{\text{Normalized voltage droop}} C_{out}$$

- Alternative FoM for dynamic load regulation performance
- *How small the voltage droop is at the power (I_q) and area cost (C_{out})*
- Smaller is better
- pF FoM works better to compare LDOs with different $\Delta I_{load,max}$
- Should use it for designs having similar V_{in} and t_{edge}

[Kim-JSSC17]

Maximum Load Current ($I_{load,max}$)

$$Power\ FET\ unit\ current\ = I_u$$

If power FETs are sized in the power of 2

$$Maximum\ load\ current\ (I_{load\_max}) = \sum_{i=0}^{N_{DAC}-1} 2^i \cdot I_u$$

DAC Number of Bits (N_{DAC})

$$Power\ FET\ unit\ current\ = I_u$$

If power FETs are sized in the power of 2

$$Maximum\ load\ current\ (I_{load,\ max}) = \sum_{i=0}^{N_{DAC}-1} 2^i \cdot I_u$$

$$I_{load,\ max} = I_u \cdot (2^{N_{DAC}} - 1) \quad \Rightarrow \quad N_{DAC} = \log_2\left(\frac{I_{load,\ max}}{I_u} + 1\right)$$

DAC Step Size ($V_{DAC,SS}$)

$$Power\ FET\ unit\ current\ = I_u$$

If power FETs are sized in the power of 2

$$Maximum\ load\ current\ (I_{load,\ max}) = \sum_{i=0}^{N_{DAC}-1} 2^i \cdot I_u$$

$$I_{load,\ max} = I_u \cdot (2^{N_{DAC}} - 1) \quad \Rightarrow \quad N_{DAC} = \log_2\left(\frac{I_{load,\ max}}{I_u} + 1\right)$$

Output voltage resolution (worst-case) ---> $V_{DAC,\ SS} = I_u \cdot R_{load,max}$

Minimum Load Current ($I_{load,min}$)

$$Power\ FET\ unit\ current\ = I_u$$

If power FETs are sized in the power of 2

$$Maximum\ load\ current\ (I_{load,max}) = \sum_{i=0}^{N_{DAC}-1} 2^i \cdot I_u$$

$$I_{load,max} = I_u \cdot (2^{N_{DAC}} - 1) \quad \Rightarrow \quad N_{DAC} = \log_2\left(\frac{I_{load,max}}{I_u} + 1\right)$$

Output voltage resolution (worst-case) --->

$$V_{DAC,SS} = I_u \cdot R_{load,max} = I_u \cdot \frac{V_{out}}{I_{load,min}} = I_u \cdot \frac{V_{out}}{1/r \cdot I_u} = r \cdot V_{out}$$

r=0.01 if targeting $V_{DAC,SS}$=1% of V_{out}

Minimum Load Current ($I_{load,min}$)

$$Power\ FET\ unit\ current\ = I_u$$

If power FETs are sized in the power of 2

$$Maximum\ load\ current\ (I_{load,max}) = \sum_{i=0}^{N_{DAC}-1} 2^i \cdot I_u$$

$$I_{load,max} = I_u \cdot (2^{N_{DAC}} - 1) \Rightarrow N_{DAC} = \log_2\left(\frac{I_{load,max}}{I_u} + 1\right)$$

Output voltage resolution (worst-case) ⇢

$$V_{DAC,SS} = I_u \cdot R_{load,max}$$

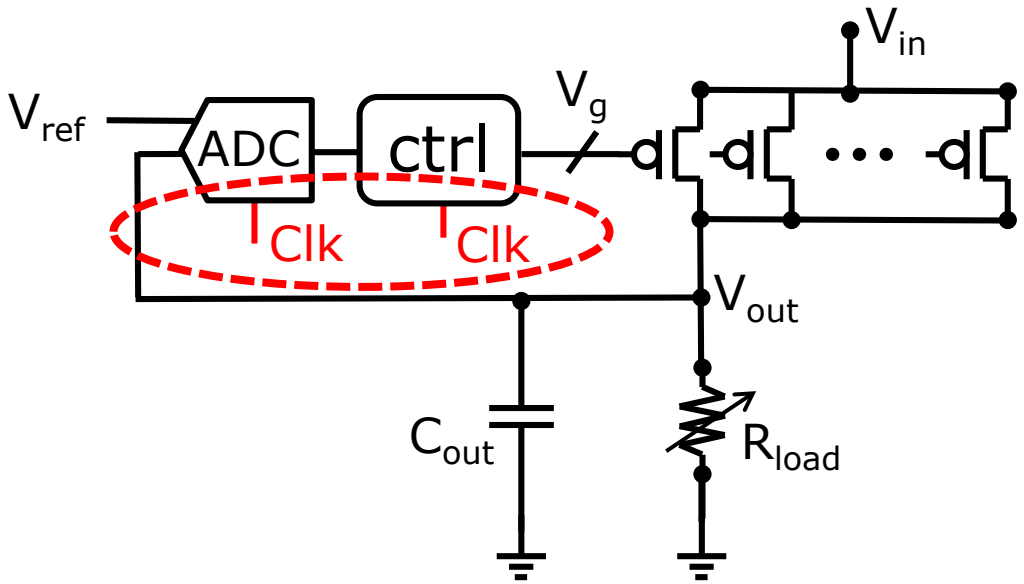
$$= I_u \cdot \frac{V_{out}}{I_{load,min}} = I_u \cdot \frac{V_{out}}{1/r \cdot I_u} = r \cdot V_{out}$$

r=0.01 if targeting $V_{DAC,SS}$=1% of V_{out}

$$I_{load,min} = I_u \cdot \frac{V_{out}}{V_{DAC,SS}} = I_u \cdot \frac{V_{out}}{r \cdot V_{out}} = \frac{I_u}{r} \gg I_u$$

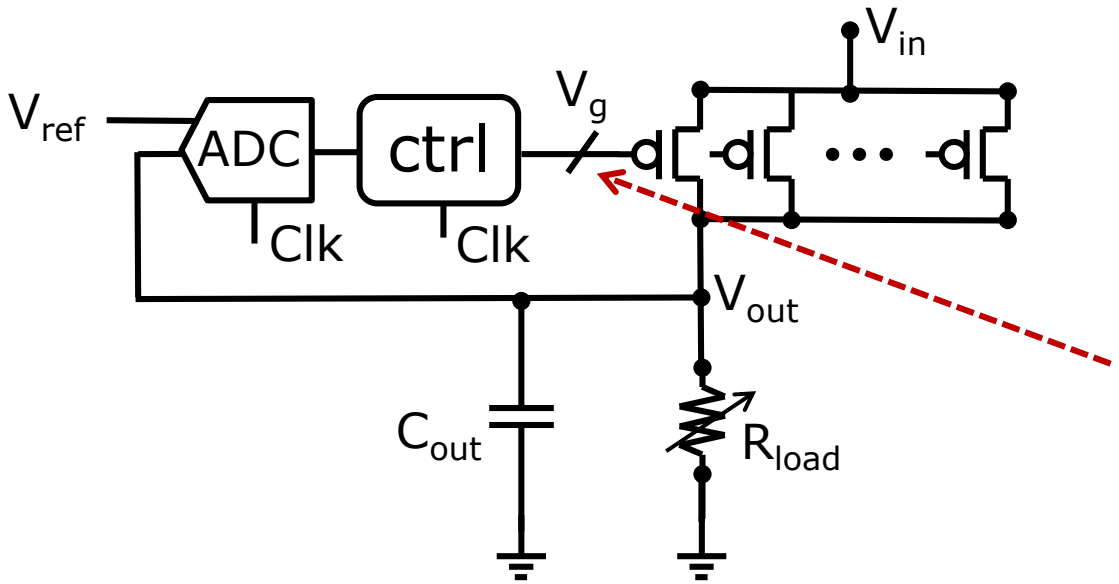
e.g., $I_{load,min}$=100·I_u for r=0.01

Clock Frequency (f_{clk})



- Clock for a synchronous ADC and a controller
- High clock frequency (f_{clk}) improves $t_{response}$, t_{settle}, V_{droop}, and $V_{overshoot}$
- High f_{clk} increases I_q, thus degrading CE

Output Ripple Size (V_{ripple})



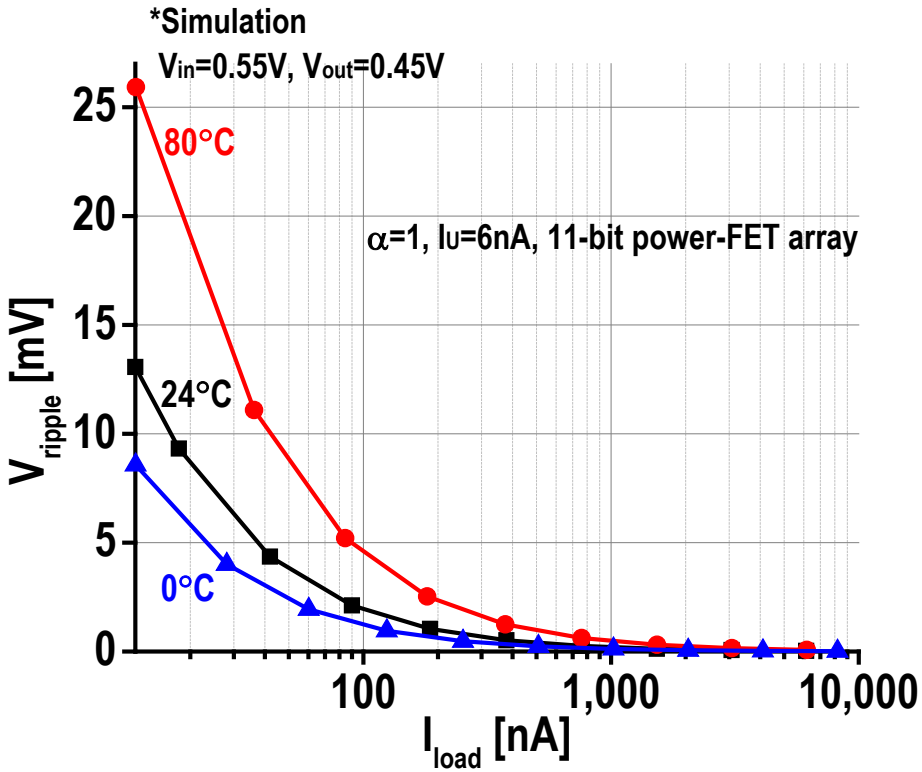
The controller output alternates between two codes with 1 LSB difference

$$V_{ripple} \cong \alpha \cdot I_u \cdot R_{load}\,,\, \text{where } \alpha = 1 \text{ for } f_{clk} \ll \frac{I_{load,min}}{V_{out} \cdot C_{out}}$$

- High f_{clk} increases V_{ripple}
- Because a controller makes a correction before the previous correction is fully applied on a load [Nasir-TPE16]

Output Ripple Size (V_{ripple})

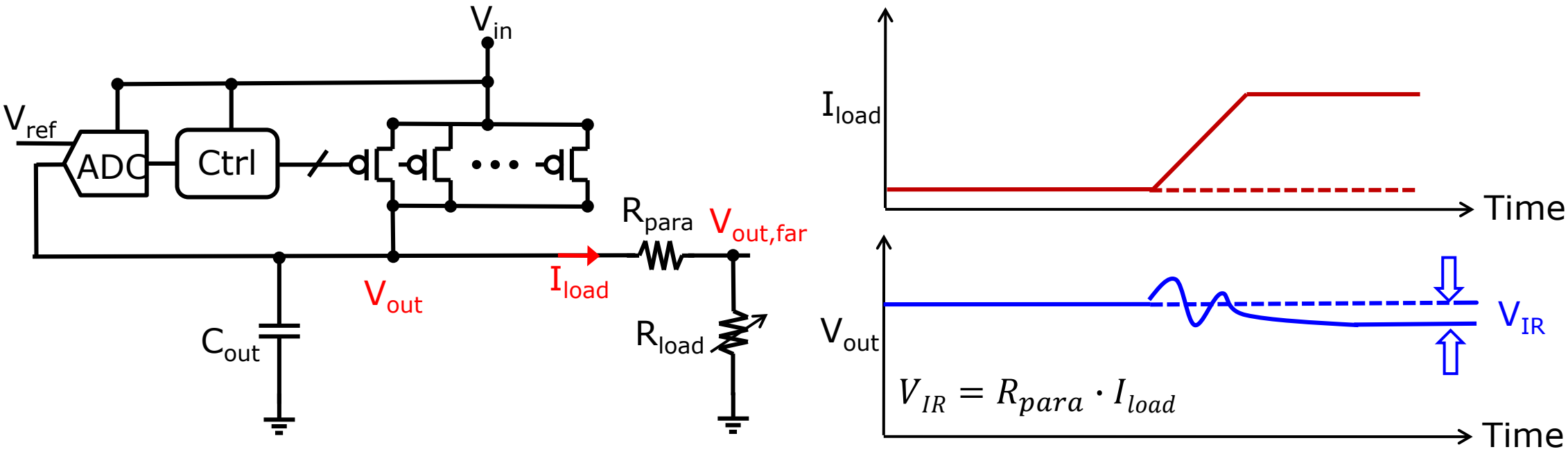
$$V_{ripple} \cong \alpha \cdot I_u \cdot R_{load}, \text{ where } \alpha = 1 \text{ for } f_{clk} \ll \frac{I_{load,min}}{V_{out} \cdot C_{out}}$$



Source: S.J. Kim (Columbia)

- V_{ripple} is also a function of
  - temperature &
  - I_{load}
- Worst-case V_{ripple} @ $I_{load,min}$ and high temperature

IR Drop (V_{IR})



- Parasitic resistance (R_{para}) can make $V_{out} \neq V_{out,far}$
- *The ADC senses V_{out}, not $V_{out,far}$*
- This deviation, V_{IR}, grows with I_{load}

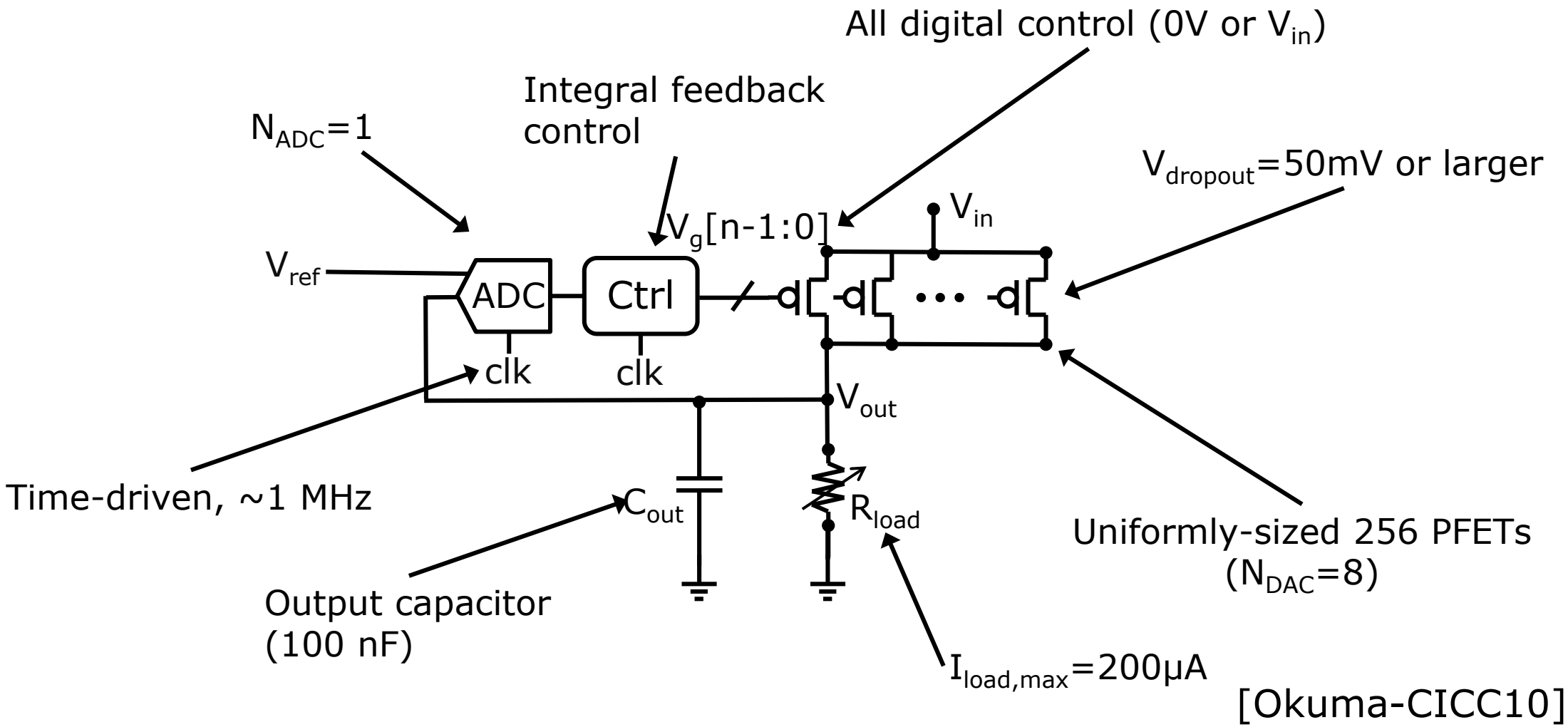
Outline

- Motivation
- Digital vs. Analog LDOs
- Key Specifications
- **Interim Q/A**
- State-of-the-Art Digital LDO Architectures
- Stability Analysis
- Concluding Remarks

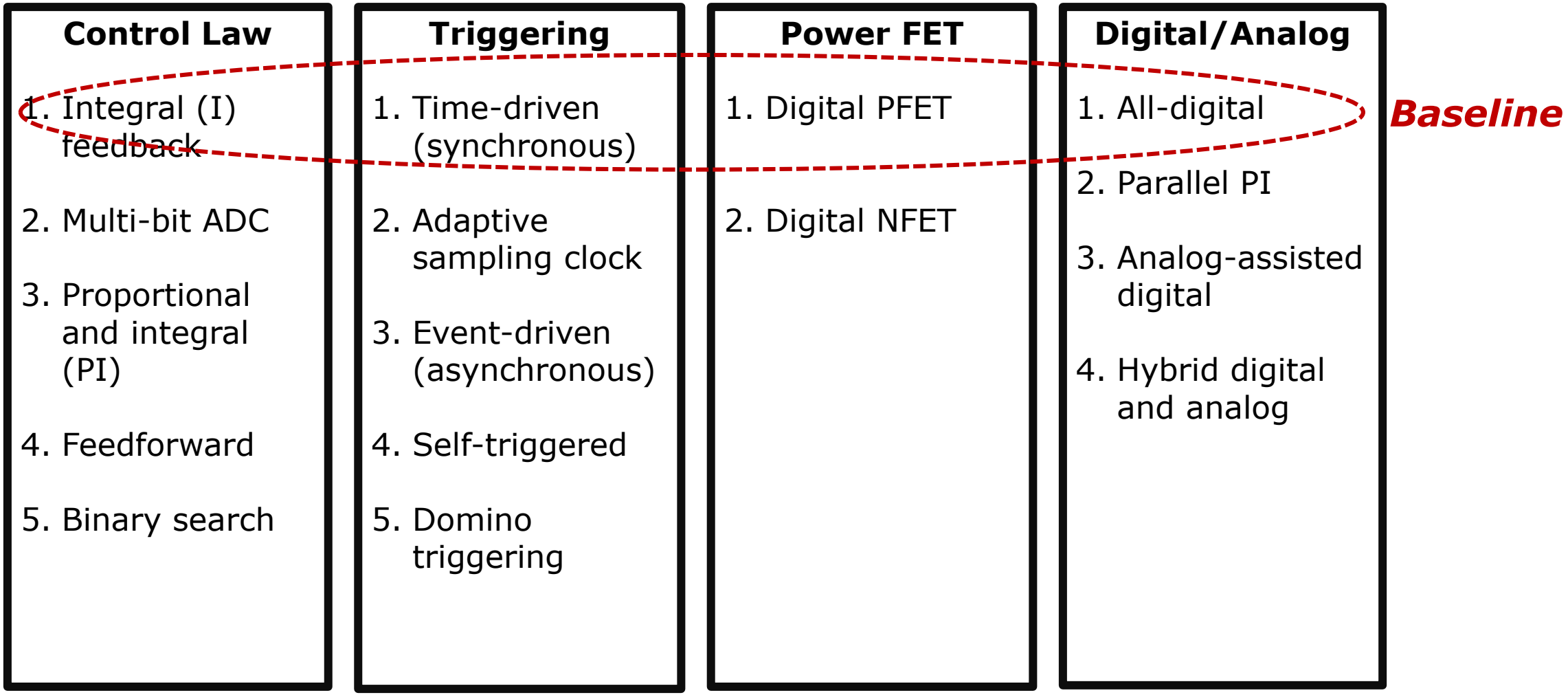
Outline

- Motivation
- Digital vs. Analog LDOs
- Key Specifications
- Interim Q/A
- **State-of-the-Art Digital LDO Architectures**
- Stability Analysis
- Concluding Remarks

Baseline Digital LDO Architecture



Overview



Overview

Control Law

1. Integral (I) feedback
2. Multi-bit ADC
3. Proportional and integral (PI)
4. Feedforward
5. Binary search

Triggering

1. Time-driven (synchronous)
2. Adaptive sampling clock
3. Event-driven (asynchronous)
4. Self-triggered
5. Domino triggering

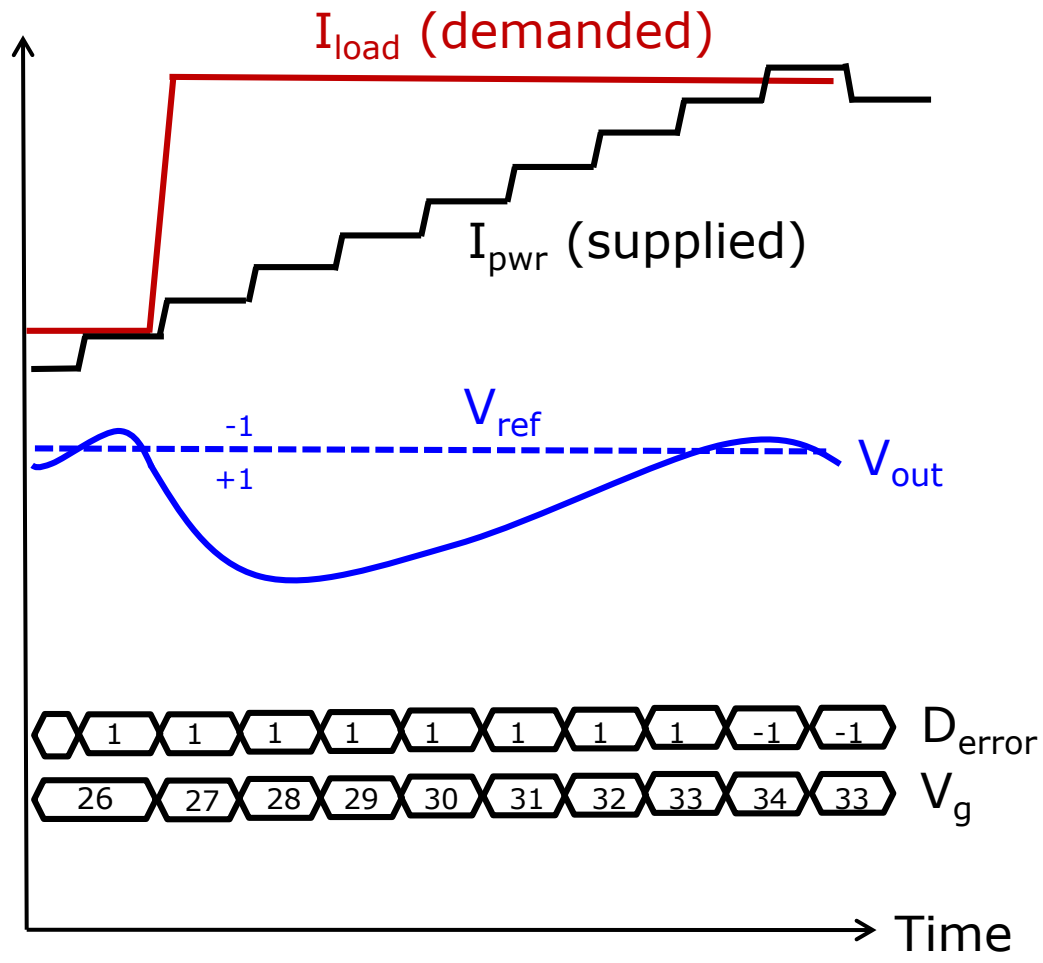
Power FET

1. Digital PFET
2. Digital NFET

Digital/Analog

1. All-digital
2. Parallel PI
3. Analog-assisted digital
4. Hybrid digital and analog

Integral Control

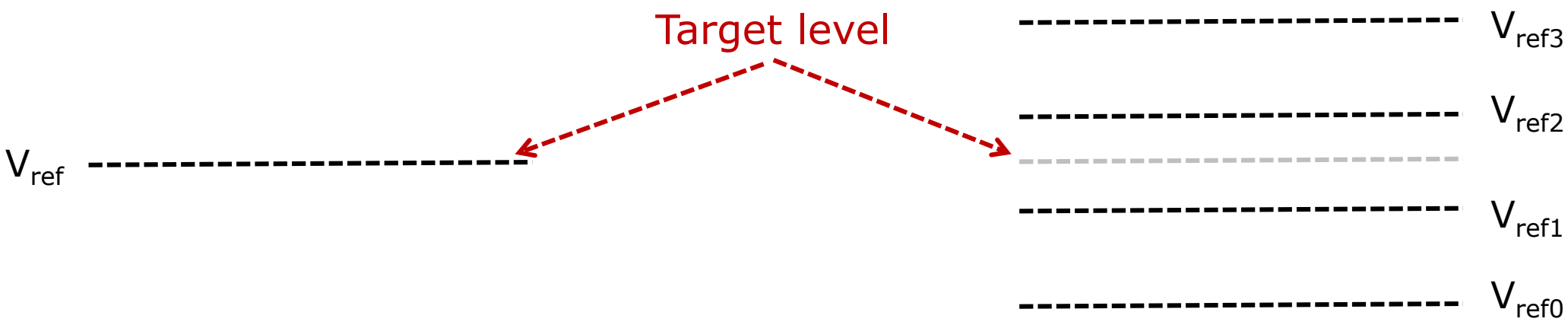


$$V_g[k] = i[k]$$
$$i[k] = i[k-1] + err[k] \cdot K_I$$

- i[k] = integration result
- err[k] = +1 or -1
- K_I = integral gain
- K_I = 1 for small $V_{DAC,SS}$
- Worst-case $t_{settle} = {}^{1}/_{f_{clk}} \cdot 2^{N_{DAC}}$

Multi-bit ADC

ADC number of bits: $N_{ADC} = \log_2(No.quantization\ level + 1)$



$N_{ADC} = \log_2(1+1) = 2\ bit$

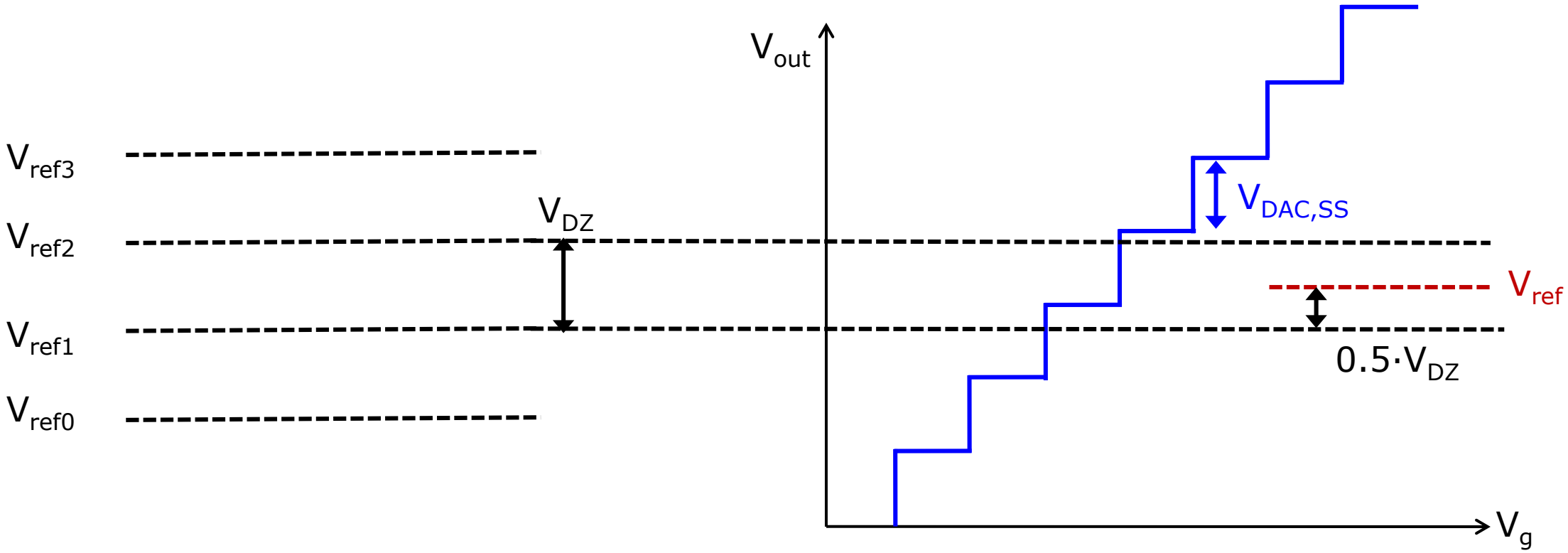
$N_{ADC} = \log_2(4+1) = 2.32\ bit$

- Most common

[Kim-JSSC17]

- For high-performance control
- V_{ref} is between V_{ref1} and V_{ref2}
- Non-uniform quantization is common
- More silicon, power, and references

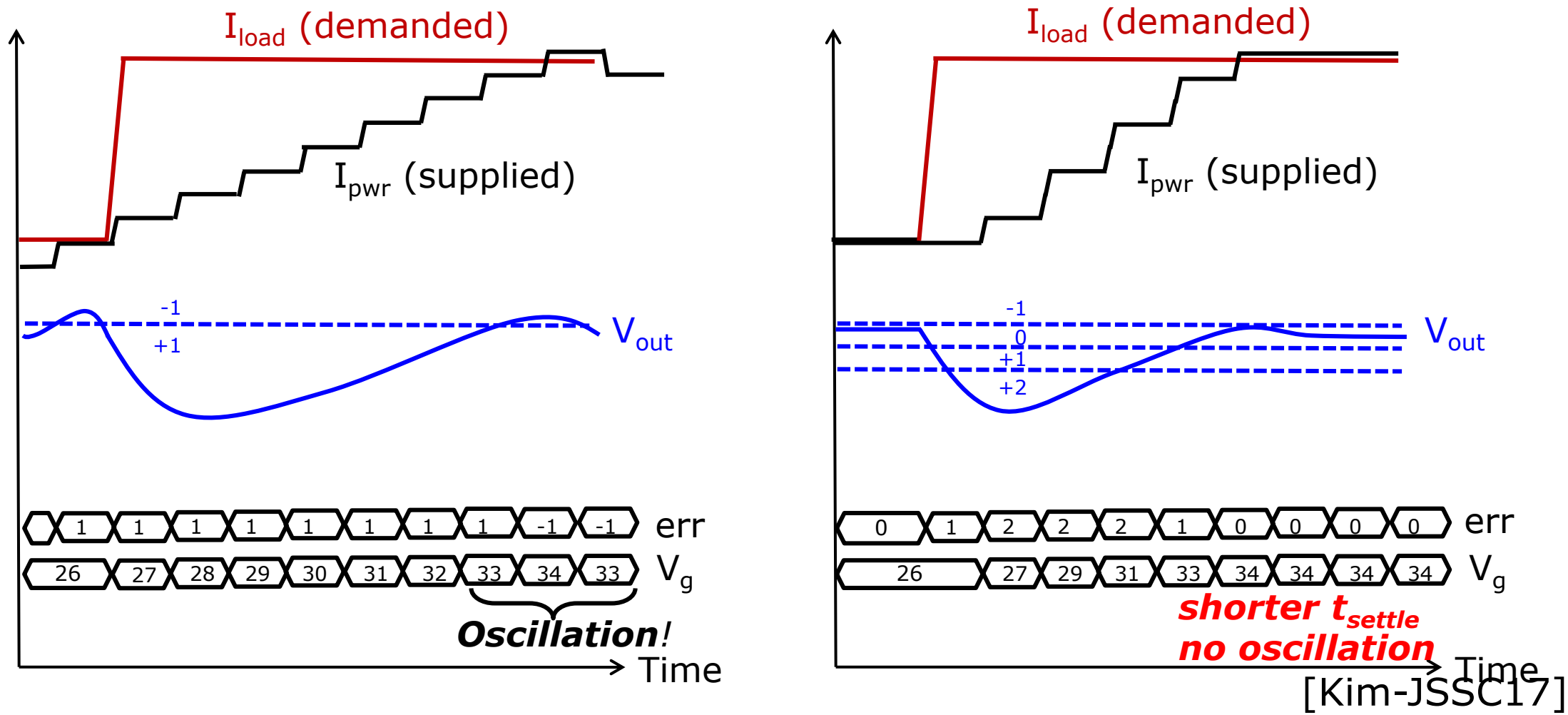
Multi-bit ADC with Deadzone



- Deadzone (V_{DZ}): a voltage range where a controller doesn't update its output
- No ripple if $0.5 \cdot V_{DAC,SS} < 0.5 \cdot V_{DZ}$ ($V_{DAC,SS}$: DAC step size)

[Kim-JSSC17]

Multi-bit ADC-based Integral Control



[Kim-JSSC17]

Proportional-Integral (PI) Control

$$Integral\ Output, i[k] = i[k-1] + K_I \cdot err[k]$$

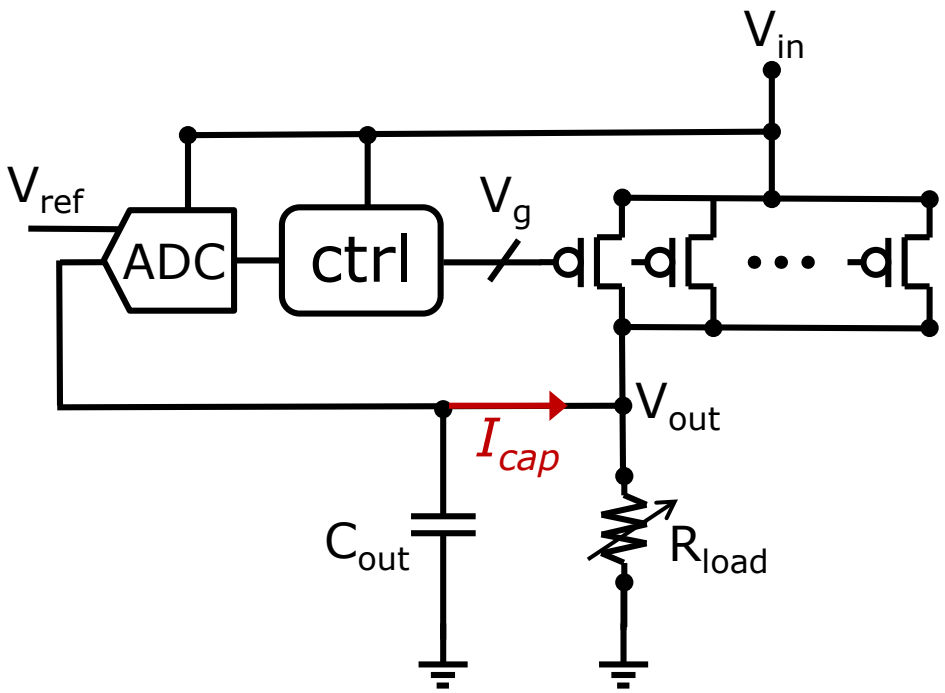
$$Proportional\ Ouptut, p[k] = K_P \cdot err[k]$$

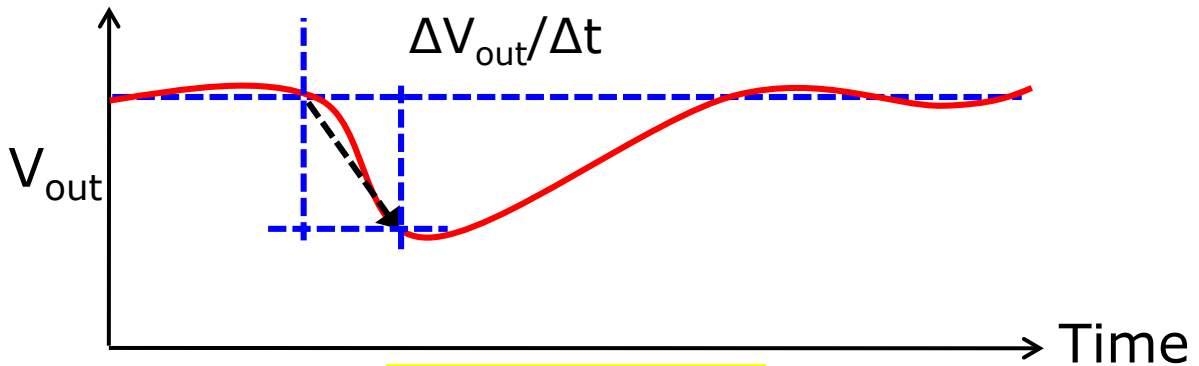
$$Controller\ Output, V_g[k] = i[k] + p[k]$$

- p[k] = instantaneous error-gain product (aka proportional control output)
- K_P set > 1 since it does not affect the DC error (i.e., err[k]=0 → p[k]=0)
- Increasing K_P:
  - V_{droop} and $t_{response}$ improvement
  - Stability degradation

[Kim-JSSC17]

Feedforward Control (aka Initialization)





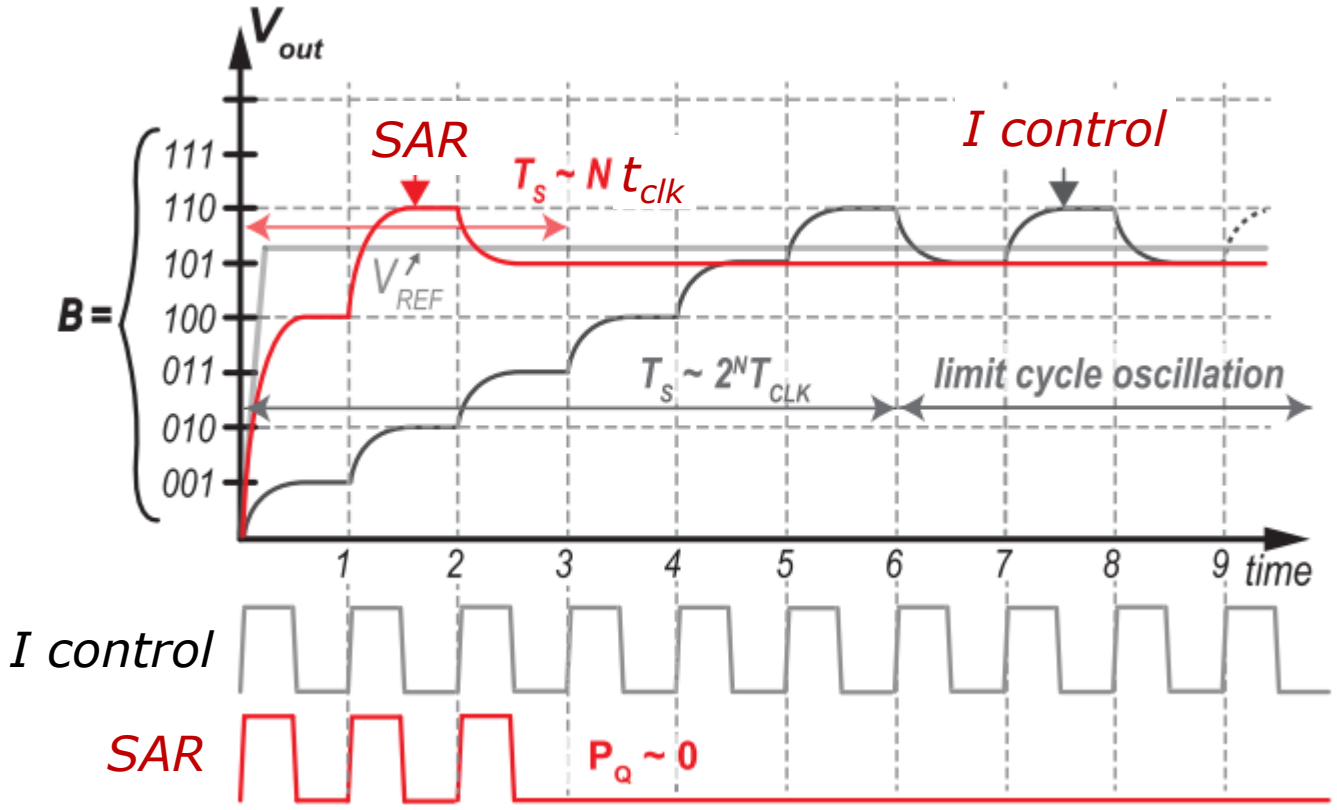
$$I_{cap} = C \cdot \frac{\Delta V_{out}}{\Delta t}$$

$$V_g[k] = i[k] + ff[k]$$

$$ff[k] = LUT\left(\frac{\Delta V_{out}}{\Delta t}\right)$$

- Predict the needed amount of additional current (I_{cap}) by measuring V_{out} slope
- ff[k] = the output term of feedforward control
- LUT = look-up table, to avoid multiplication and division [Kim-VLSI18]

Binary-Search Control



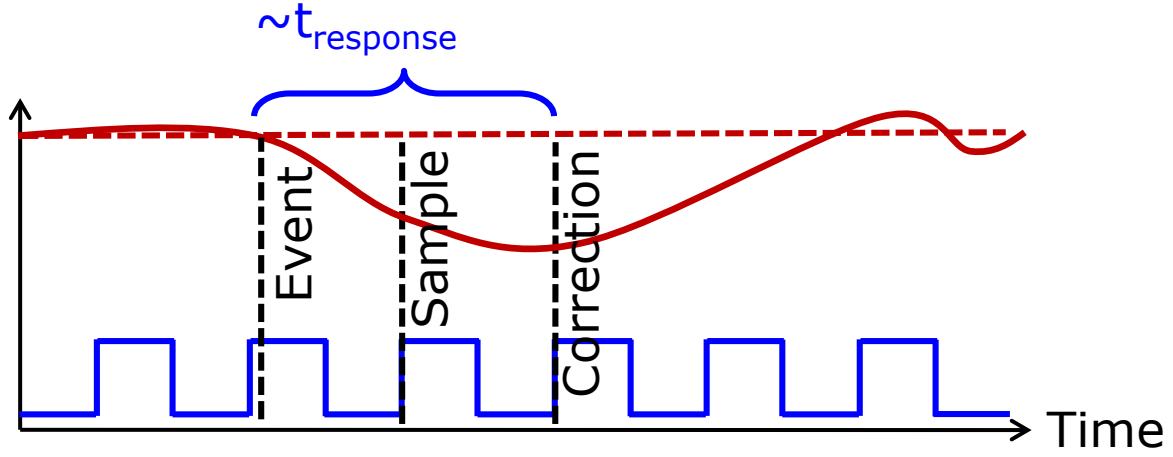
- Perform binary search
- Proportional-derivative (PD) control is proposed to mitigate V_{out} *spikes* during search
- $t_{settle} = \sim N_{DAC} \cdot t_{clk}$
- t_{clk}: clock period

[Salem-JSSC18]

Overview

Control Law	Triggering	Power FET	Digital/Analog
1. Integral (I) feedback	1. Time-driven (synchronous)	1. Digital PFET	1. All-digital
2. Multi-bit ADC	2. Adaptive sampling clock	2. Digital NFET	2. Parallel PI
3. Proportional and integral (PI)	3. Event-driven (asynchronous)		3. Analog-assisted digital
4. Feedforward	4. Self-triggered		4. Hybrid digital and analog
5. Binary search	5. Domino triggering		

Synchronous, aka Time-Driven (TD)



- The worst-case response time ($t_{response}$) is ~2 clock cycle
  - One cycle to wait for the next sampling edge
  - One cycle to calculate and update V_g
- F_s = 1 MHz → $t_{response}$ = 2 μs

Adaptive LDO Sampling Clock

$$V_{ripple} \cong \alpha \cdot I_u \cdot R_{load}\text{,, where } \alpha = 1 \text{ for } f_{clk} \ll \frac{I_{load,min}}{V_{out} \cdot C_{out}}$$

$$if\ I_{load} = I_{load,max}, then\ f_{clk}\ can\ be\ large$$

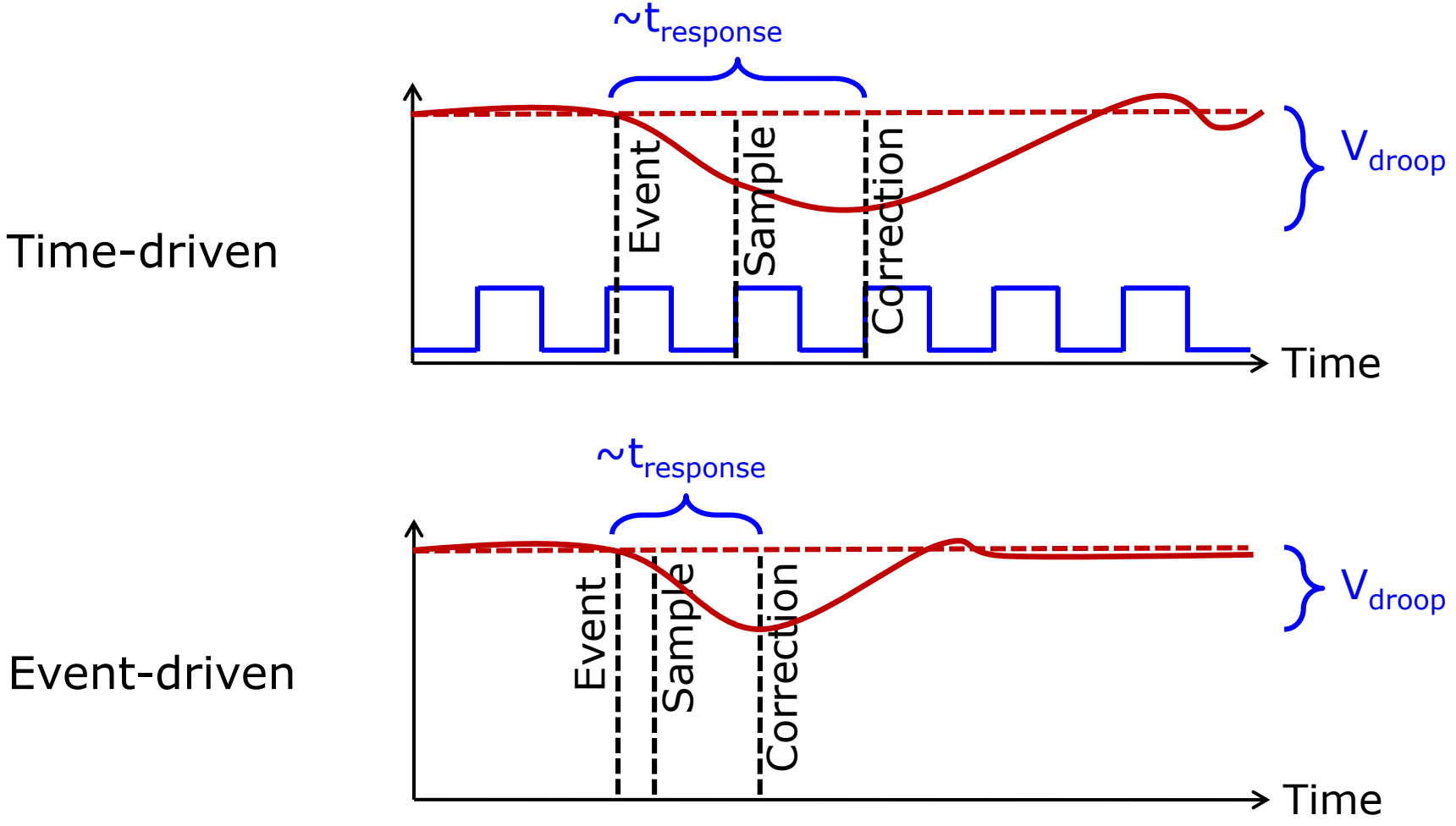
$$if\ I_{load} = I_{load,min}, then\ f_{clk}\ should\ be\ small$$

Adaptively change f_{clk} based on the number of power FETs that are turned on

- Adaptively change f_{clk} based on the present I_{load} level

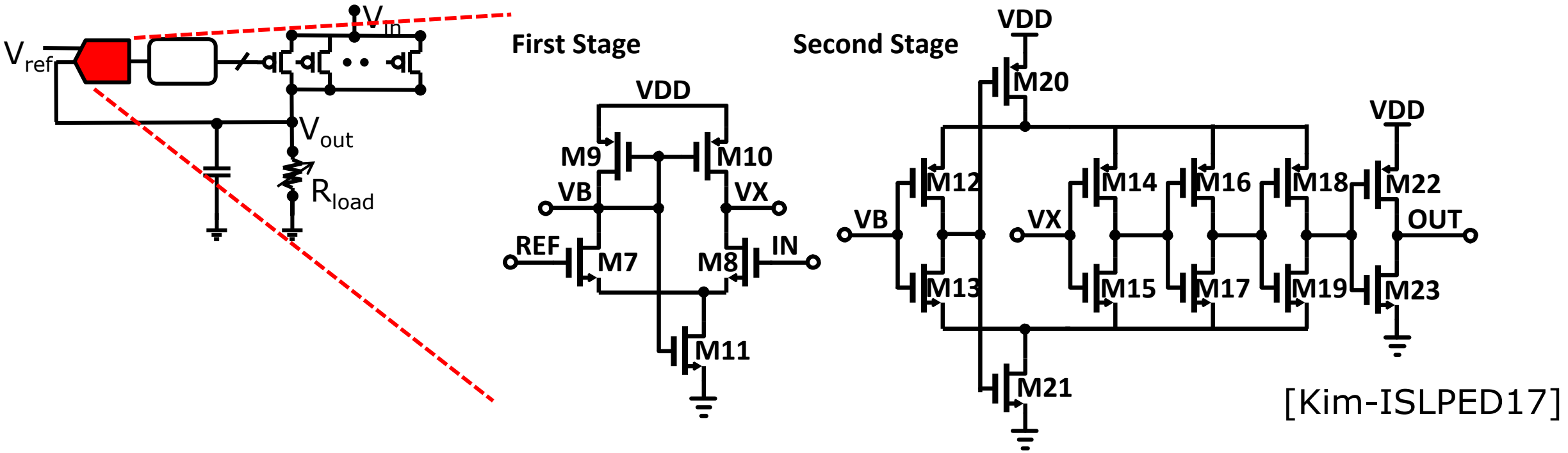
[Nasir-TPE16]

Asynchronous (a.k.a. Event-Driven)



[Kim-JSSC'17]

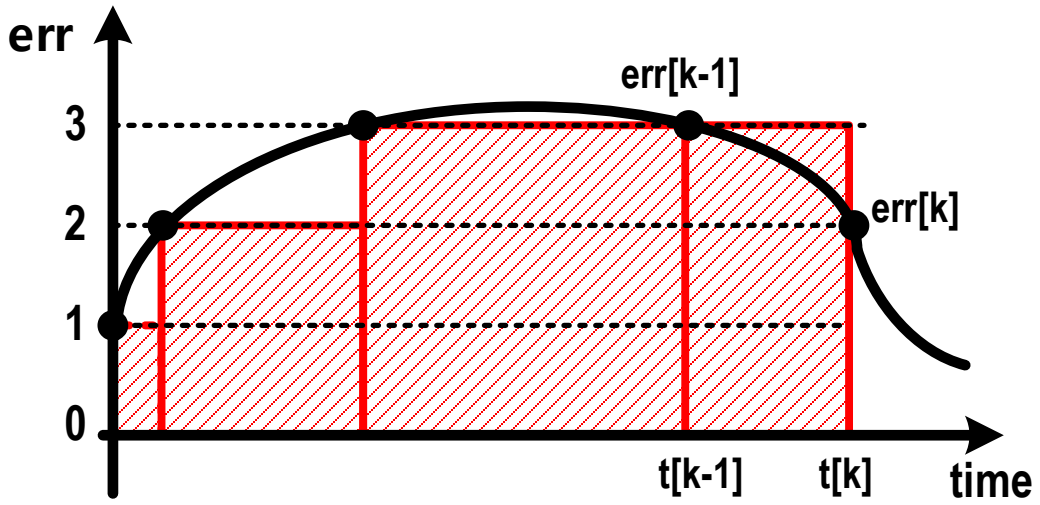
Asynchronous Comparator



[Kim-ISLPED17]

- Operating at low supply voltage
- Superior latency over synchronous (i.e., clocked) comparator
- Typically worse in the sampling rate and energy consumption per sampling

Integral Control in Event-Driven Triggering



Need a hardware multiplier

$$V_g[k] = i[k]$$
$$i[k] = i[k-1] + K_I \cdot err[k-1] \cdot (t[k] - t[k-1])$$

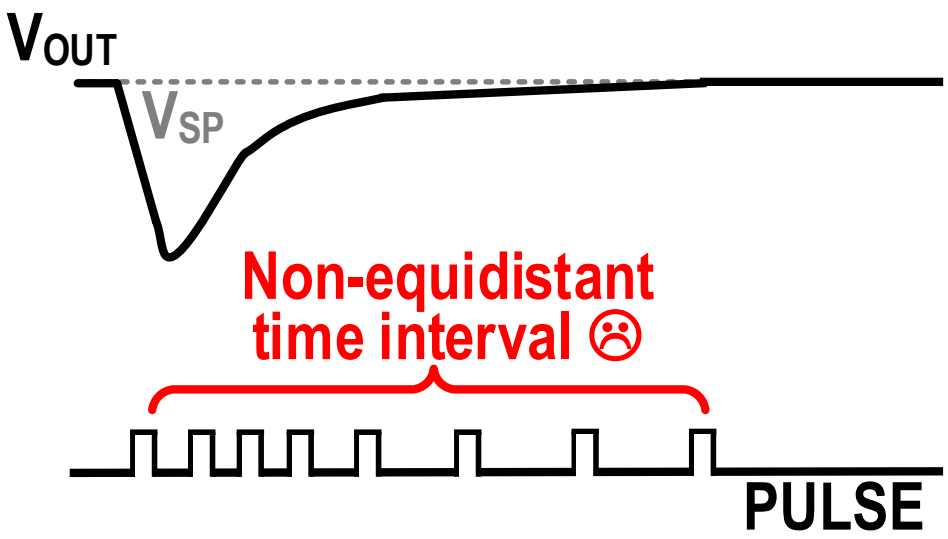
V_{ref}-V_{out}[k-1]

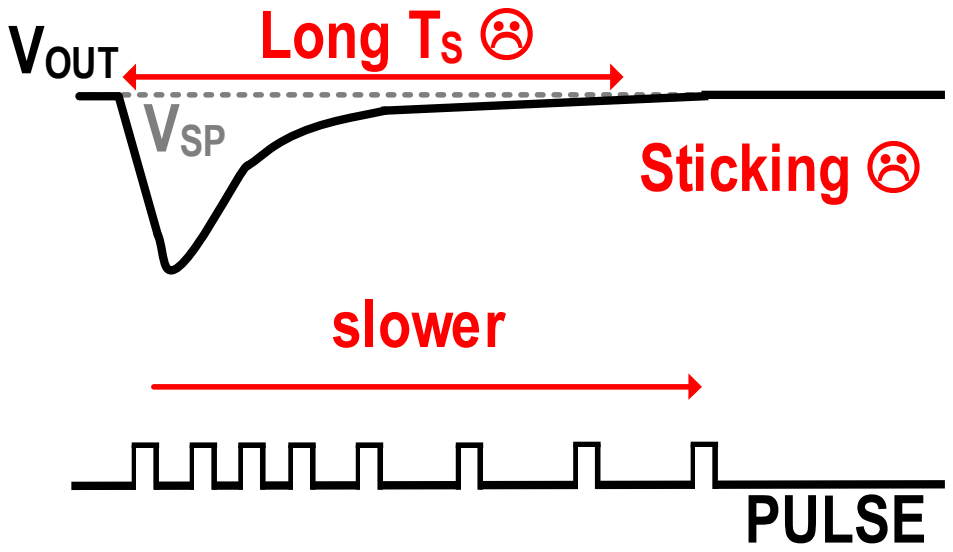
Time interval between two events

- Integration with non-uniform triggering requires time interval measurement
- Also, it requires a hardware multiplier

[Kim-JSSC17]

Challenges in Event-Driven Trigger

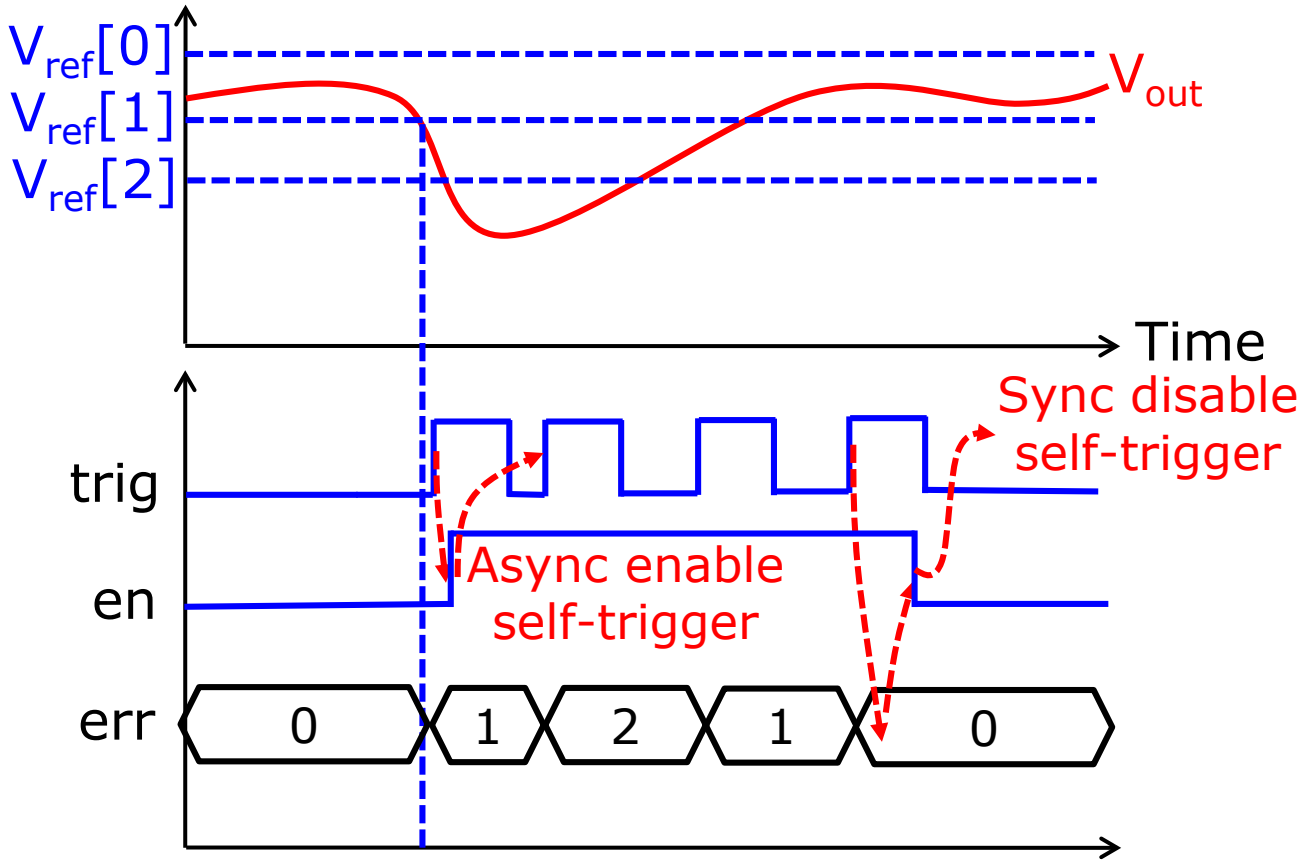




- Need to measure the time interval between two events
- Need to have a multiplier
- As V_{out} gets closer to V_{ref}, the event generation becomes slower
- Called a sticking problem. Bad for t_{settle}

[Kim-VLSI18]

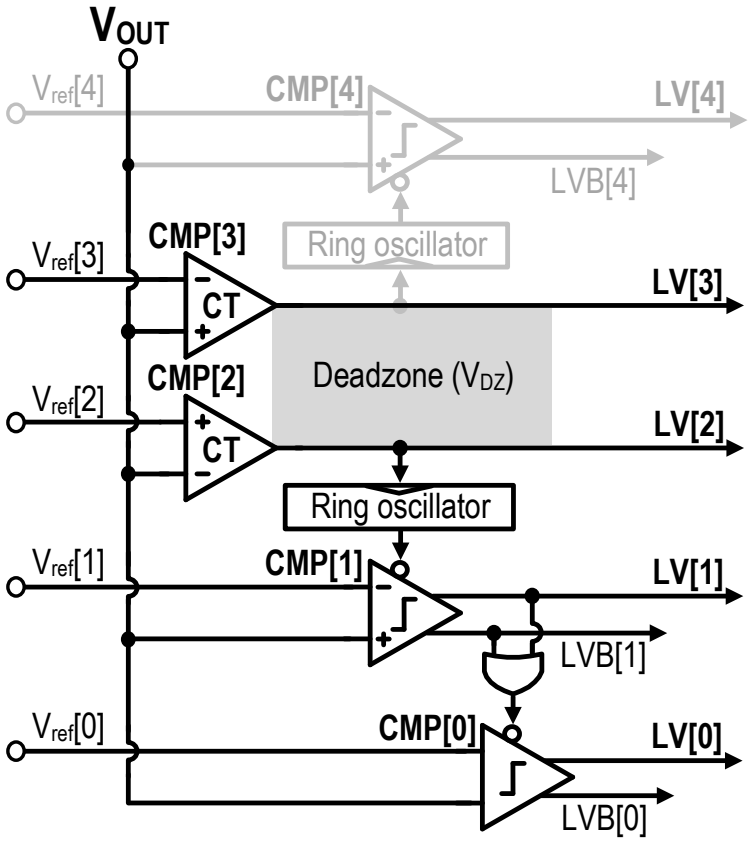
Self-Trigger

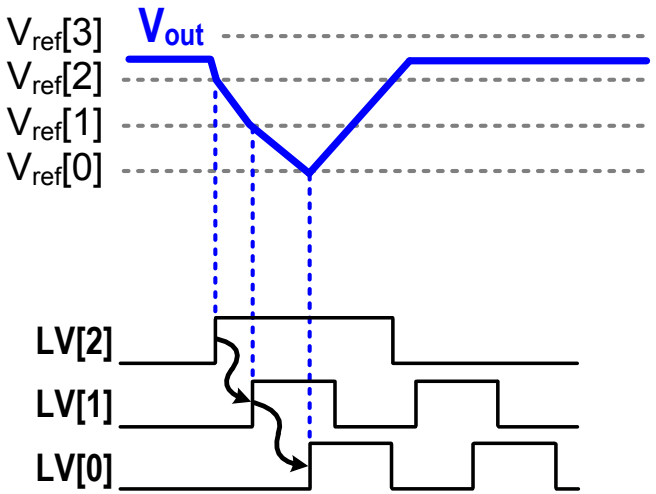


- Time measurement and multiplication are not needed
- No sticking problem → Improving t_{settle}

[Kim-VLSI18]

Domino Trigger



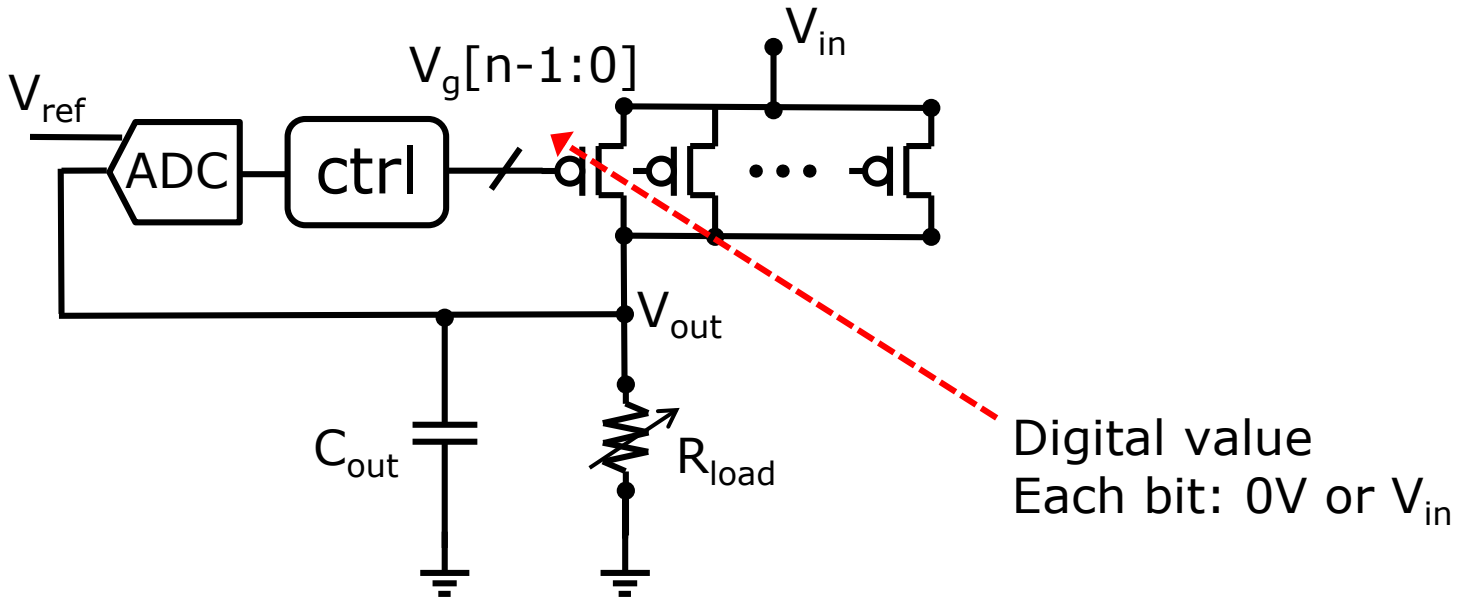


- A comparator output change triggers the next comparator
- Improve $t_{response}$ and V_{droop} [Kim-VLSI19]

Overview

Control Law	Triggering	Power FET	Digital/Analog
1. Integral (I) feedback	1. Time-driven (synchronous)	1. Digital PFET	1. All-digital
2. Multi-bit ADC	2. Adaptive sampling clock	2. Digital NFET	2. Parallel PI
3. Proportional and integral (PI)	3. Event-driven (asynchronous)		3. Analog-assisted digital
4. Feedforward	4. Self-triggered		4. Hybrid digital and analog
5. Binary search	5. Domino triggering		

Digital PFET



Linear region

$$I_{load} \propto (V_{in} - V_g - V_{th}) \cdot (V_{in} - V_{out})$$

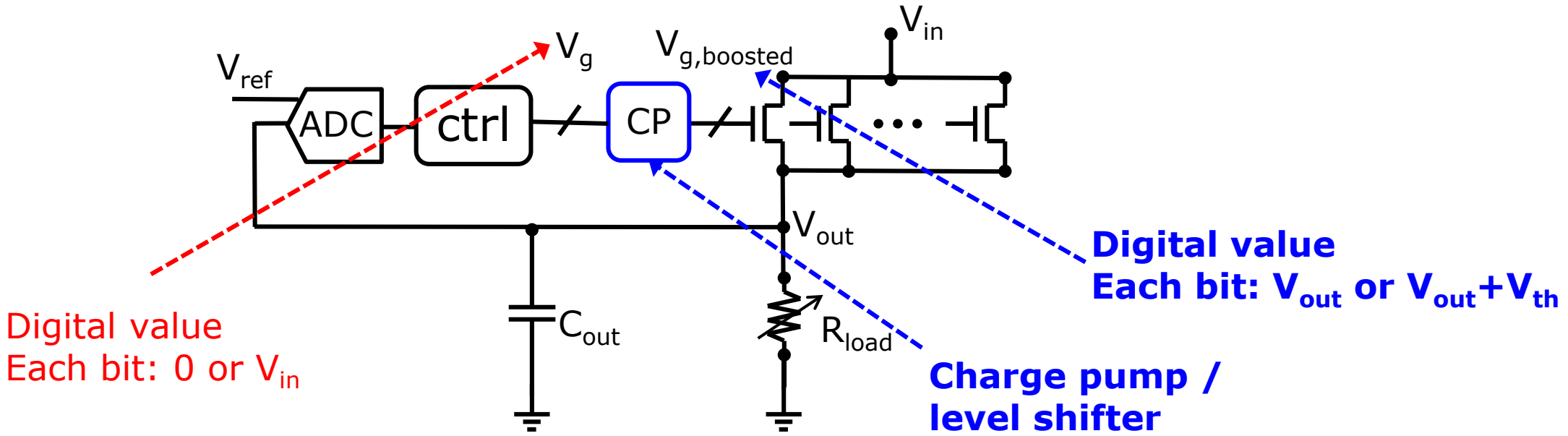
Poor PSRR
Small $V_{dropout}$

Saturation region

$$I_{load} \propto (V_{in} - V_g - V_{th})^{\alpha}$$

Poor PSRR
Large $V_{dropout}$

Digital NFET



Linear region

$$I_{load} \propto (V_{g,boosted} - V_{out} - V_{th}) \cdot (V_{in} - V_{out})$$

Poor PSRR
Small $V_{dropout}$

Saturation region

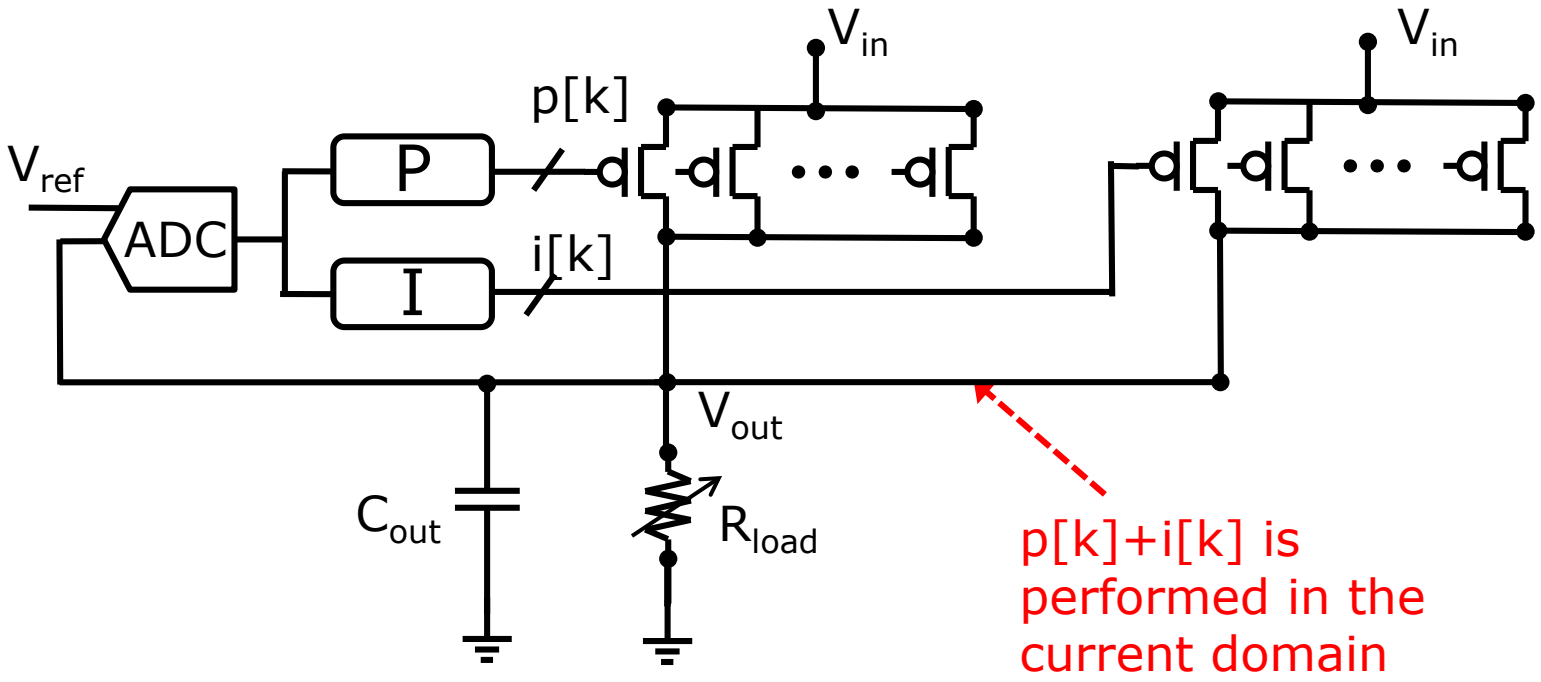
$$I_{load} \propto (V_{g,boosted} - V_{out} - V_{th})^{\alpha}$$

No V_{in}: Good PSRR
Large $V_{dropout}$

Overview

Control Law	Triggering	Power FET	Digital/Analog
1. Integral (I) feedback	1. Time-driven (synchronous)	1. Digital PFET	1. All-digital
2. Multi-bit ADC	2. Adaptive sampling clock	2. Digital NFET	2. Parallel PI
3. Proportional and integral (PI)	3. Event-driven (asynchronous)		3. Analog-assisted digital
4. Feedforward	4. Self-triggered		4. Hybrid digital and analog
5. Binary search	5. Domino triggering		

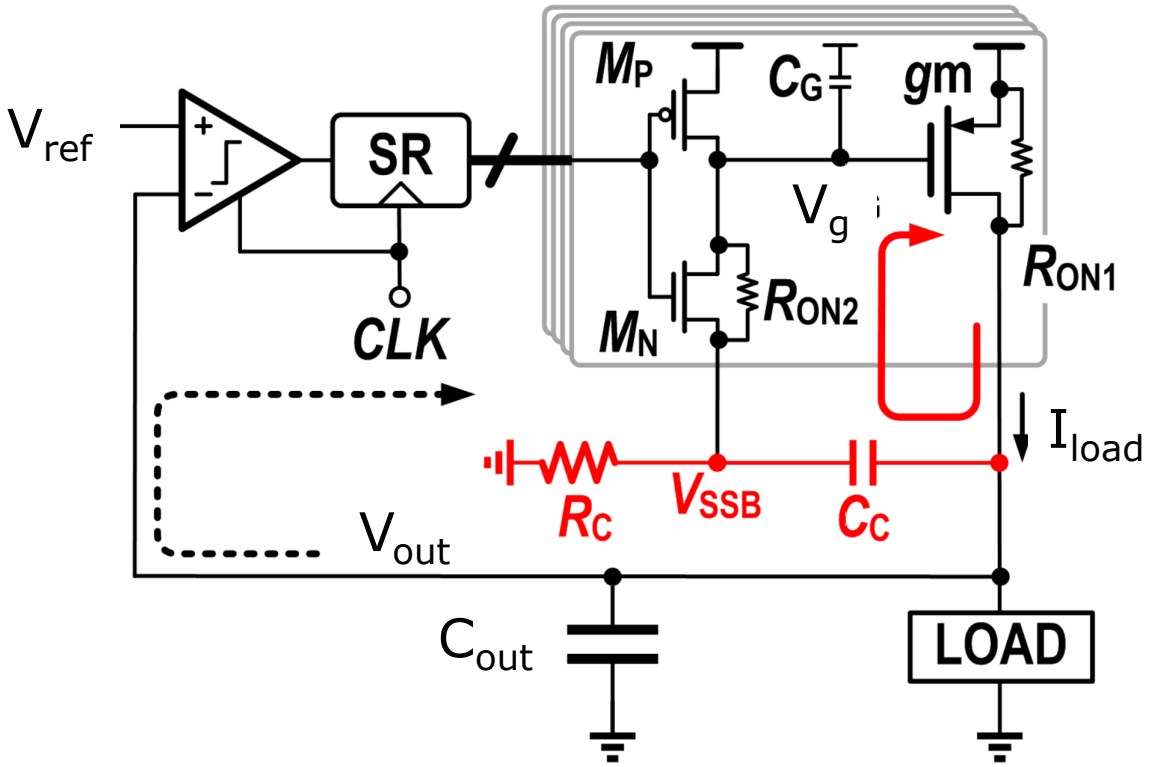
Parallel Proportional and Integral



- The output of P control is applied w/o waiting for I control
- Improve V_{droop} and $t_{response}$

[Kim-ISSCC17]

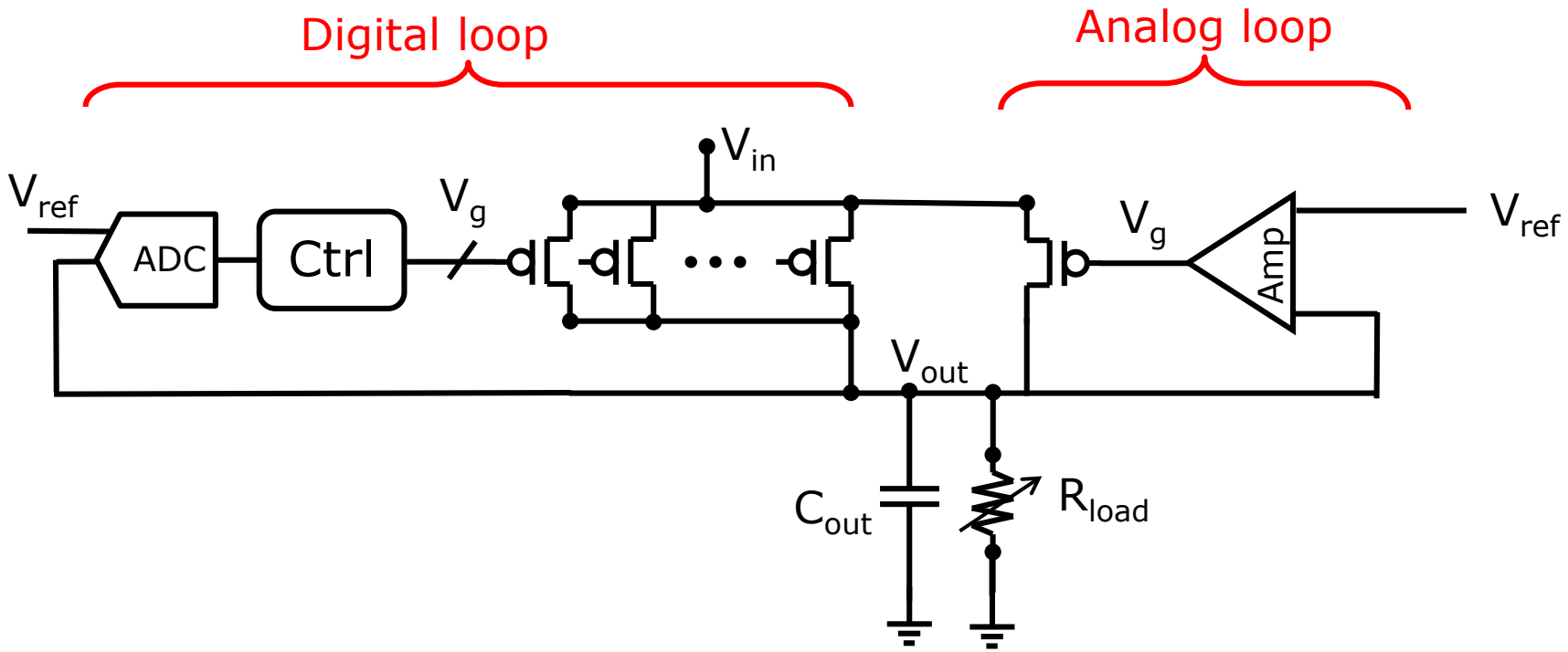
Analog-Assisted Digital



- Digital and analog loop
- ***Sharing*** the same power FETs
- V_{out} droops → V_{SSB} droops → V_G droops → power-FETs are more strongly turned on
- *Performance depends on the g_m of power-FETs*
- Weaker performance for low-to-high I_{load} transition

[Huang-JSSC18]

Hybrid Digital and Analog

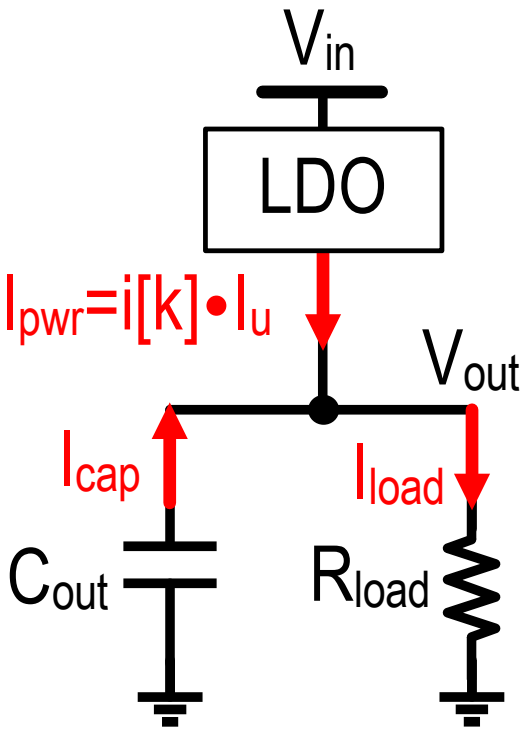


- ***Two sets*** of power-FETs
- Coordination between two loops is needed
- Example: i) recovery from a large droop: use digital loop; ii) fine-grained output control & steady state: use analog loop [Liu-ISSCC19]

Outline

- Motivation
- Digital vs. Analog LDOs
- Key Specifications
- Interim Q/A
- State-of-the-Art Digital LDO Architectures
- **Stability Analysis**
- Concluding Remarks

State Space Representation: Error State



Error state: $err[k] = V_{ref} - V_{out}[k]$

Output voltage: $V_{out}[k+1] = V_{out}[k] + I_{cap}[k] \cdot R_{load} \cdot (1 - e^{-T_s/(R_{load} \cdot C_{out})})$

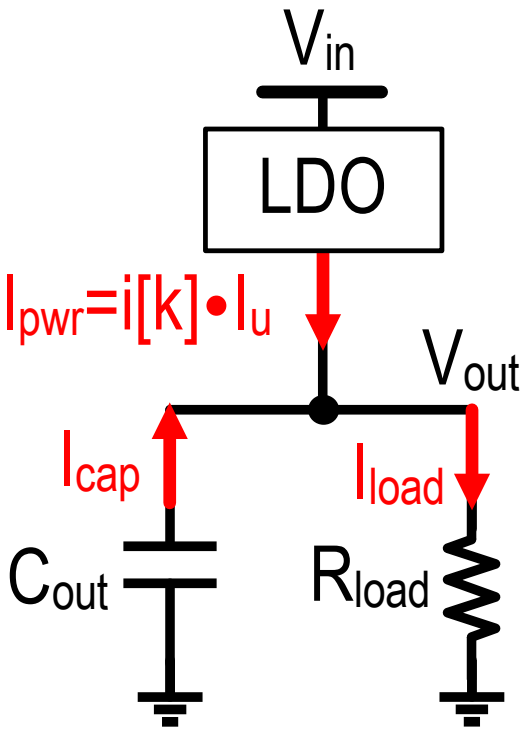
Let's define it as *A*

$$\therefore err[k+1] = V_{ref} - V_{out}[k+1]$$
$$= V_{ref} - V_{out}[k] - I_{cap}[k] \cdot A$$
$$= err[k] - (I_{pwr}[k] - I_{load}[k]) \cdot A$$

Time interval b/w two samples, i.e., $1/f_{clk}$

[Kim-JSSC17]

State Space Representation: Error State



Error state: $err[k] = V_{ref} - V_{out}[k]$

Let's define it as A

Output voltage: $V_{out}[k+1] = V_{out}[k] + I_{cap}[k] \cdot R_{load} \cdot (1 - e^{-T_s/(R_{load} \cdot C_{out})})$

Time interval b/w two samples, i.e., $1/f_{clk}$

$$\therefore err[k+1] = V_{ref} - V_{out}[k+1]$$
$$= V_{ref} - V_{out}[k] - I_{cap}[k] \cdot A$$
$$= err[k] - (I_{pwr}[k] - I_{load}[k]) \cdot A$$

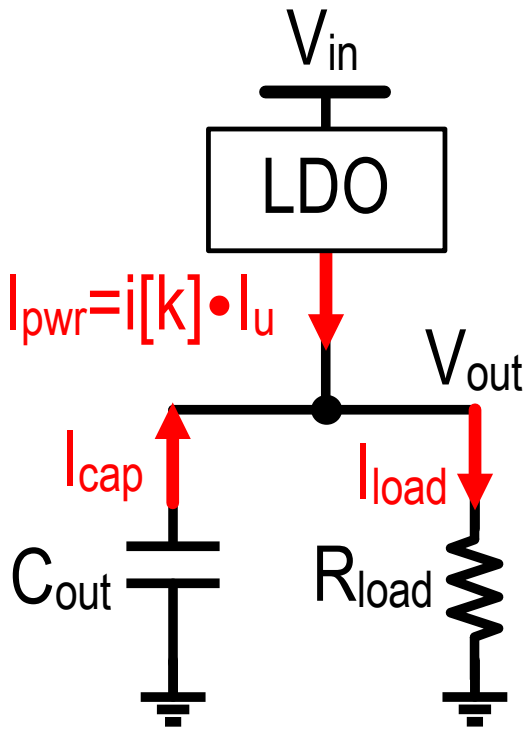
Power FET current: $I_{pwr}[k] = i[k] \cdot I_u$

Load current: $I_{load}[k] = \frac{V_{out}[k]}{R_{load}} = \frac{V_{ref} - err[k]}{R_{load}}$

$$\therefore err[k+1] = err[k] - \left(i[k] \cdot I_u - \frac{V_{ref} - err[k]}{R_{load}} \right) \cdot A$$
$$= \left(1 - \frac{1}{R_{load}} \cdot A \right) err[k] - (I_u \cdot A) i[k] + \frac{V_{ref}}{R_{load}} \cdot A$$

[Kim-JSSC17]

State Space Representation: Integral Control State



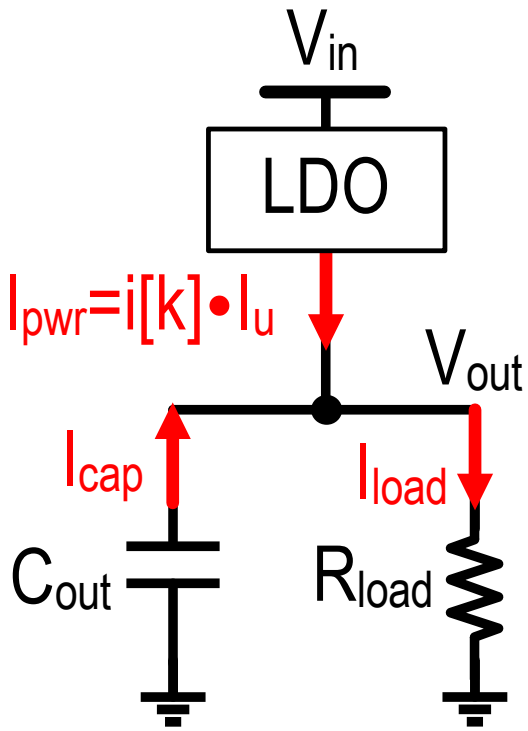
Error state equation: $err[k+1] = \left(1 - \frac{1}{R_{load}} \cdot A\right) err[k] - (I_u \cdot A) i[k] + \frac{V_{ref}}{R_{load}} \cdot A$

Integral control state equation: $i[k+1] = i[k] + K_i \cdot err[k]$

$$\begin{bmatrix} err[k+1] \\ i[k+1] \end{bmatrix} = \begin{bmatrix} 1 - \frac{1}{R_{load}} \cdot A & -I_u \cdot A \\ K_i & 1 \end{bmatrix} \begin{bmatrix} err[k] \\ i[k] \end{bmatrix} + \begin{bmatrix} \frac{V_{ref}}{R_{load}} \cdot A \\ 0 \end{bmatrix}$$

[Kim-JSSC17]

State Space Representation: Stability Condition



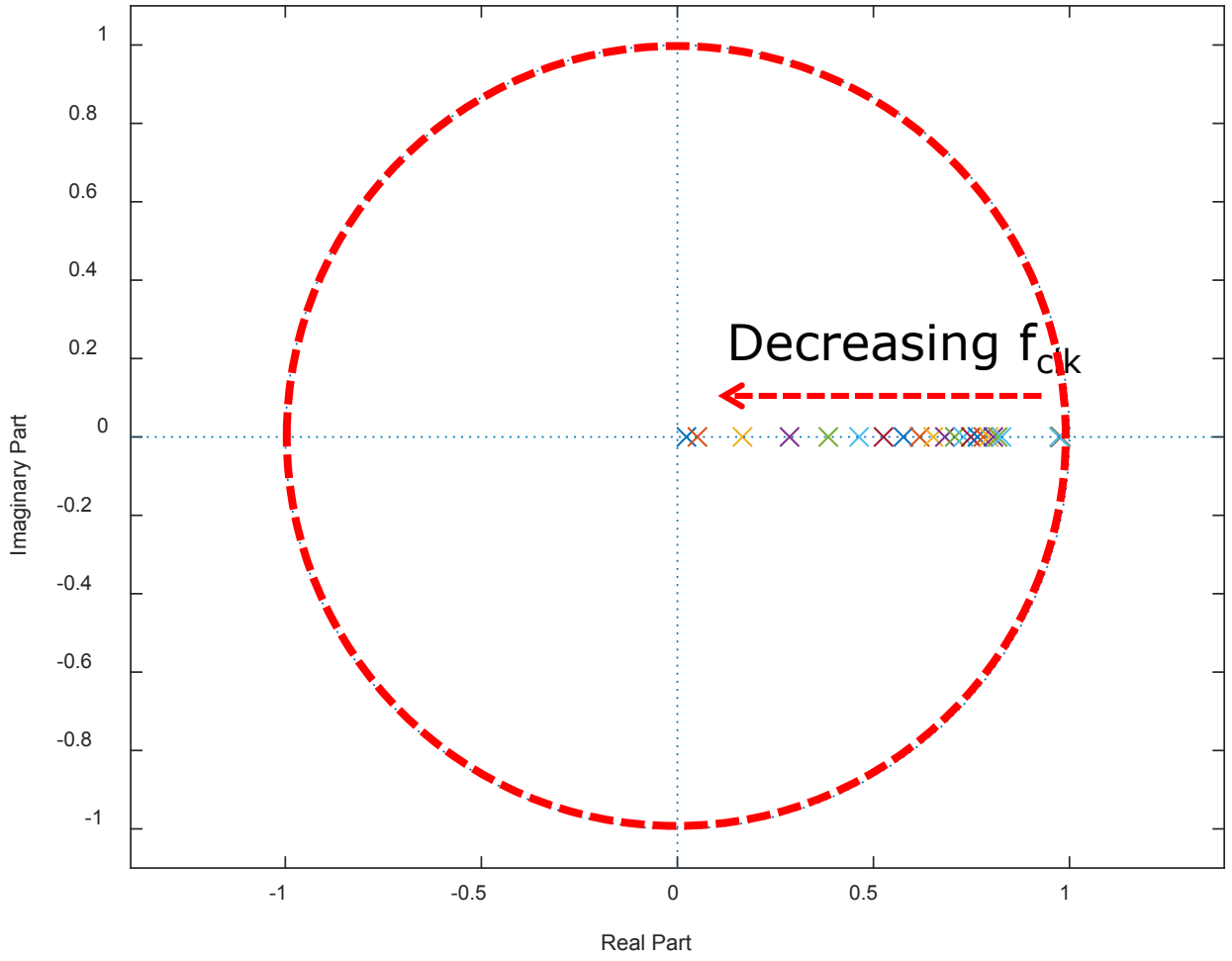
Error state equation: $err[k+1] = \left(1 - \frac{1}{R_{load}} \cdot A\right) err[k] - (I_u \cdot A) i[k] + \frac{V_{ref}}{R_{load}} \cdot A$

Integral control state equation: $i[k+1] = i[k] + K_i \cdot err[k]$

$$\begin{bmatrix} err[k+1] \\ i[k+1] \end{bmatrix} = \underbrace{\begin{bmatrix} 1 - \frac{1}{R_{load}} \cdot A & -I_u \cdot A \\ K_i & 1 \end{bmatrix}}_{\text{Stable if |eigenvalue| < 1}} \begin{bmatrix} err[k] \\ i[k] \end{bmatrix} + \begin{bmatrix} \frac{V_{ref}}{R_{load}} \cdot A \\ 0 \end{bmatrix}$$

[Kim-JSSC17]

State Space Representation: Results



Parameters:

V_{in}=500mV,
V_{ref}=450mV,
R_{load}=450Ω,
I_u=25uA,
C_{out}=100pF,
f_{clk}=1MHz~100MHz,
K_I=1

Outline

- Motivation
- Digital vs. Analog LDOs
- Key Specifications
- Interim Q/A
- State-of-the-Art Digital LDO Architectures
- Stability Analysis
- **Concluding Remarks**

Papers to See This Year

Session 25 Relevant Papers:

- 25.1: A Fully Synthesizable Distributed and Scalable All-Digital LDO in 10nm CMOS
- 25.2: A 480mA Output-Capacitor-Free Synthesizable Digital LDO Using CMP-Triggered Oscillator and Droop Detector with 99.99% Current Efficiency, 1.3ns Response Time and 9.8A/mm^2 Current Density
- 25.3: A 65nm Edge-Chasing Quantizer-Based Digital LDO Featuring 4.58ps-FoM and Side-Channel-Attack Resistance

Session 32 Relevant Papers:

- 32.4: A 0.4-to-1.2V 0.0057mm^2 55fs-Transient-FoM Ring-Amplifier-Based Low-Dropout Regulator with Replica-Based PSR Enhancement
- 32.5: A Scalable and PCB-Friendly Daisy-Chain Approach to Parallelize LDO Regulators with 2.613% Current-Sharing Accuracy Using Dynamic Element Matching for Integrated Current Sensing

Key References

Referred in the slides

- **[Kim-VLSI19]** Sung J. Kim, et al., "A 0.5-1V Input Event-Driven Multiple Digital Low-Dropout-Regulator System for Supporting a Large Digital Load," IEEE Symposium on VLSI Circuits (VLSI), 2019
- **[Hazucha-JSSC05]** Peter Hazucha, et al., "Area-efficient linear regulator with ultra-fast load regulation," IEEE Journal Solid-State Circuits (JSSC), vol. 40, no. 4, pp. 933–940, Apr. 2005
- **[Kim-JSSC17]** Doyun Kim, et al., "A Fully-Integrated Digital Low-Drop-Out Regulator based on Event-Driven Explicit-Time-Coding Architecture," IEEE Journal of Solid-State Circuits (JSSC), 2017
- **[Nasir-TPE16]** Saad B. Nasir, et al., "All-Digital Low-Dropout Regulator With Adaptive Control and Reduced Dynamic Stability for Digital Load Circuits," in IEEE Transactions on Power Electronics, vol. 31, no. 12, pp. 8293-8302, Dec. 2016.
- **[Okuma-CICC10]** Yasuyuki Okuma et al., "0.5-V input digital LDO with 98.7% current efficiency and 2.7-μA quiescent current in 65nm CMOS," IEEE Custom Integrated Circuits Conference 2010, San Jose, CA, 2010, pp. 1-4.
- **[Kim-VLSI18]** Doyun Kim, et al., "0.5V-VIN, 165-mA/mm2 Fully-Integrated Digital LDO based on Event-Driven Self-Triggering Control," IEEE Symposium on VLSI Circuits (VLSI), 2018
- **[Salem-JSSC18]** Loai G. Salem, et al., "A Successive Approximation Recursive Digital Low-Dropout Voltage Regulator With PD Compensation and Sub-LSB Duty Control," in IEEE Journal of Solid-State Circuits, vol. 53, no. 1, pp. 35-49, Jan. 2018.
- **[Kim-ISLPED17]** Sung J. Kim, et al., "Comparative Study and Optimization of Synchronous and Asynchronous Comparators at Near-threshold Voltages," ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2017
- **[Huang-JSSC18]** Mo Huang, et al., "An Analog-Assisted Tri-Loop Digital Low-Dropout Regulator," in IEEE Journal of Solid-State Circuits, vol. 53, no. 1, pp. 20-34, Jan. 2018.
- **[Liu-ISSCC19]** Xiaosen Liu et al., "14.7 A Modular Hybrid LDO with Fast Load-Transient Response and Programmable PSRR in 14nm CMOS Featuring Dynamic Clamp Tuning and Time-Constant Compensation," 2019 IEEE International Solid- State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2019, pp. 234-236.

More References

- Y. Okuma, et al., "0.5-V input digital LDO with 98.7% current efficiency and 2.7-μA quiescent current in 65nm CMOS", CICC 2010, paper 11.5.
- J. F. Bulzacchelli et al., "Dual-loop system of distributed microregulators with high DC accuracy, load response time below 500 ps, and 85-mV dropout voltage," JSSC, Apr. 2012, pp. 863–874.
- C. Chiu et al., "A 0.6 V resistance-locked loop embedded digital low dropout regulator in 40 nm CMOS with 77% power supply rejection improvement," Symp. VLSI Circuits 2013, pp. 166–167.
- Y. H. Lee et al., "A low quiescent current asynchronous digital-LDO with PLL-modulated fast-DVS power management in 40 nm SoC for MIPS performance improvement," JSSC, Apr. 2013, pp. 1018–1030.
- S. Gangopadhyay, et al., "A 32 nm embedded, fully-digital, phase-locked low dropout regulator for fine grained power management in digital circuits," JSSC, Nov. 2014, pp. 2684–2693.
- E. Fluhr et al., "The 12-Core POWER8™ Processor With 7.6 Tb/s IO Bandwidth, Integrated Voltage Regulation, and Resonant Clocking," JSSC, Jan. 2015, pp. 10-23.
- S. Nasir, et al., "A 0.13μm Fully Digital Low-Dropout Regulator with Adaptive Control and Reduced Dynamic Stability for Ultra-Wide Dynamic Range", ISSCC 2015, paper 5.6.
- F. Yang and et al., "A 0.6–1 V input capacitor-less asynchronous digital LDO with fast transient response achieving 9.5 b over 500 mA loading range in 65-nm CMOS," ESSCIRC 2015, pp. 180–183.
- F. Yang and et al., "Fast-transient asynchronous digital LDO with load regulation enhancement by soft multi-step switching and adaptive timing techniques in 65-nm CMOS," CICC 2015, paper 19.4.
- S. Nasir, et al., "All-Digital Low-Dropout Regulator With Adaptive Control and Reduced Dynamic Stability for Digital Load Circuits," Trans. Power Electron., Dec 2016, pp. 8293-8302.
- Y. Li, et al., "A 0.45-to-1.2-V fully digital low-dropout voltage regulator with fast-transient controller for near/subthreshold circuits," Trans. Power Electron., Sep. 2016, pp. 6341–6350.
- K. Luria, J. Shor, M. Zelikson, and A. Lyakhov, "Dual-mode low-drop-out regulator/power gate with linear and on–off conduction for microprocessor core on-die supply voltages in 14 nm," JSSC, Mar. 2016, pp. 792–762.

More References

- D. Kim, et al., "Fully Integrated Low-Drop-Out Regulator Based on Event-Driven PI Control", ISSCC 2016, paper 8.2.
- Y. Lee, et al., "A 200mA Digital Low-Drop-Out Regulator with Coarse-Fine Dual Loop in Mobile Application Processors", ISSCC 2016, paper 8.3.
- S. Nasir, et al., "A 130 nm hybrid low dropout regulator based on switched mode control for digital load circuits," ESSCIRC 2016, pp. 317–320.
- D. Kim, et al., "A Fully Integrated Digital Low-Dropout Regulator Based on Event-Driven Explicit Time-Coding Architecture", JSSC, Nov. 2017, pp. 3071-3080.
- Y.-J. Lee et al., "A 200-mA digital low drop-out regulator with coarse fine dual loop in mobile application processor," JSSC, Jan. 2017, pp. 64–76.
- W. Tsou, et al., "Digital Low-Dropout Regulator with Anti PVT-Variation Technique for Dynamic Voltage Scaling and Adaptive Voltage Scaling Multicore Processor", ISSCC 2017, paper 20.2.
- L. Salem, et al., "A 100nA-to-2mA Successive-Approximation Digital LDO with PD Compensation and Sub-LSB Duty Control Achieving a 15.1ns Response Time at 0.5V", ISSCC 2017, paper 20.3.
- M. Huang, et al., "An Output-Capacitor-Free Analog-Assisted Digital Low-Dropout Regulator with Tri-Loop Control", ISSCC 2017, paper 20.4.
- D. Kim, et al., "A 0.5V-VIN 1.44mA-Class Event-Driven Digital LDO with a Fully Integrated 100pF Output Capacitor", ISSCC 2017, paper 20.6.
- A. Fahmy, et al., "A synthesizable time-based LDO using digital standard cells and analog pass transistor," ESSCIRC 2017, pp. 271-274.
- R. Muthukaruppan, et al., "A digitally controlled linear regulator for per-core wide-range DVFS of atom™ cores in 14nm tri-gate CMOS featuring non-linear control, adaptive gain and code roaming," ESSCIRC 2017, pp. 279-278.
- T. Mahajan, et al., "Digitally Controlled Voltage Regulator Using Oscillator-based ADC with fast transient-response and wide dropout range in 14nm CMOS", CICC 2017, paper 25.3.

More References

- D. Kim, et al., "0.5V-VIN, 165-mA/mm2 Fully-Integrated Digital LDO based on Event-Driven Self-Triggering Control", Symp. VLSI Circuits 2018, paper 10.4.
- L. Salem, et al., "A Successive Approximation Recursive Digital Low-Dropout Voltage Regulator With PD Compensation and Sub-LSB Duty Control," JSSC, Jan. 2018, pp. 35-49.
- M. Huang, et al., "An Analog-Assisted Tri-Loop Digital Low-Dropout Regulator," JSSC, Jan. 2018, pp. 20-34.
- S. Nasir, et al., "Switched-Mode-Control Based Hybrid LDO for Fine-Grain Power Management of Digital Load Circuits," JSSC, Feb. 2018, pp. 569-581
- C. Gonzalez, et al., "The 24-Core POWER9 Processor With Adaptive Clocking, 25-Gb/s Accelerator Links, and 16-Gb/s PCIe Gen4," JSSC, Jan. 2018, pp. 91-101.
- X. Ma, et al., "A 0.4V 430nA Quiescent Current NMOS Digital LDO with NAND-Based Analog-Assisted Loop in 28nm CMOS", ISSCC 2018, paper 18.4.
- S. Kundu, et al., "A Fully Integrated 40pF Output Capacitor Beat-Frequency-Quantizer-Based Digital LDO with Built-In Adaptive Sampling and Active Voltage Positioning", ISSCC 2018, paper 18.5.
- Y. Lu, et al., "A 500mA Analog-Assisted Digital-LDO-Based On-Chip Distributed Power Delivery Grid with Cooperative Regulation and IR-Drop Reduction in 65nm CMOS", ISSCC 2018, paper 18.6.
- L. Salem, et al., "A Sub-1.55mV-Accuracy 36.9ps-FOM Digital-Low-Dropout Regulator Employing Switched-Capacitor Resistance", ISSCC 2018, paper 18.7.
- J. Lin, et al., "A High-Efficiency and Fast-Transient Digital-Low-Dropout Regulator with the Burst Mode Corresponding to the Power-Saving Modes of DC-DC Switching Converters", ISSCC 2018, paper 18.8.
- J. Tang, et al., "A 0.7V Fully-on-Chip Pseudo-Digital LDO Regulator with 6.3μA Quiescent Current and 100mV Dropout Voltage in 0.18-μm CMOS," ESSCIRC 2018, pp. 206-209.
- Y. Lim, et al., "A 320μV-Output Ripple and 90ns-Settling Time at 0.5V Supply Digital-Analog-Hybrid LDO Using Multi-Level Gate-Voltage Generator and Fast-Decision PD Detector," ESSCIRC 2018, pp. 210-213.

More References

- S. Kudva, et al., "A Switching Linear Regulator Based on a Fast-Self-Clocked Comparator with Very Low Probability of Meta-stability and a Parallel Analog Ripple Control Module", CICC 2018, paper 6.5.
- S. Kim, et al., "A 0.5-1V Input Event-Driven Multiple Digital Low-Dropout-Regulator System for Supporting a Large Digital Load", Symp. VLSI Circuits 2019, paper 12.3.
- H. Krishnamurthy, et al., "A Variation-Adaptive Integrated Computational Digital LDO in 22nm CMOS with Fast Transient Response", Symp. VLSI Circuits 2019, paper 12.1.
- J. Lee, et al., "A 0.5V-VIN, 0.29ps-Transient-FOM, and Sub-2mV-Accuracy Adaptive-Sampling Digital LDO Using Single-VCO-Based Edge-Racing Time Quantizer", Symp. VLSI Circuits 2019, paper 12.4.
- S. Choi, et al., "A Quasi-Digital Ultra-Fast Capacitor-less Low-Dropout Regulator Based on Comparator Control for x8 Current Spike of PCRAM systems", Symp. VLSI Circuits 2018, paper 10.3.
- S. Kundu, et al., "A Fully Integrated Digital LDO With Built-In Adaptive Sampling and Active Voltage Positioning Using a Beat-Frequency Quantizer," JSSC, Jan. 2019, pp. 109-120.
- X. Sun, et al., "A 0.6-to-1.1V Computationally Regulated Digital LDO with 2.79-Cycle Mean Settling Time and Autonomous Runtime Gain Tracking in 65nm CMOS", ISSCC 2019, paper 14.5.
- S. Li, et al., "A 745pA Hybrid Asynchronous Binary-Searching and Synchronous Linear-Searching Digital LDO with 3.8×105 Dynamic Load Range, 99.99% Current Efficiency, and 2mV Output Voltage", ISSCC 2019, paper 14.6.
- X. Liu, et al., "A Modular Hybrid LDO with Fast Load-Transient Response and Programmable PSRR in 14nm CMOS Featuring Dynamic Clamp Tuning and Time-Constant Compensation", ISSCC 2019, paper 14.7.
- Y. Lu, et al., "A Single-Controller-Four-Output Analog-Assisted Digital LDO with Adaptive-Time-Multiplexing Control in 65-nm CMOS", ESSCIRC 2019, pp. 289-292.
- B. Nguyen, et al., "A Sub-1V Analog-Assisted Inverter-Based Digital Low-Dropout Regulator with a Fast Response Time at 25mA/100ps and 99.4% Current Efficiency", CICC 2019, paper 9.5.

More References

- M. Huang, et al., "An Analog-Proportional Digital-Integral Multi-Loop Digital LDO with Fast Reponse, Improved PSR and Zero Minimum Load Current", CICC 2019, paper 9.6.
- X. Wang, et al., "A Charge-Pump-based LDO Employing an AC-Coupled High-Z Feedback Loop Towards a sub-4fs FoM and a 105,000x Stable Dynamic Current Range", CICC 2019, paper 9.7.
- M. Perez, et al., "Distributed Network of LDO Microregulators Providing Submicrosecond DVFS and IR Drop Compensation for a 24-Core Microprocessor in 14nm SOI CMOS", CICC 2019, paper 9.8.
- J. Kang, et al., "Time-Based Digital LDO Regulator with Fractionally Controlled Power Transistor Strength and Fast Transient Response", ASSCC 2019, paper 4.4.