ISSCC 2020 Tutorials
Digital Fractional-N Phase Locked Loop Design

Mike Shuo-Wei Chen
swchen@usc.edu

Feb, 2020

Outline

- Basics of PLL (Analog vs Digital)
- Fractional-N Operation

-----Interim Q&A-----

- Critical Building Blocks
- Challenging Frac-N Design Issues
- New Opportunities
- SOA Fractional-N Digital PLL Examples

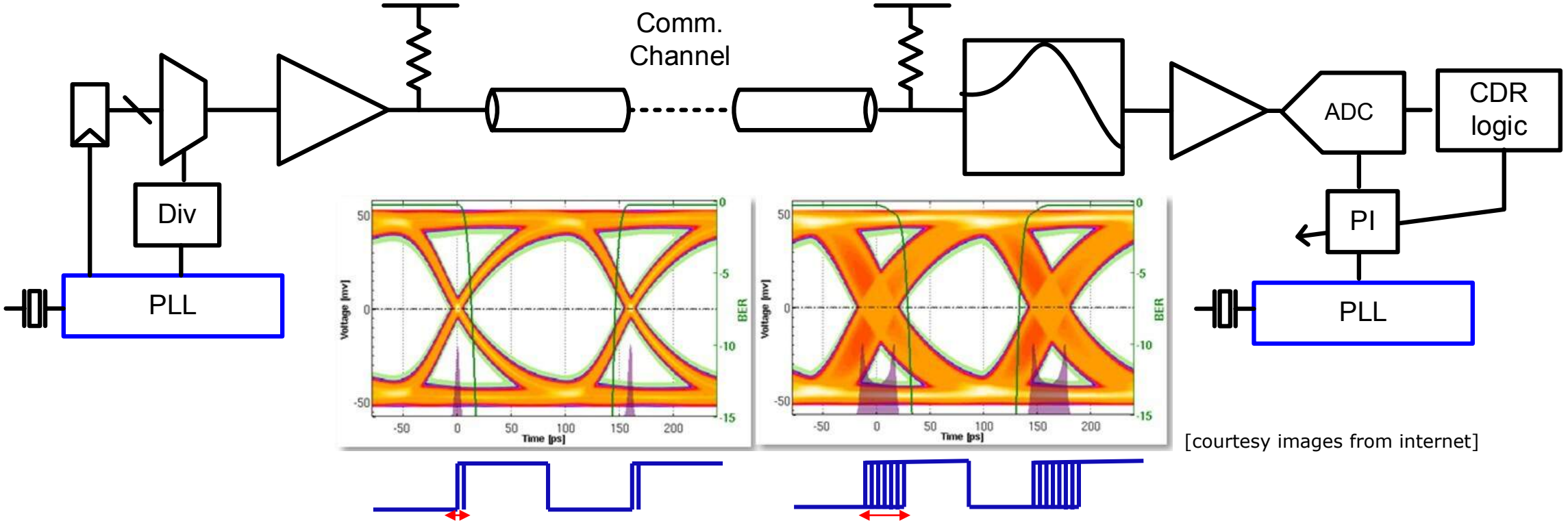
A good clock is important

- Most of the electronic systems operate in synchronous fashion.
- Just like a traffic light that puts traffic (electrons/holes in IC) in order
- Without a clock or a malfunctioning clock, it can be a mess!

[courtesy images from internet]

Why PLL for Wireline?

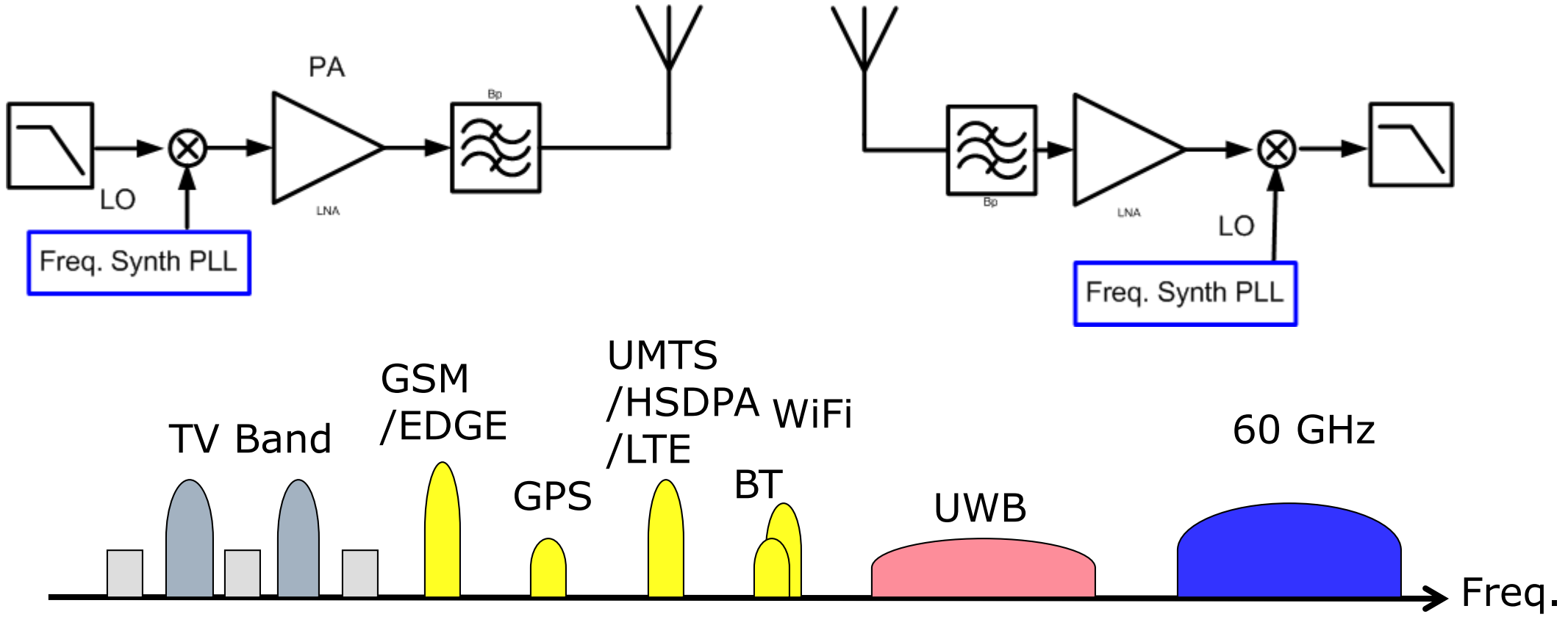
- Clock generation for wireline transmitter and receiver
- Clock provides timing reference to generate and latch data symbols



[courtesy images from internet]

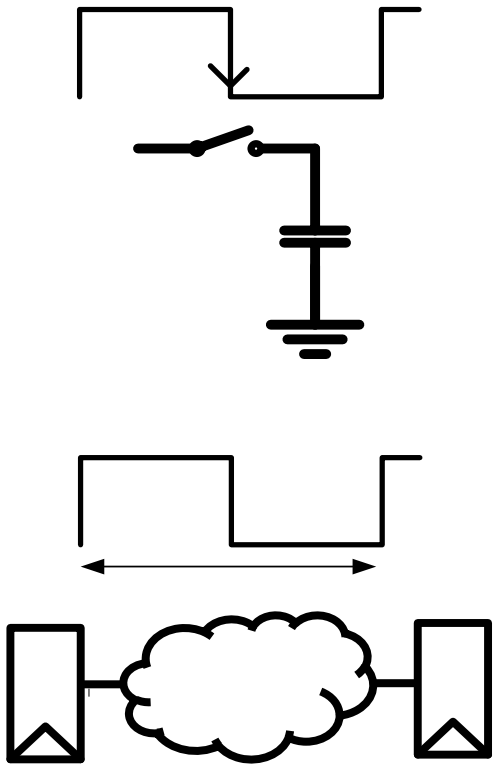
Why PLL for Wireless?

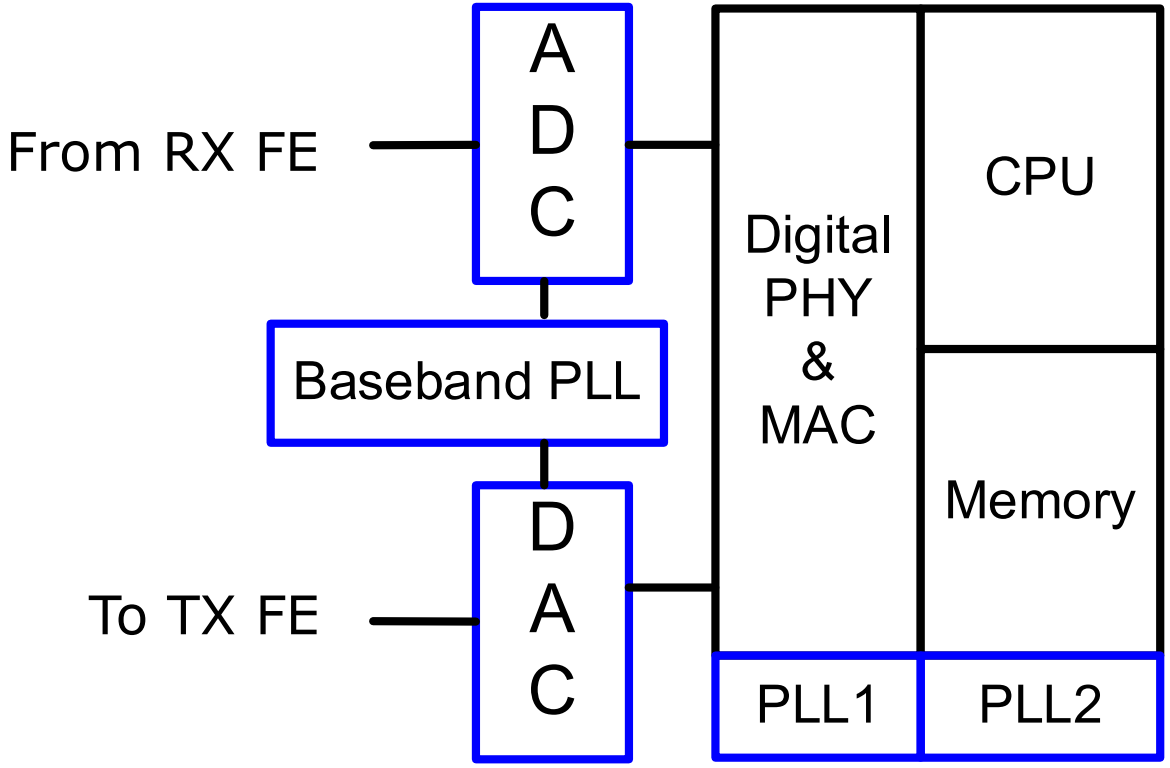
- In wireless communications, a LO is typically required to upconvert/downconvert the baseband signal for transmitter and receiver.



Why PLL for SoC?

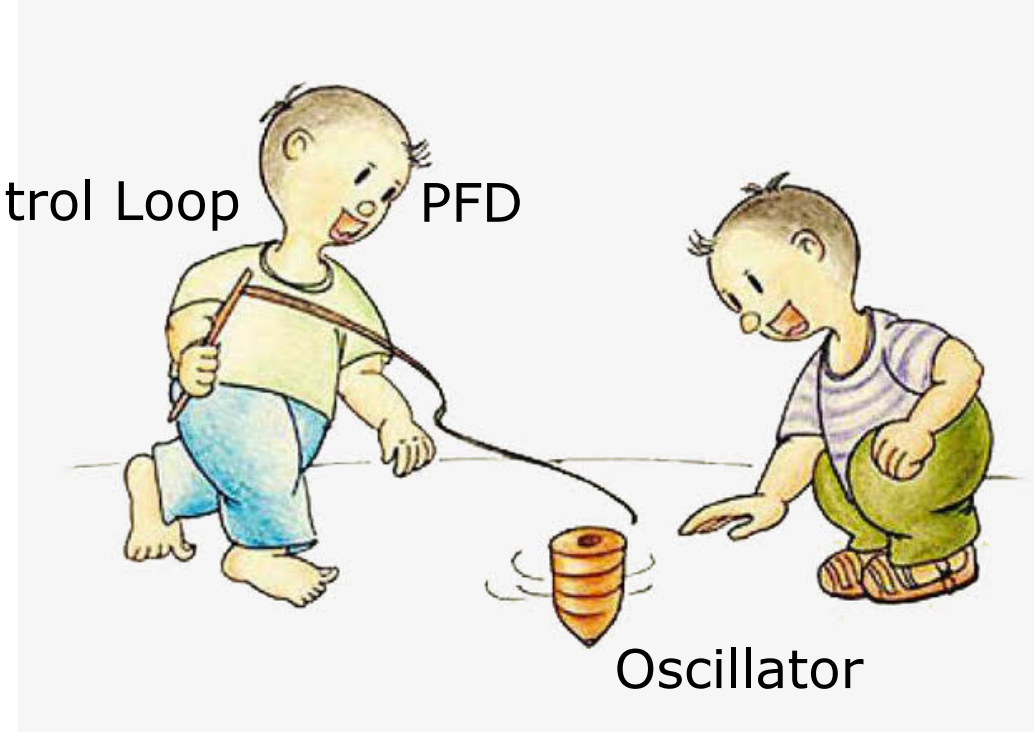
- Sampling clocks for ADC and DAC
- Clocks to drive sequential logic in digital processors





How does PLL work?

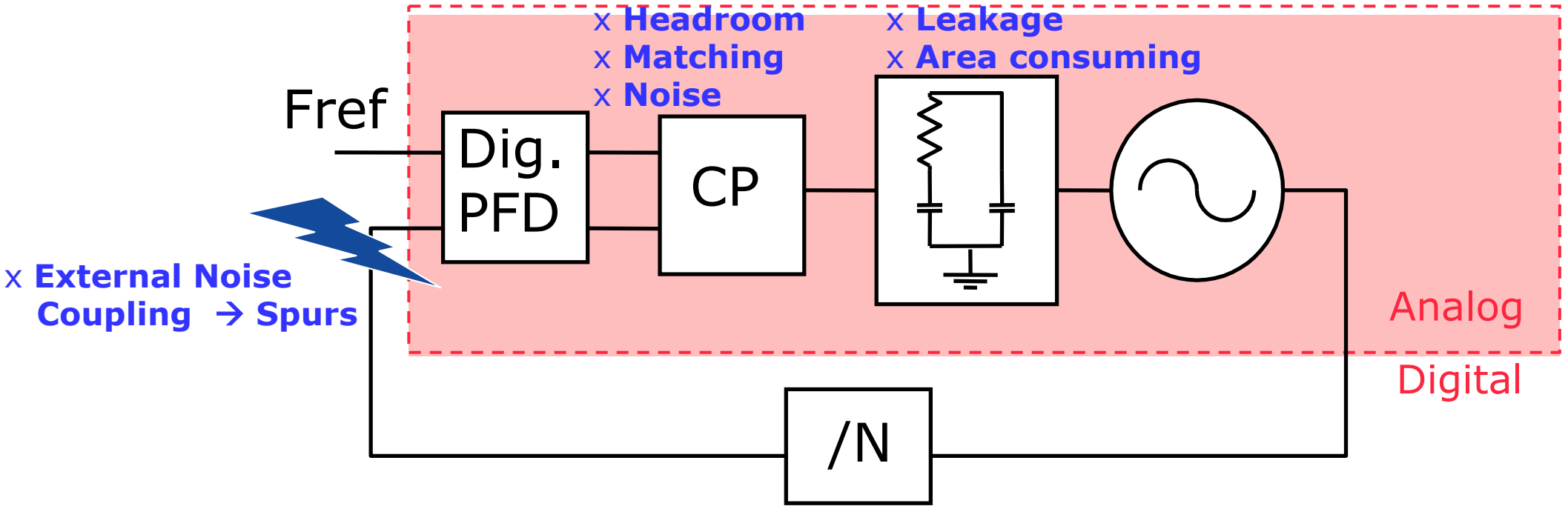
- Playing with top or fidget spinner works just like a PLL
- Oscillator + Freq/Phase detector(PFD) + Control Loop



[courtesy images from internet]

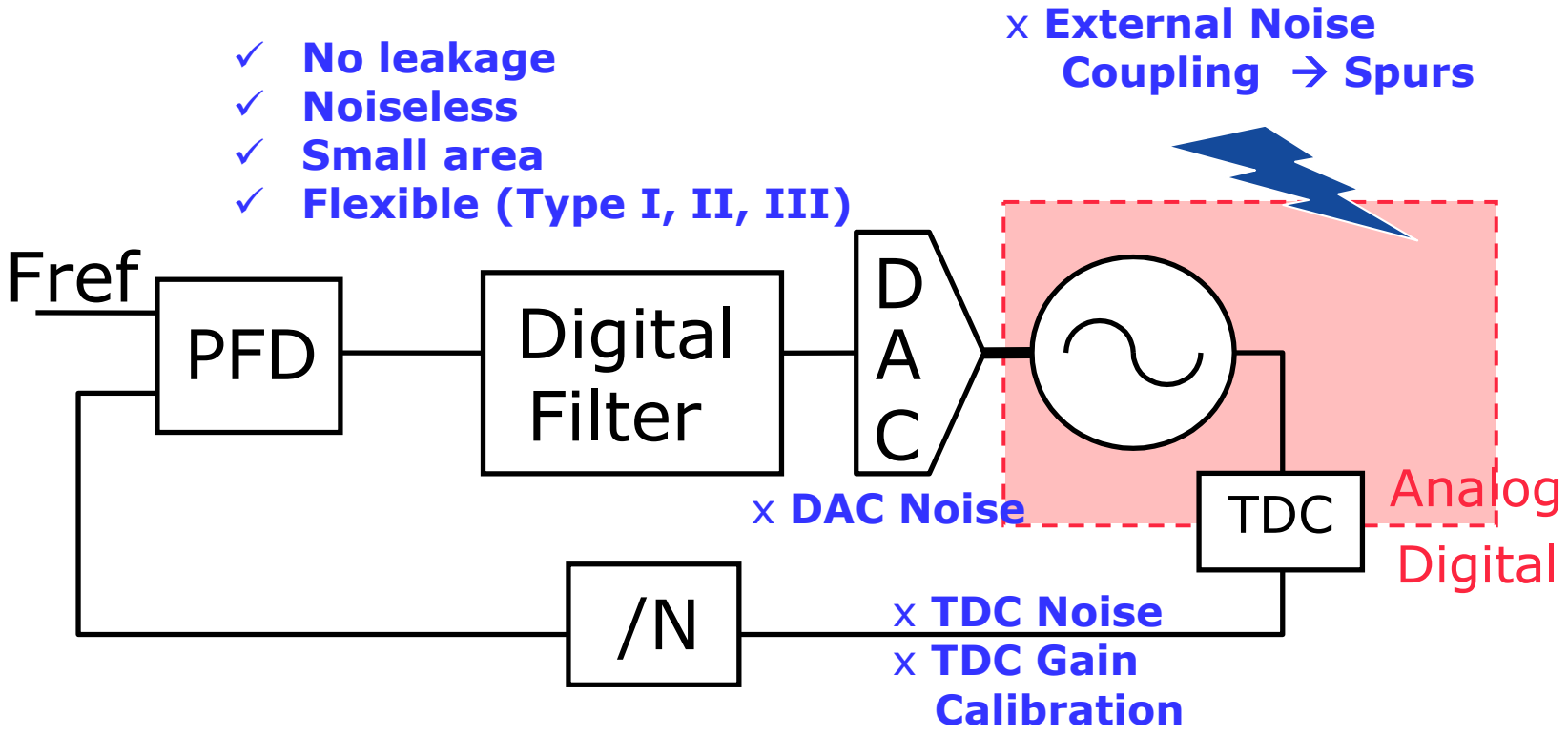
Analog PLL

- A proven and popular solution for PLL implementation
- A charge-pump PLL relies on analog control loop.



Digital PLL

- Emerging interests in a more digital intensive design
- Why?

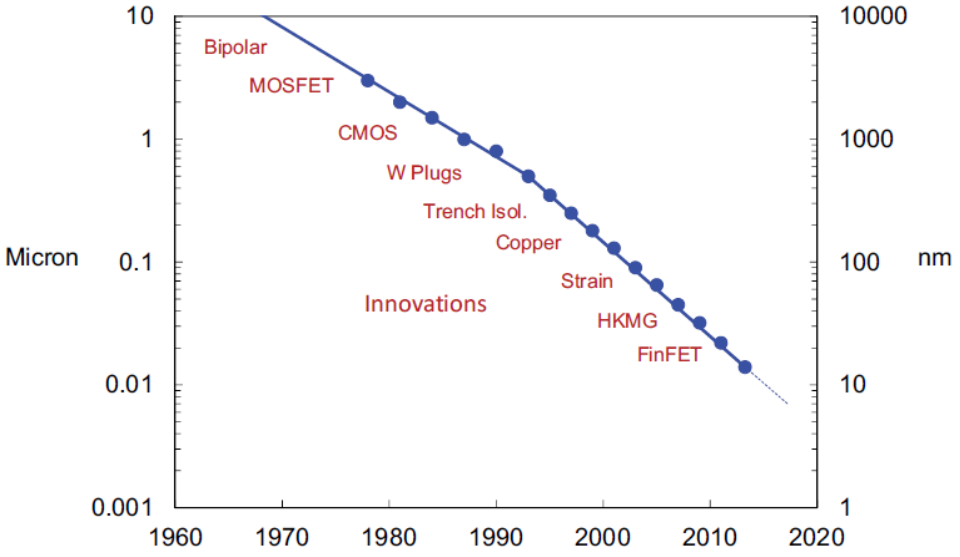


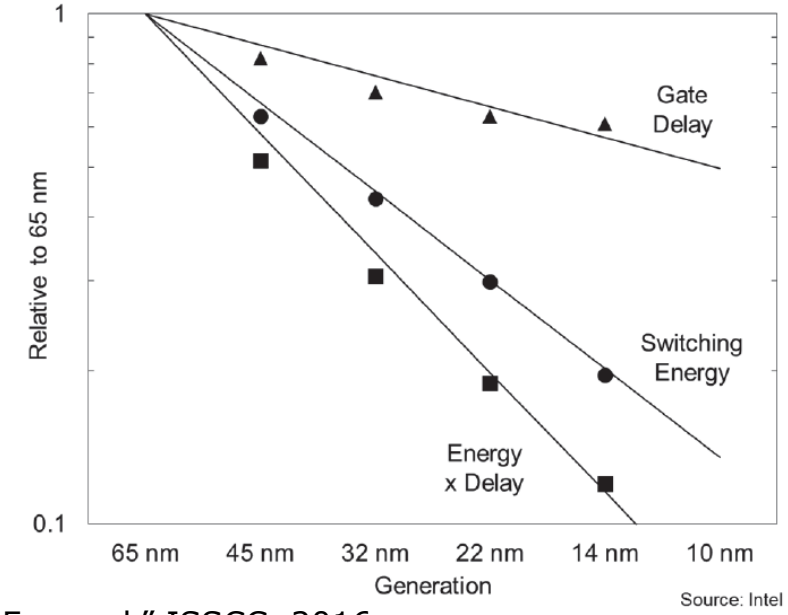
Evolutions of Digital PLL

- 1st wave → small area, technology scaling
- 2nd wave → close the performance gap to analog PLL
- 3rd wave → performance beyond analog PLL?
  [TDC (cost/calibration), spur]

When to use Analog vs. Digital PLL?

- Smaller inverter (FO4) delay favors digital PLL; however, higher PLL output frequency requires finer TDC for fixed in-band phase noise floor (dBc/Hz).
- In general, older technology or lower noise→ analog PLL remains attractive.
- In terms of area/power/portability, digital PLL is more attractive.

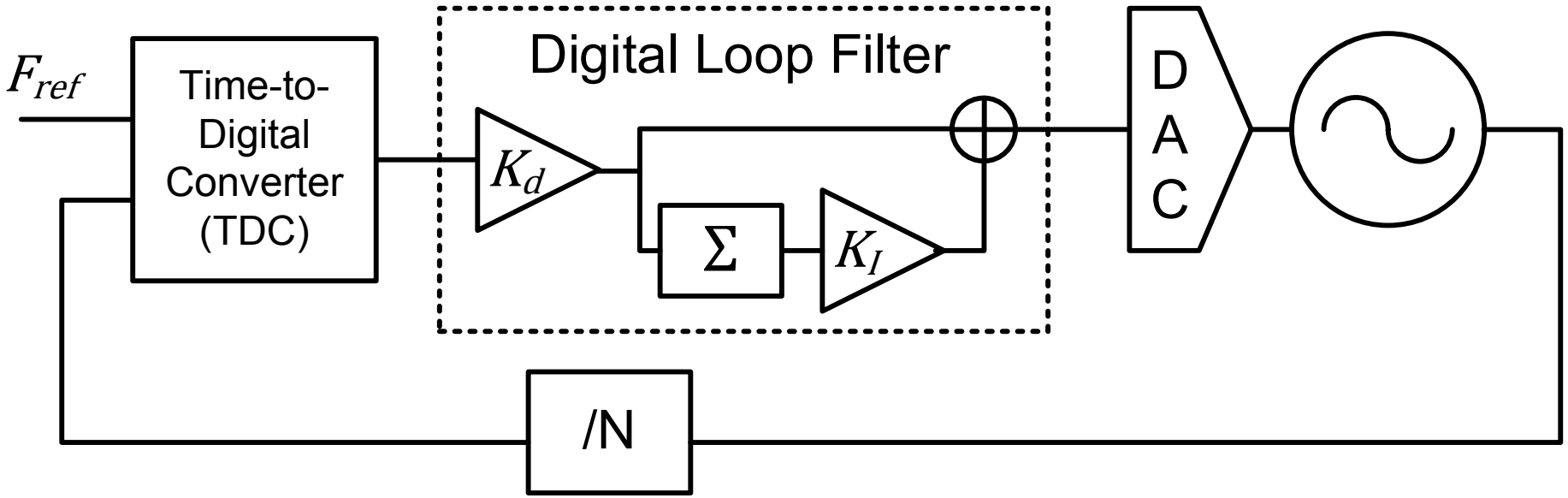




W. Holt, "Moore's Law: A Path Moving Forward," ISSCC, 2016

Operation of Basic Integer-N DPLL

- Consider a type-II digital loop filter
- Built-in ADC to quantize oscillator phase, i.e. TDC
- Built-in DAC to control oscillator

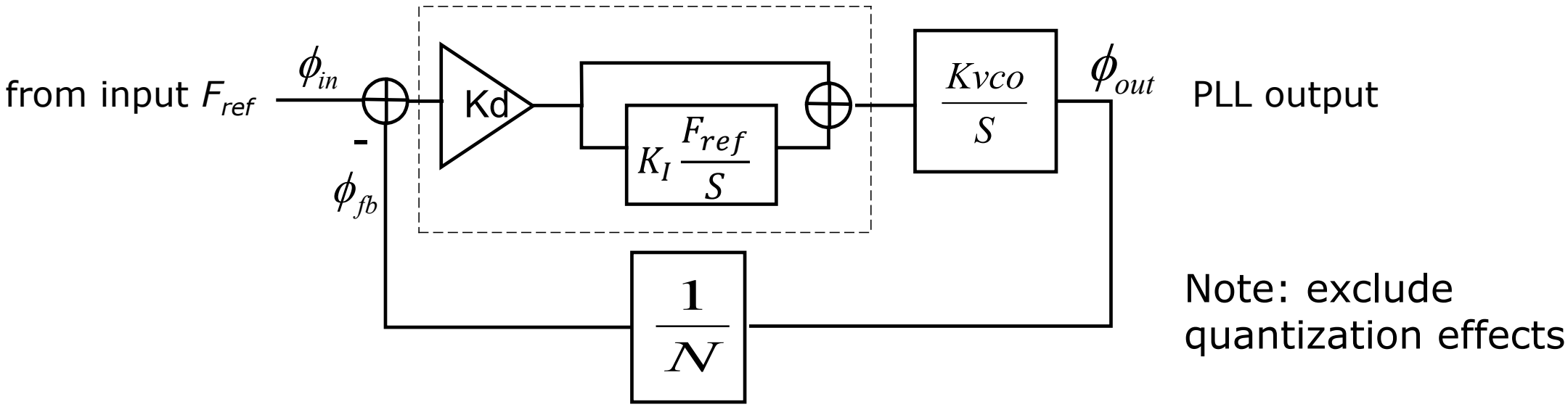


Approximated Laplace Response in Phase

- The circuit operation is in voltage domain, but easier to analyze in phase domain.
- Used Euler approximation for loop analysis in the steady state

CT-DT Transformation ➔ $\frac{1}{S} = \frac{1}{F_{ref}(1 - Z^{-1})}$

- K_{vco}: VCO gain, N: PLL division ratio, F_{ref}: input reference frequency

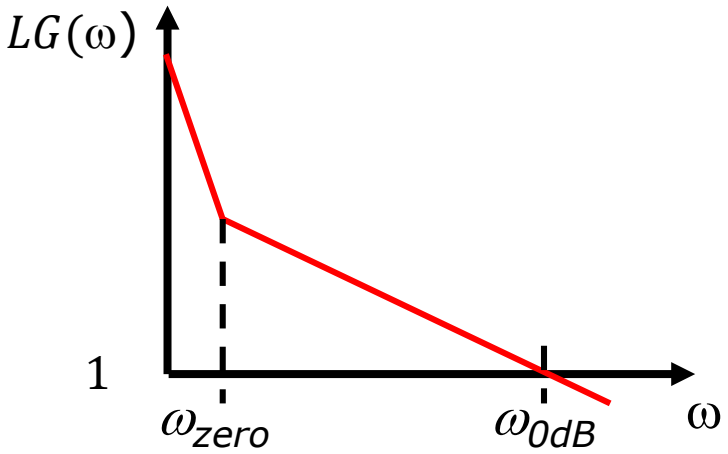


Loop Parameter Selection

- How to choose loop filter parameter, i.e. K_d and K_I?
- Examine closed-loop response in the phase domain.
- K_{vco}: VCO gain, N: PLL division ratio, F_{ref}: input reference frequency

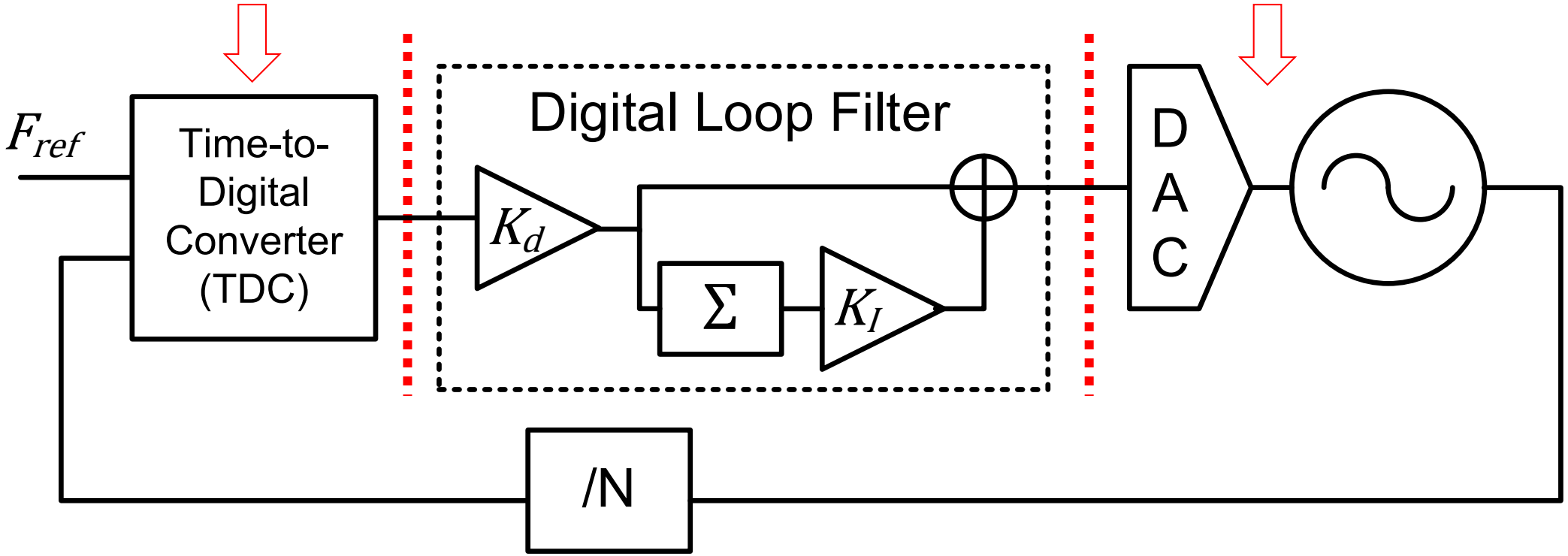
- Loop gain: $$LG(S) = K_d \frac{S + K_I F_{ref}}{S} \frac{K_{vco}}{S} \frac{1}{N}$$
- K_I: $$\omega_{zero} = K_I \cdot F_{ref}$$
- K_d: $$K_d \sim N \cdot \omega_{0dB} \frac{1}{K_{vco}}$$

if ω_{zero} << ω_{0dB} (unity gain BW)



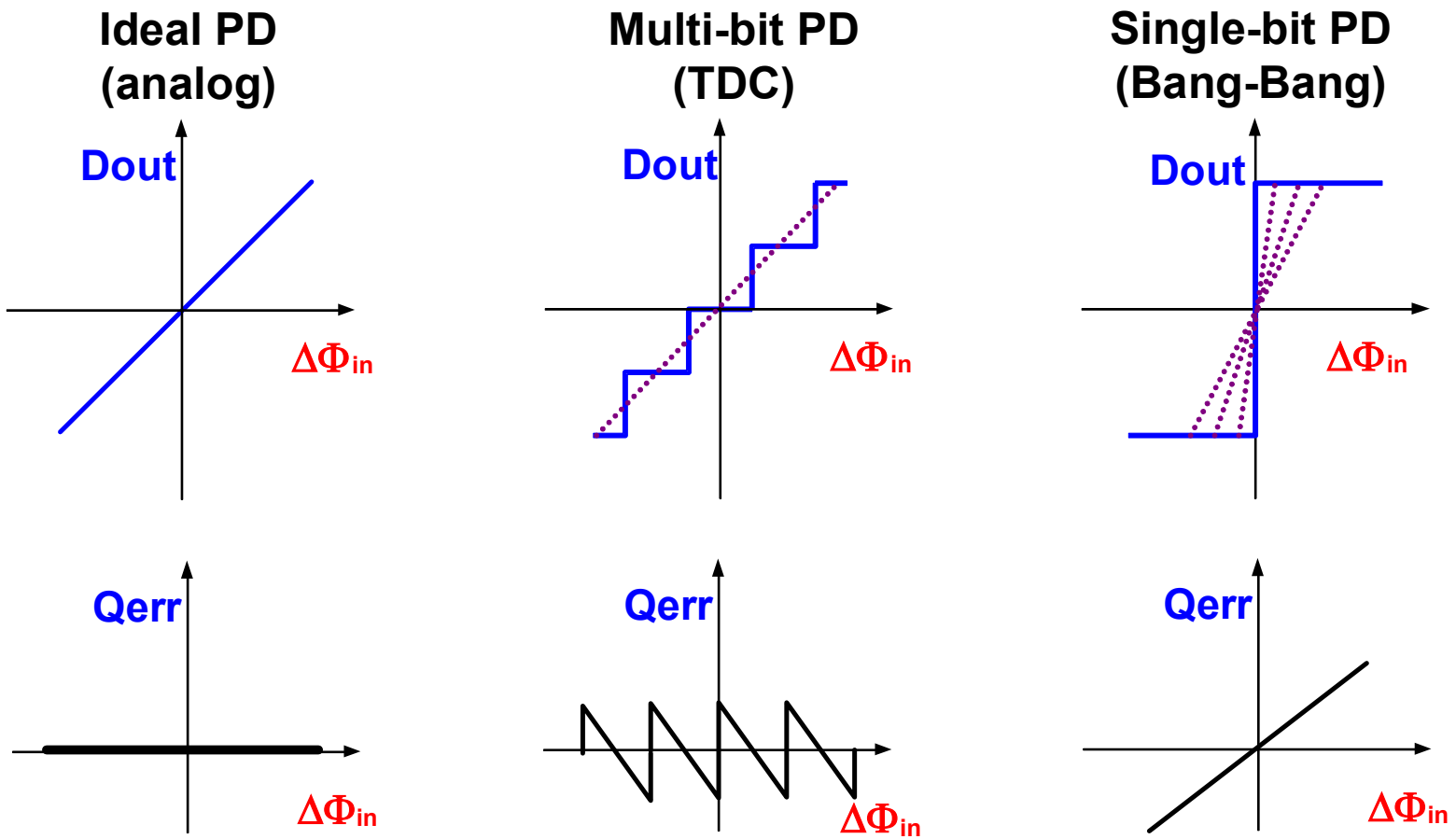
Modeling Quantization Effects

- Two main quantization sources:
  - Phase quantizer: time-to-digital converter (TDC)
  - Frequency quantizer: digitally controlled oscillator (DCO)

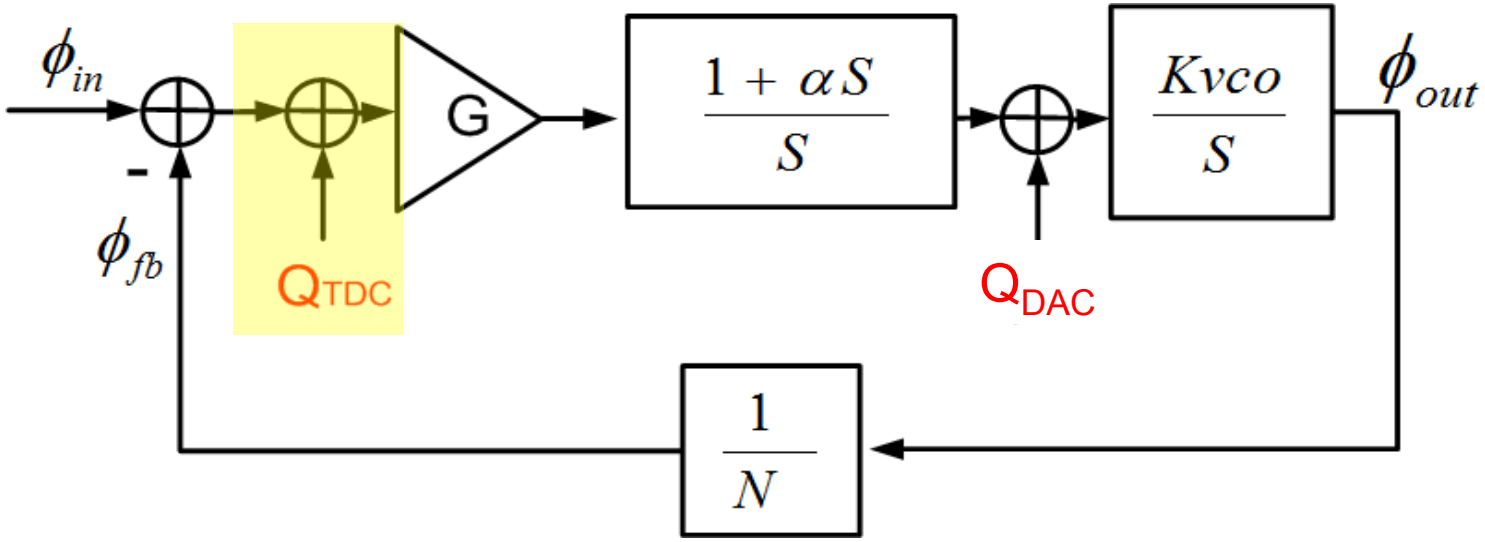


Phase Quantizer

- Different types of phase quantizer, i.e. phase detector (PD)



Phase Quantization Modeling



$$\alpha = \frac{1}{K_I \cdot F_{ref}}$$

$$G = K_d \cdot K_I \cdot F_{ref}$$

- Degrade in-band phase noise
- Overhead (both cost and performance) in a digital PLL
- Noise transfer function (NTF_{TDC}), i.e. phase quantization noise to PLL output, shows a lowpass response:

$$NTF_{TDC} = \frac{\varphi_{out}}{Q_{TDC}} = \frac{K_{VCO} \cdot G \cdot (1 + \alpha \cdot S)}{S^2 + K_{VCO}/N \cdot G(1 + \alpha \cdot S)}$$

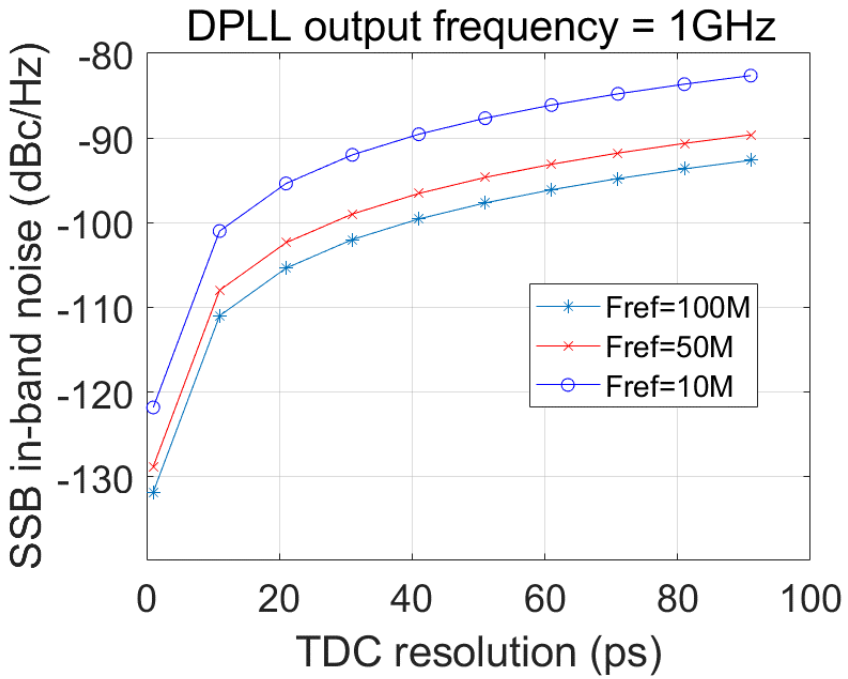
TDC Specification

- TDC resolution affects in-band phase noise.
- For uniformly distributed quantization error, the noise spectrum is spread over TDC's sample rate, i.e. F_{ref}.
- Example: t_{res}(TDC LSB resolution)=100ps, T_{vco}=1ns, F_{ref}=100MHz.
  → -92 dBc/Hz single-side band (SSB) in-band noise floor

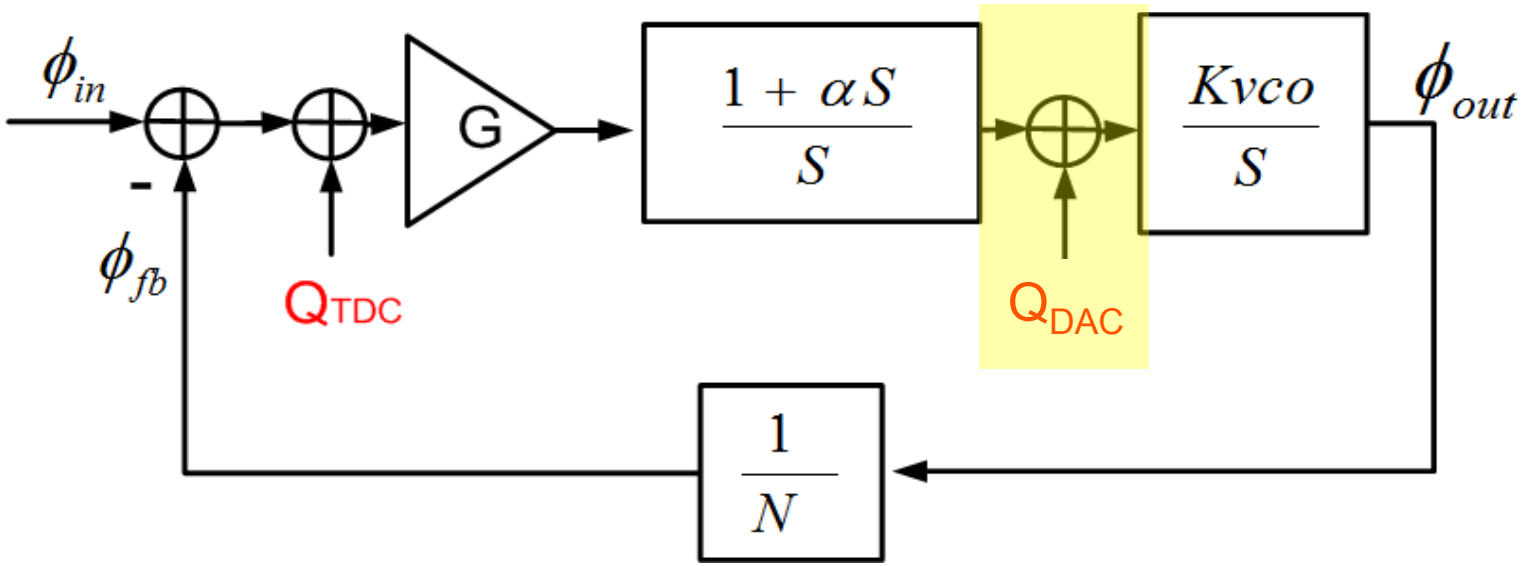
$$\Delta_\phi = \frac{t_{res}}{T_{vco}} \cdot 2\pi$$

$$L_{SSB} = 10\log\left(\frac{\Delta^2_\phi}{12}\frac{2}{F_{ref}}\right)$$

Is this assumption correct?



Frequency Quantization Modeling



- Typically use oversampling DAC to shape the quantization noise to out of band or design a high resolution DAC to avoid phase noise degradation
- Noise transfer function (NTF_{FDAC}), i.e. frequency quantization noise to PLL output, shows a bandpass response:

$$NTF_{FDAC} = \frac{\varphi_{out}}{Q_{DAC}} = \frac{K_{VCO} \cdot S}{S^2 + K_{VCO}/N \cdot G(1 + \alpha \cdot S)}$$

More Noise Sources

- Other than the quantization noise, circuit noise in DPLL still degrades output phase noise, similar to analog PLL:
  - Oscillator phase noise (high pass)

$$NTF_{DCO} = \frac{S^2}{S^2 + K_{VCO}/N \cdot G(1 + \alpha \cdot S)}$$

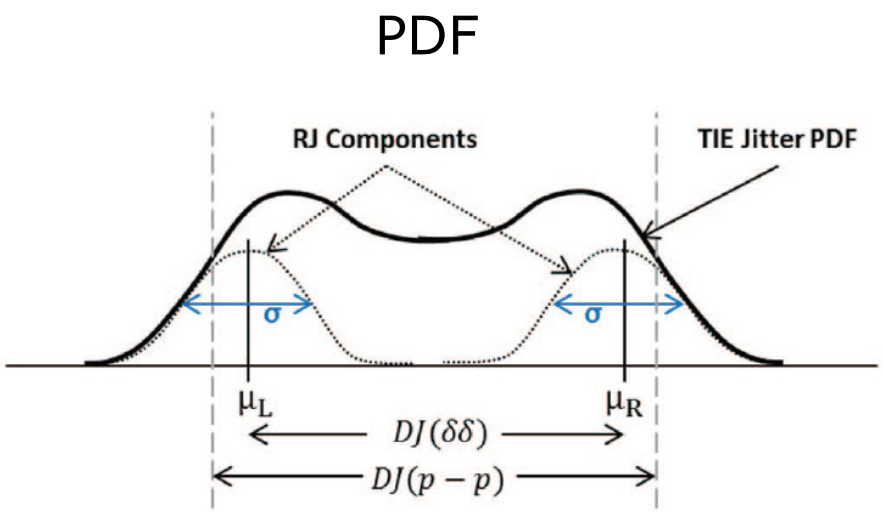
  - Reference clock noise (low pass)
  - Intrinsic noise of TDC (low pass)

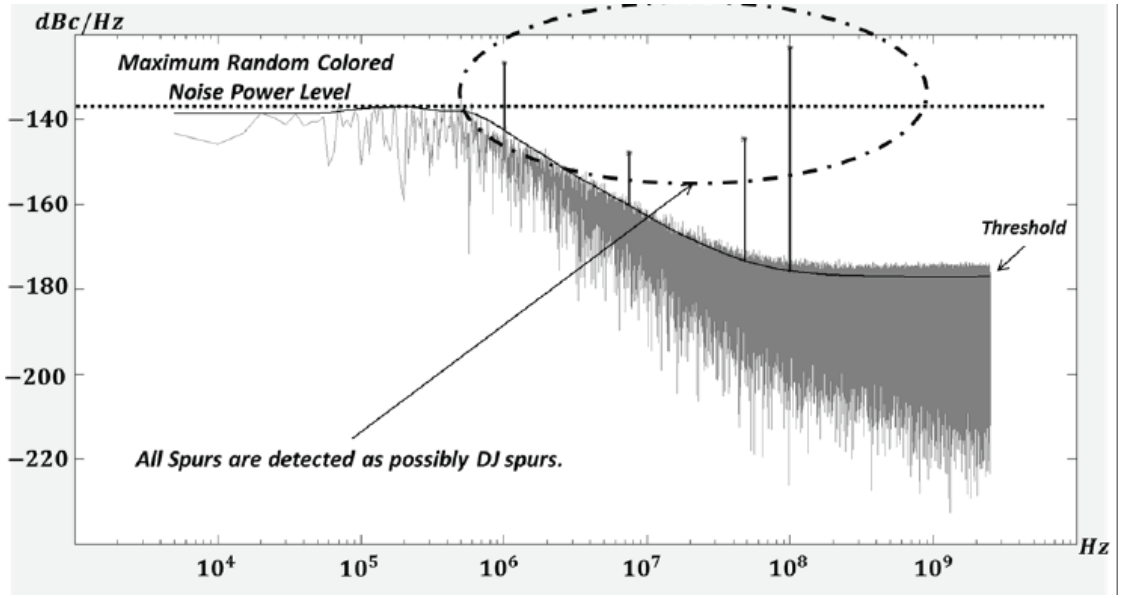
$$NTF_{input} = NTF_{TDC} = \frac{K_{VCO} \cdot G \cdot (1 + \alpha \cdot S)}{S^2 + K_{VCO}/N \cdot G(1 + \alpha \cdot S)}$$

- No charge-pump noise as in analog PLL; instead, there is numerical noise in the digital loop filter

PLL Specifications

- Typical wireline specifications related to PLL design:
  - Random jitter (RJ): integrated phase noise at PLL output spectrum
  - Deterministic jitter (DJ): PLL spurious tones, i.e. periodic noise pattern.



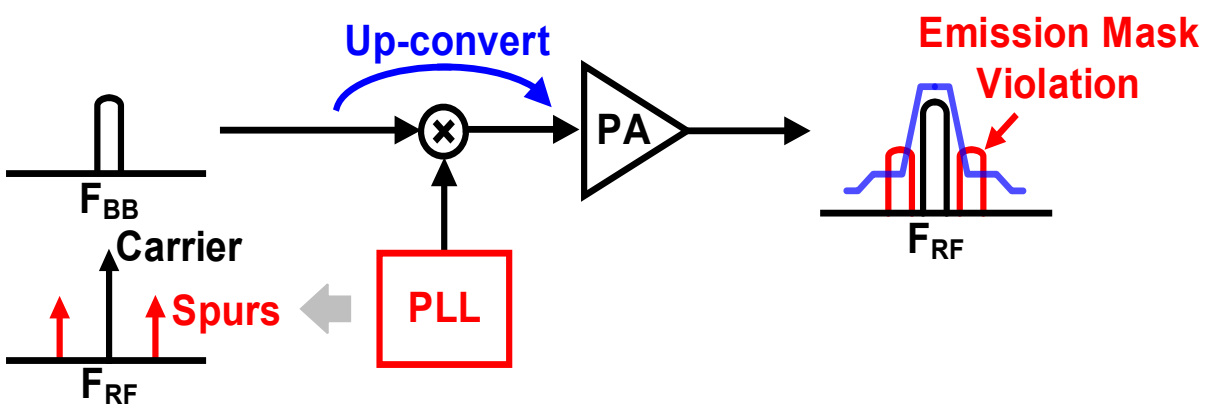


Ref: K. Bidaj, et al., "RJ/DJ jitter decomposition technique for high speed links, " IEEE ICECS 2016.

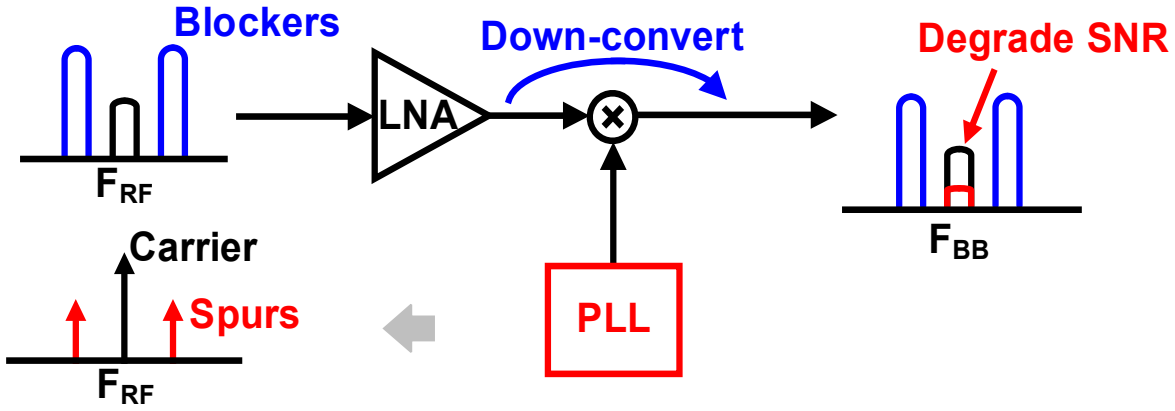
PLL Specifications

- For wireless application, PLL spurs causes unwanted signal mixing.
- Phase noise of PLL can degrade overall system SNR or EVM.

TX: spectral violation



RX: reciprocal mixing



Outline

- Basics of PLL
- Fractional-N Operation

-----Interim Q&A-----

- Critical Building Blocks
- Challenging Frac-N Design Issues
- New Opportunities
- SOA Fractional-N Digital PLL Examples

What is Fractional-N Operation?

- Sometimes, the system requires a clock with fine frequency resolution, e.g. wireless channels can be KHz apart.
- Sometimes, the system demands a higher reference frequency (F_{ref}).
- As a result, PLL output frequency (F_{out}) is no longer an integer multiple of F_{ref}. This is considered as fractional-N operation.

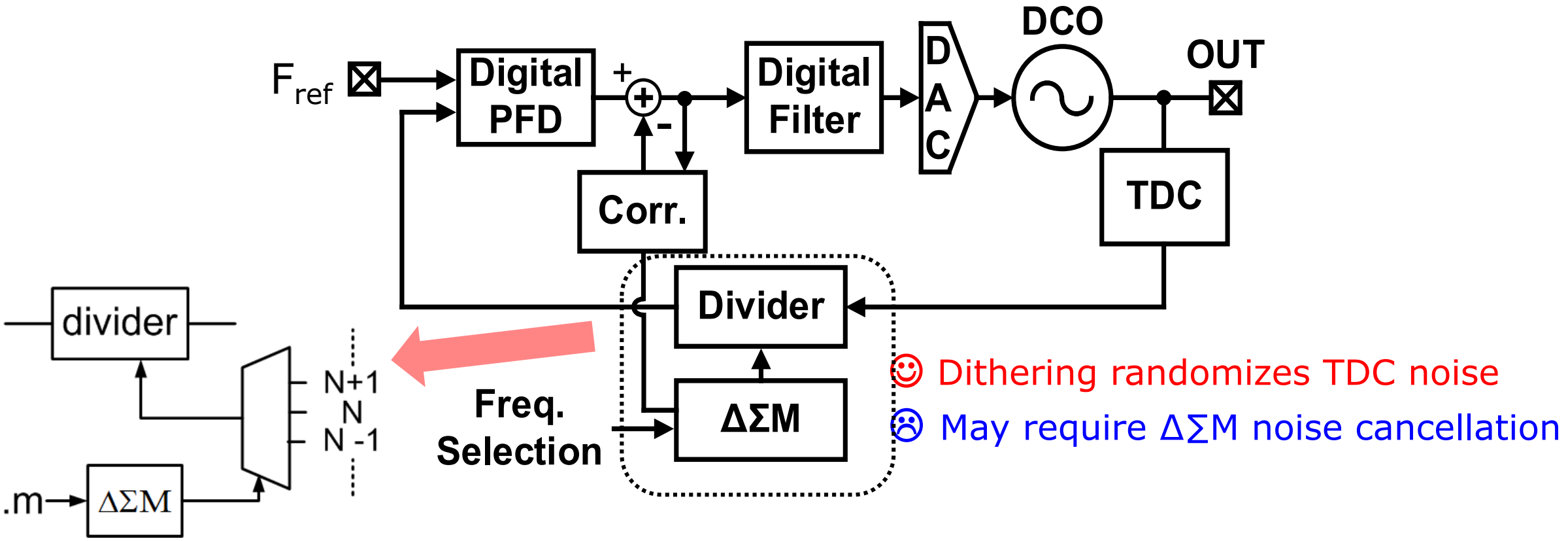
  → F_{out} = N.m · F_{ref}

  Example: 8.0, 8.2, 8.4, 8.6, 8.8 allows F_{ref} to increase by 5X (compared to int-N PLL)
- How to "force" the oscillator to behave according to what we want?

*Note: If N=8, m=4, the frequency multiplication ratio is 8.4

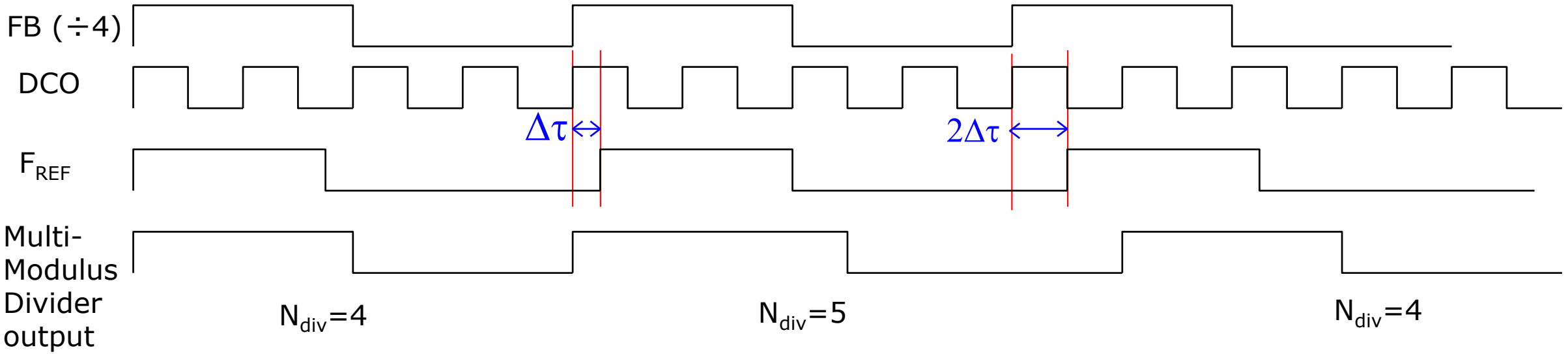
Method 1: Dither Feedback Divider Ratio

- Multi-modulus divider typically controlled by a delta-sigma modulator
- Change integer divider ratio (…, N-1, N, N+1, …) over time



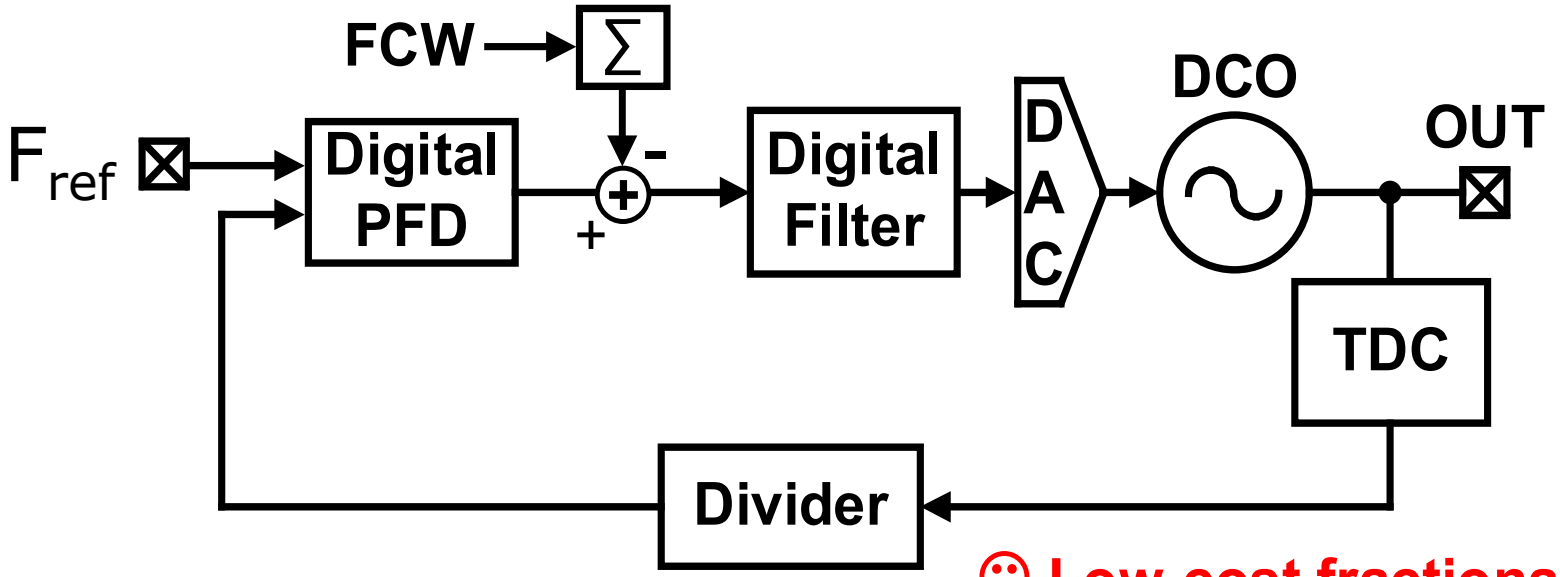
Timing of an ideal Fractional-N

- Time difference between the period of reference clock (F_{REF}) and integer-divided feedback signal (FB) is $\Delta\tau$.
- For N.m=4.25, multi-modulus divider ratio (N_{div}) is dithered between 4 (75%) and 5 (25%).



Method 2: Frequency Accumulation

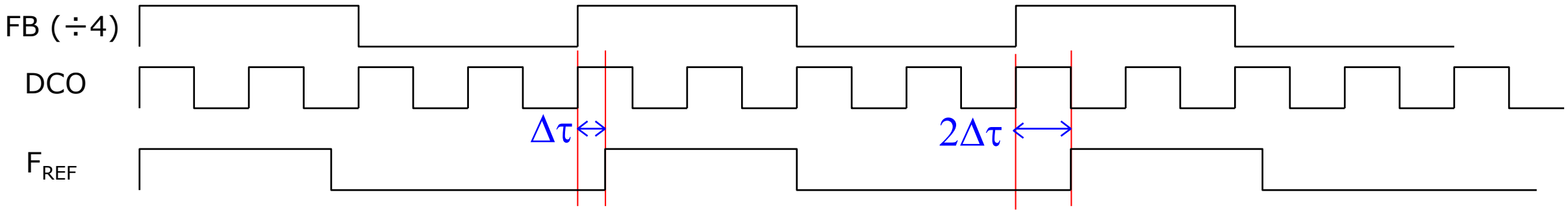
- Still use an integer divider
- Inject frequency offset in the digital domain



☺ Low-cost fractional-N operation

☹ Worse frac-N spurious performance

Analysis of Fractional-N PLL



$$T_{REF} = (1+k)T_{FB} \text{ ,where } k \cdot T_{FB} = \Delta\tau$$

$$\frac{1}{F_{REF}} = (1+k)\frac{1}{F_{FB}}$$

Fractional-N operation

$$F_{DCO} = NF_{FB} = N(1+k)F_{REF} = N(F_{REF} + \Delta f)$$

$$Note: N.m = N(1+k)$$

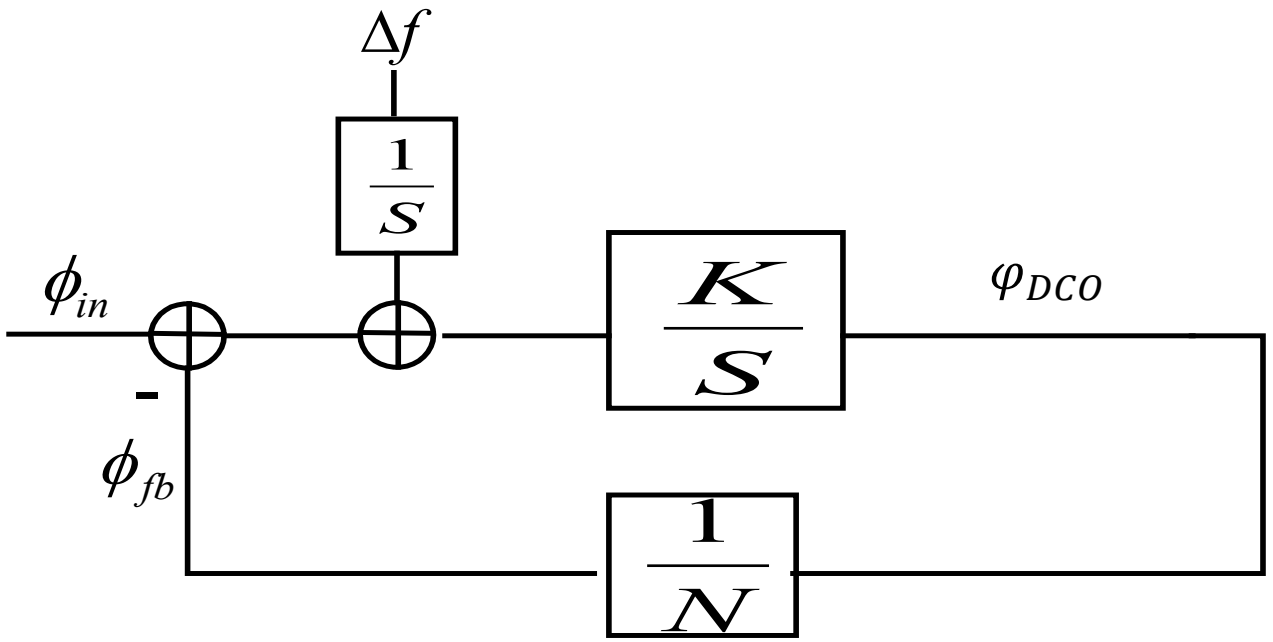
Theoretical Derivations

$$[(\varphi_{ref}(s) - \frac{\varphi_{DCO}(s)}{N}) + \frac{\Delta f}{S}] \cdot \frac{K}{S} = \varphi_{DCO}(s) \quad (1)$$

Apply final value theorem:

$$\lim_{t\to\infty} F_{DCO}(t) = \lim_{t\to\infty} \frac{d\varphi_{DCO}(t)}{dt}$$

$$= \lim_{S\to 0} S\,[S \cdot \varphi_{DCO}] \quad (2)$$

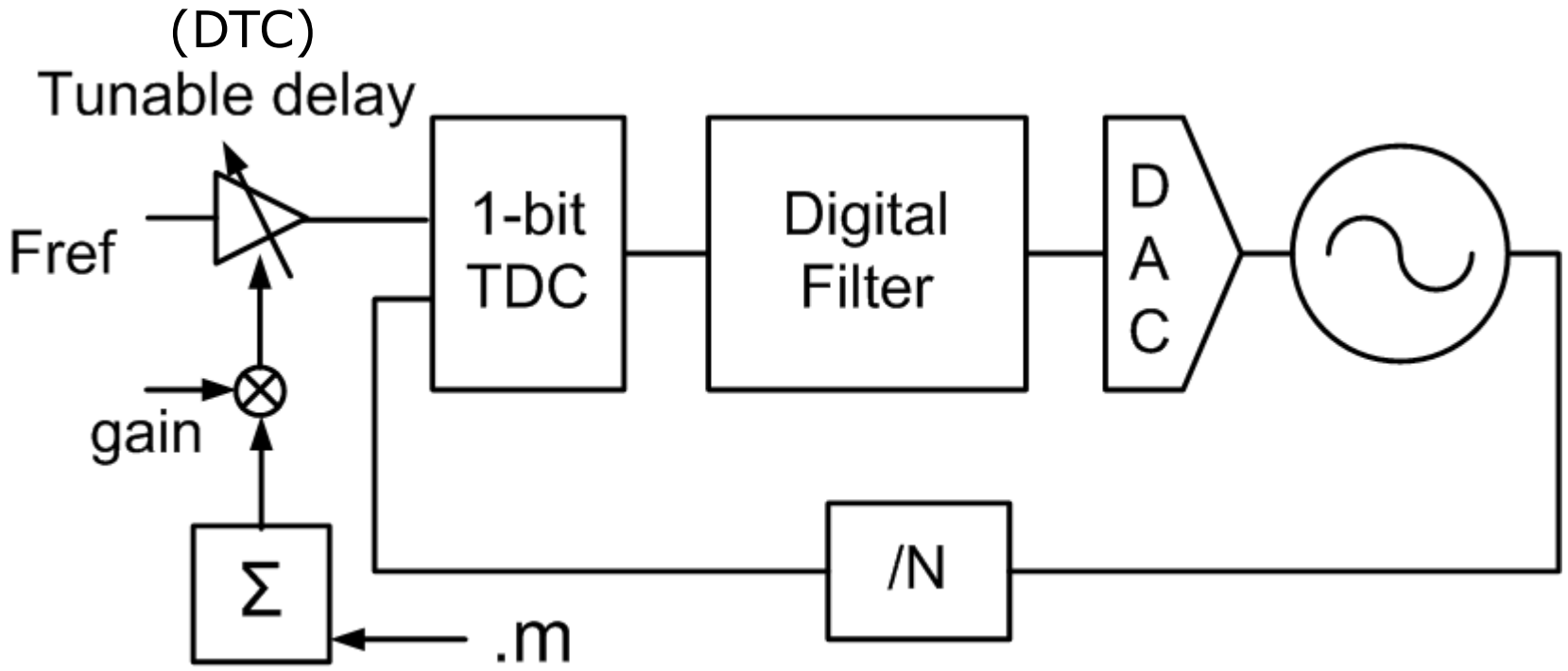


Apply (1) in (2):

$$F_{DCO} = N(F_{ref} + \Delta f) \quad \rightarrow \text{steady state relationship}$$

Alternative Fractional-N arch. with 1-bit TDC (I)

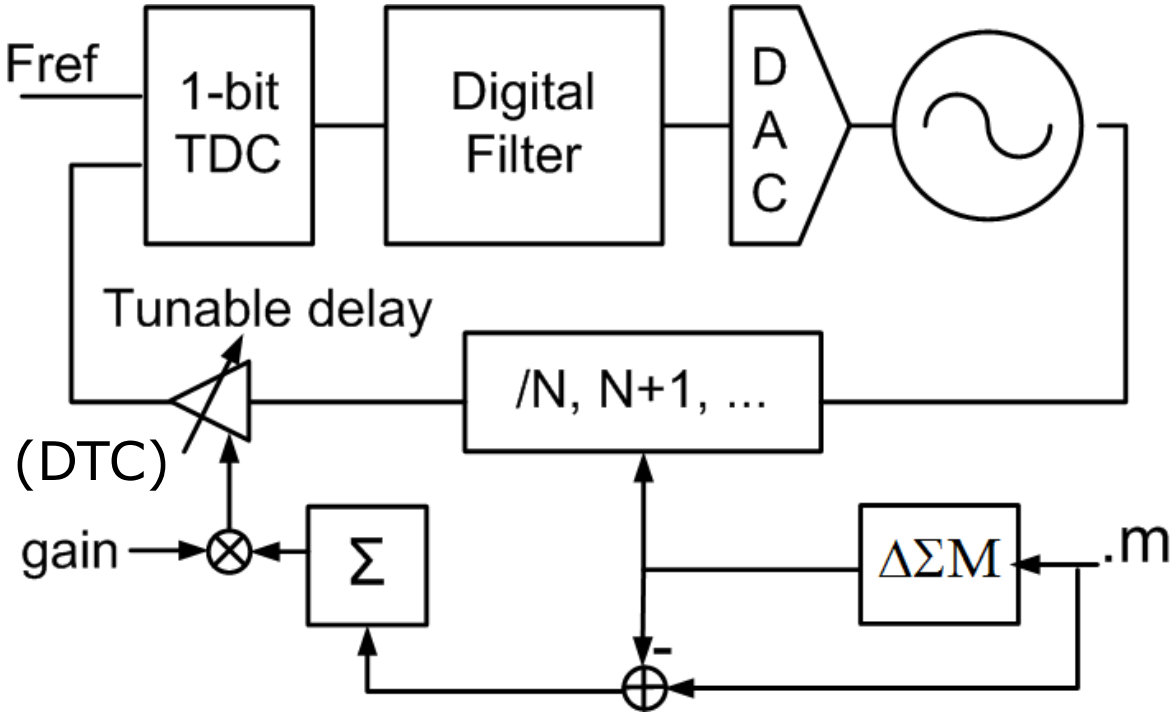
- Introduce fractional delay at PLL input path
- Challenges: digital-to-time converter (DTC) gain and linearity



N. Pavlovic, et al., "A 5.3GHz digital-to-time-converter-based fractional-N all-digital PLL," ISSCC 2011

Alternative Fractional-N arch. with 1-bit TDC (II)

- Introduce additional delay in the feedback path
- Challenges: DTC gain and linearity



D. Tasca, et al., "A 2.9-to-4.0GHz fractional-N digital PLL with bang-bang phase detector and and 560fsrms integrated jitter at 4.5mW power, " ISSCC, 2011

What type of Frac-N topology to use?

- Multi-modulus Frac-N
  - TDC requirement: TDC dynamic range is shorter, as FB signal follows closer to F_{ref} .
  - Divider complexity: more complex multi-modulus divider + commonly used delta-sigma modulator (ΔΣM).
  - Noise: Frac.-N noise can be shaped to higher frequency.

- Frequency Accumulation Frac-N:
  - TDC requirement: TDC dynamic range should cover T_{ref}, as FB signal drifts away from F_{ref} .
  - Divider complexity: simple int-N divider.
  - Noise: Frac.-N noise appears as harmonic tones.
  - Solutions:
    - ➔ Embedded or Injection-Locked TDC solves TDC detection range issue
    - ➔ Feedforward spur cancellation mitigates frac.-N spurs

Any question?

- DPLL basics
- Fractional-N operation principles

Outline

- Basics of PLL
- Fractional-N Operation
- Critical Building Blocks
  - DCO, TDC, Loop Filter
- Challenging Frac-N Design Issues
- New Opportunities
- SOA Fractional-N Digital PLL Examples

Digitally Controlled Oscillator (DCO)

- Voltage controlled oscillator (used in analog PLL):
  - Use continuous voltage to control oscillation frequency

    $F_{vco} = K_{vco} * V_{in}$

    K_{vco} *(Hz/v)*

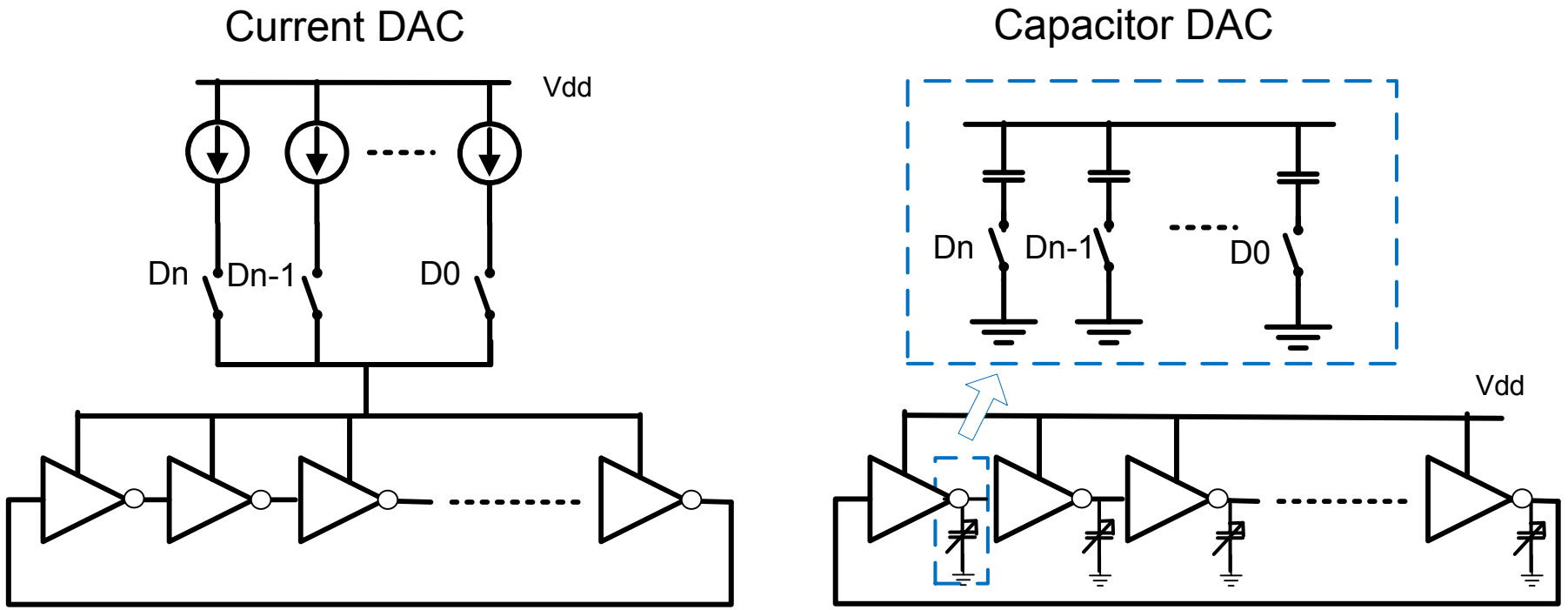
- Digitally controlled oscillator (used in digital PLL):
  - Use digital code to control oscillation frequency

    $F_{dco} = K_{dco} * D_{in}$

    K_{dco} *(Hz/code)*

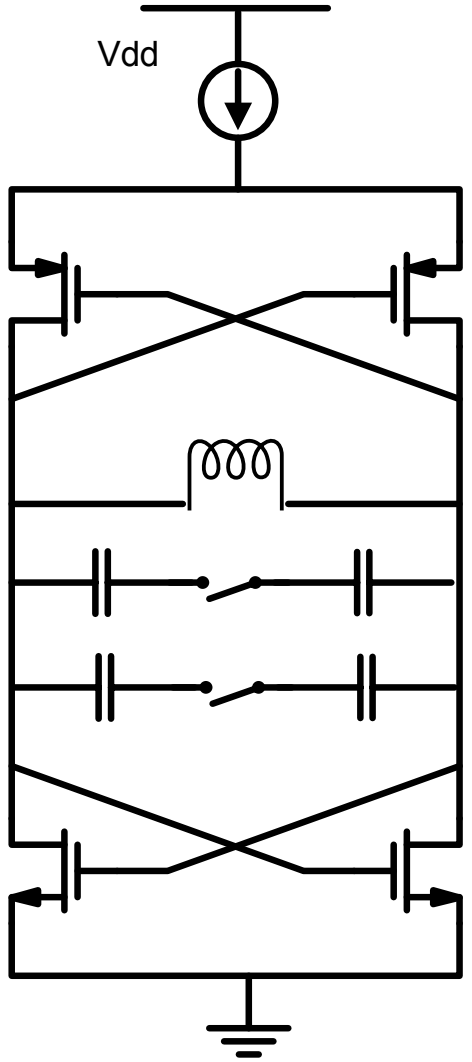
Ring Oscillator Based DCO

- Consume smaller silicon area but worse phase noise
- Popular choice for SoC PLLs
- Current or capacitor DAC array to control RO frequency



LC Based DCO

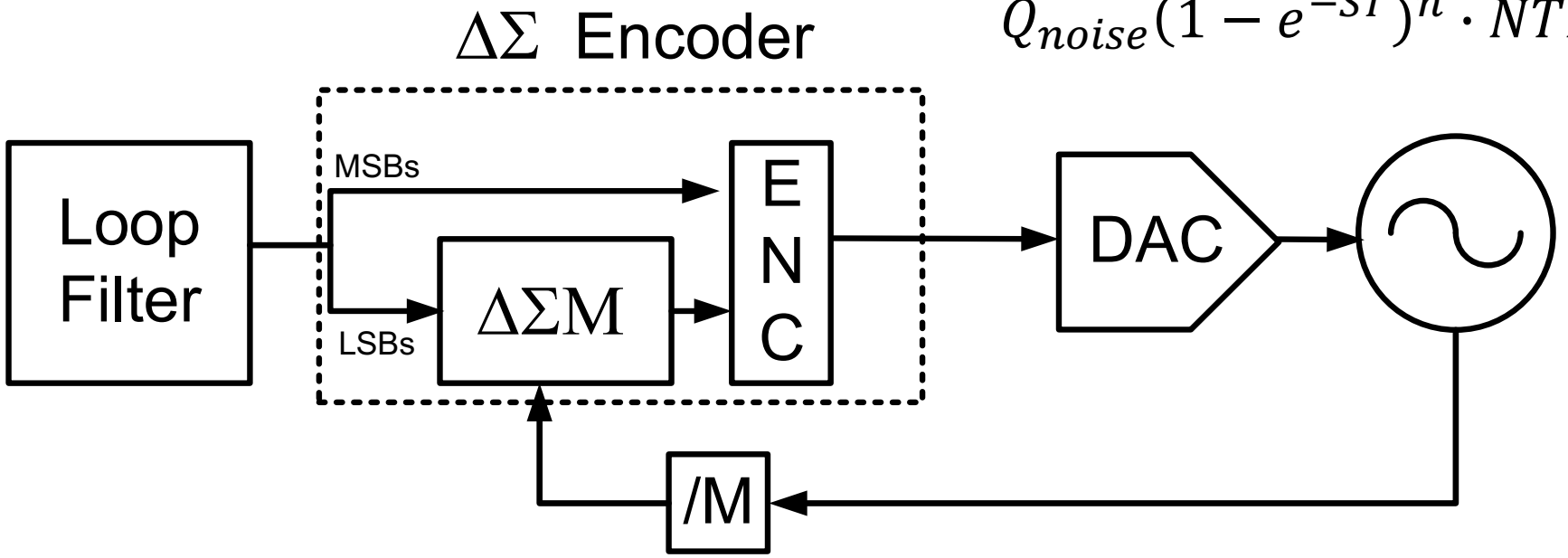
- Bulky but better phase noise, usually used in high performance clock generation
- Switched capacitor array to tune the frequency
- Typically divided into several banks for coarse and fine frequency tuning.
  - The coarse tuning determines the tuning range and PVT.
  - The fine tuning determines the steady-state phase noise.



An Oversampling DAC

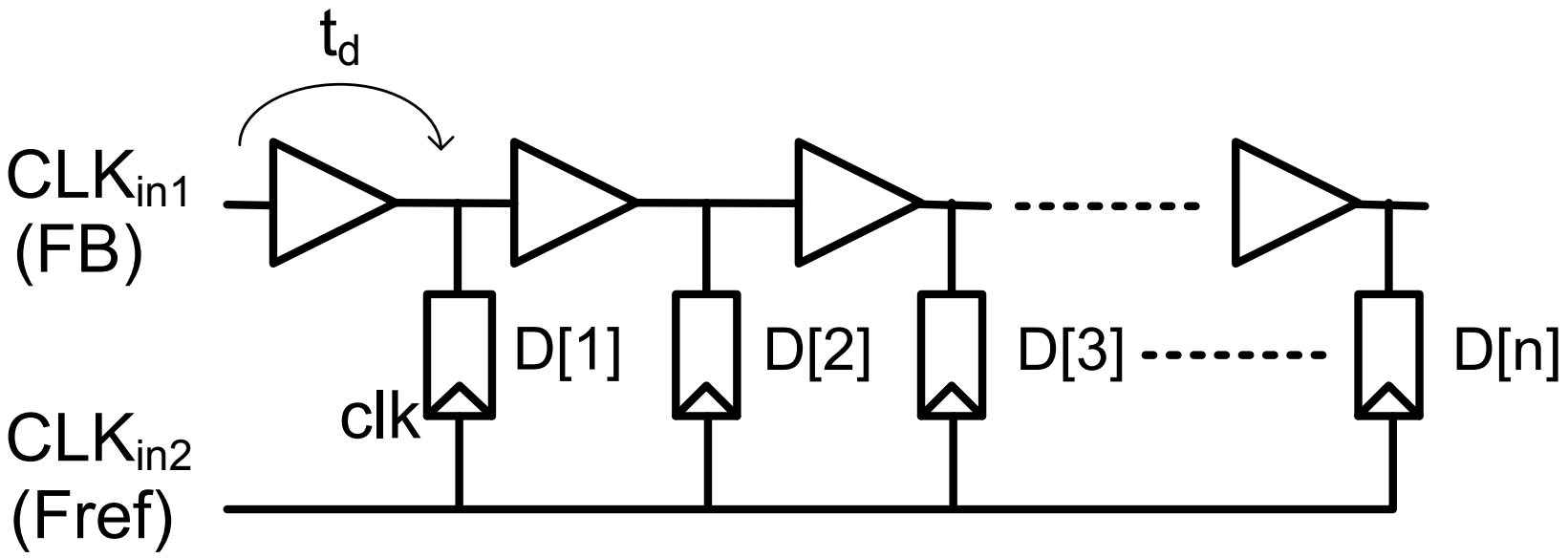
- If LSB of DCO is not sufficiently fine, delta-sigma modulator (ΔΣM) DAC allows finer frequency tuning.
- Oversampling clock rate is typically much higher than F_{ref}.
- ΔΣM quantization noise shaped to higher frequencies, and filtered by bandpass response (i.e. NTF_{DCO} in slide 18).

$$Q_{noise}(1 - e^{-ST})^n \cdot NTF_{DCO}$$



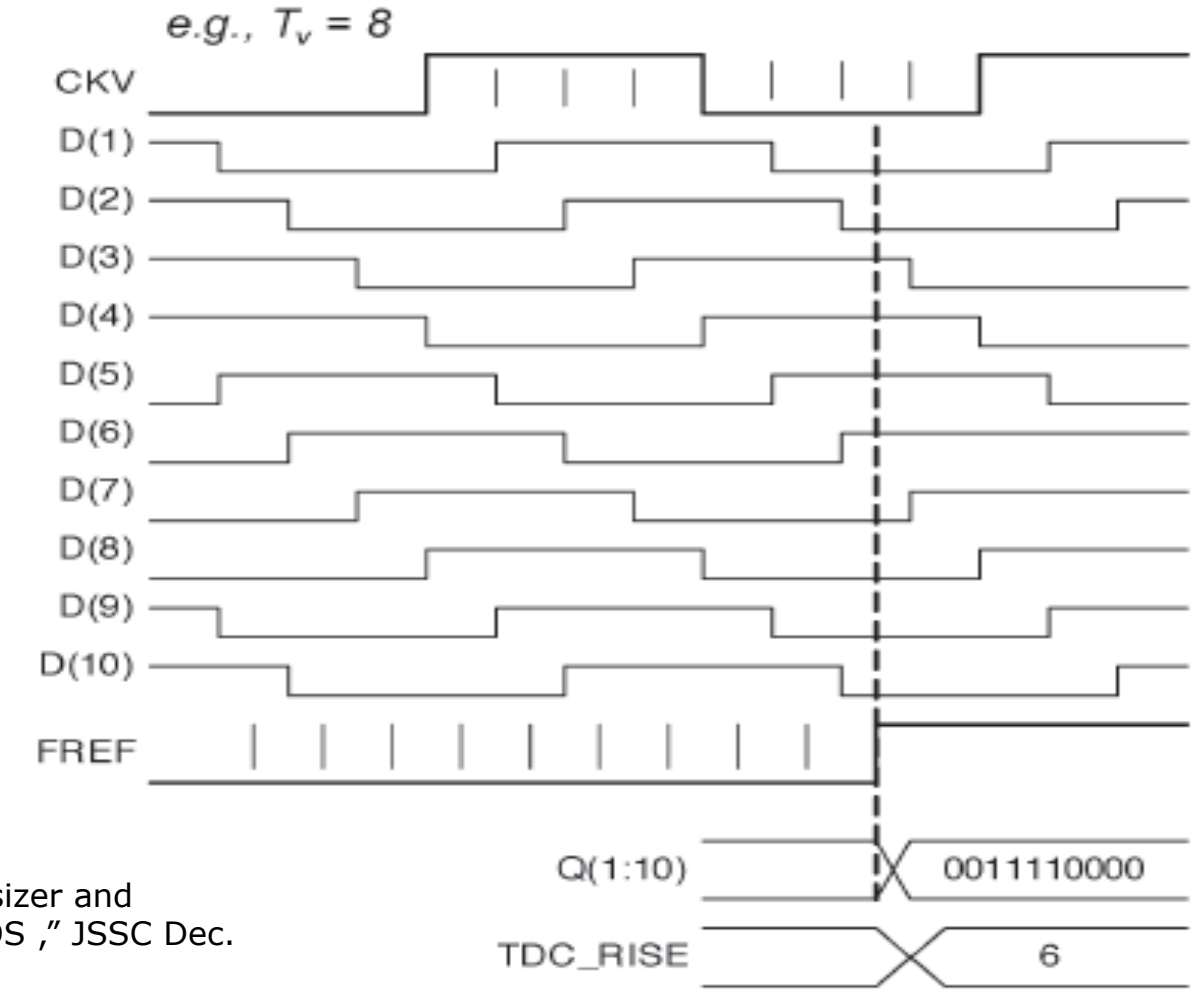
Basic TDC

- A chain of inverters (delay element) as the basis of phase quantization.
- Measure the time difference between feedback and reference clocks.
- Technology scaling helps shorten the inverter delay (t_d)



Time Domain View

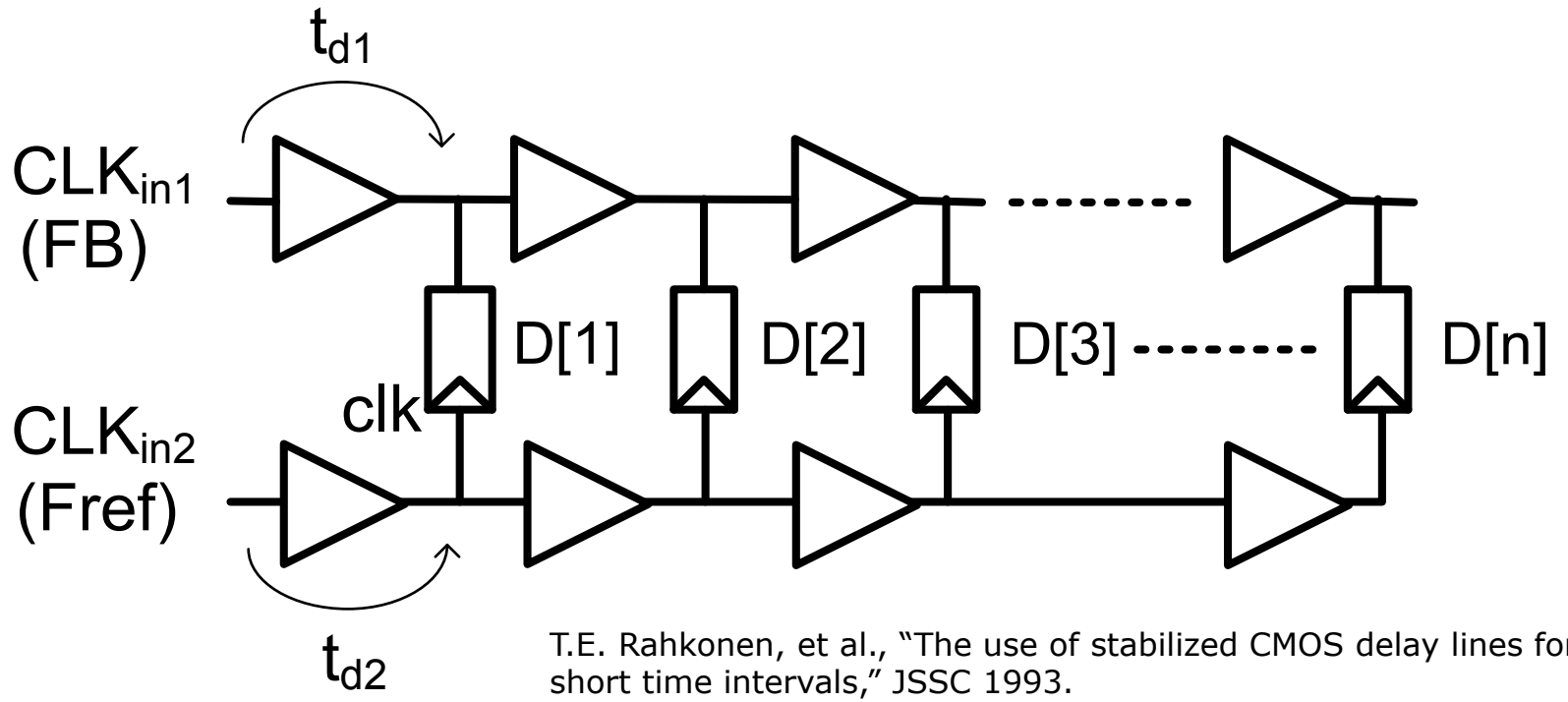
- Cyclic thermometer code
- The time information is quantized at unit delay element.
- The delay must be calibrated.



Ref: R. Staszewski et al., "All-Digital TX Frequency Synthesizer and Discrete-Time Receiver for Bluetooth Radio in 130-nm CMOS ," JSSC Dec. 2004.

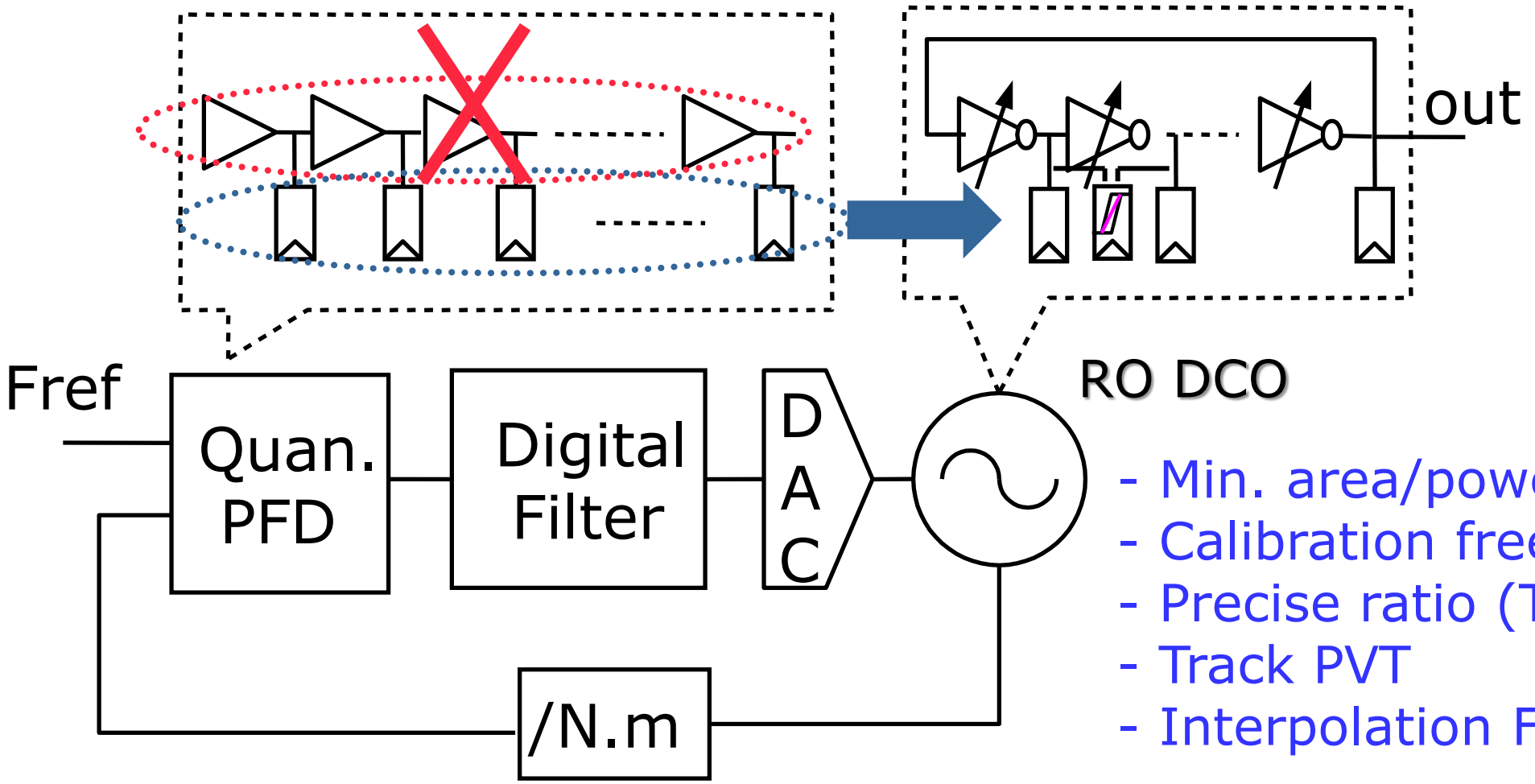
Vernier Delay Line

- Use delay difference ($|t_{d1}-t_{d2}|$) to measure the time.
- Fine resolution (a fraction of an inverter delay), but costly as two delay chains are required
- The time accuracy depends on the matching, and also requires calibration.



T.E. Rahkonen, et al., "The use of stabilized CMOS delay lines for the digitization of short time intervals," JSSC 1993.

Embedded TDC (for RO-based DCO)

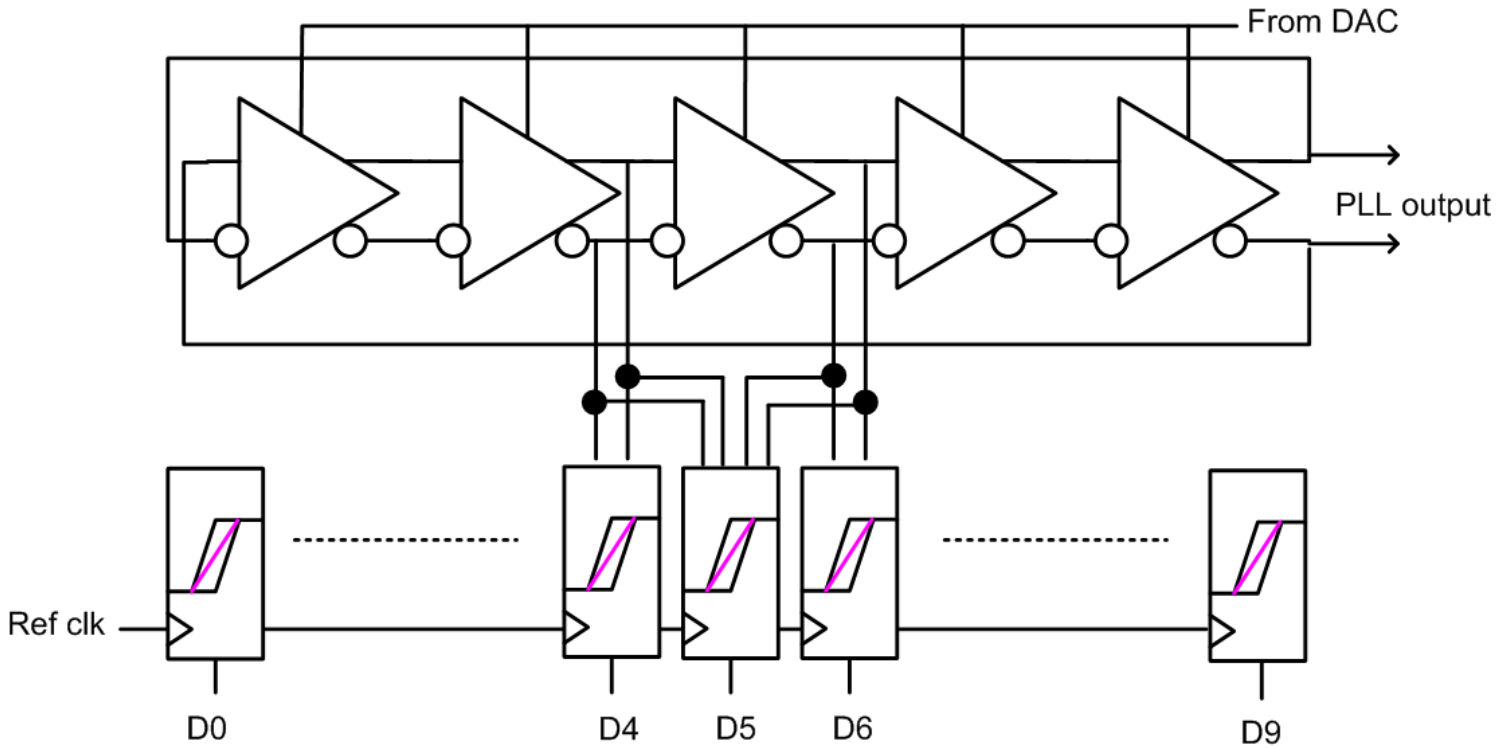


- Min. area/power
- Calibration free
- Precise ratio (Tvco/ΔT)
- Track PVT
- Interpolation Flip flop

M.S.-W. Chen, D. Su, S. Mehta, "A Calibration-Free 800MHz Fractional-N Digital PLL with Embedded TDC," ISSCC 2010/JSSC 2010.

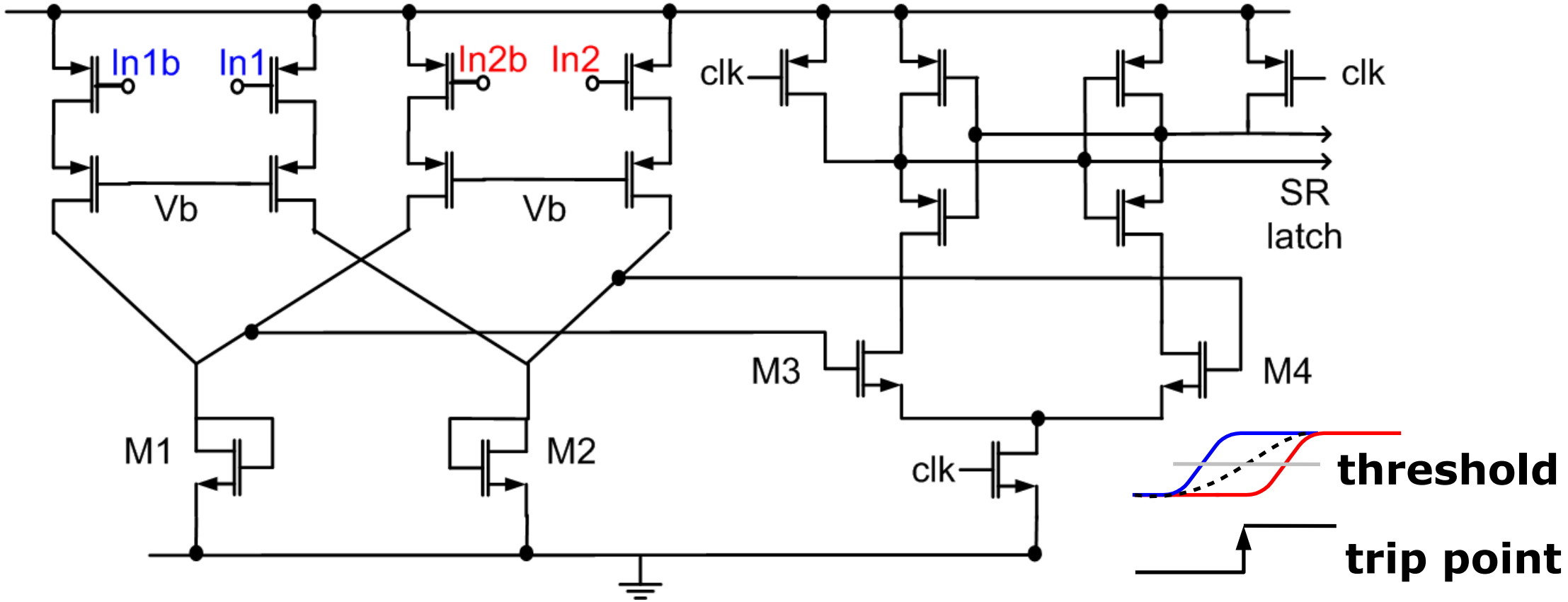
Embedded TDC Scheme

- N differential stages → naturally provide 2·N phases.
- Interpolation flip-flops interpolate between the two inputs and reduce number of delay stages.



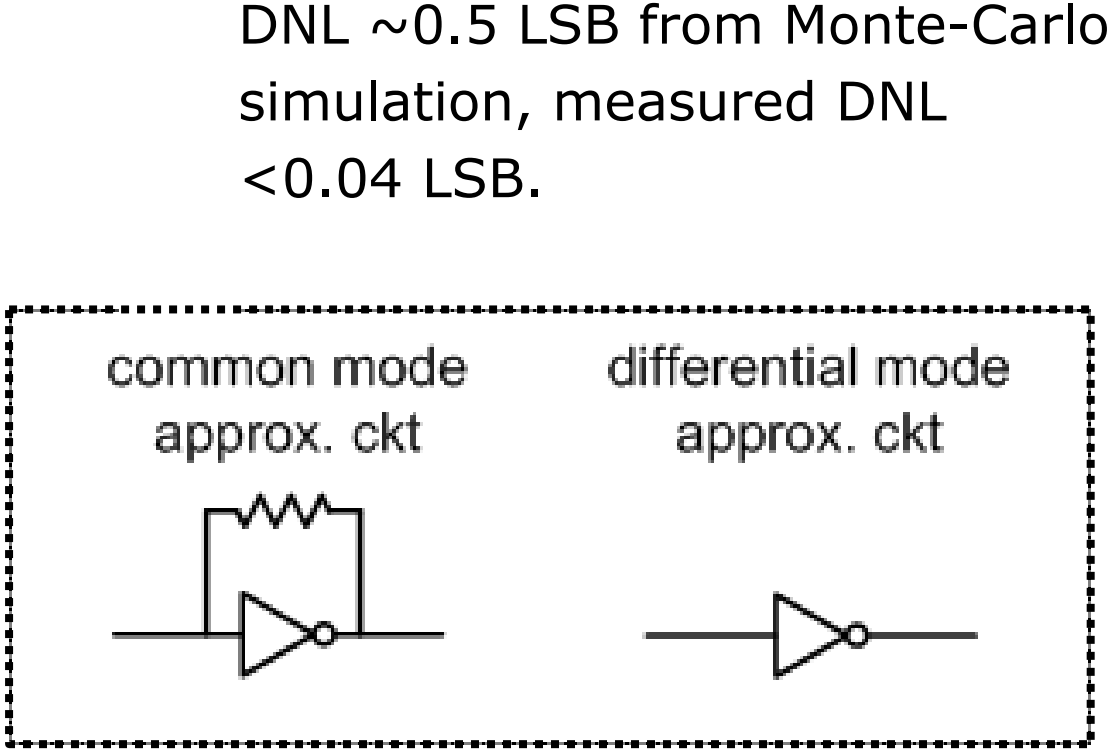
Interpolation Flip-Flop

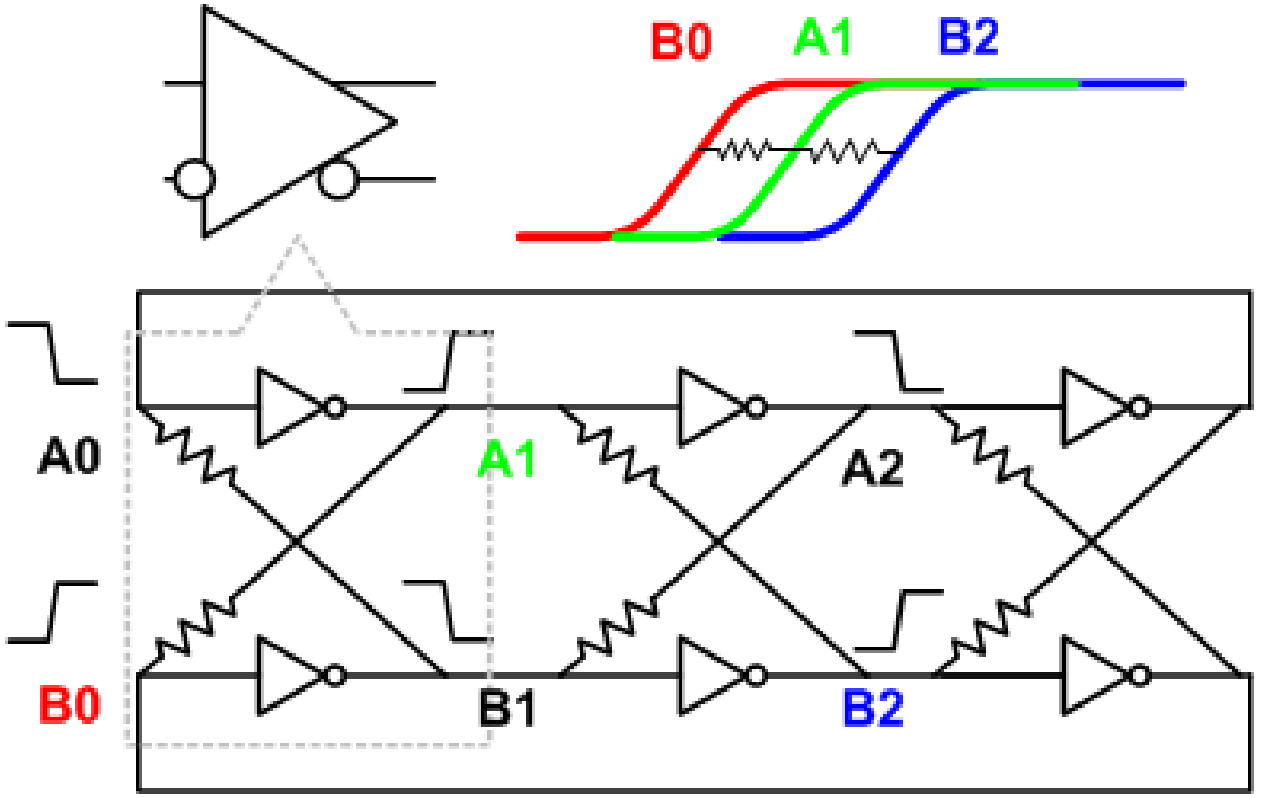
- A flip-flop that interpolates between the two inputs.



Mismatch Filtering Delay Cell

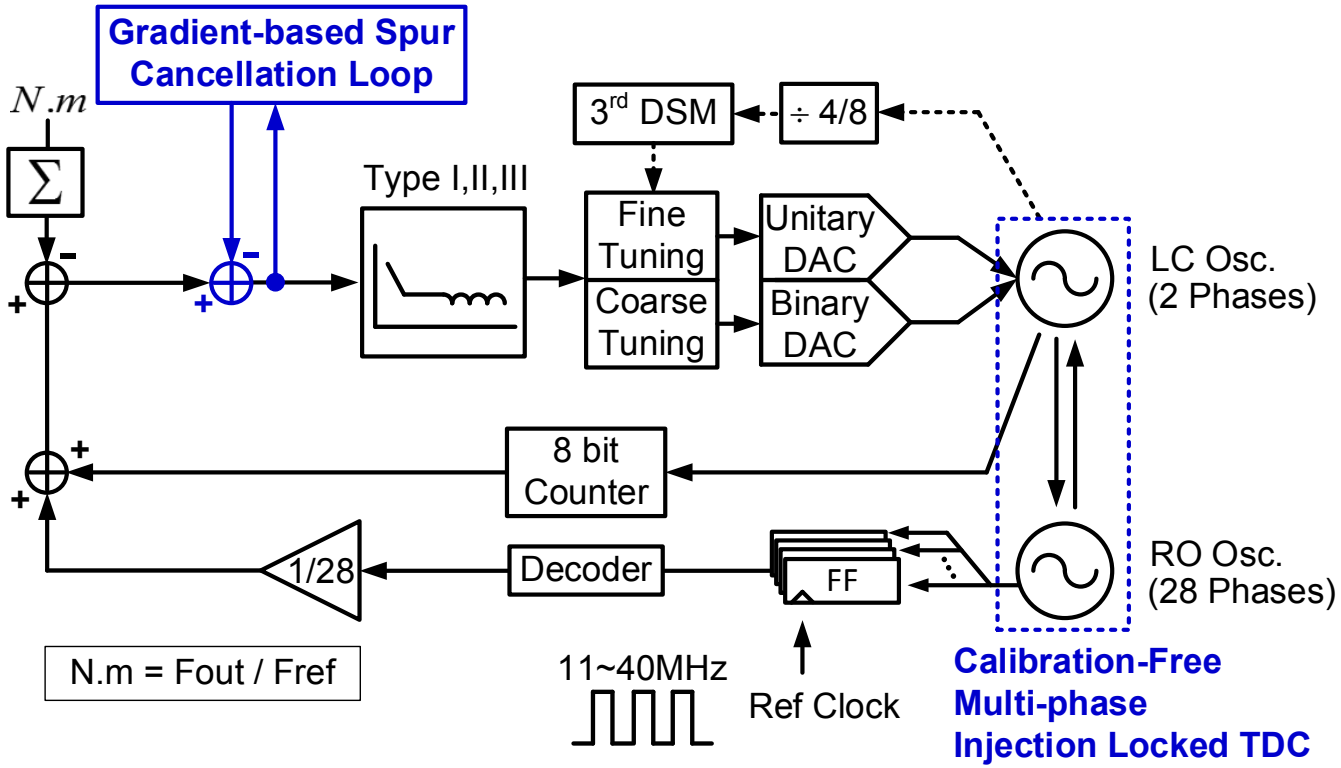
- Resistive divider network to improve DNL
- Without cross-coupled resistors, DNL ~0.5 LSB from Monte-Carlo simulation, measured DNL <0.04 LSB.





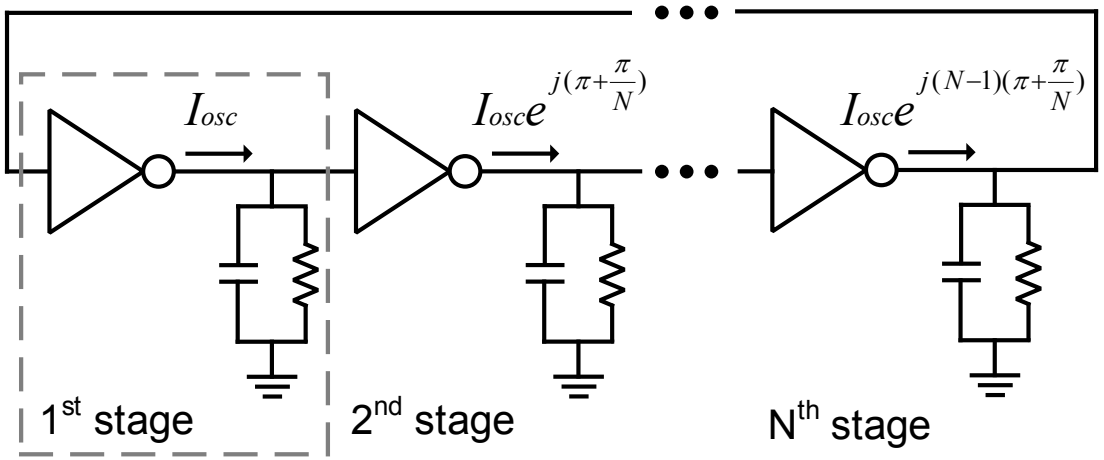
Injection-Locked TDC (for LC-based DCO)

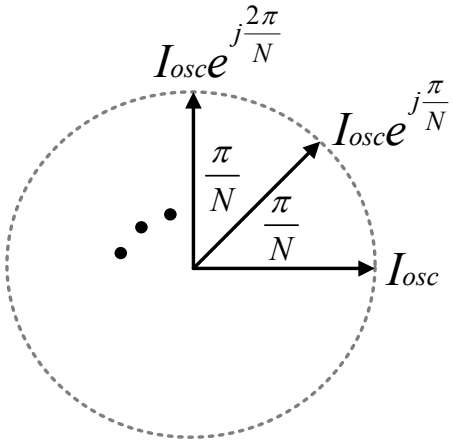
- Proposed Gradient-based Spur Cancellation -> Interference Coupling
- Multi-phase Injection-Locked TDC -> TDC Overhead



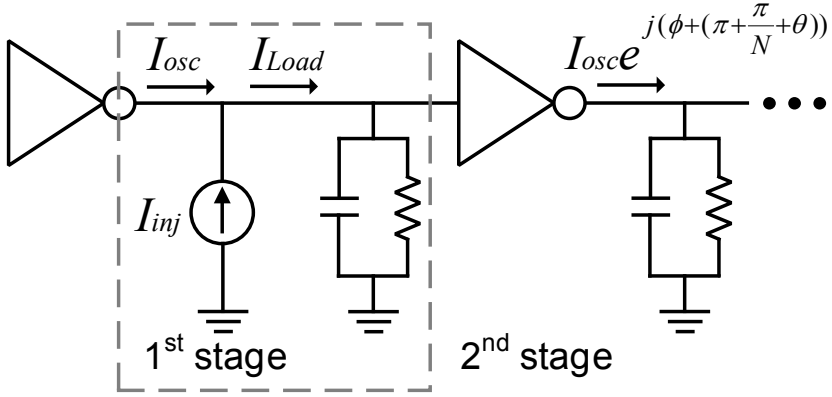
C.R. Ho, M. S.-W. Chen, "A Fractional-N DPLL with Adaptive Spur Cancellation and Calibration-Free Injection-Locked TDC in 65nm CMOS," *RFIC* 2014, TCAS-I 2016.

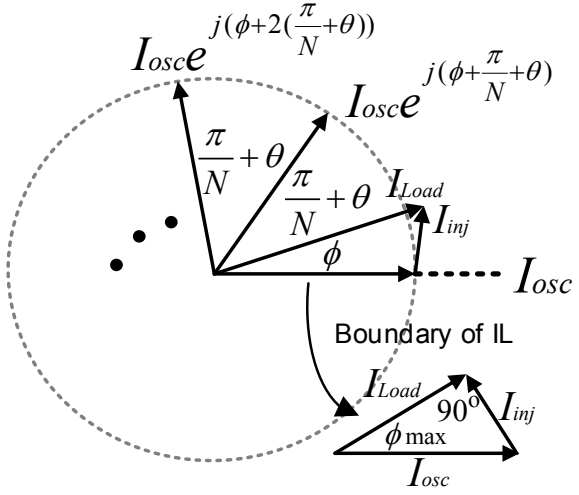
Frequency Locking Range (I)





With injection:





Frequency Locking Range (II)

- Barkhausen criteria:

$$\phi + N\left(\frac{\pi}{N} + \theta + \pi\right) = 2k\pi, \text{ where } k = 1,2,3 \ldots$$

- In the boundary of injection-locking, the maximum phase shift (ϕ_{max}) occurs when the injection current I_{inj} is orthogonal to the output current I_{Load},

$$\phi_{max} \approx \left|\frac{I_{inj}}{I_{osc}}\right|$$

Frequency Locking Range (III)

- Phase shift depends on the frequency difference between DCO (i.e. ω_{inj}) and TDC (i.e. ω_{RO})

$$\tan^{-1}(\tan(\frac{\pi}{N})\frac{\omega_{inj}}{\omega_{RO}}) = \frac{\pi}{N} + \theta$$

- Apply Taylor series expansion → frequency locking range depends on injection strength

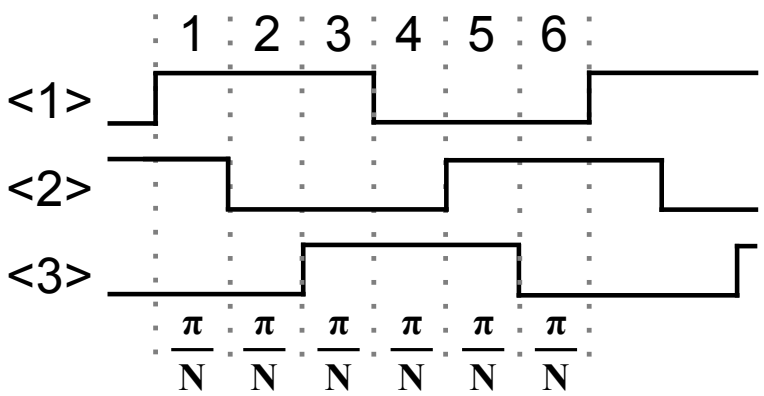
$$\theta \approx \frac{\Delta\omega}{\omega_{RO}}[\sin(\frac{\pi}{N})\cos(\frac{\pi}{N})]$$

$$|\theta| = \frac{1}{N}|\phi| \leq \frac{1}{N}|\phi_{max}|$$

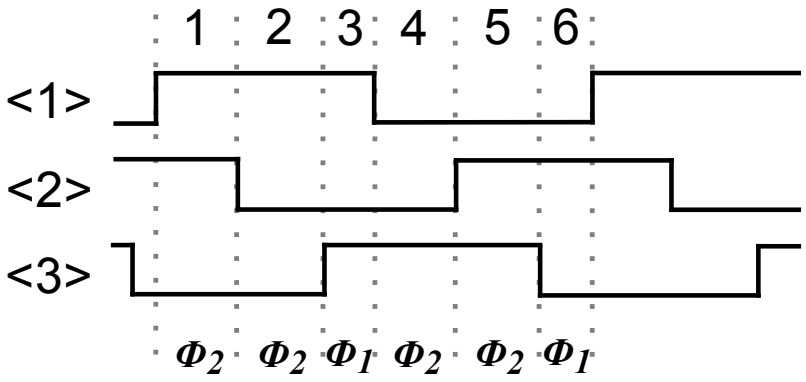
$$\frac{\Delta\omega}{\omega_{RO}} \leq \frac{1}{N}[\frac{1}{\sin(\frac{\pi}{N})\cos(\frac{\pi}{N})}][|\frac{I_{inj}}{I_{osc}}|] = \frac{\omega_{BW,IL}}{\omega_{RO}}$$

DNL of IL TDC (I)

- TDC output waveforms under different injection scenarios

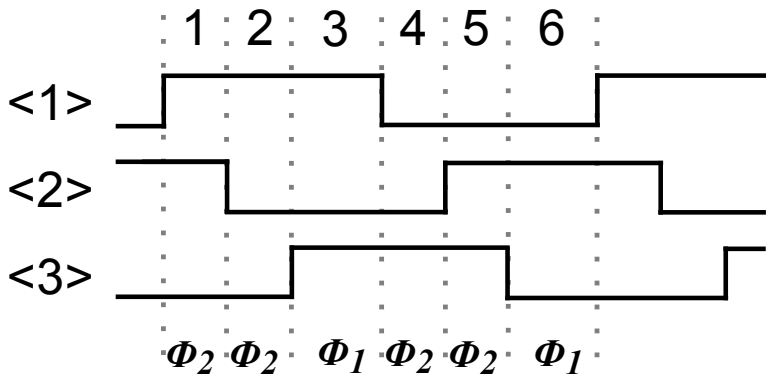


Without injection



With injection:

$$\omega_{inj} = \omega_{RO} + \Delta\omega$$



With injection:

$$\omega_{inj} = \omega_{RO} - \Delta\omega$$

DNL of IL TDC (II)

$$\Phi 1 = \pi/N + \theta + \phi = \pi/N + (1-N)\theta$$

$$\Phi 2 = \pi/N + \theta$$

- Replace θ with Taylor approximation

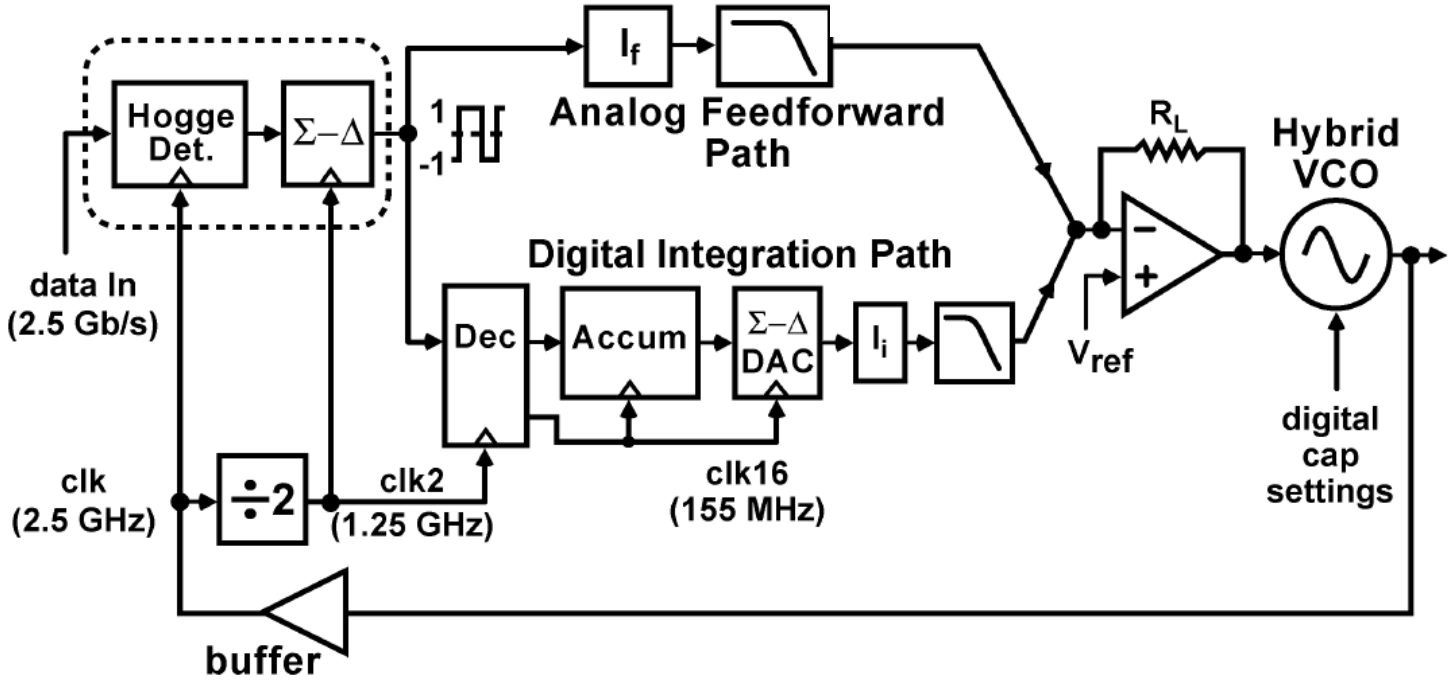
$$\mathrm{DNL1} = \frac{N(1-N)}{\pi}\frac{\Delta\omega}{\omega_{RO}}\left[\sin\left(\frac{\pi}{N}\right)\cos\left(\frac{\pi}{N}\right)\right]$$

$$\mathrm{DNL2} = \frac{N}{\pi}\frac{\Delta\omega}{\omega_{RO}}\left[\sin\left(\frac{\pi}{N}\right)\cos\left(\frac{\pi}{N}\right)\right]$$

Note: This DNL analysis considers the injection lock only → reduce Δω!

Mixed-Signal Loop Filter

- A hybrid of digital and analog loop filter is possible.
- Proportional path in analog domain and the integral path in digital domain.



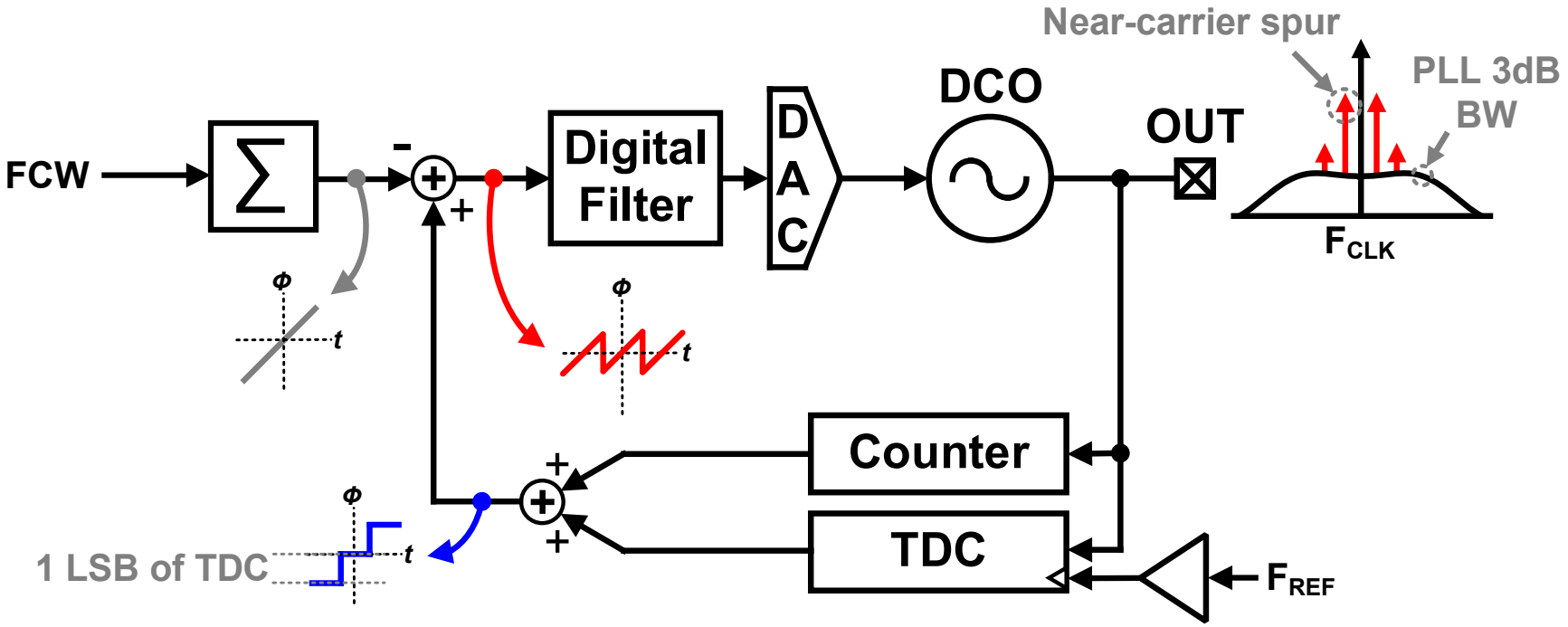
M.H. Perrott, et al., "A 2.5 Gb/s Multi-Rate 0.25µm CMOS CDR Utilizing a Hybrid Analog/Digital Loop Filter," ISSCC 2006

Outline

- Basics of PLL
- Fractional-N Operation
- Critical Building Blocks
- Challenging Fractional-N Design Issues
- New Opportunities
- SOA Fractional-N Digital PLL Examples

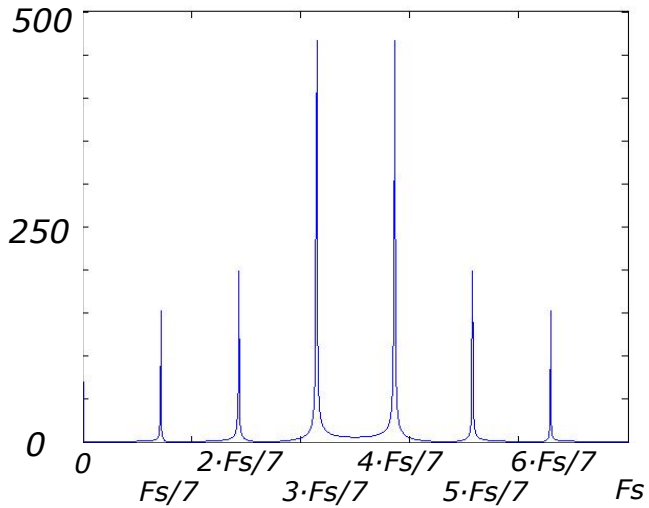
What causes fractional spur?

- In frequency accumulation type of Frac.-N DPLL, the sawtooth quantization noise pattern causes harmonic tones at fractional frequencies.
- Example: a frac. divider ratio of 16.25 generates spurs at integer multiples of $0.25*F_{ref}$ from DCO's oscillation frequency.



What causes fractional spur?

- In multi-modulus type of frac.-N DPLL, the limit cycles of ΔΣM causes the fractional-N spurs.
- Example: a 1-bit quantizer and first-order ΔΣM loop, a DC input of 1/7 will make quantizer output [1 1 -1 1 -1 1 -1] and repeat itself → ΔΣM output spectrum shows integer harmonics of *Fs*/7, where *Fs* is the sample rate of ΔΣM.

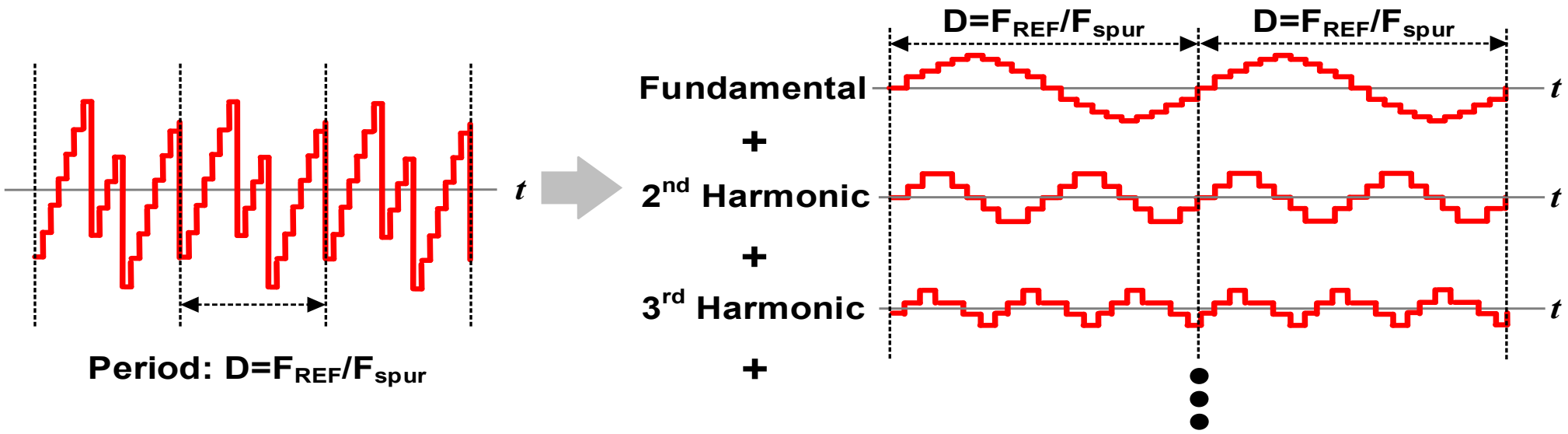


- Use higher order ΔΣM or dithering inside the ΔΣM loop can help.

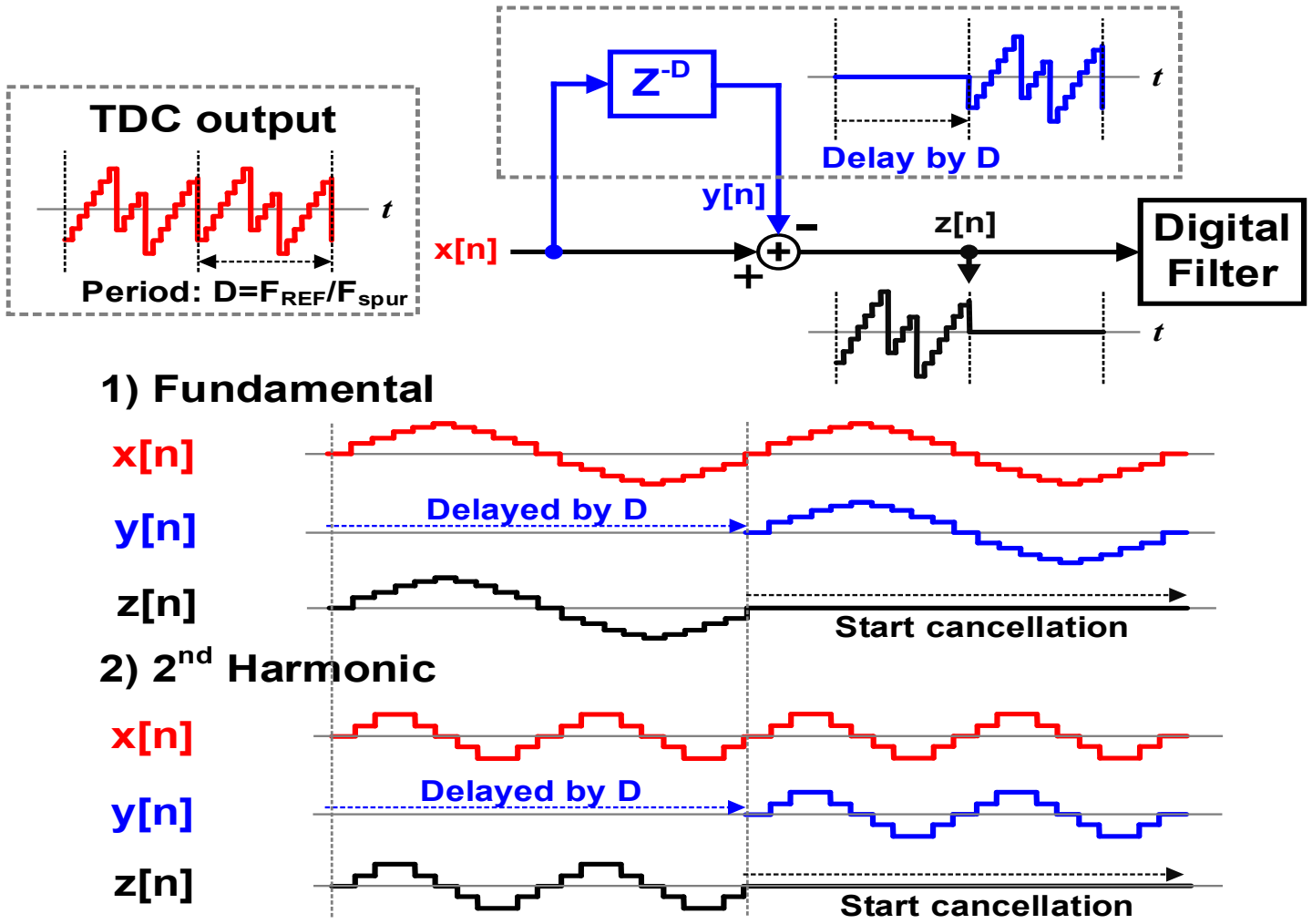
Feedforward Direct Spur Cancellation

Decomposition of Spur Pattern

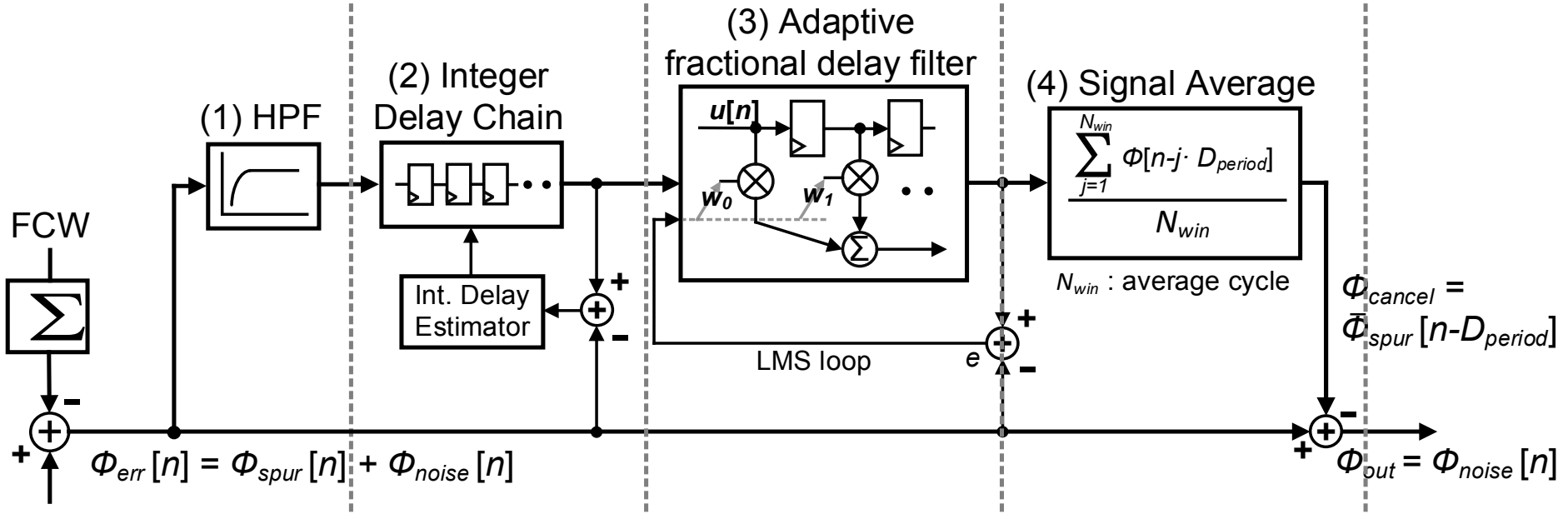
- Spur period (D) is determined by its fundamental.
- Example, if divider ratio is 16.25, D=4.



Feedforward Spur Cancellation



Block Diagram of Cancellation Scheme

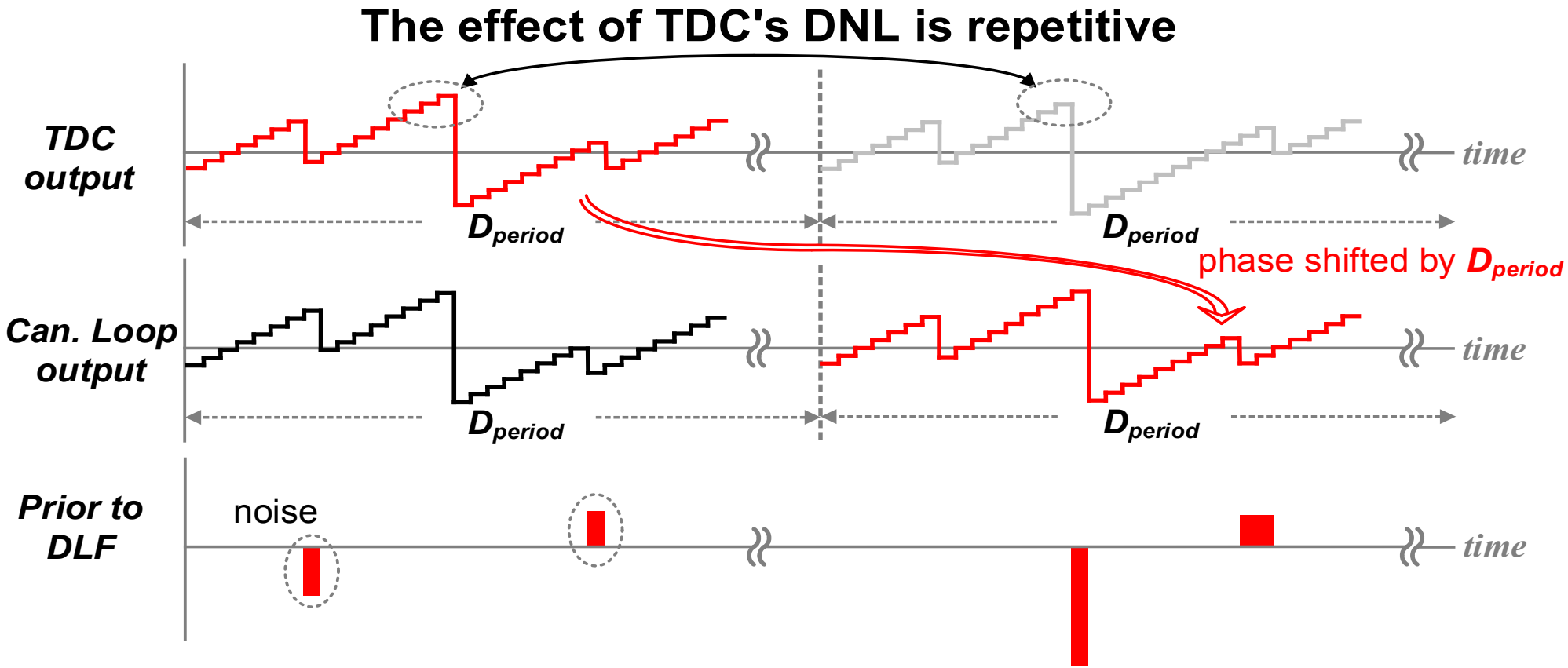


- **Compensate DC gain degradation**
- **Filter in-band noise component**
- **Provide integer period of delay**
- **Provide sub-period delay**
- **Filter noise at spur frequencies**
- **Provide fractional averaging**

C.R. Ho, M. S.-W. Chen, "A Digital PLL with Feedforward Multi-Tone Spur Cancelation Loop Achieving <-73dBc Fractional Spur and <-110dBc Reference Spur in 65nm CMOS," ISSCC, Feb. 2016.

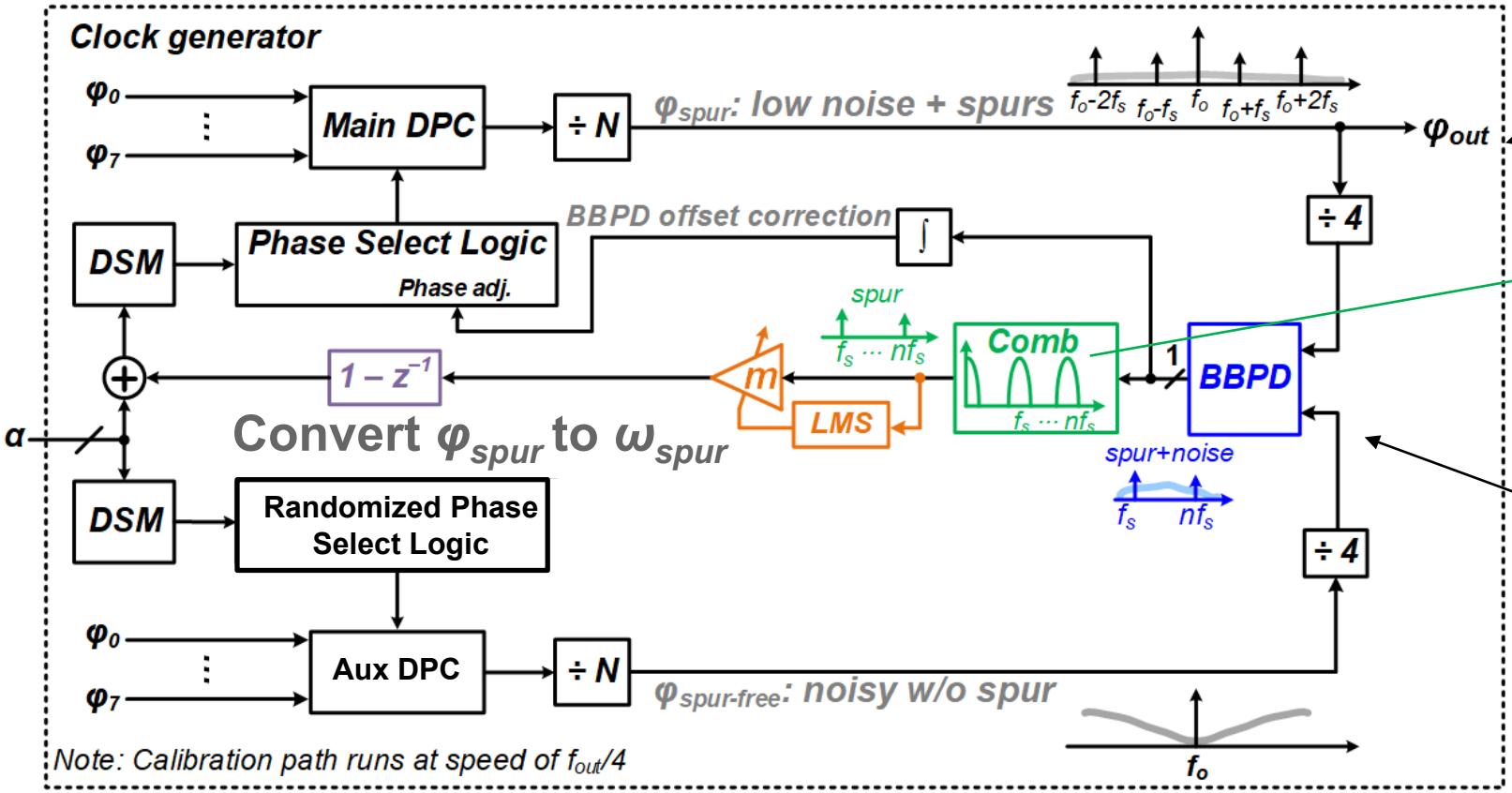
DNL-insensitive Fractional-N Spur Cancellation

- Sawtooth pattern and DNL error are cancelled altogether.
- A direct spur cancellation scheme



Direct Spur Cancellation Extension

- Extract and cancel harmonic spurs outside of DPLL loop



Low noise main clock

Comb-filter based harmonic spur extraction

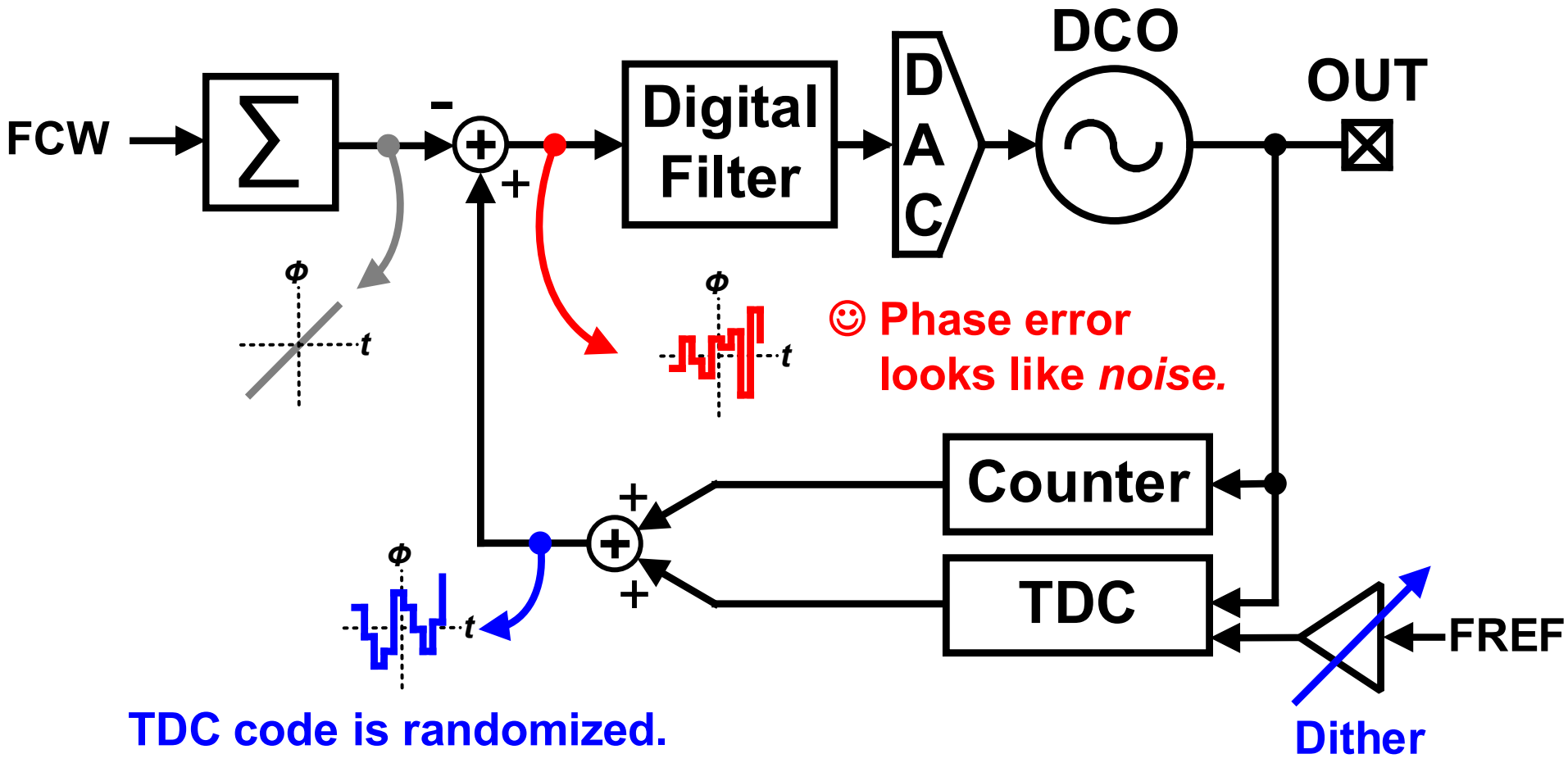
Noisy, but spur-free auxiliary clock

S.Y. Hung, S. Pamarti, "A 0.5-to-2.5GHz Multi-Output Fractional Frequency Synthesizer with 90fs Jitter and -106dBc Spurious Tones Based on Digital Spur Cancellation," ISSCC, Feb. 2019.

Dither-based Spur Mitigation

Randomize Spur Pattern

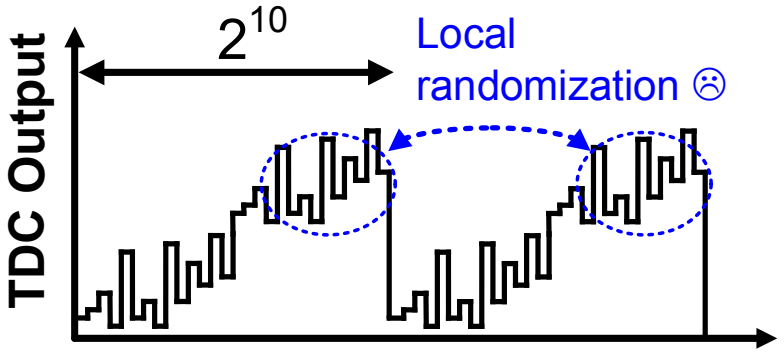
- Dither is used to smear out spurious tones.



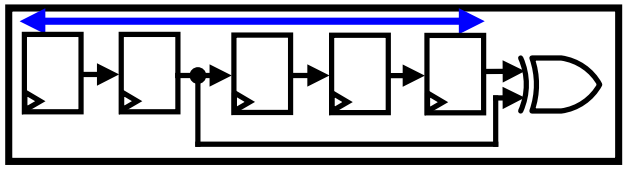
Hardware Complexity of Dither Generator

- Example: FCW = $120+2^{-10}$ and spur period = 2^{10}.

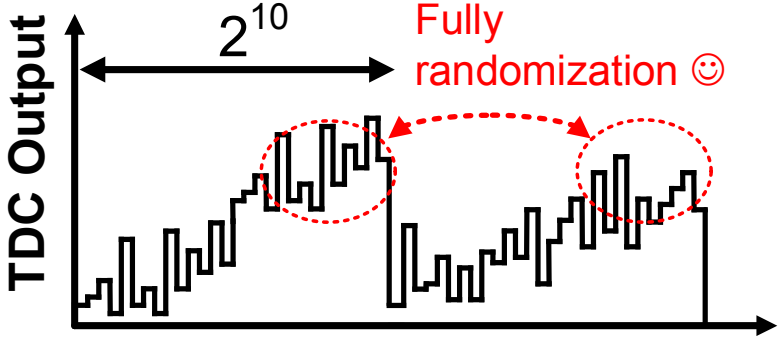
Dither signal, length of 2^5



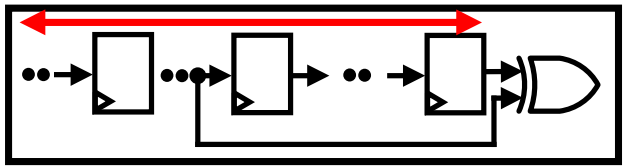
5 Stage of DFFs



Dither signal, length of 2^{20}

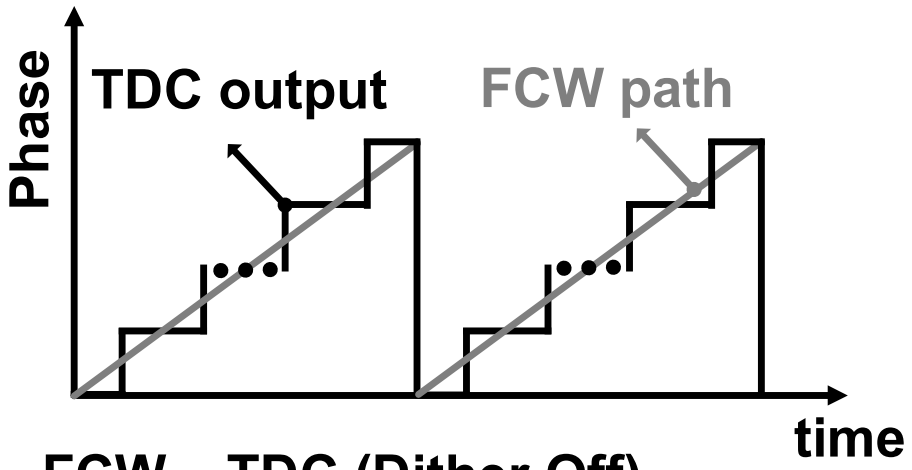


20 Stage of DFFs

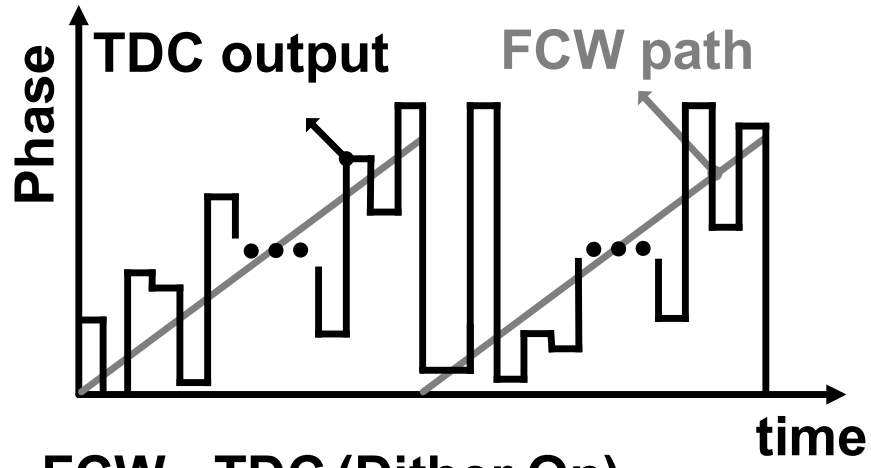


Hardware complexity = O(n)

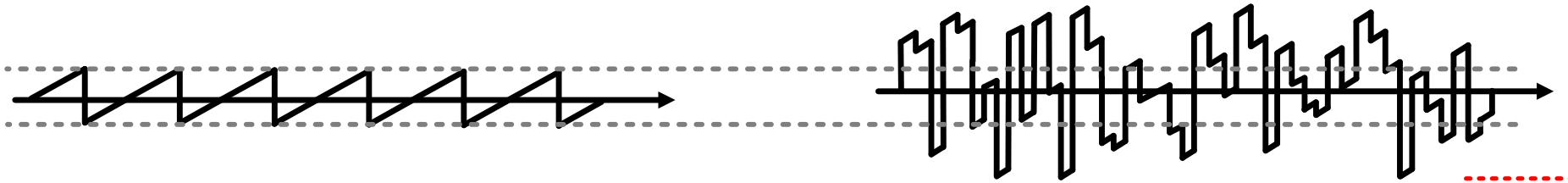
Challenge: Noise Degradation due to Dither



FCW – TDC (Dither Off)



FCW - TDC (Dither On)



$$= \sum_{m} A_m \cdot \sin\left(2\pi \cdot m \cdot \frac{k}{2^n}\right)$$

Fourier expansion of sinusoids

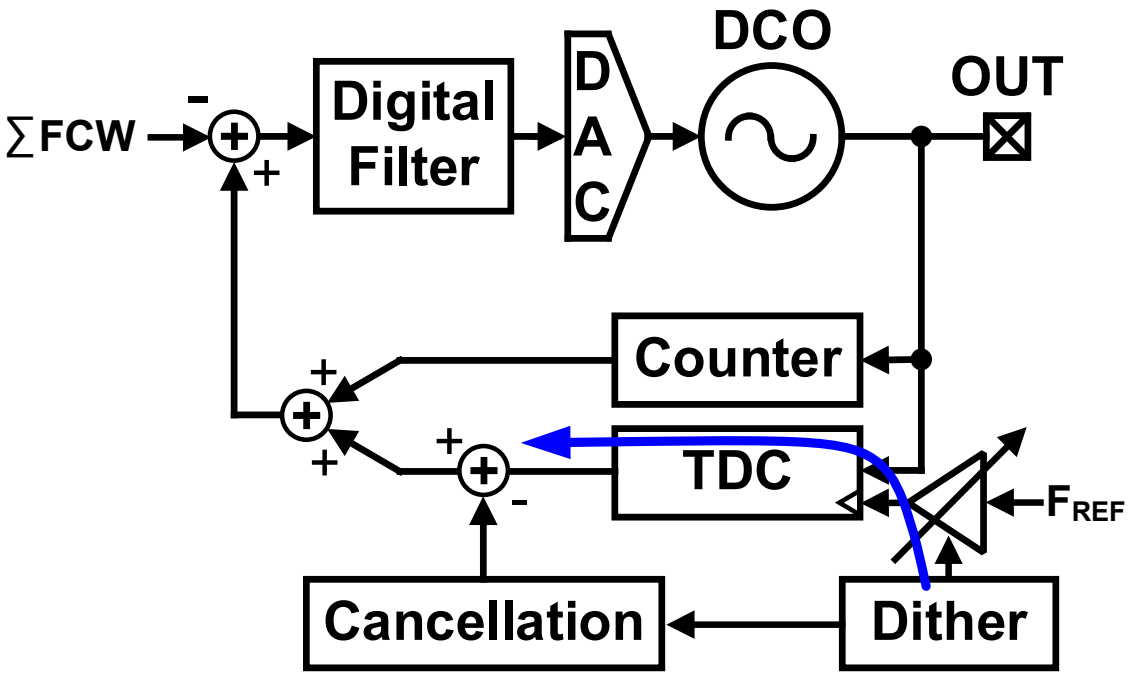
$$= \Phi_{Dither} + \sum_{n} A_n \cdot \sin\left(2\pi \cdot n \cdot \left\{\frac{k}{2^n} + \frac{\Phi_{Dither}}{\Phi_{DCO}}\right\}\right)$$

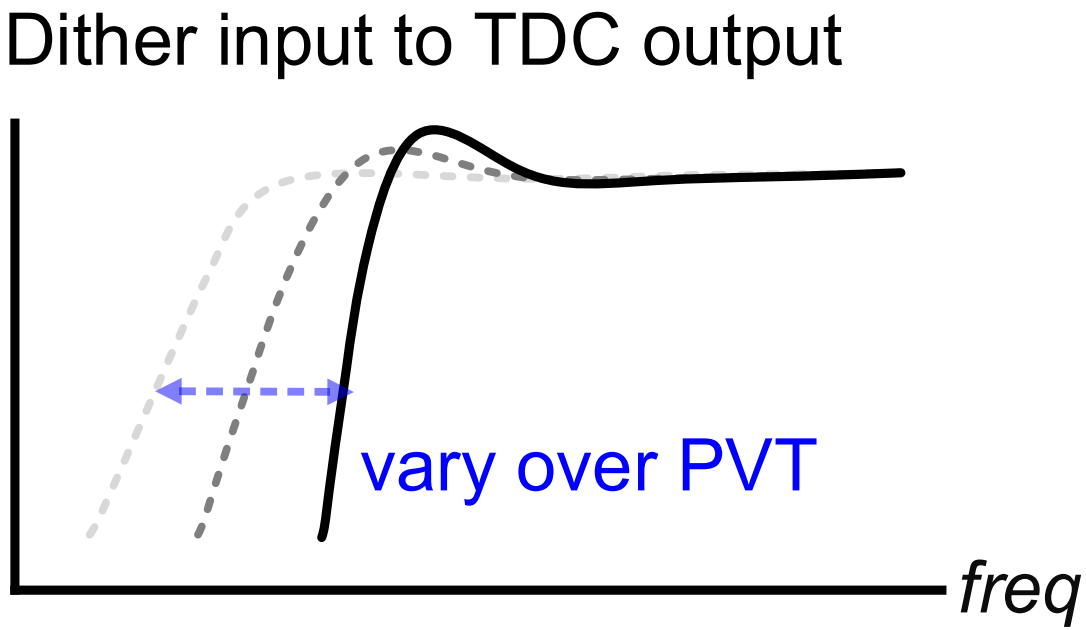
Dither signal☹

Quantization error is phase modulated ☺

Challenge: Volt. and Temp. Variations

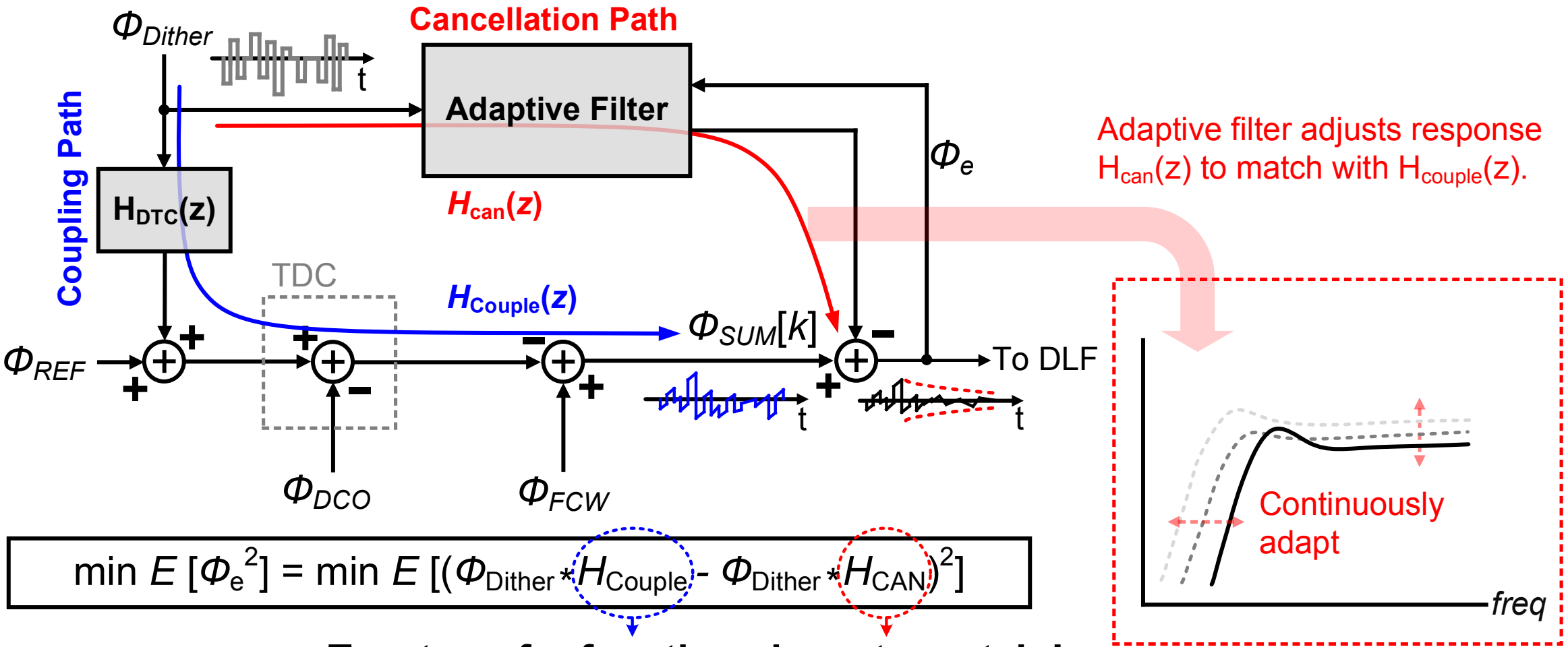
- Loop dynamic changes due to DCO, TDC and DTC gain variation under PVT





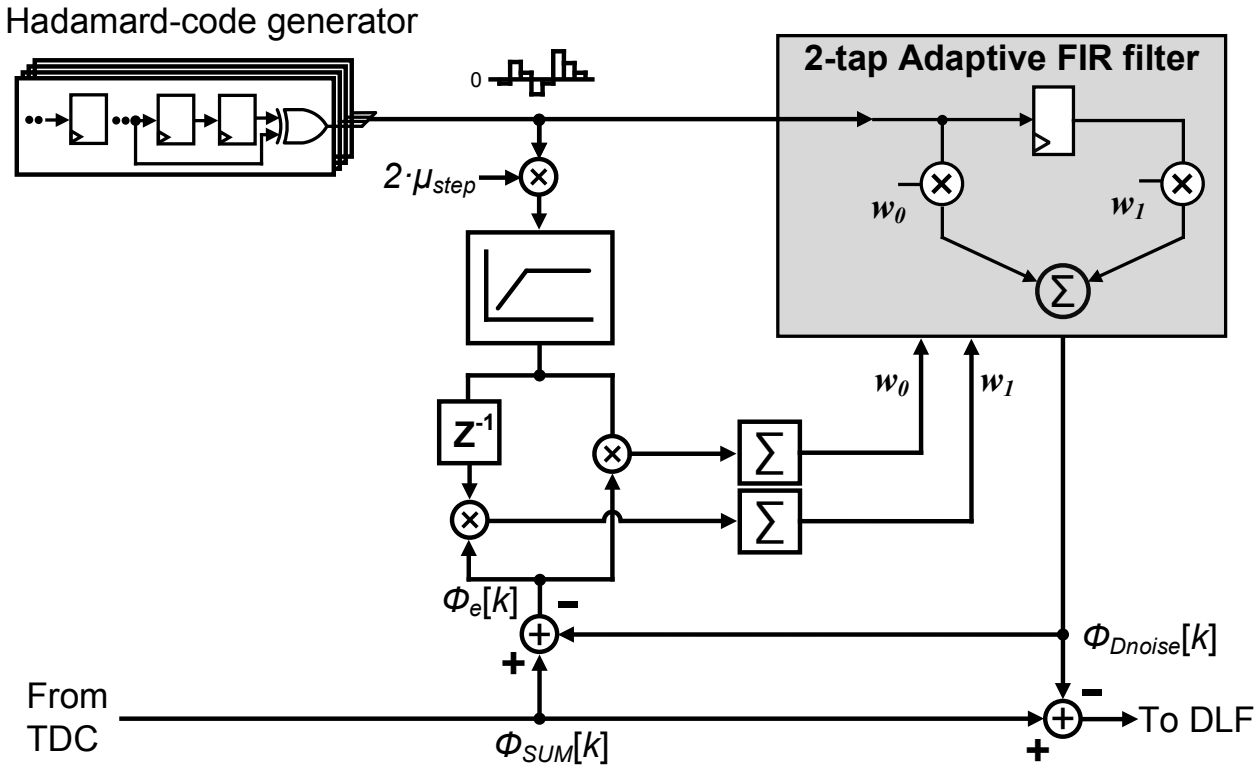
Require cancellation loop to adapt over PVT.

Background Dither Cancellation Loop



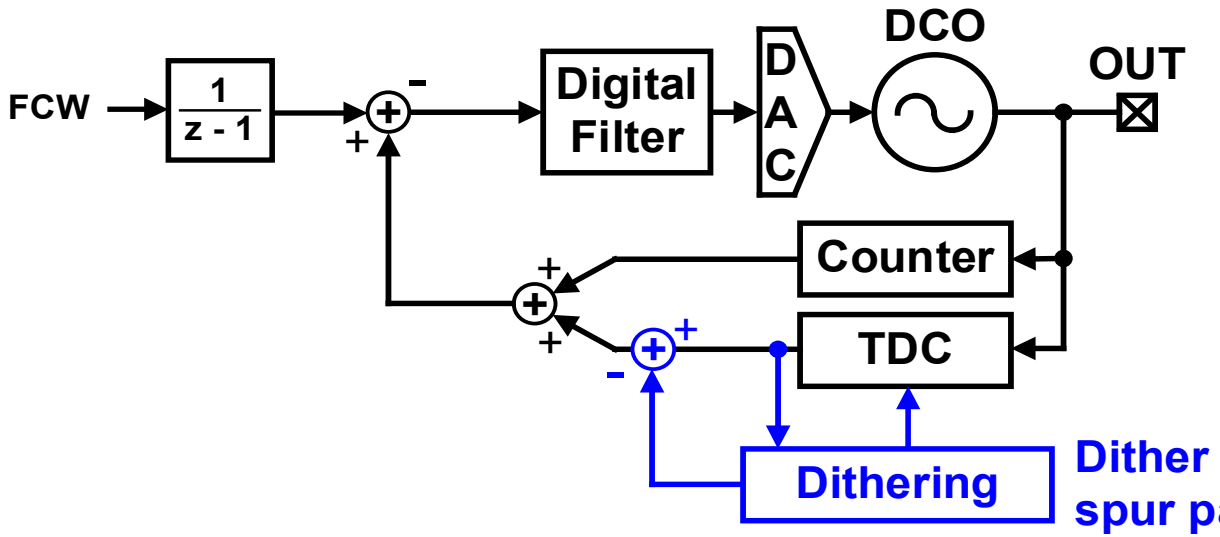
Implementation Block Diagram

- A 2-tap FIR filter is used to compensate the gain and phase variation.

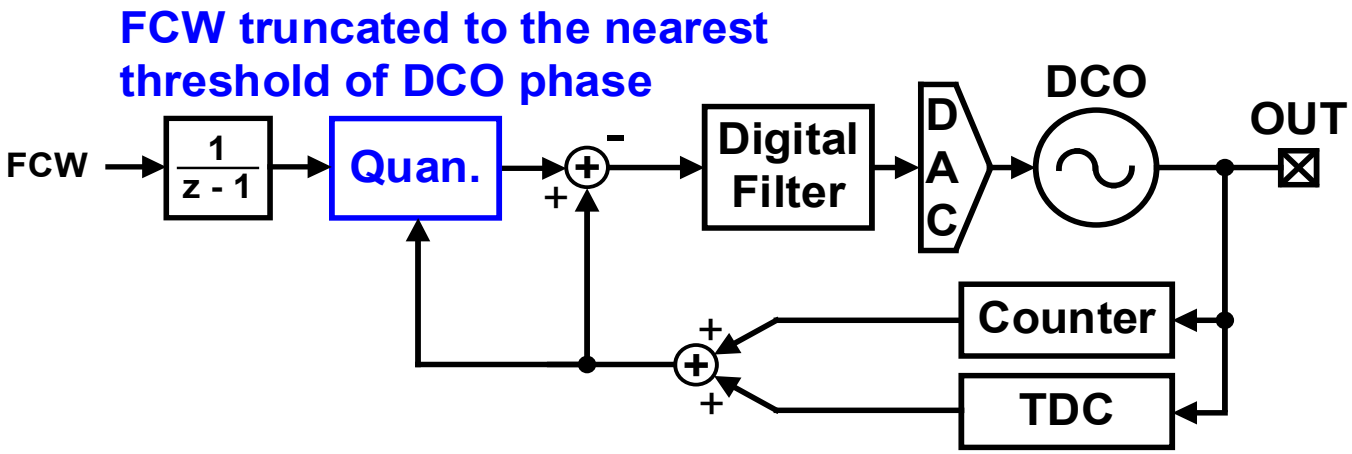


C.R. Ho, M. S.-W. Chen, "A fractional-N digital PLL with background dither noise cancellation loop achieving <-62.5dBc worst-case near-carrier fractional spur in 65nm CMOS," ISSCC, Feb. 2018.

More Frac.-N Spur Mitigations



C. Weltin-Wu et al, "A 3.5GHz wideband ADPLL with fractional spur suppression through TDC dithering and feedforward compensation," ISSCC 2010



F. Opteynde, "A 40nm CMOS All-Digital Fractional-N Synthesizer without Requiring Calibration ," ISSCC 2012

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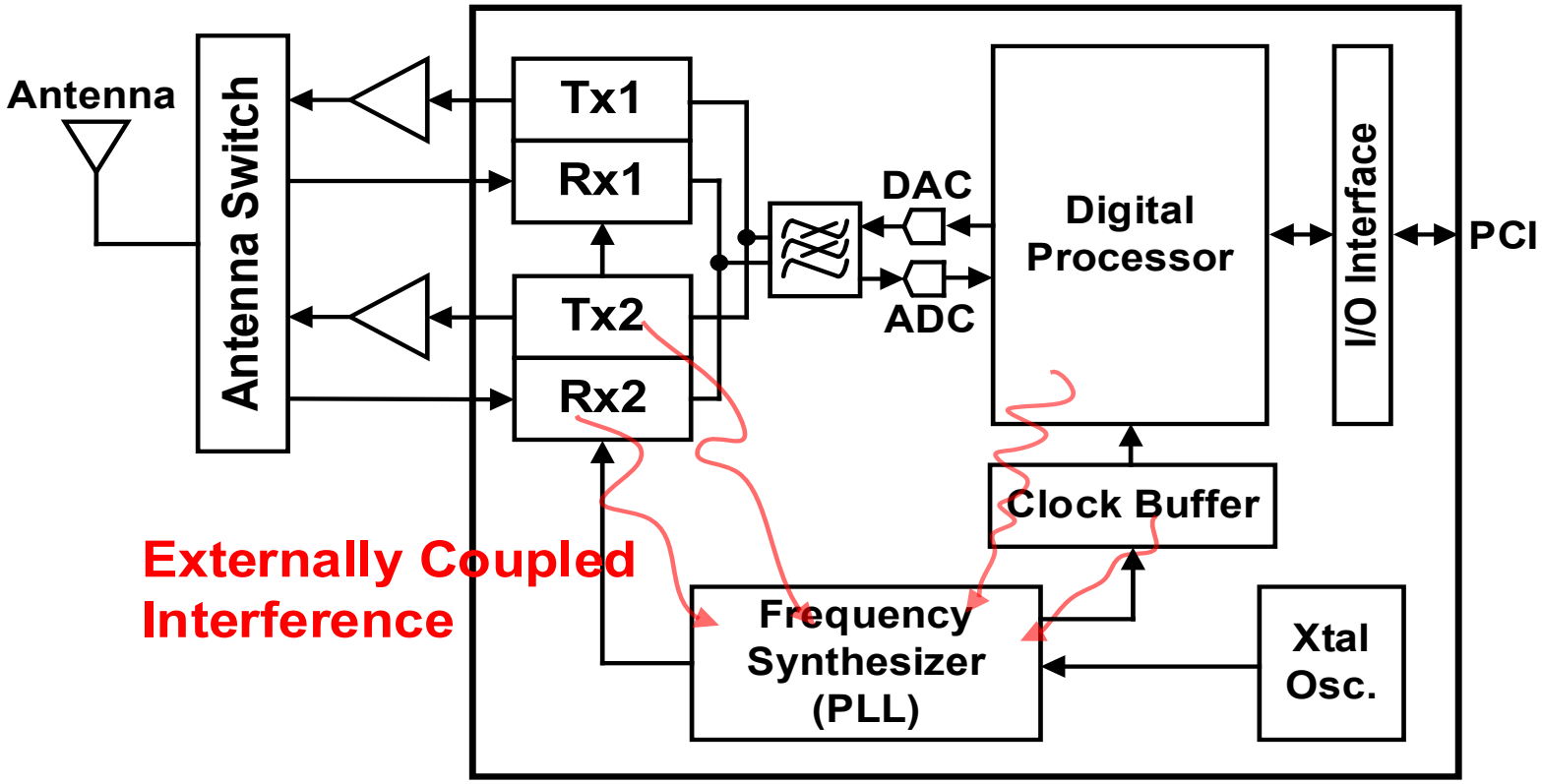
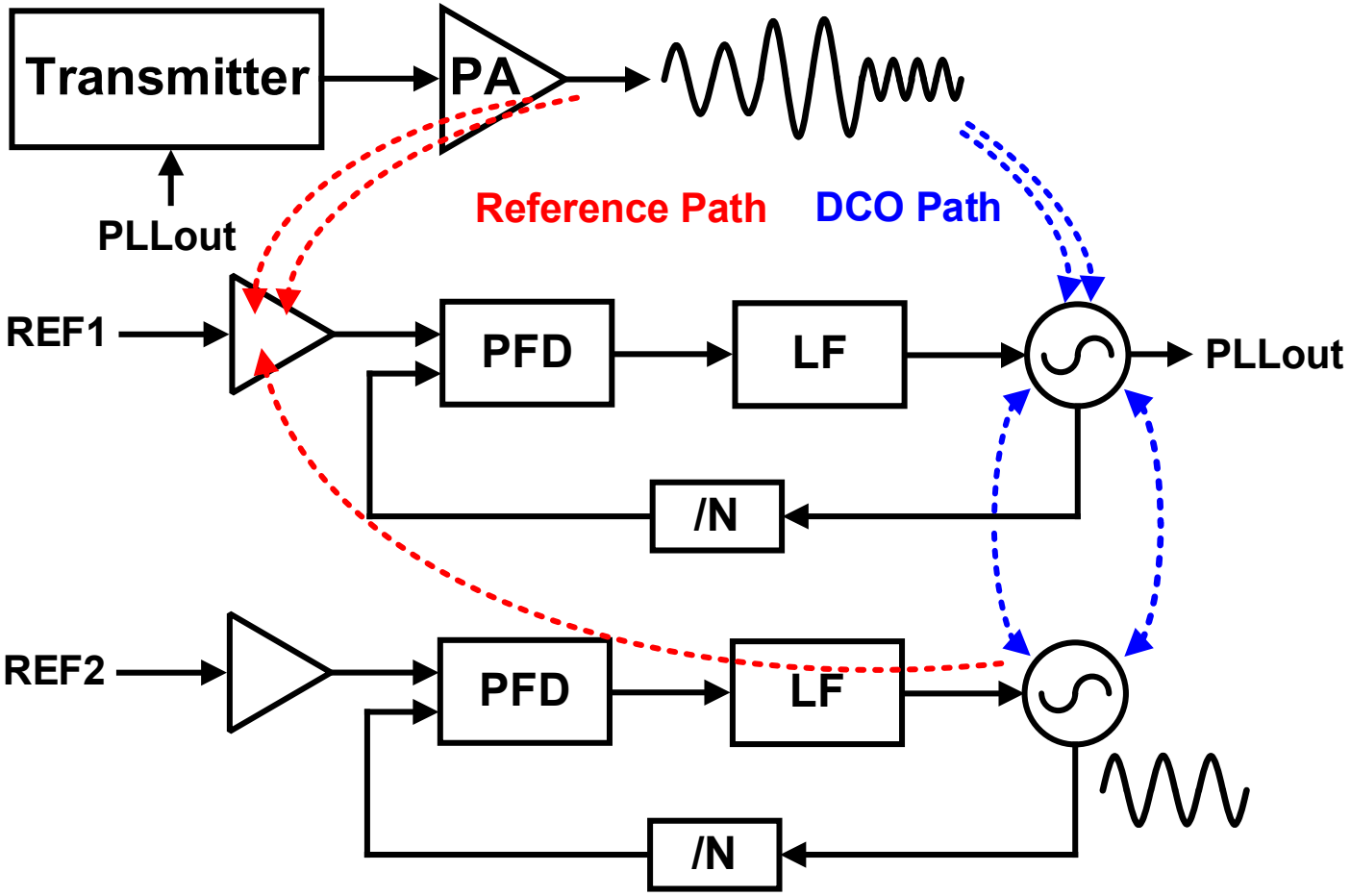
New Opportunities: Robust PLL

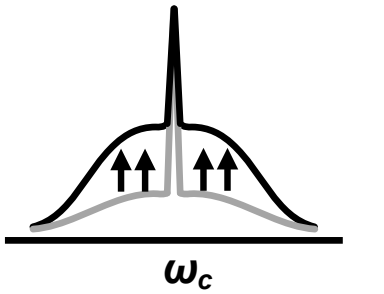
- Since digital PLL processes phase information in digital, there are new DSP opportunities beyond conventional analog PLL.
- PLLs in SoC can suffer from external noise interference, such as pulling.



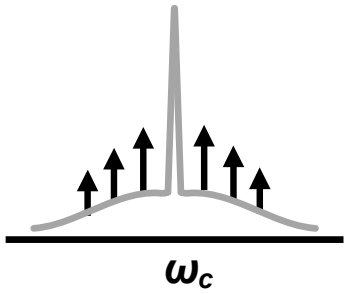
Simultaneous Coupling Paths

- Aggressors' signal will also couple to the reference path.





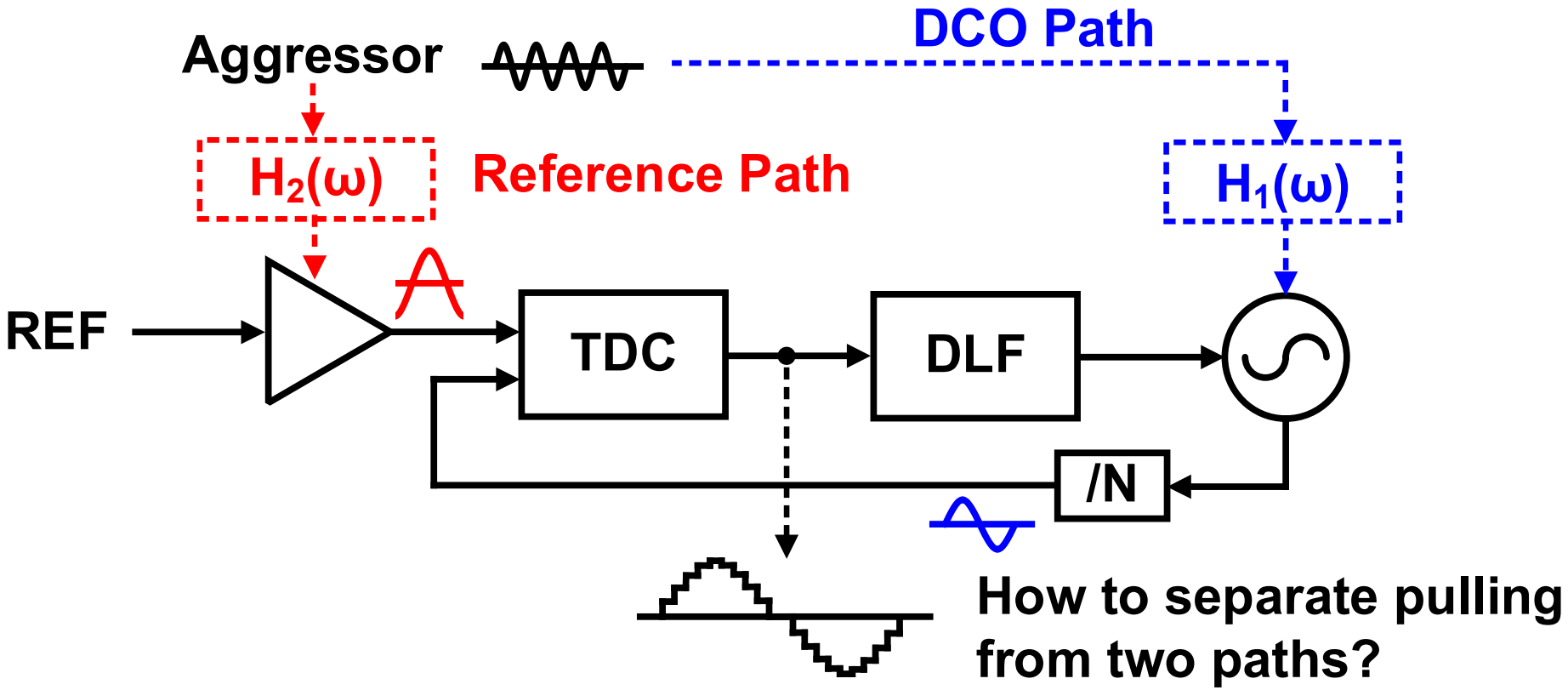
PA Pulling
(Modulated signal)



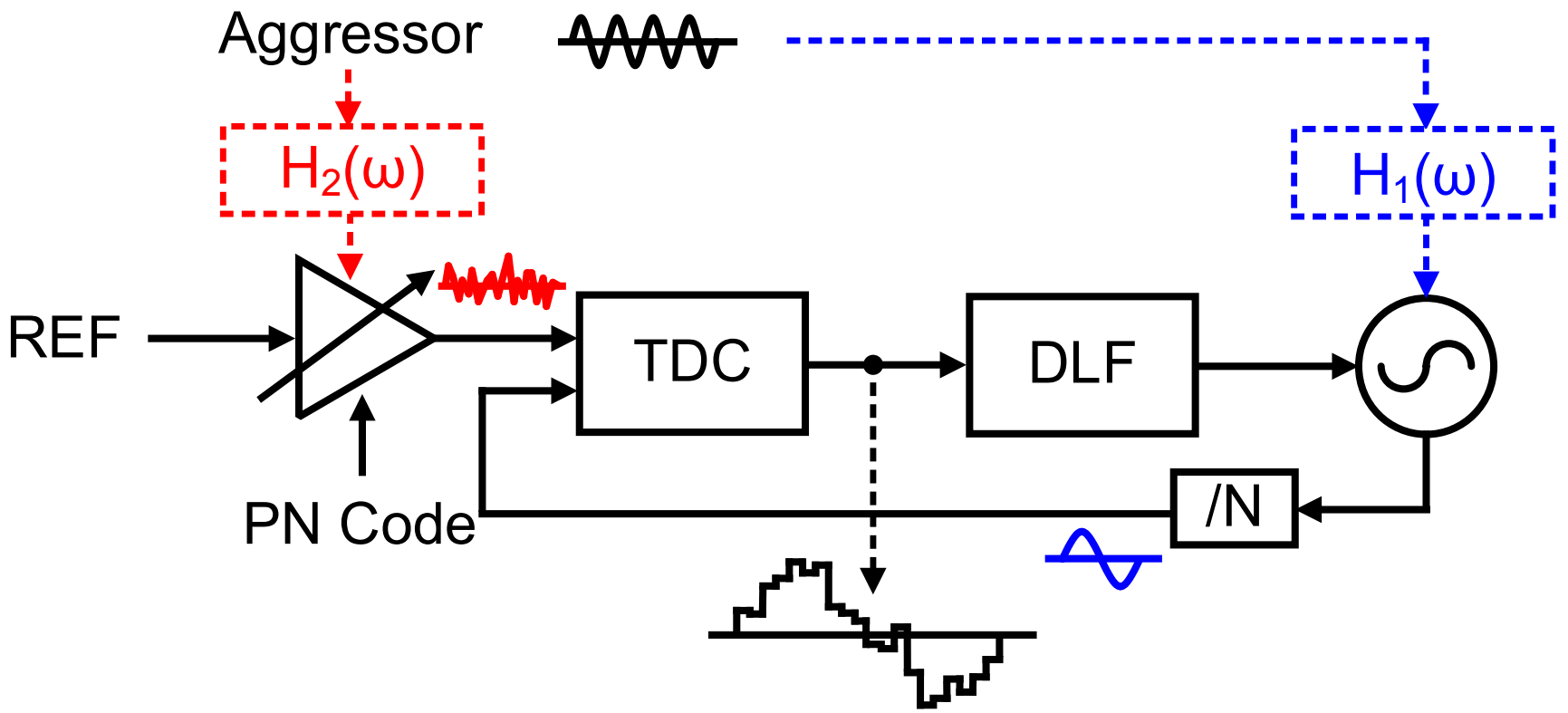
Mutual Pulling
(Sinusoidal signal)

Mixture of Two Pulling Signals

- Without separating the pulling from the two paths, erroneous mitigation will appear again.

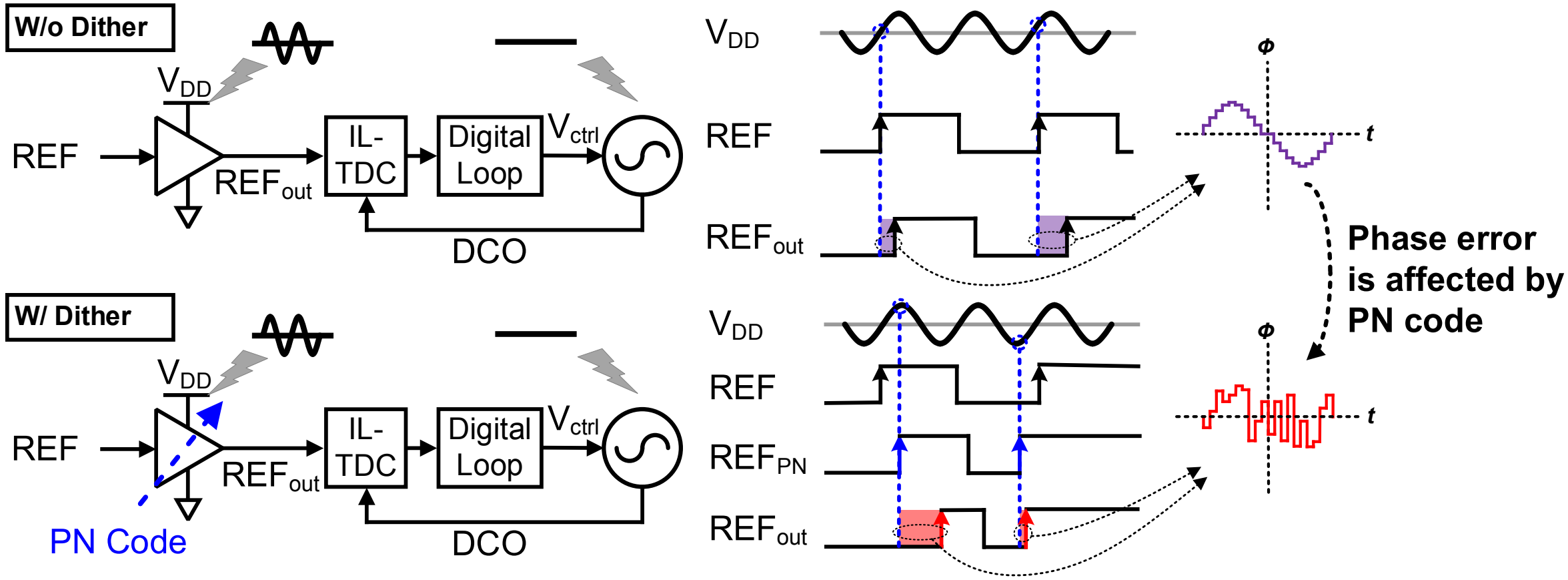


Orthogonalization: Dither-assisted Scheme

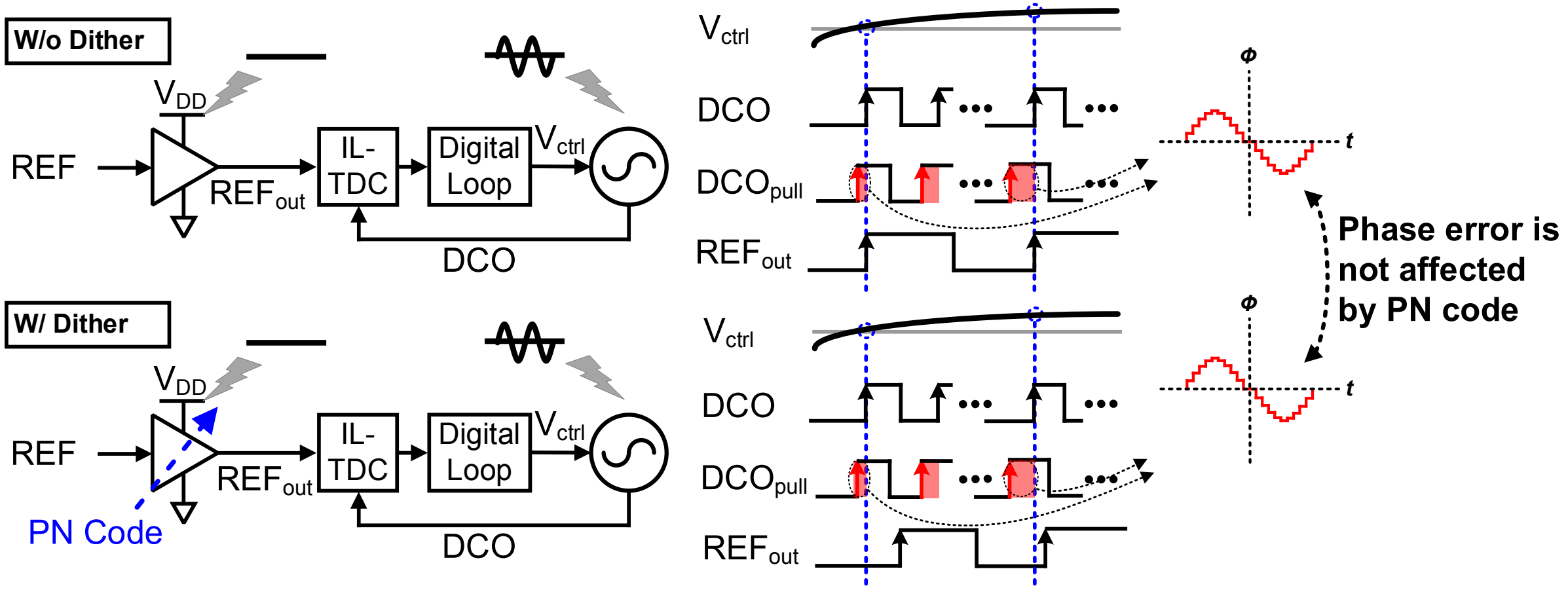


1. Reference pulling becomes **noise.**
2. DCO pulling preserves **original pattern.**

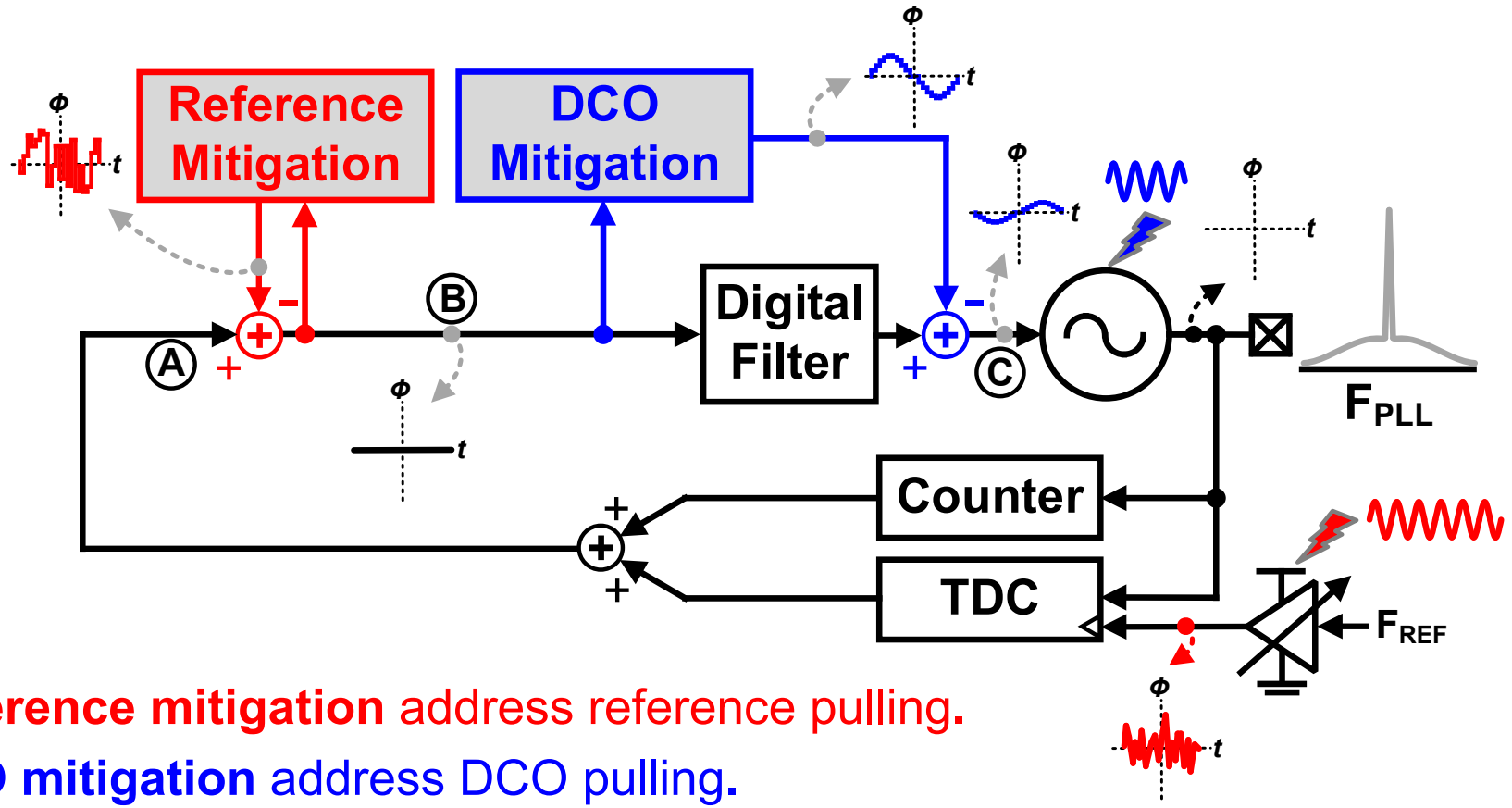
Phase Error Due to Reference Pulling



Phase Error due to DCO Puling



Dual-loop Mitigation Scheme



1. Reference mitigation address reference pulling.

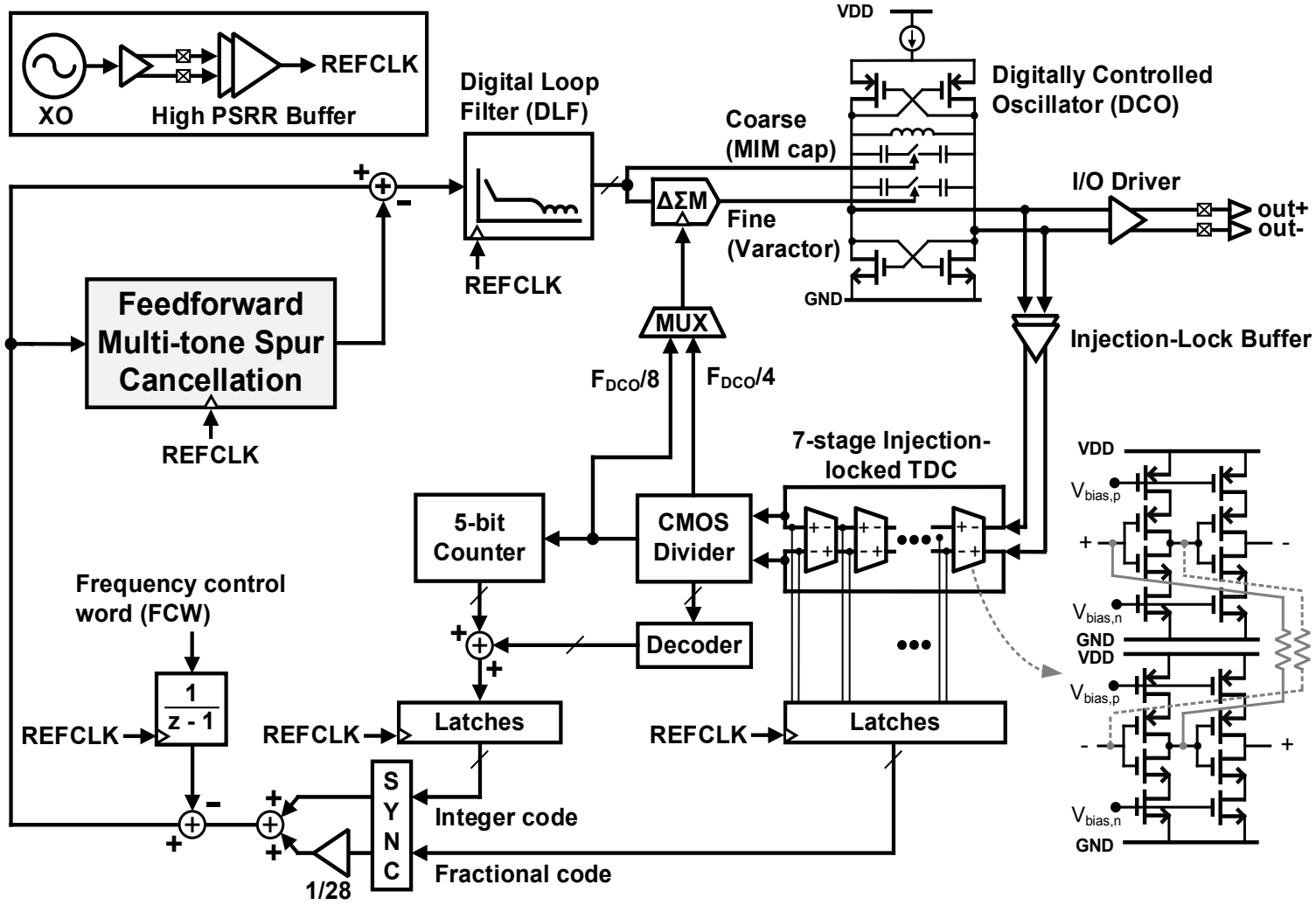
2. DCO mitigation address DCO pulling.

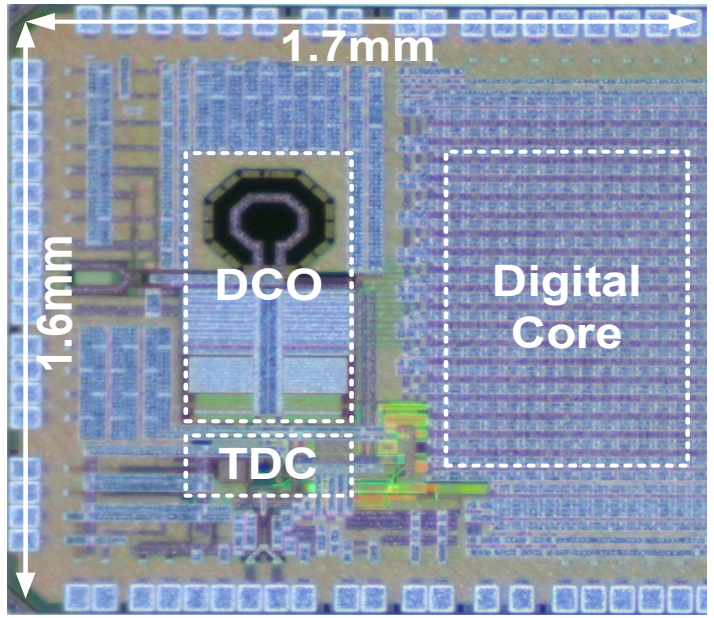
C.R. Ho, M. S-W Chen, "A digital frequency synthesizer with dither-assisted pulling mitigation for simultaneous DCO and reference path coupling," ISSCC, Feb. 2018.

Outline

- Basics of PLL
- Fractional-N Operation
- Critical Building Blocks
- Challenging Frac-N Design Issues
- New Opportunities
- SOA Fractional-N Digital PLL Examples

A SOA Fractional-N Digital PLL

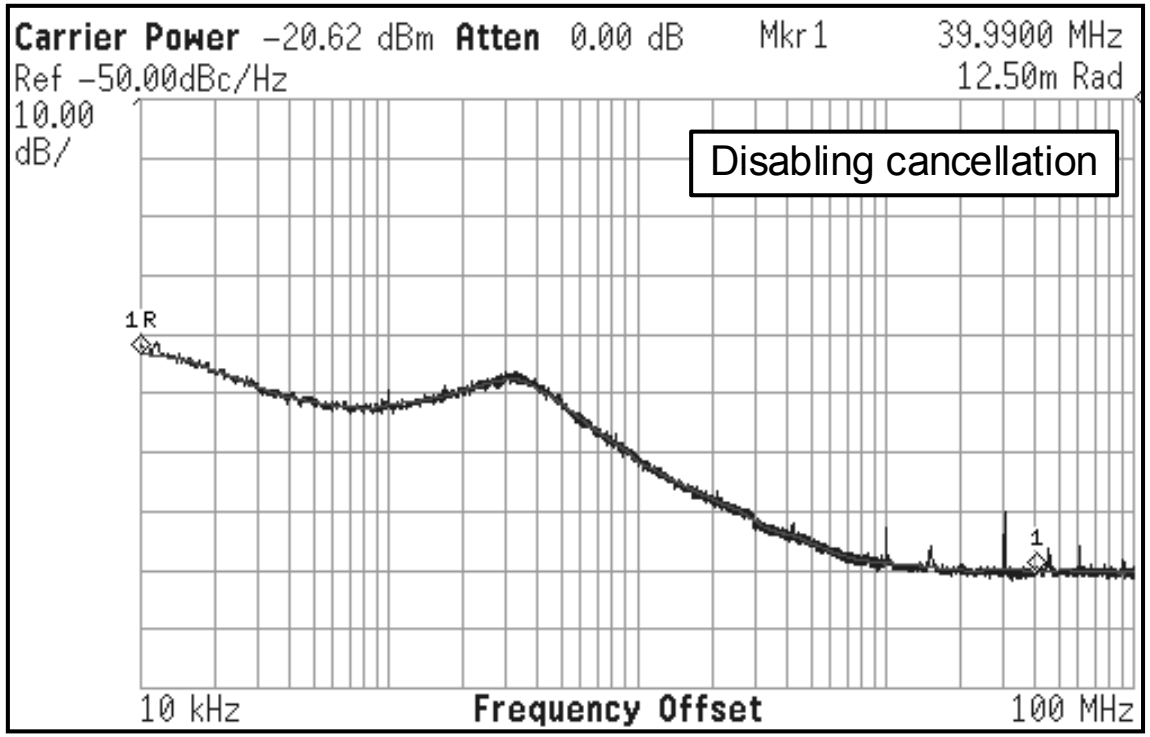


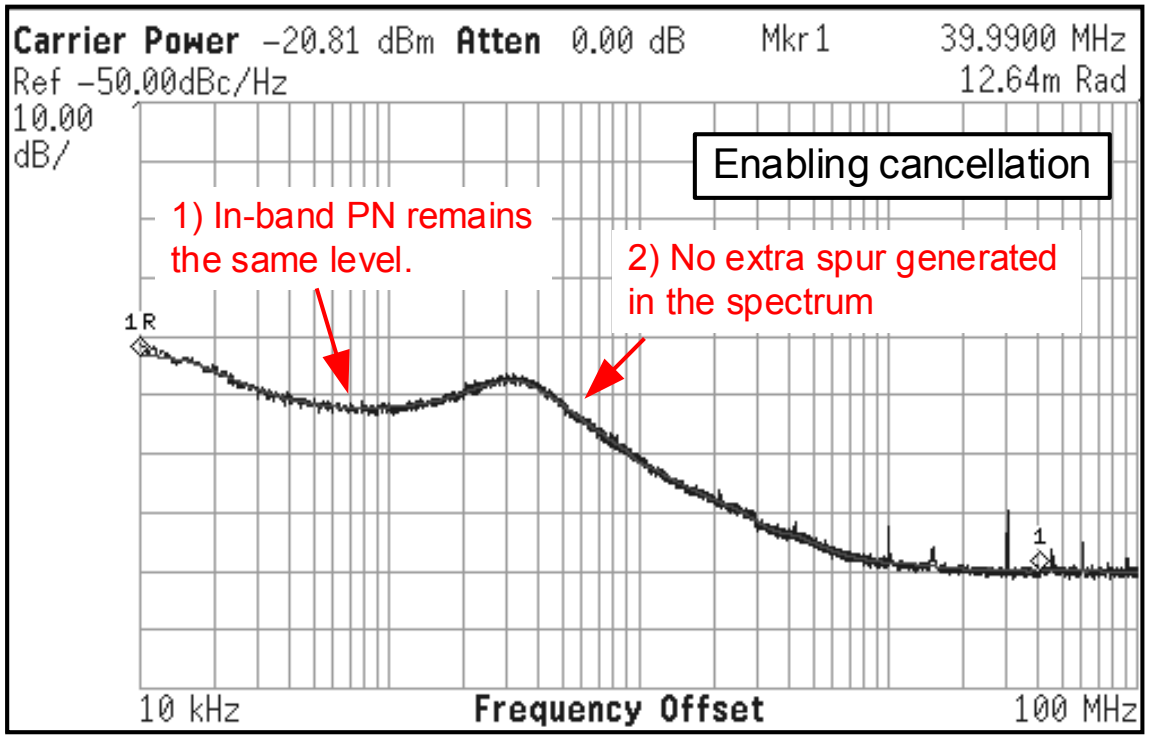


C.R. Ho and M. S-W Chen, "A Digital PLL with Feedforward Multi-Tone Spur Cancellation Loop Achieving <-73dBc Fractional Spur and <-110dBc Reference Spur in 65nm CMOS," ISSCC, JSSC (invited) 2016.

Measured Phase Noise

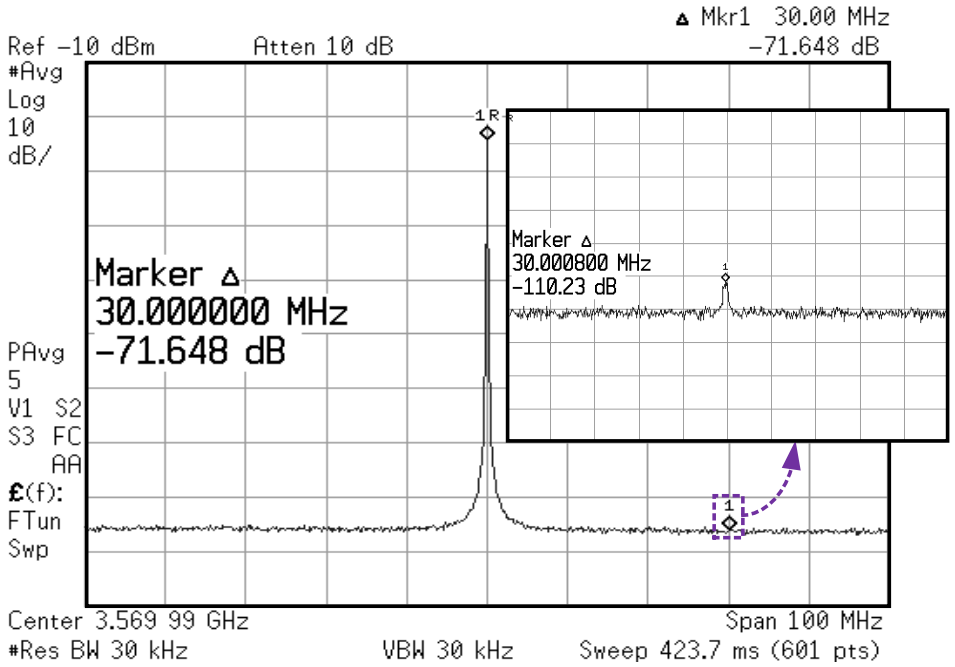
- Without interferers

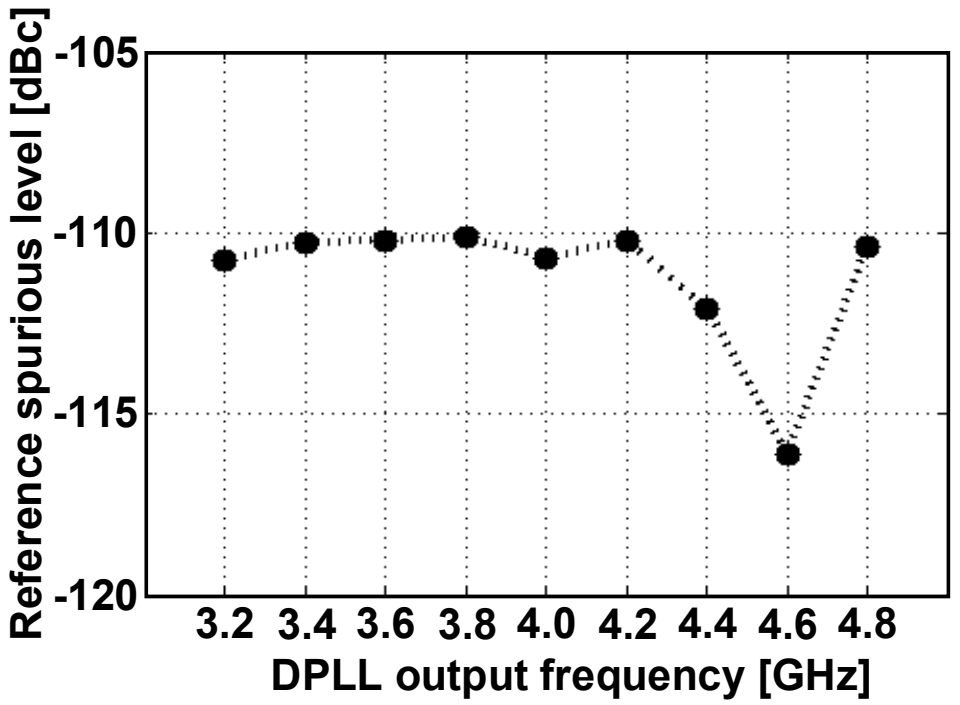




Measured Reference Spur

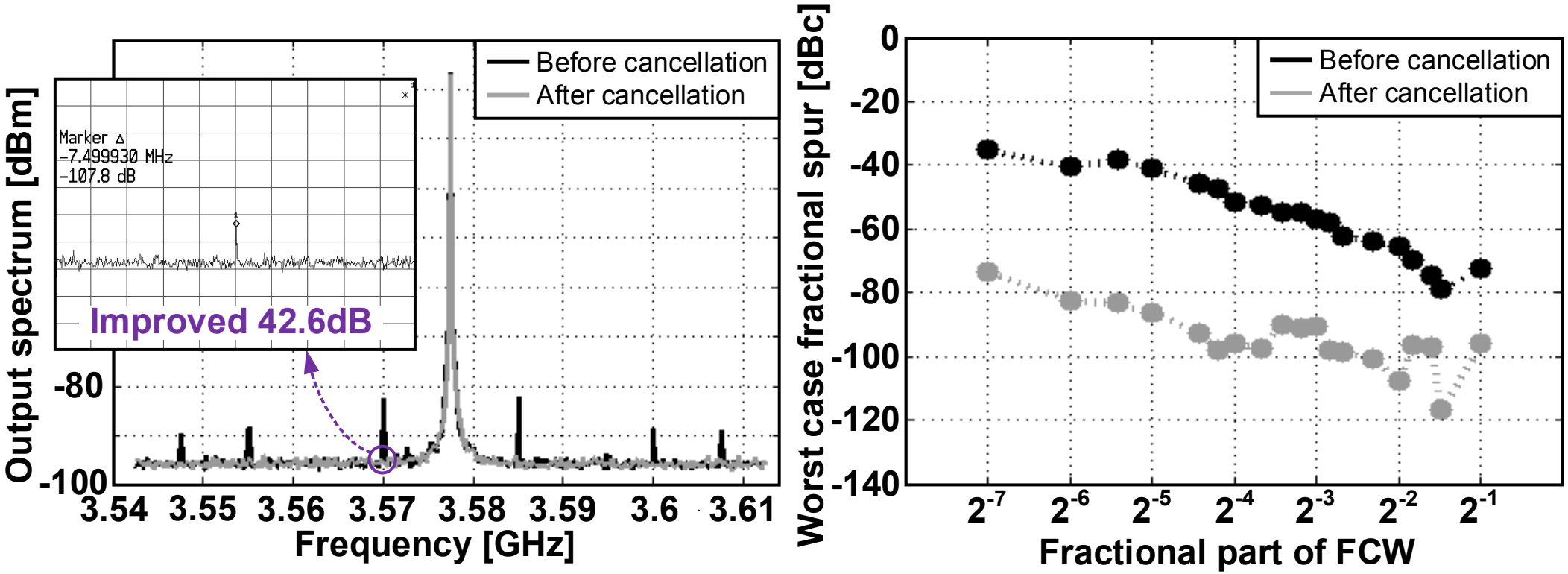
- Measured reference spur with worst-case -110dBc and best-case of -116dBc.
- Record performance compared to SOA PLLs.





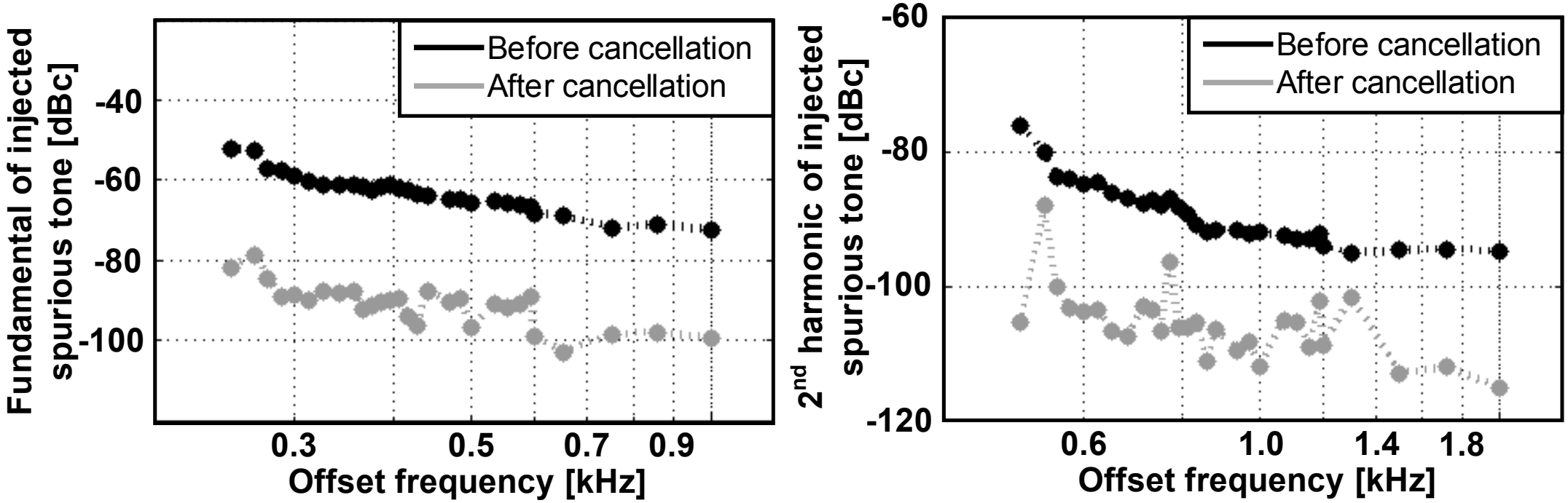
Measured Frac.-N Spur Performance

- Measured fractional spur with worst-case -73dBc and best-case of -119dBc.



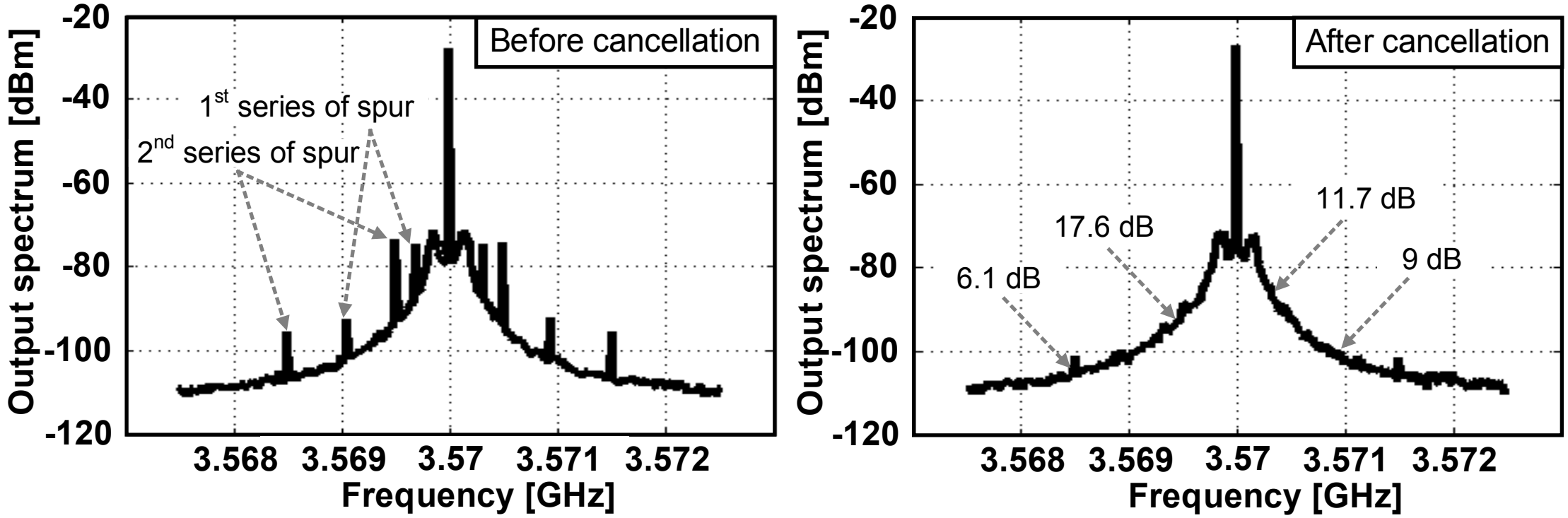
Measured External Spur Performance

- Measured external spurs at 0.23-1 MHz offset from F_{DCO} = 3.57 GHz with PLL BW ~400kHz.



Measured Multi-tone Spur Cancellation

- Measured two series of triangular external spurs at offset frequency of 312kHz and 495kHz.



State-of-the-arts Comparison

	ISSCC 2010 C. Weltin-Wu	ISSCC 2012 F. Opteynde	ISSCC 2013 T.K. Kao	ISSCC 2014 Y.L. Hsueh	ISSCC 2015 T.H Tsai	ISSCC 2015 H. Kim	This Work
Technology	65nm	40nm	40nm	40nm	16nm	65nm	65nm
PLL Type	Digital	Digital	Analog	Analog	Digital	Digital	Digital
VCO Type	LC Osc.	LC Osc.	Ring Osc.	LC Osc.	Ring Osc.	Ring Osc.	LC Osc.
Supply [V]	1.2	N/A	2.5/1.2	1.3	0.52 – 0.8	1	1
Freq. [GHz]	2.8 – 3.8	0.23 – 4.5	1.87 – 1.97	4.9 – 5.8	0.25 – 4	5 – 5.4	3 – 5
Ref. [MHz]	35	25	26	26	200	50	30
Frac-N spur rejection	Yes	Yes	Yes	No	No	No	Yes
Fractional spur (Worst case) [dBc]	-58	-51	-50	-65	-31.4	-42	-73.7
External spur rejection	No	No	No	No	No	No	Yes
Reference spur [dBc]	-61	N/A	-N/A	-104.2	N/A	-98.2	-110.2
Integrated noise [dBc]	N/A	-37.6 (1k~10MHz)	-29.7 (4k~40MHz)	-49.6 (1k~10MHz)	-33 (10k~500MHz)	-35.5 (100~40MHz)	-38.1 (10k~40M)
Phase noise (In-band) [dBc/Hz]	-101 (@ 1MHz)	-95.35 (@ 100kHz)	-100 (@ 100kHz)	-105 (@ 100kHz)	-110 (@ 1MHz)	-95.8 (@ 100kHz)	-103 (@ 100kHz)
Phase noise (Out-band) [dBc/Hz]	-123 (@ 3MHz)	-146.46 (@ 20MHz)	-109.3 (@ 10MHz)	-141.8 (@ 10MHz)	-123 (@ 3MHz)	-133.5 (@ 10MHz)	-122 (@ 3MHz)
Core Power [mW]	8.7	N/A	9.95	17.5	9.3	9.52	20.9
Active Area [mm^2]	0.4	N/A	0.055	0.29	0.029	0.223	0.77

Conclusion

- Fractional-N Digital PLL architectures emerge as technology scales in recent years.
- Critical building blocks of DPLL including TDC and DCO are key overhead of DPLL and their cost can be reduced through innovations.
- Flexibility, performance, portability and robustness can be jointly optimized for DPLL thanks to new DSP opportunities.
- Exciting time for DPLL designers (beyond analog PLLs)
  → A lot of new possibilities ahead!

Papers to See This Year

Suggest papers based on Advance Program

- 17.1: "A -240dB-FoM jitter and -115dBc/Hz PN @ 100kHz, 7.7GHz Ring-DCO-Based Digital PLL Using P/I-Gain Co-Optimization and Sequence-Rearranged Optimally Spaced TDC for Flicker-Noise Reduction"
- 17.2: "A 66fsrms Jitter 12.8-to-15.2GHz Fractional-N Bang-Bang PLL with Digital Frequency-Error Recovery for Fast Locking"
- 17.3: "A -58dBc-Worst-Fractional-Spur and -234dB-FoMjitter, 5.5GHz Ring-DCO-Based Fractional-N DPLL Using a Time-Invariant-Probability Modulator, Generating a Nonlinearity-Robust DTC-Control Word"
- 17.6: "A 21.7-to-26.5GHz Charge-Sharing Locking Quadrature PLL with Implicit Digital Frequency-Tracking Loop Achieving 75fs Jitter and -250dB FoM"
- 25.5: "A Self-Calibrated 1.2-to-3.8GHz 0.0052mm^2 Synthesized Fractional-N MDLL Using a 2b Time-Period Comparator in 22nm FinFET CMOS"

References

1. DPLL Basics/Overview

- R. Best, Phase-Locked Loops, 5th Edition Mc Graw Hill 2003.
- M. S.-W. Chen, "Overhead Minimization Techniques for Digital Phase-Locked Loop Frequency Synthesizer, " IEEE MWSCAS, Aug. 2012.
- C.R. Ho, M. S-W. Chen, "Clock Generation in the future with Digital Signal Processing Technique for Mitigating Spur and Interference," IEEE Microwave Magazine 2019

2. TDC

- T.E. Rahkonen, et al., "The use of stabilized CMOS delay lines for the digitization of short time intervals," JSSC 1993.
- R. Staszewski et al., "All-Digital TX Frequency Synthesizer and Discrete-Time Receiver for Bluetooth Radio in 130-nm CMOS ," JSSC Dec. 2004.
- M. S.-W. Chen, D. Su, S. Mehta, "A Calibration-Free 800MHz Fractional-N Digital PLL with Embedded TDC," ISSCC/JSSC 2010.
- C.R. Ho, M. S.-W. Chen, "A Fractional-N DPLL with Calibration-free Multi-phase Injection-locked TDC and Adaptive Single-tone Spur Cancellation," TCAS-I, 2016.
- B. Mesgarzadeh and A. Alvandpour, "A study of Injection Locking in Ring Oscillators," *IEEE International Symposium in Circuit and Systems,* vol.6, pp.5456-5468, May. 2005

References

3. Spur Cancellation

- C.R. Ho, M. S.-W. Chen, "A Digital PLL with Feedforward Multi-Tone Spur Cancelation Loop Achieving <-73dBc Fractional Spur and <-110dBc Reference Spur in 65nm CMOS," ISSCC, Feb. 2016.
- C.R. Ho, M. S.-W. Chen, "A digital frequency synthesizer with dither-assisted pulling mitigation for simultaneous DCO and reference path coupling," ISSCC, Feb. 2018.
- C.R. Ho, M. S.-W. Chen, "A fractional-N digital PLL with background dither noise cancellation loop achieving <-62.5dBc worst-case near-carrier fractional spur in 65nm CMOS," ISSCC, Feb. 2018.
- C.R. Ho, M. S.-W. Chen, "Interference-Induced DCO Spur Mitigation for Digital Phase Locked Loop in 65-nm CMOS," ESSCIRC, Sep. 2016.
- C.R. Ho, M. S.-W. Chen, "A Fractional-N DPLL with Calibration-free Multi-phase Injection-locked TDC and Adaptive Single-tone Spur Cancellation Scheme," IEEE Transactions on Circuits and Systems (TCAS-I) 2016
- C. Weltin-Wu et al, "A 3.5GHz wideband ADPLL with fractional spur suppression through TDC dithering and feedforward compensation," ISSCC 2010
- F. Opteynde, "A 40nm CMOS All-Digital Fractional-N Synthesizer without Requiring Calibration ," ISSCC 2012
- S.Y. Hung, S. Pamarti, "A 0.5-to-2.5GHz Multi-Output Fractional Frequency Synthesizer with 90fs Jitter and -106dBc Spurious Tones Based on Digital Spur Cancellation," ISSCC, Feb. 2019.

References

4. More Frac.-N DPLL Examples

- N. Pavlovic, et al., "A 5.3GHz digital-to-time-converter-based fractional-N all-digital PLL," ISSCC 2011.
- D. Tasca, et al., "A 2.9-to-4.0GHz fractional-N digital PLL with bang-bang phase detector and and 560fsrms integrated jitter at 4.5mW power, " ISSCC, 2011
- M.H. Perrott, et al., "A 2.5 Gb/s Multi-Rate 0.25μm CMOS CDR Utilizing a Hybrid Analog/Digital Loop Filter," ISSCC 2006