Analog Building Blocks of DC-DC Converters

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Outline

- Introduction
- Power Transistors
- Gate Drivers
- Level Shifters
- Control Loop
- System Design

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DC-DC Conversion


12/48V

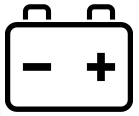

24/36V


3-15V


12/24/48V


20-75V


5-20V




< 30 V

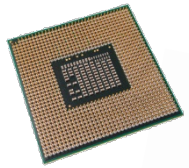

1-3V


2.5-4.4V

DC-DC Conversion

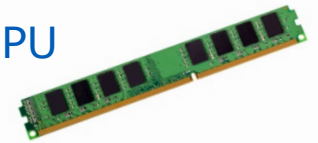
- Size, volume, footprint
- Efficiency
- Reliability
- Cost

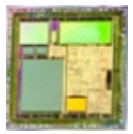

ECUs




Sensors

µC,CPU


RAM,HD,SSD


ICs

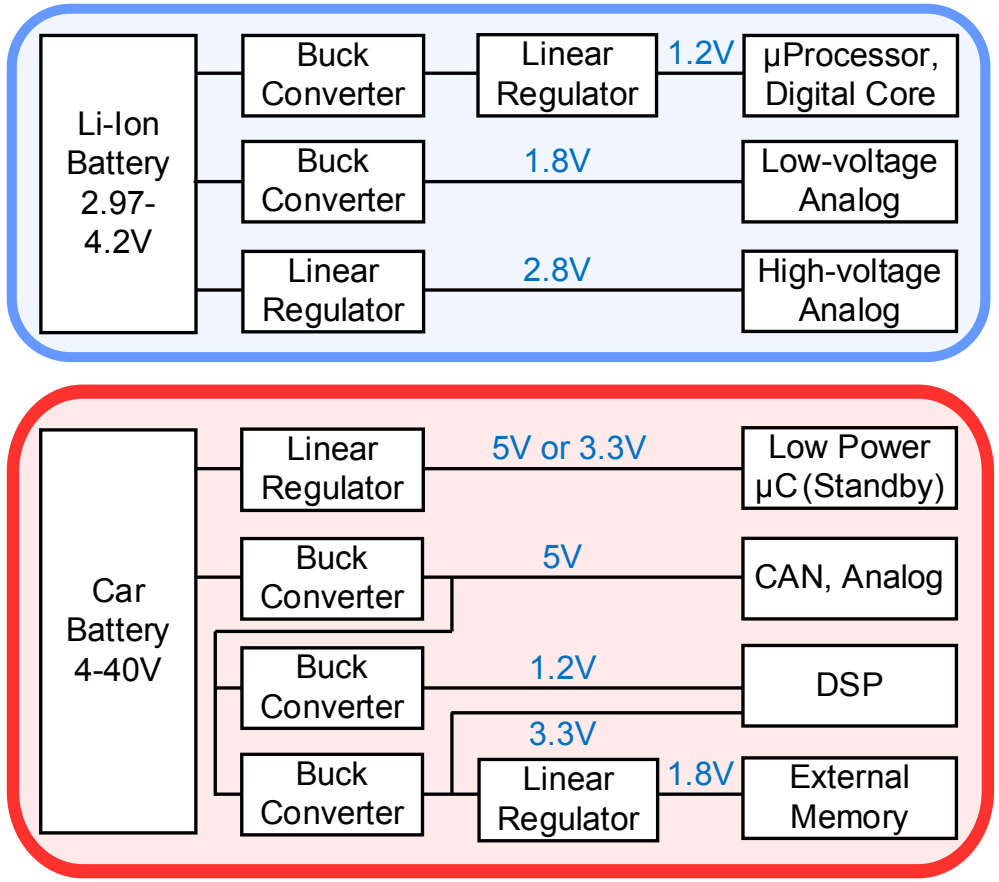
Photos: Shutterstock.com

Trend towards higher voltages → >50V

Lower supply voltages → 1V

Power Management Systems

Part of complex ICs or separate power management units: Multiple DC-DC converters to supply µCs, MPUs, DSPs, analog & mixed-signal circuits



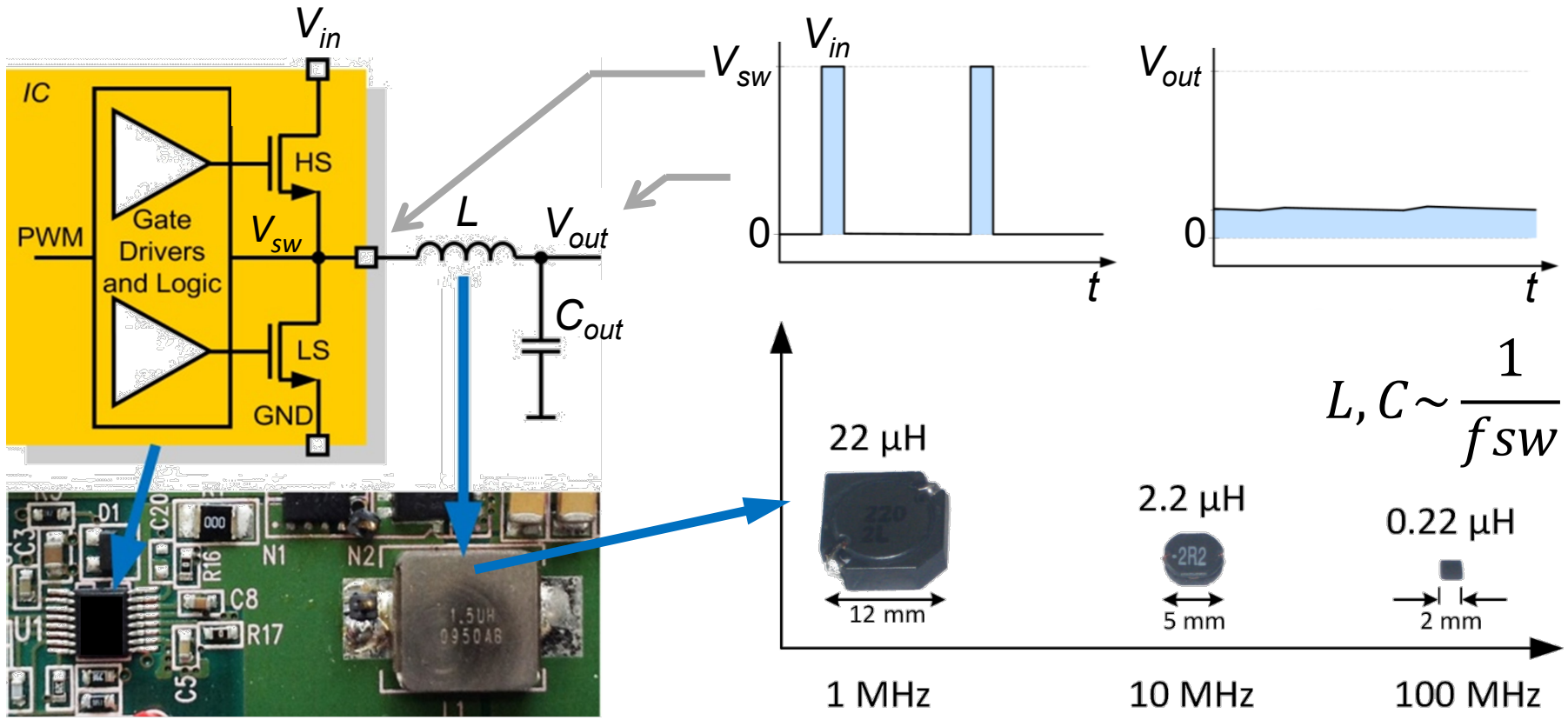
Handheld devices, PDAs, consumer products:
V_{in} ~ 4V, moderate conversion ratios

Automotive / Industrial, server applications:
V_{in} > 10 - 60V, larger conversion ratios

DC-DC Conversion Fundamentals

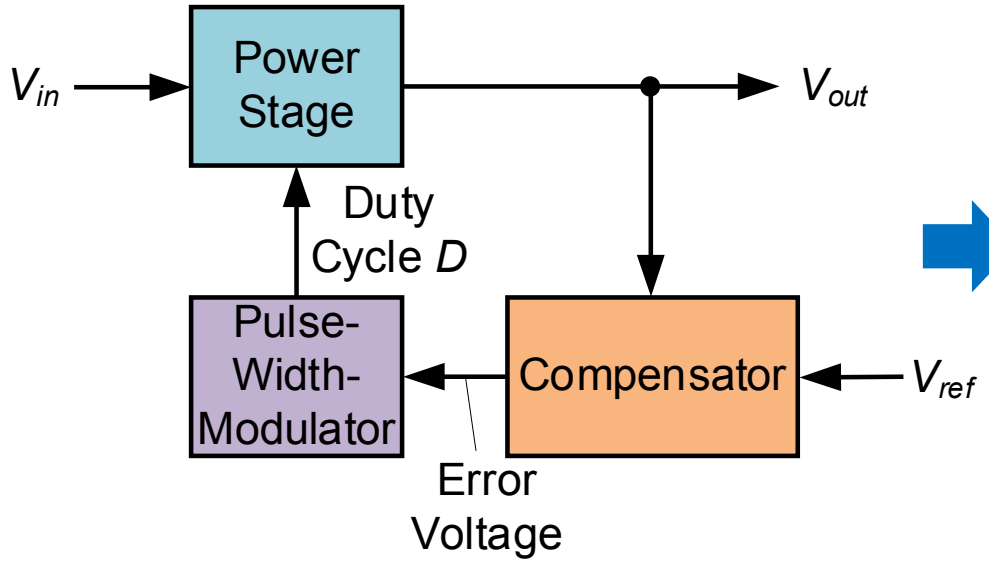
Pulse-width modulation: Much higher efficiency than a linear regulator (LDO)

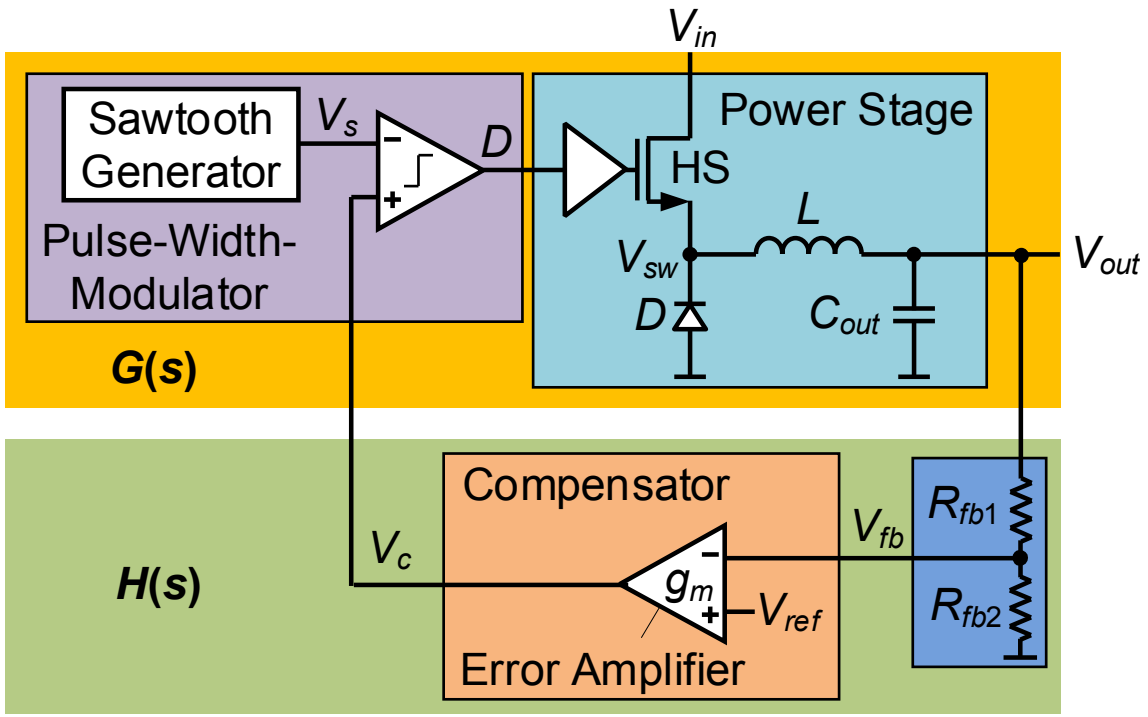
Challenges: Increasing switching losses, EMC, parasitic coupling



Analog Building Blocks in DC-DC Converters

Example: DC-DC Buck Converter



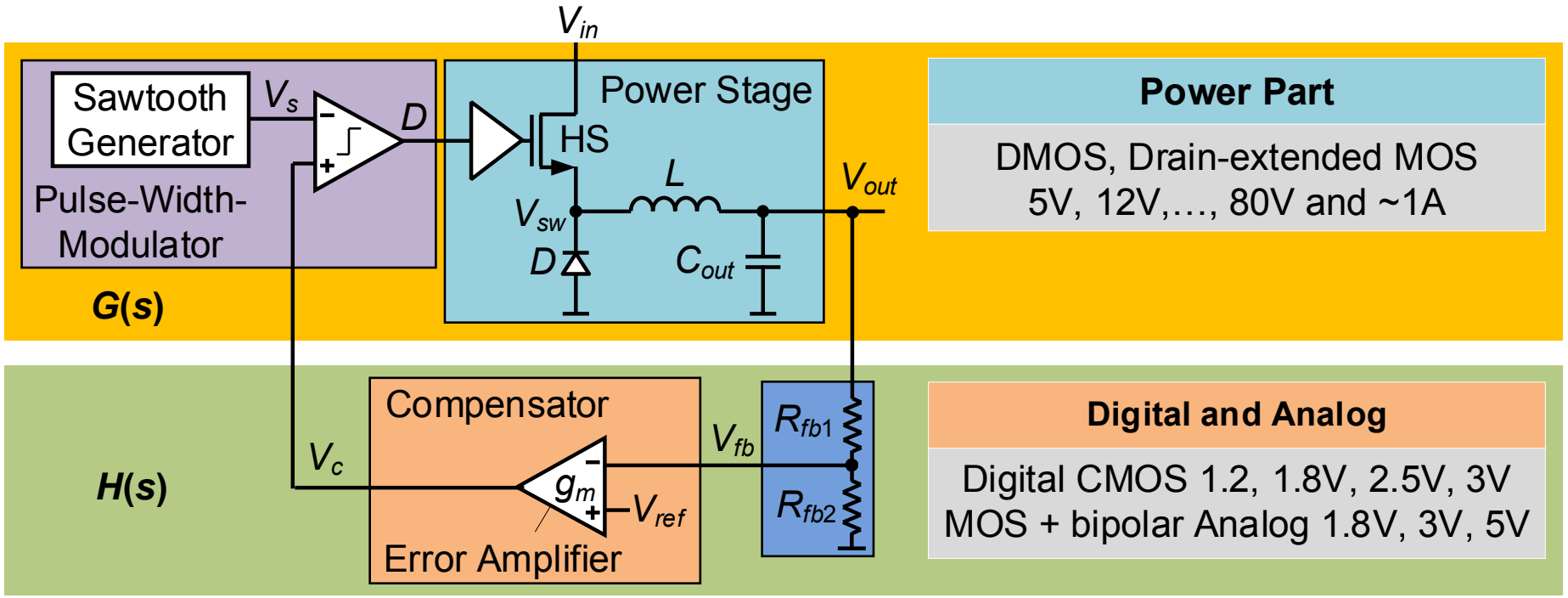


Blocks of Interest:

- Power stage: switch, gate driver, level shifter
- Error amplifier and control loop components
- Current sensing

Technology Options / Devices

- Various HV, LV transistors
- Buried layer or trench isolation
- Zener diodes, Schottky and power diodes
- OTP memory, EEPROM, flash memory



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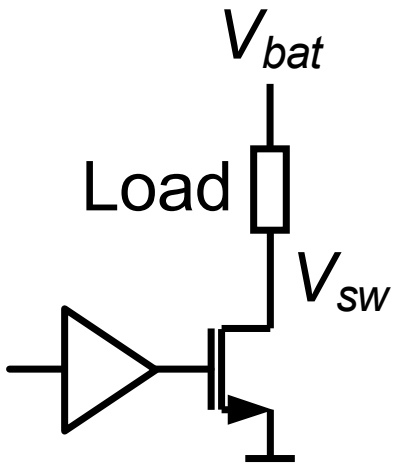
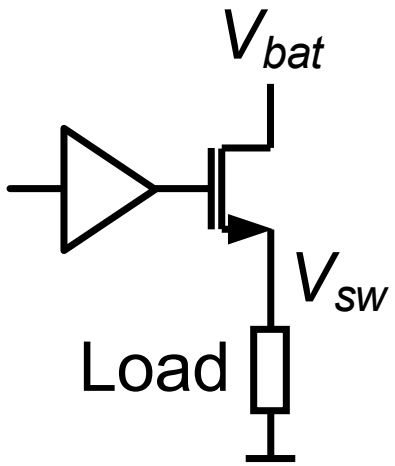
Power Switch Configurations

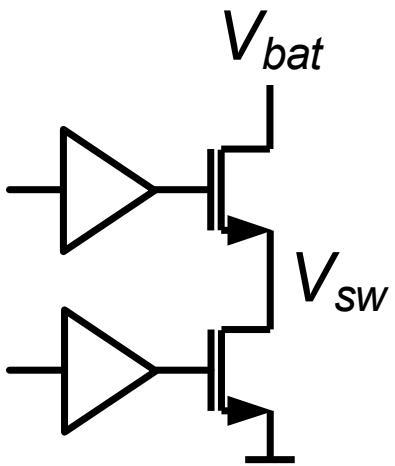
Low-Side



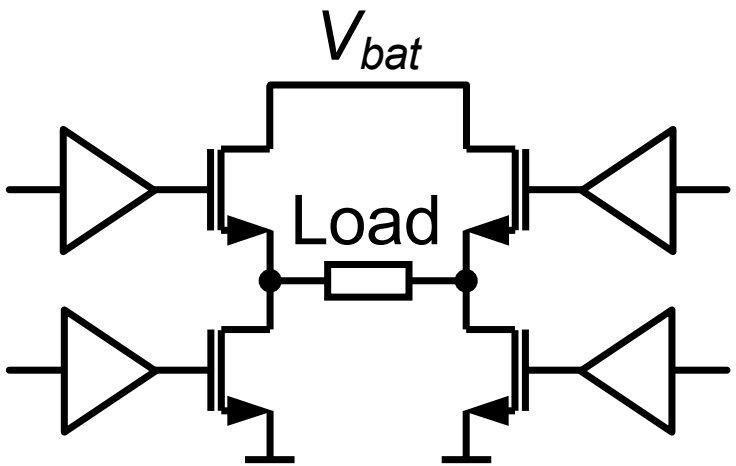
High-Side



Half-Bridge



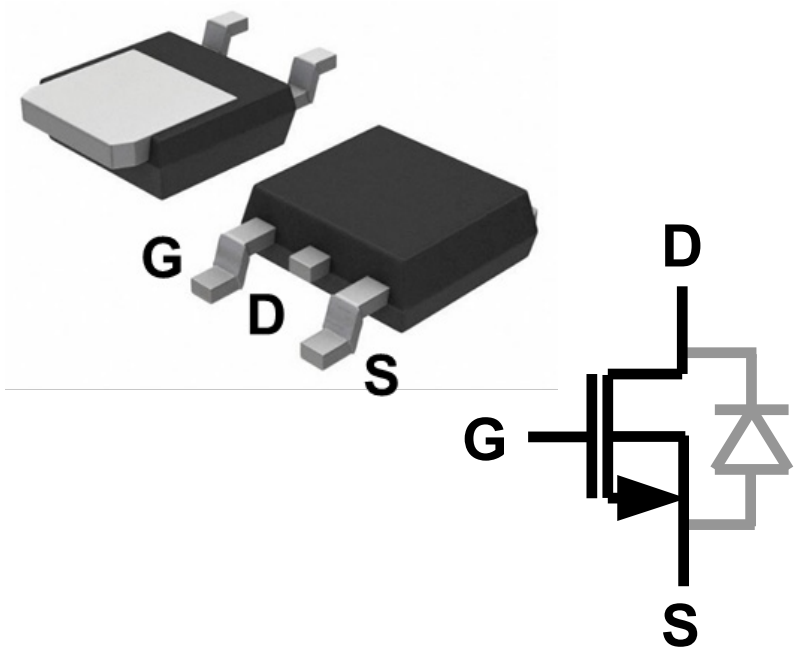
Full-Bridge (H-Bridge)



- Transistors can be on-chip (integrated) or discrete (external)
- On-chip: Any transistor can be used as a power device, if voltage ratings are suitable
- High-power and high-voltage applications prefer n-type transistors due to lower on-resistance R_{DSon}

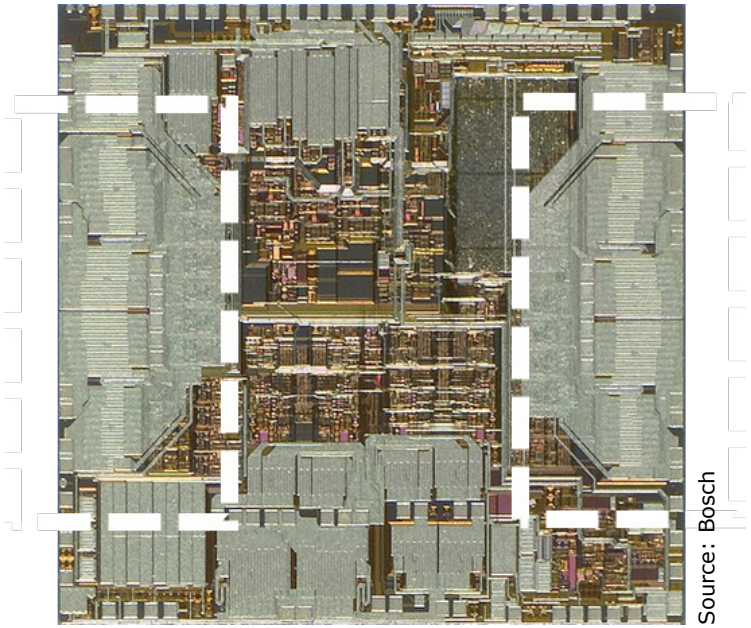
Power Transistors

Discrete power FET
(external component)



On-resistance ~ 10...100mΩ
Drain currents > 1...10A

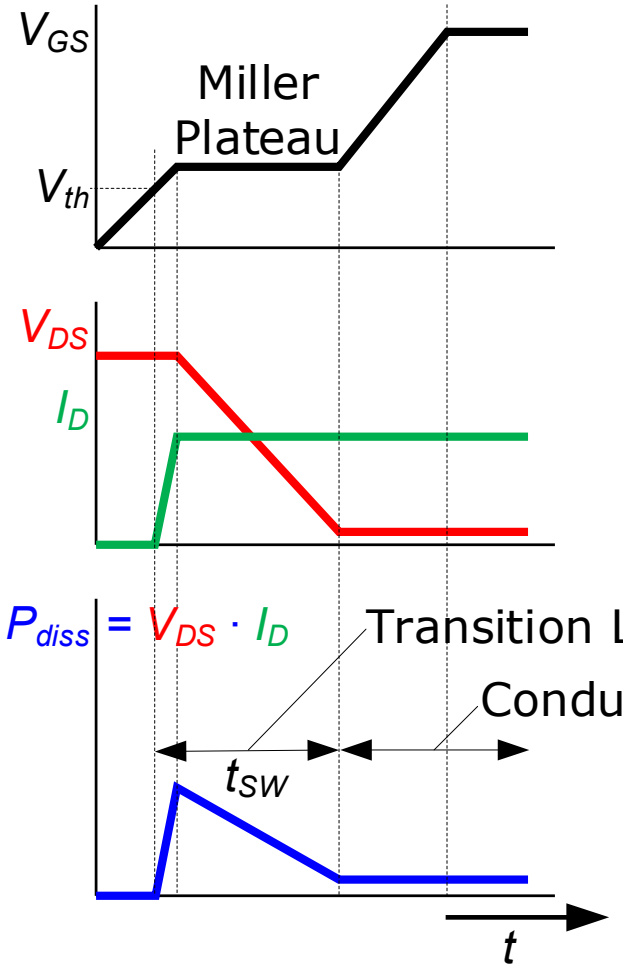
Integrated power FET in CMOS
and BCD technologies

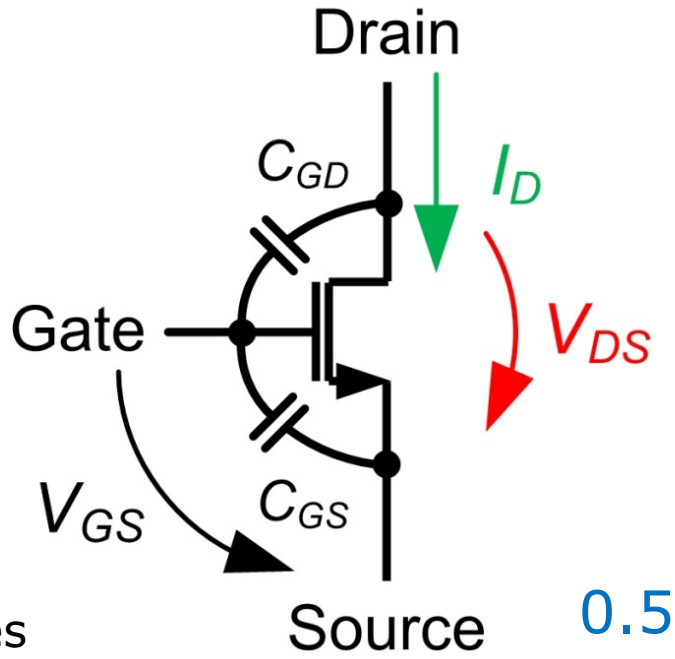


On-resistance < 1Ω
Drain currents < 1...2A
FET types for > 60V available

Transistor Switching Behavior and Losses

Inductive loads: Four phases





Example:

V_{GS} = 8V

V_{th} = 2V

I_D = 0.5A

R_{DSon} = 0.5Ω

V_{DS} = 12V

t_{sw} = 100ns

f_s = 500kHz

Transition Losses:

$0.5\ V_{DS}\ I_D\ f_s\ t_{sw}$ = 150mW

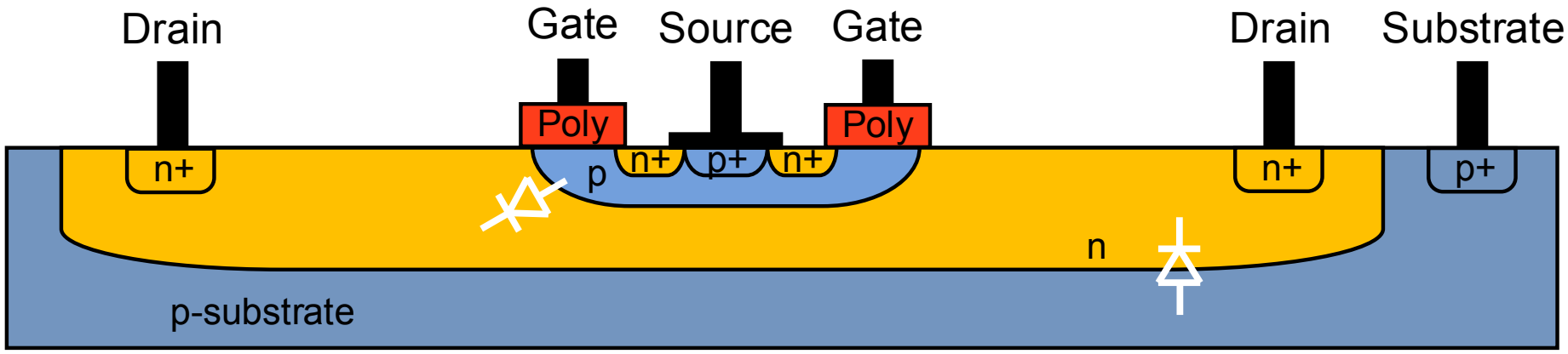
Conduction Losses:

$I_D^2\ R_{DSon}$ = 125mW

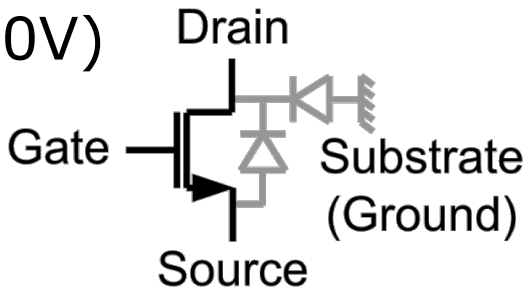
+ gate driver losses (→ see section on gate drivers)

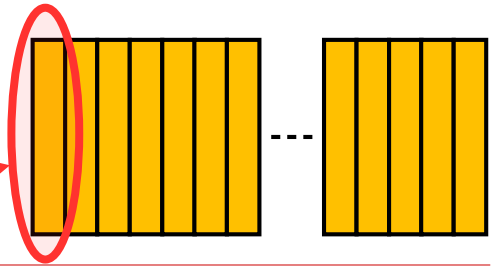
Power MOSFET: DMOS

DMOS = Double Diffused MOS (lateral oder vertical)

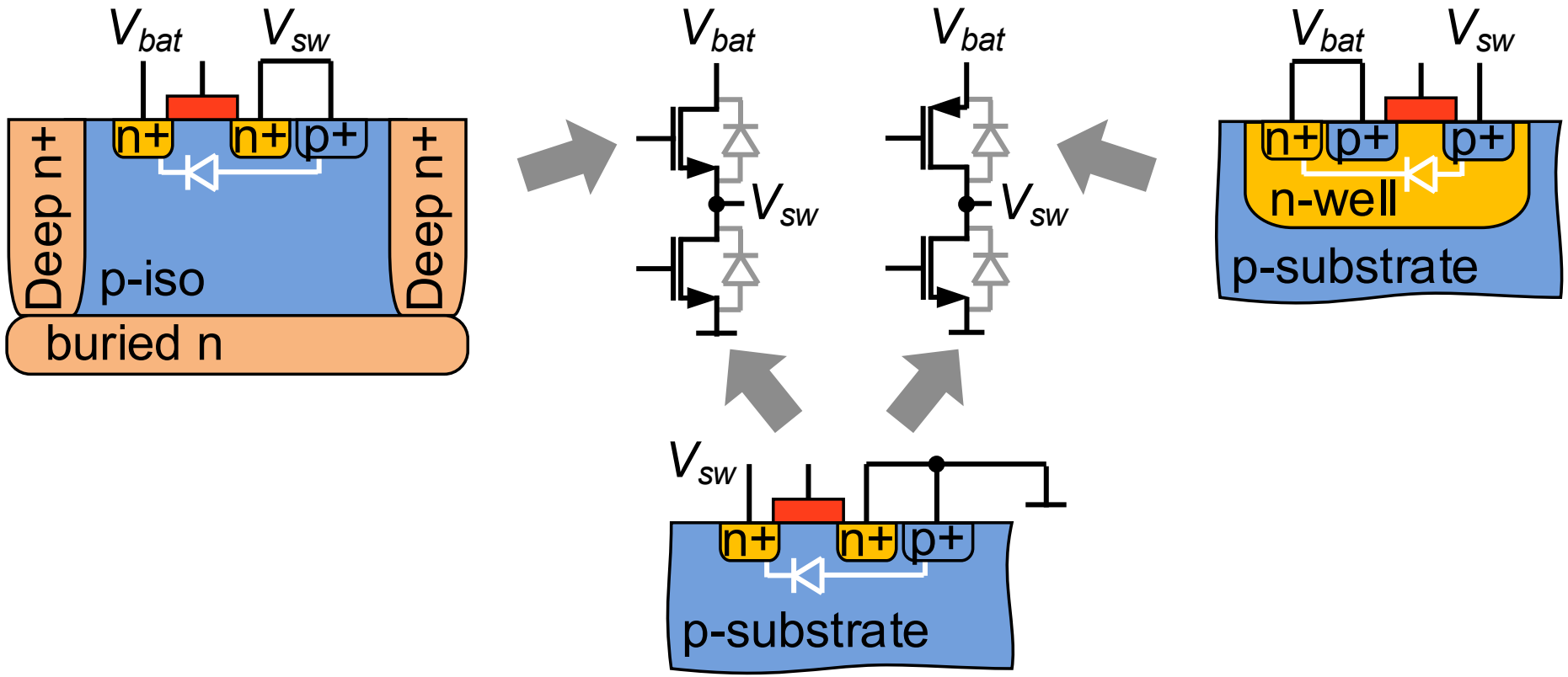


- Combines low R_{DSon} (< 1Ω, >1-2A) with large V_{DSmax} (…100V)
- Source and gate isolated from substrate
  → negative voltages possible
- Parasitic diodes at drain-source and drain-substrate
  - have to be taken care of
  - can be utilized as free-wheeling or power diode
- Layout: Multiple fingers in parallel (unit transistors)





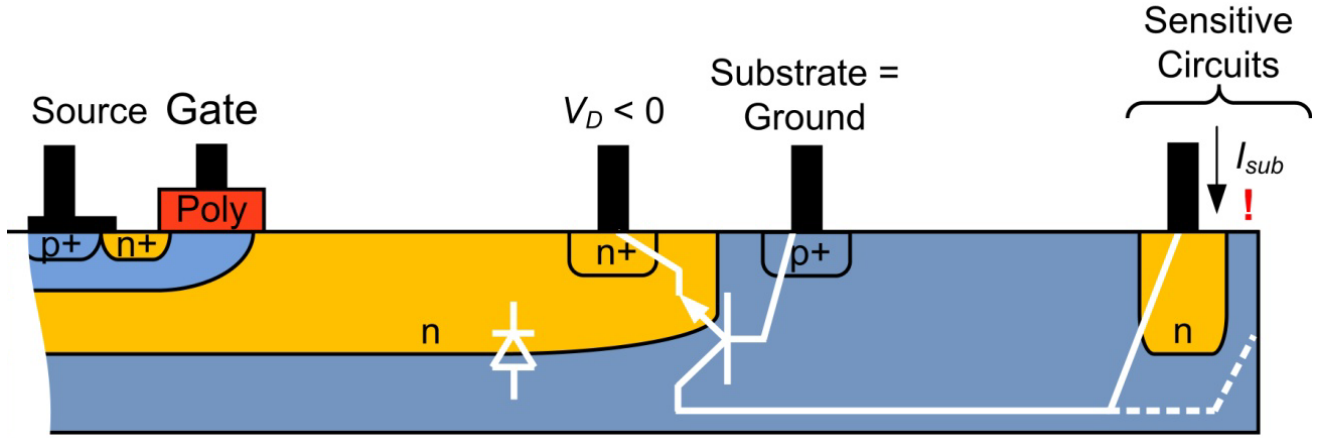
Body Diode in Standard CMOS Devices



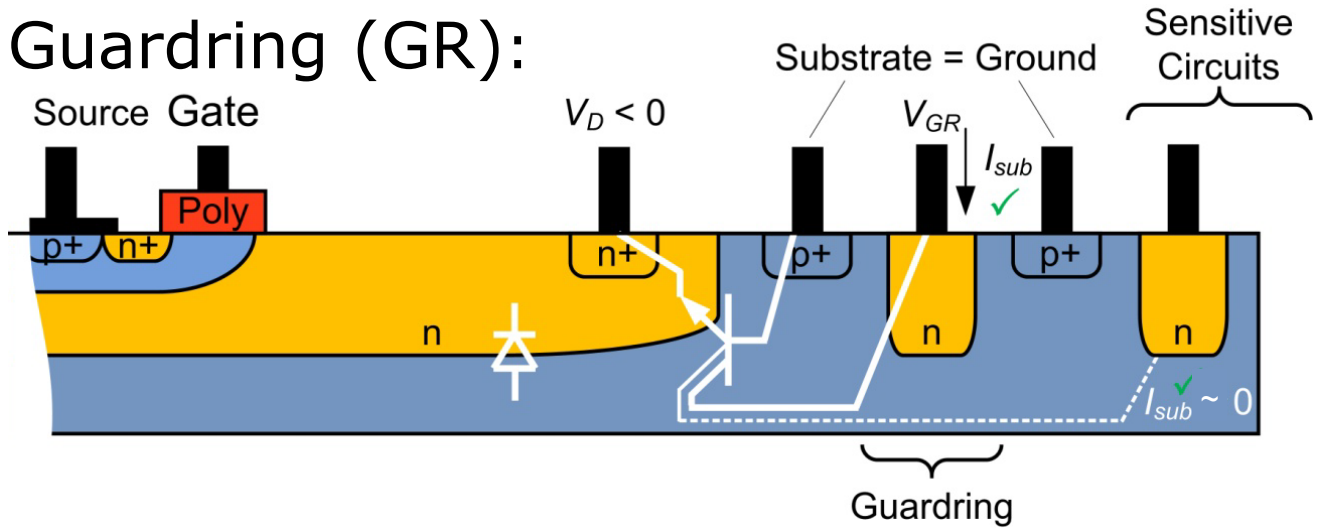
- Body diode: always present and associated with a parasitic bipolar structure
- Inductive switching: losses due to VF and reverse recovery
- Risk of back-supply (diode conducts even if switch is off)

Parasitic Effects

For $V_D < 0$ substrate currents through parasitic npn:



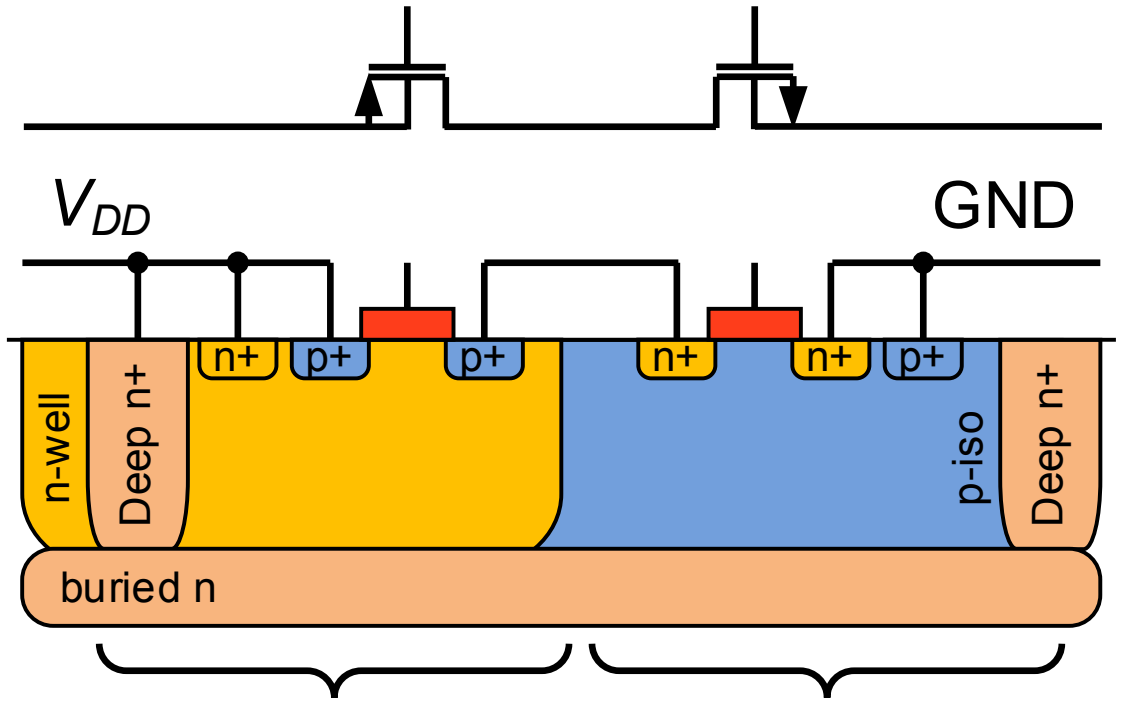
Guardring (GR):



- Disturbance of other circuits blocks
- Debiasing, latch-up

- GR around power transistor
- Nearly zero disturbance at sensitive circuits
- GR around every drain which goes to an IC Pin
- Drawback: Layout area / cost

Isolation of Circuit Blocks

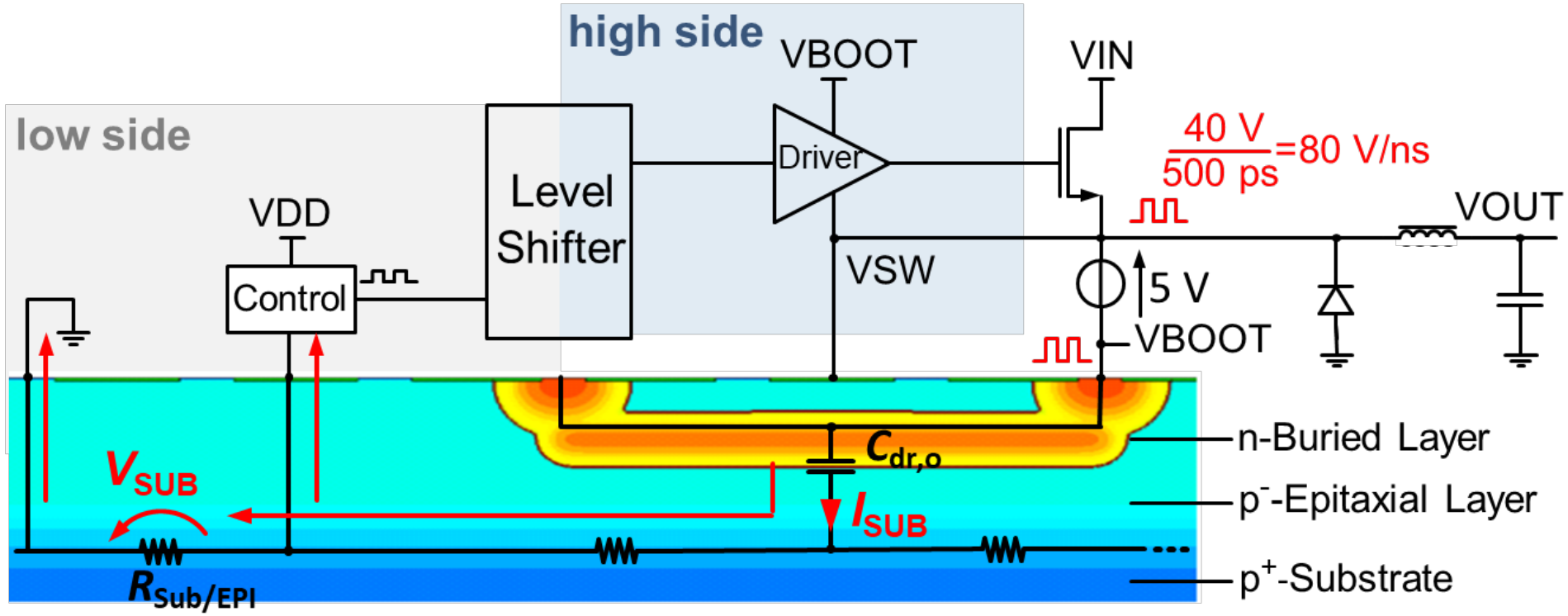


Common isolation of all p-/n-channel devices

- Rule: Isolate every (sensitive) circuit block (if possible)
- Shielding against substrate noise coupling
- Similar to guardring with full “incapsulation”

Substrate Coupling

Voltage slopes > 10V/ns cause capacitive charging currents (~100mA) during transition → substrate debiasing >4V → malfunction of analog and digital

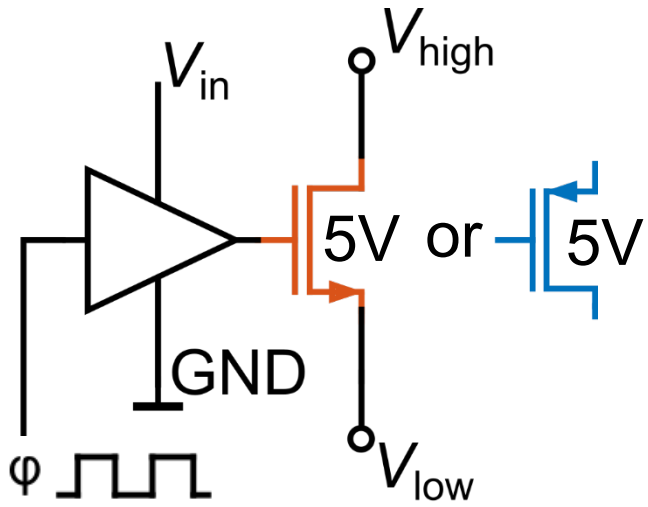


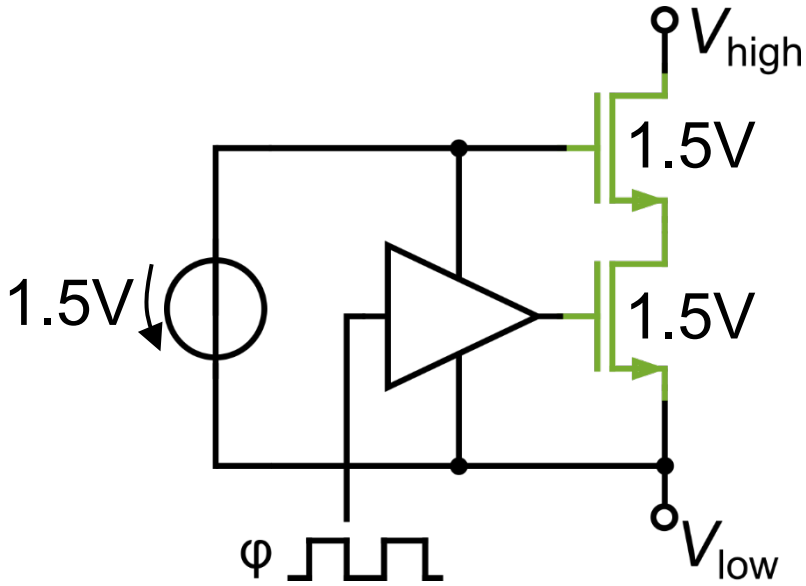
Back-side metallization reduces coupling by ~100%, conducting trench by ~90% (if available), p-Guardring is less efficient but readily available

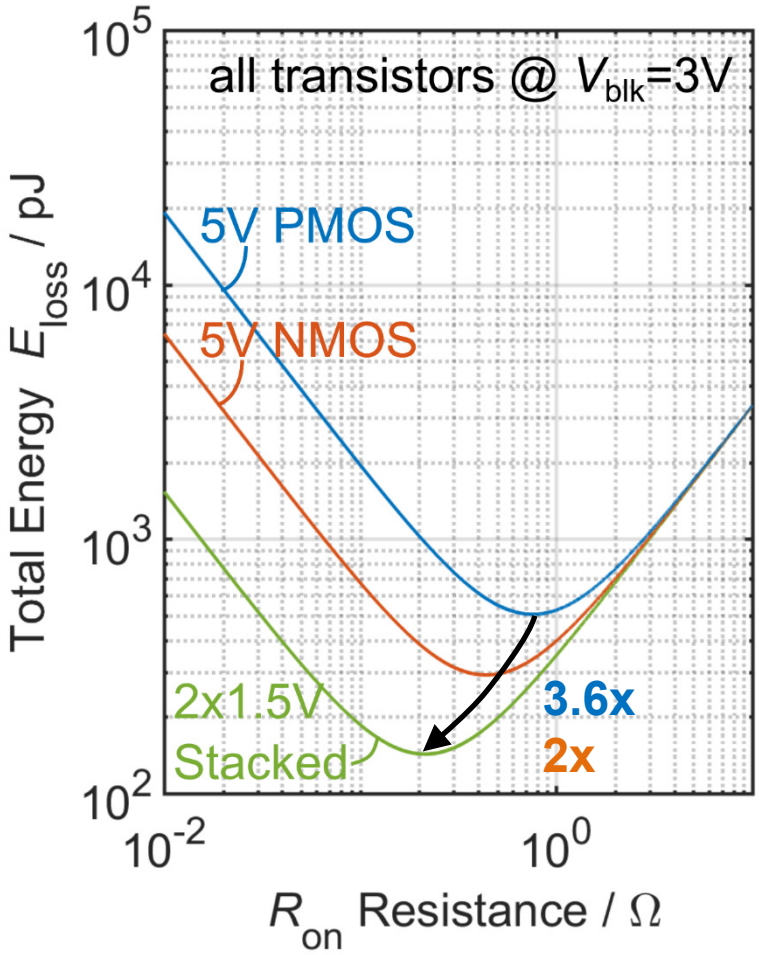
Switch Stacking

Replace HV devices by stacked LV switches
→ significant switching loss and area reduction

Renz, ISSCC 2019

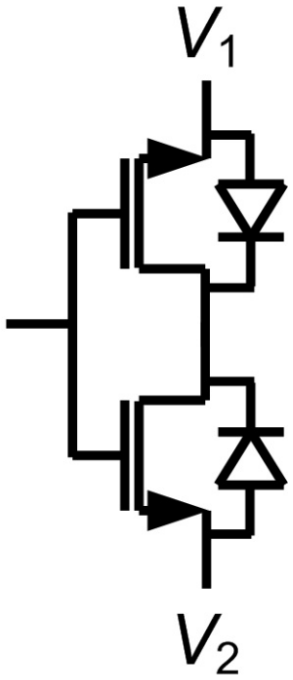






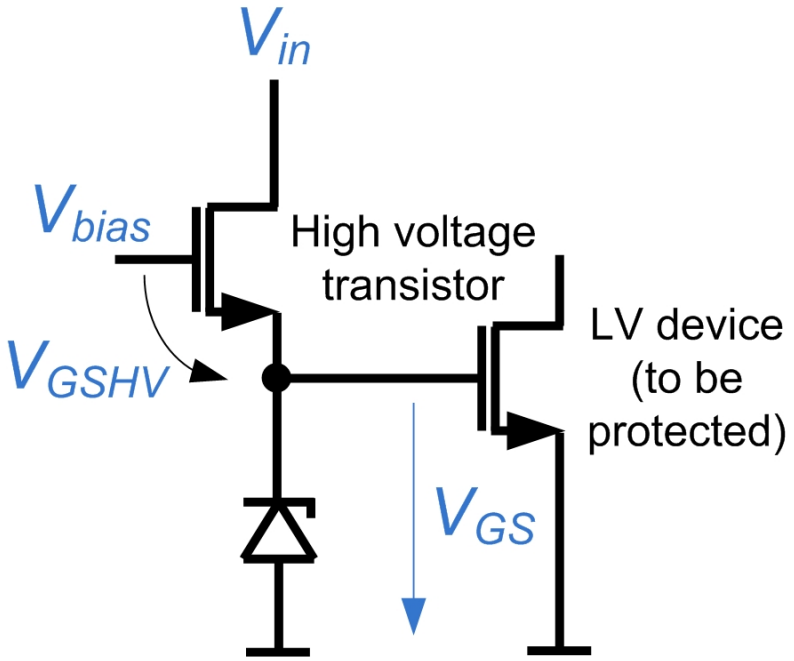
Useful Configurations

Back-to-back



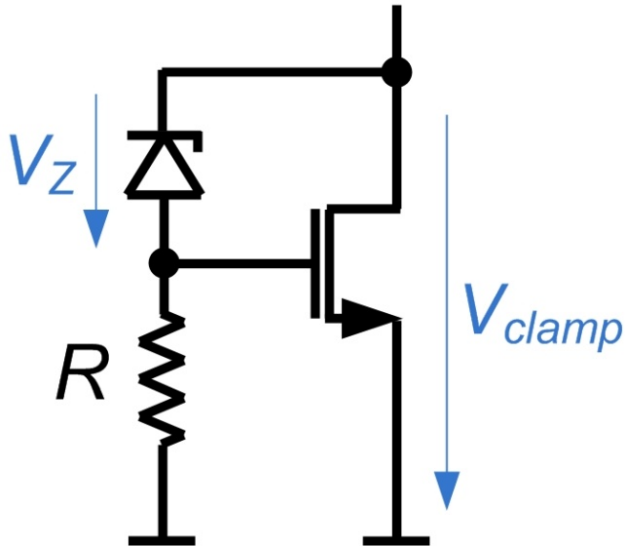
Prevents back-supply into battery or V_{in} of LDO or HS switch (but 4x area!)

Voltage Limitation



DMOS as cascode to keep VGS or VDS of LV devices within max. ratings

Active Zener

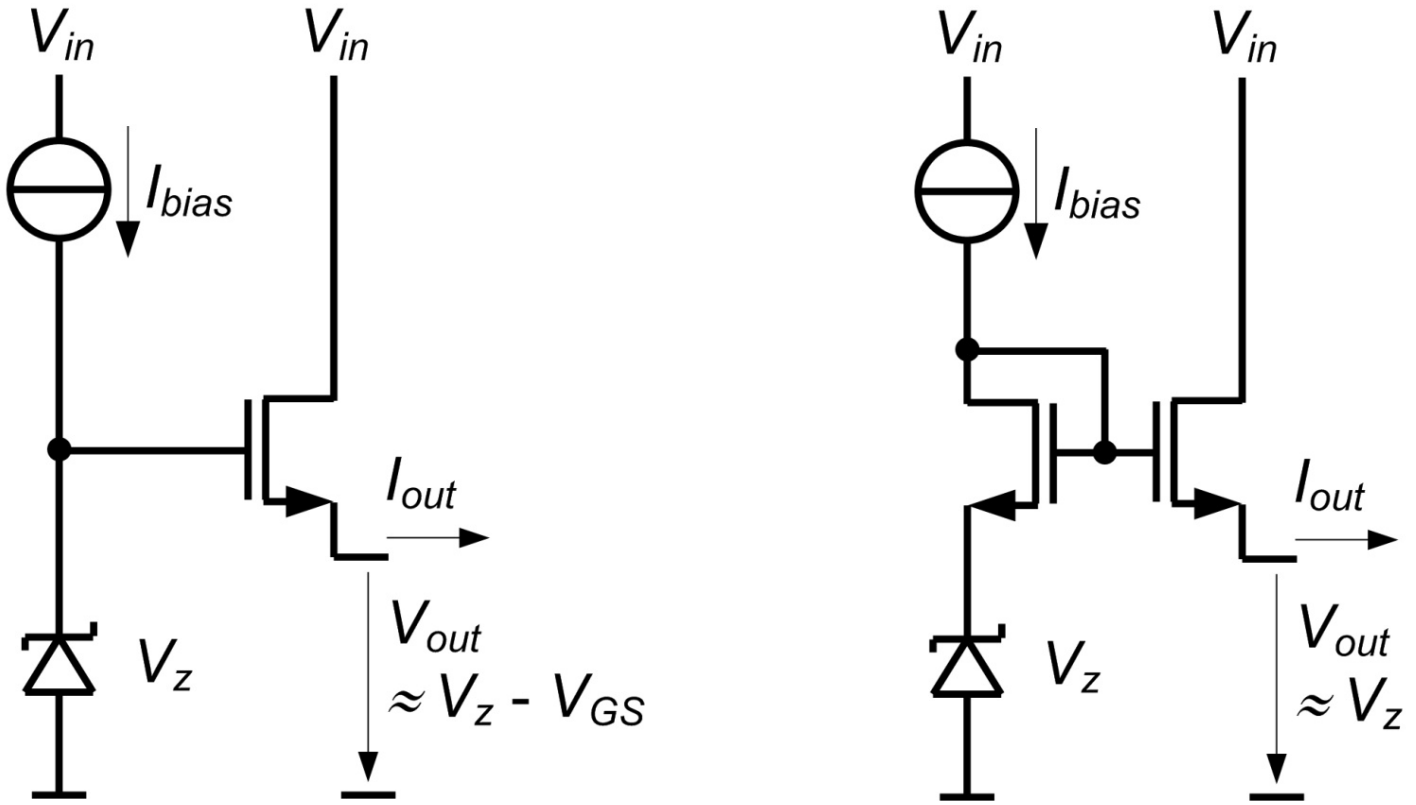


Clamp with large current capability

$V_{clamp} = V_Z + V_{GS}$

Shunt Regulator

Alternative to linear regulator, often as a coarse supply for a noncritical digital block, analog standby or as a pre-regulator



"Open loop" → fast, but not very precise

Interim Q&A Session

Please ask questions that you feel is essential to follow the rest of this tutorial

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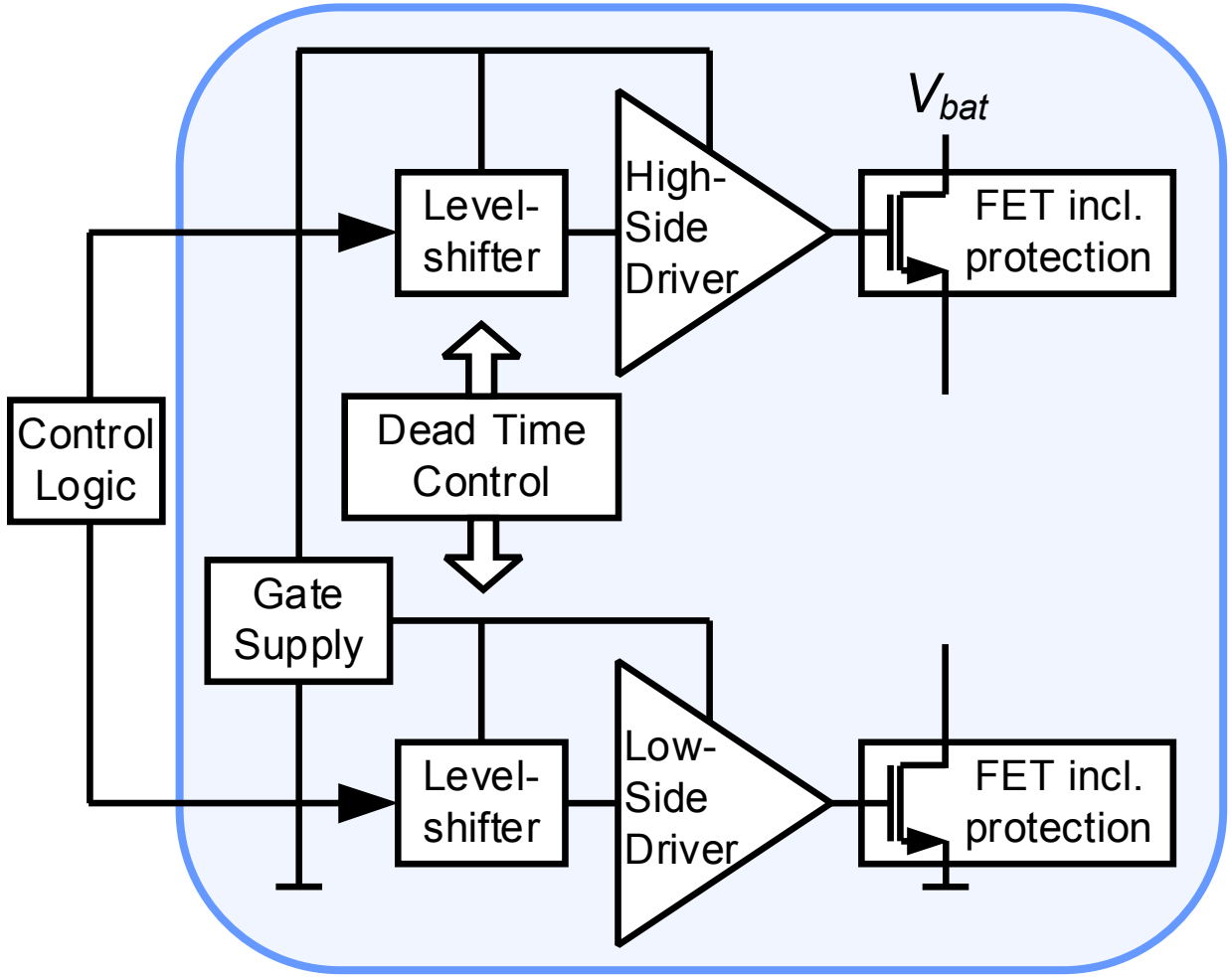
Gate Driver Block Diagram and Circuits

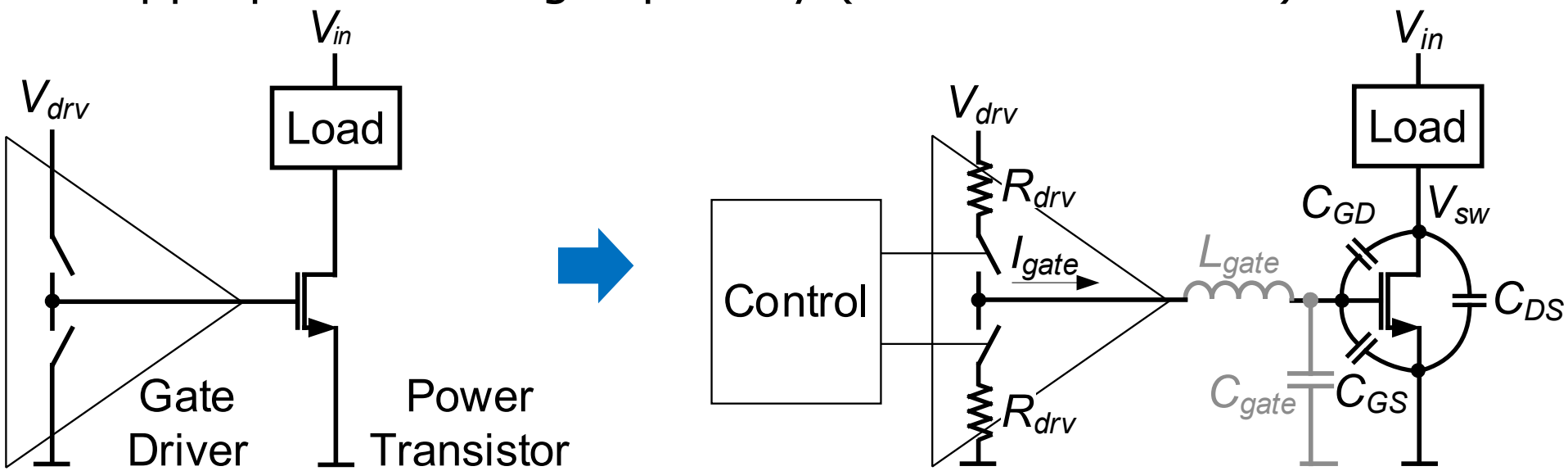
Main circuit blocks:

- Power FET (n/p-type)
- Protection
- LS / HS driver
- Level shifter
- Gate supply
- Dead time control (only for bridges)



Gate Driver Fundamentals, Key Parameters

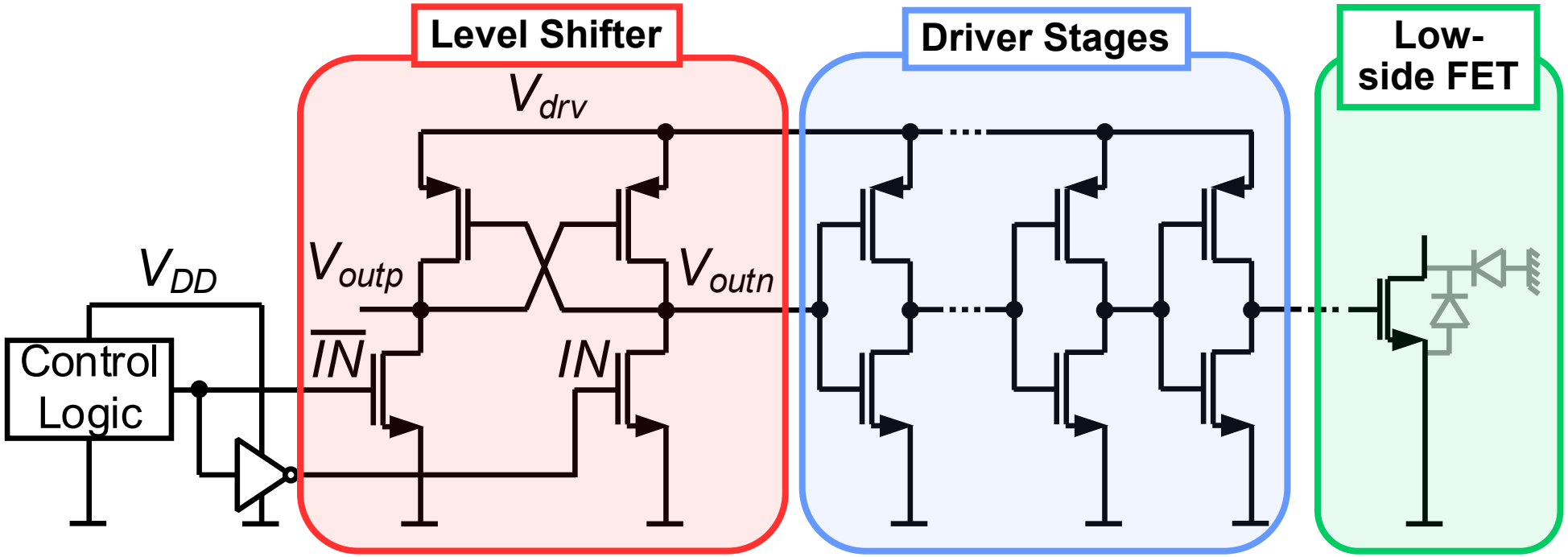
Function: Turn-on/off power switch with sufficient gate overdrive (voltage) and appropriate driving capability (current over time)



- V_{drv} defines the gate-source voltage of the power transistor 5V
- Gate driver sink / source resistance R_{drv} (at given I_{gate}) 1Ω
- Sink / source peak current I_{peak} 1A
- Parasitic L_{gate}: speed ↓, dv/dt triggered turn-on, max. V_{GS}

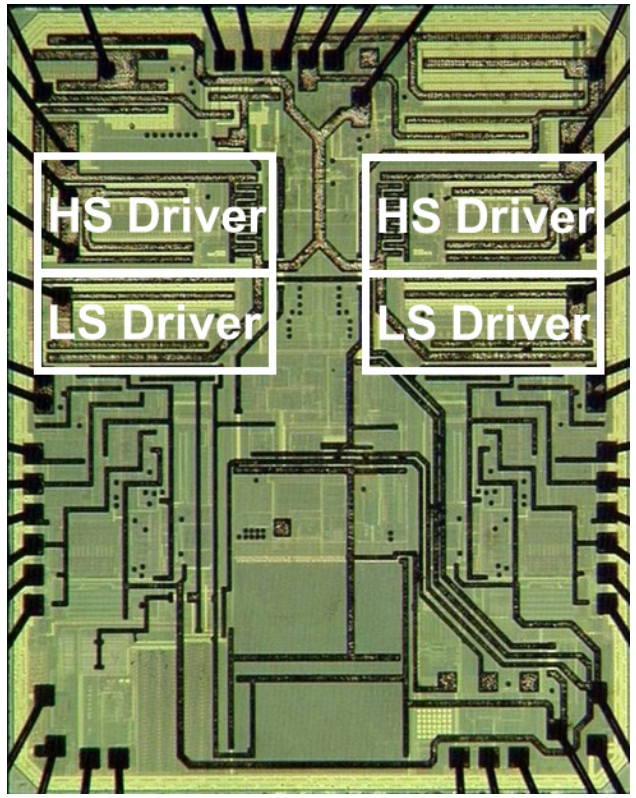
Low-Side Driver

Circuit structure:

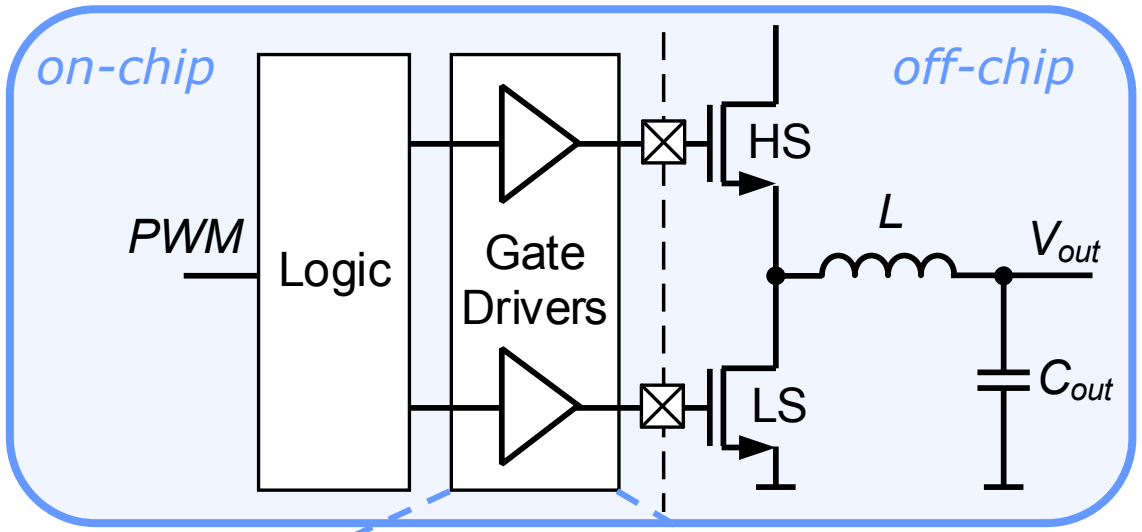


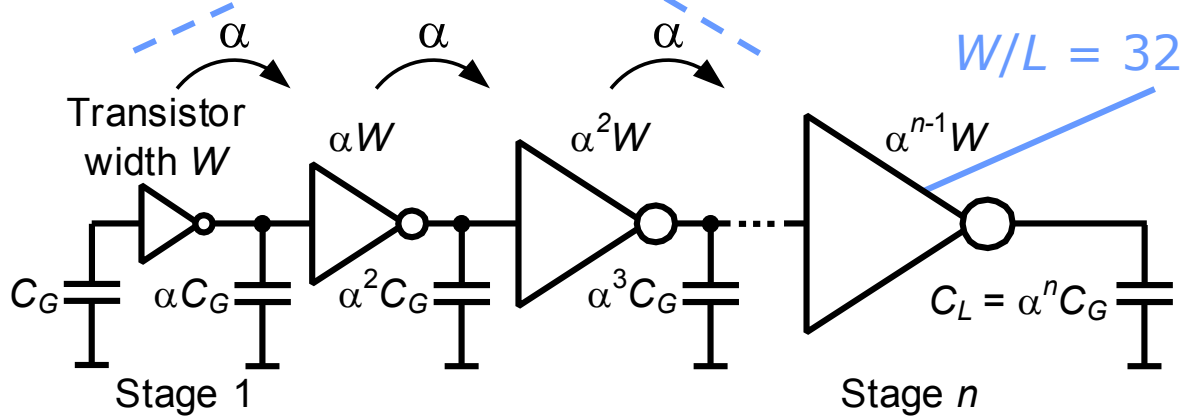
- Level shifter followed by driver stage(s) (CMOS inverter)
- Single driver stage if small power FET (low C_{gate})
- Cascaded driver stages if large power FET (large C_{gate})

Example: Integrated Half-Bridge Driver



Herzer et al. ESSCIRC 2009





Driver resistance: 3Ω
Driver peak current: 1.5A

15ns delay at C_L = 10nF

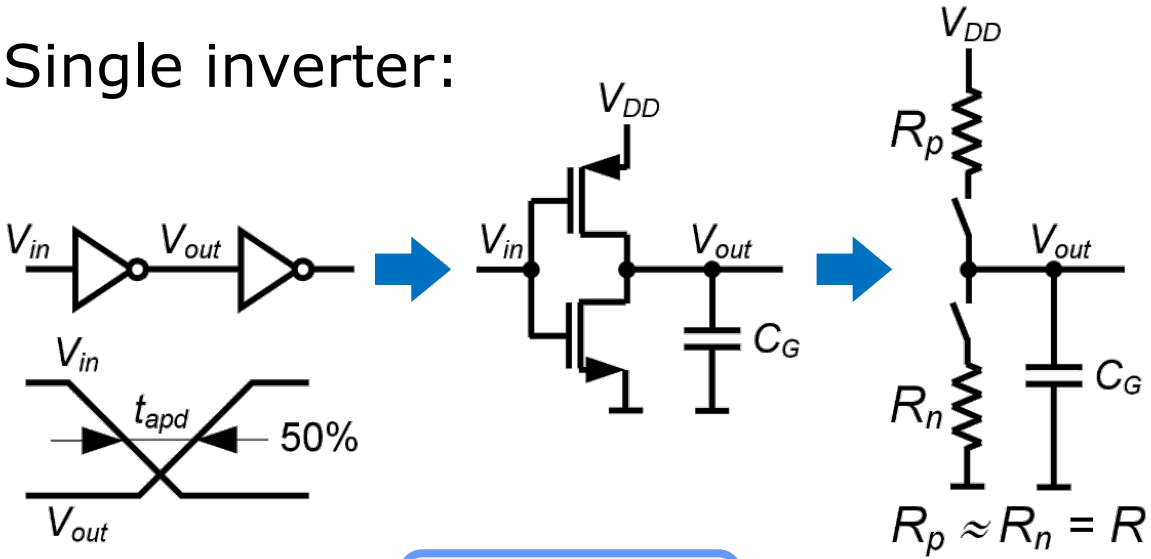
Optimization: *n* stages, each increasing in driver strength (*W*/*L*) by factor α

Cascaded Driver Stages

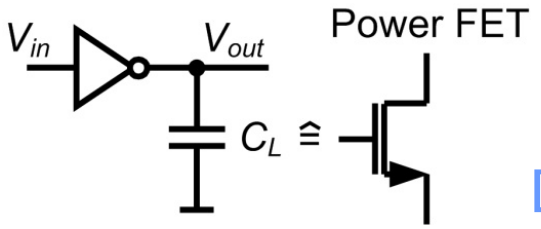
Different design goals depending on application needs:

- Design for minimum delay
- Design for minimum power (correlates with die area)
- Always: Ensure dv/dt immunity → adjust R_{drv} by W/L of last driver stage

Single inverter:



With any load C_L:



Delay scales by ratio C_L / C_G

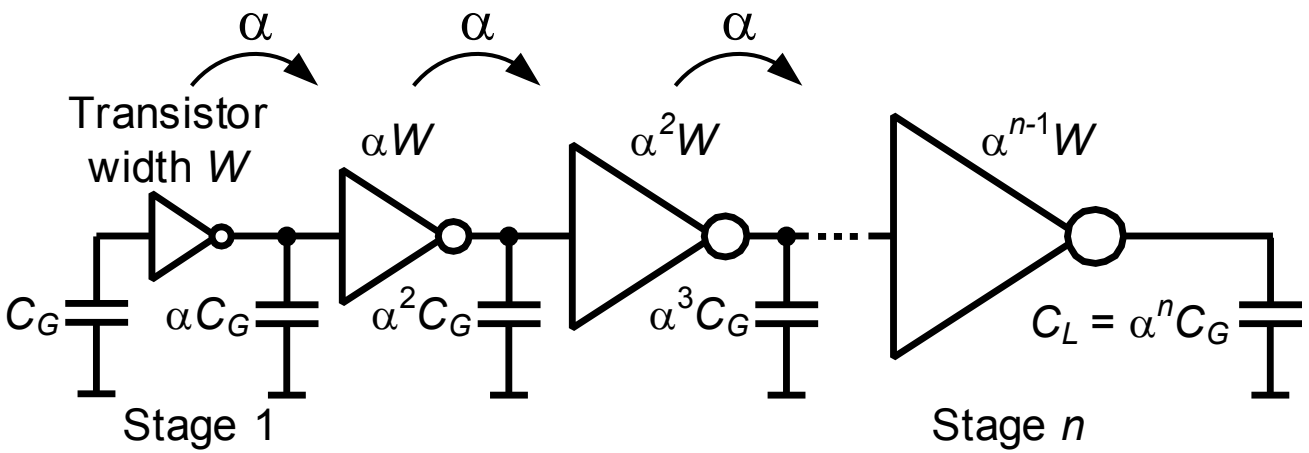
$$t_{apd} \approx R \cdot C_G \rightarrow R = t_{apd}/C_G$$

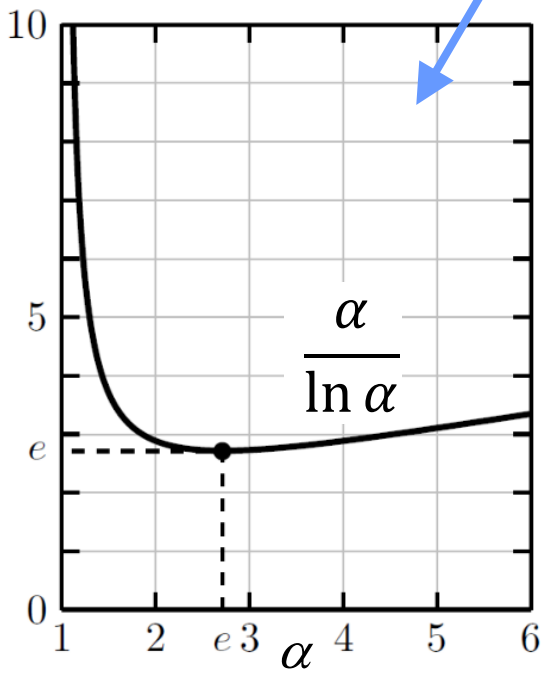
$$t_{direct} = R \cdot C_L = \frac{t_{apd}}{C_G} C_L = t_{apd} \frac{C_L}{C_G}$$

Cascaded Driver: Optimization for Speed

Speed optimization: n stages, each increasing in driver strength (W/L) by α

$$t_{direct} = t_{apd}\frac{C_L}{C_G} \Rightarrow t_{cascade} = nt_{apd}\frac{\alpha^{x+1}C_G}{\alpha^x C_G} = n\alpha t_{apd} \Rightarrow \frac{t_{cascade}}{t_{direct}} = \frac{\ln C_L/C_G}{C_L/C_G}\cdot\frac{\alpha}{\ln\alpha}$$





Practical trade-off speed vs. area, power:

Choose α = 3...6 (≫ Euler's number e) → calculate n

Example: C_L = 300pF, C_G = 30fF, t_{apd} = 1ns

→ t_{direct} = 10µs, $t_{cascade,min}$ = 25ns (α = e, n = 9), $t_{cascade}$ = 32ns (α = 6.3, n = 5)

Optimization for Power Efficiency and Area

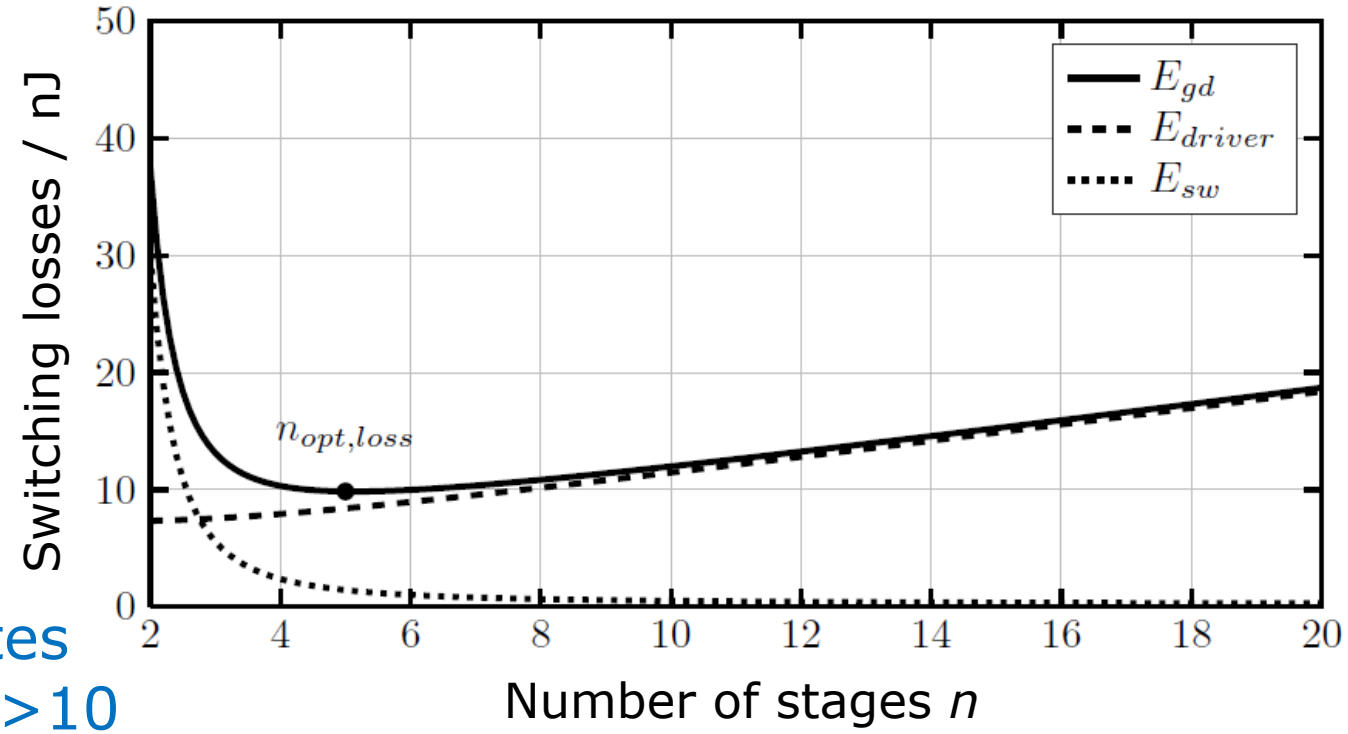
Optimization for speed does not result in minimum driver power loss:

- Too many stages: Increasing driver losses E_{driver}
- Too few stages: Increasing power FET switching losses E_{sw} due to larger rise/fall times

Options:

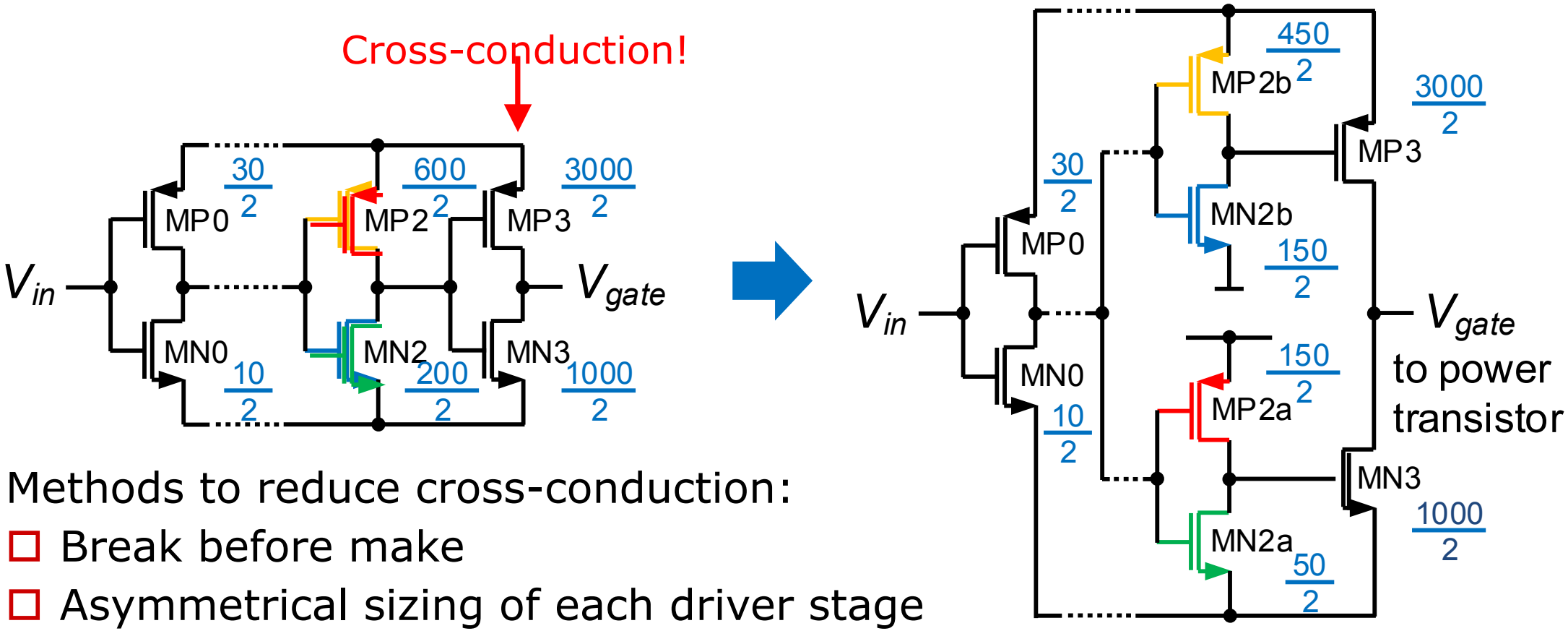
- Fixed-taper buffer
  [Villar, ISCAS 2005]
- Combination of fixed-taper and variable-taper buffers
  [Vemuru, JSSC Sept. 1991]

Rule: Fewer stages n → correlates to larger scaling factors α → 6…>10



Optimization for Power Efficiency: Last Stage

Further power reduction by eliminating cross-conduction in last driver stage
→ separate branches for pull-up / down path → no area penalty

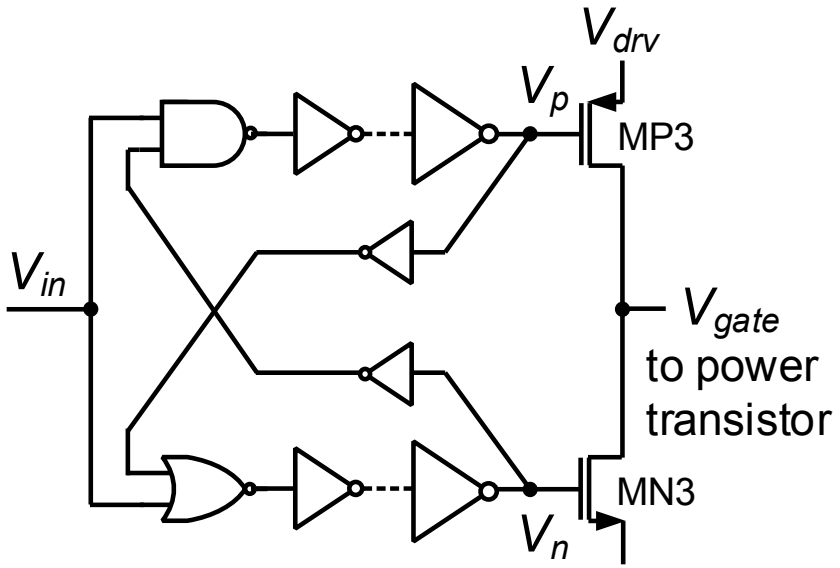


Methods to reduce cross-conduction:

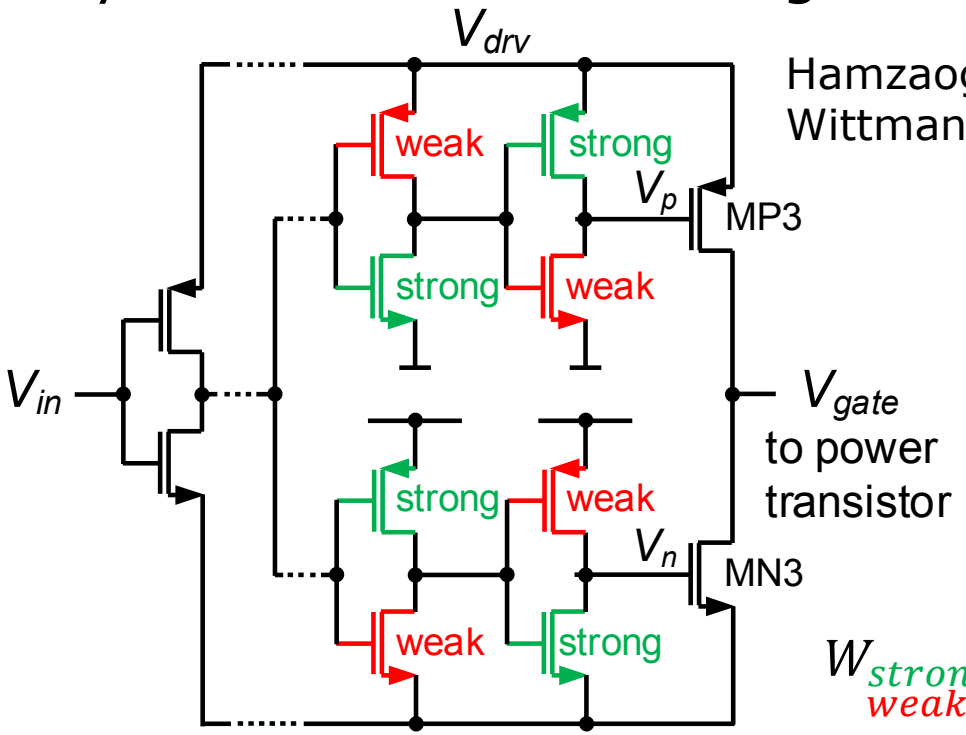
- Break before make
- Asymmetrical sizing of each driver stage

Reduction of Cross-conduction in Last Stage

Break before Make



Asymmetrical Driver Sizing



Hamzaoglu TCAS II Oct. 2001
Wittmann JSSC July 2018

$$W_{\substack{strong \\ weak}} = W\left(1 \pm \frac{AF}{100\%}\right)$$

Drawback:

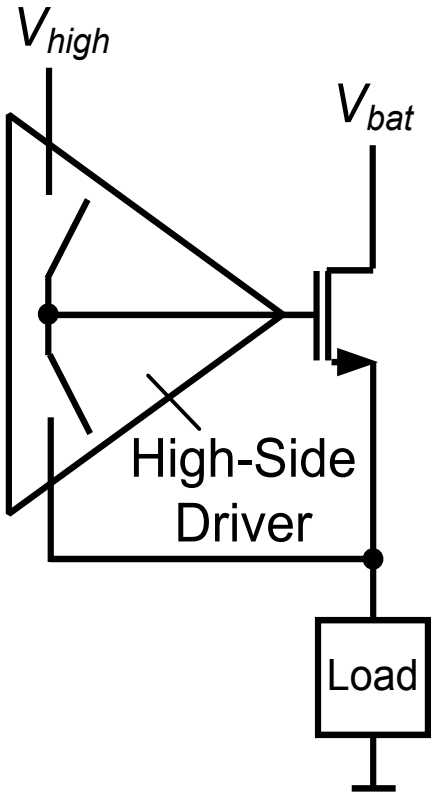
- Large delay (switching signal propagates 2x through buffer)
- Delay margin required to cope with process variations

Adjust width *W* found for optimum speed or losses by asymmetry factor *AF* = 20-30%:

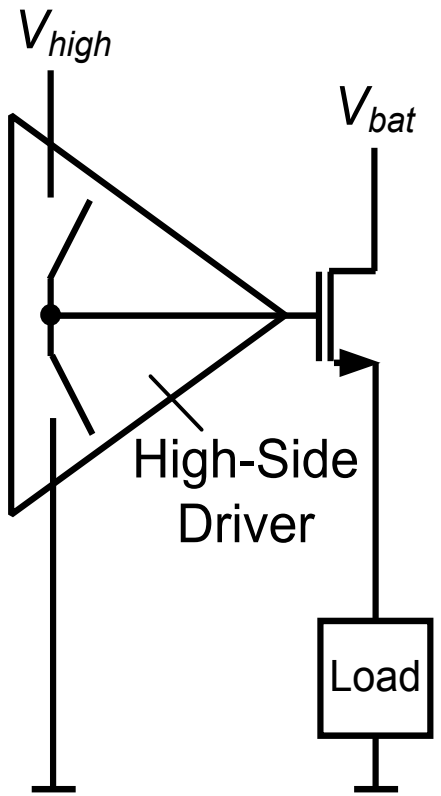
- Fast Turn-off of MN3, slow turn-on MP3 and in pre-stages

High-Side Driver

Type 1 Floating Driver



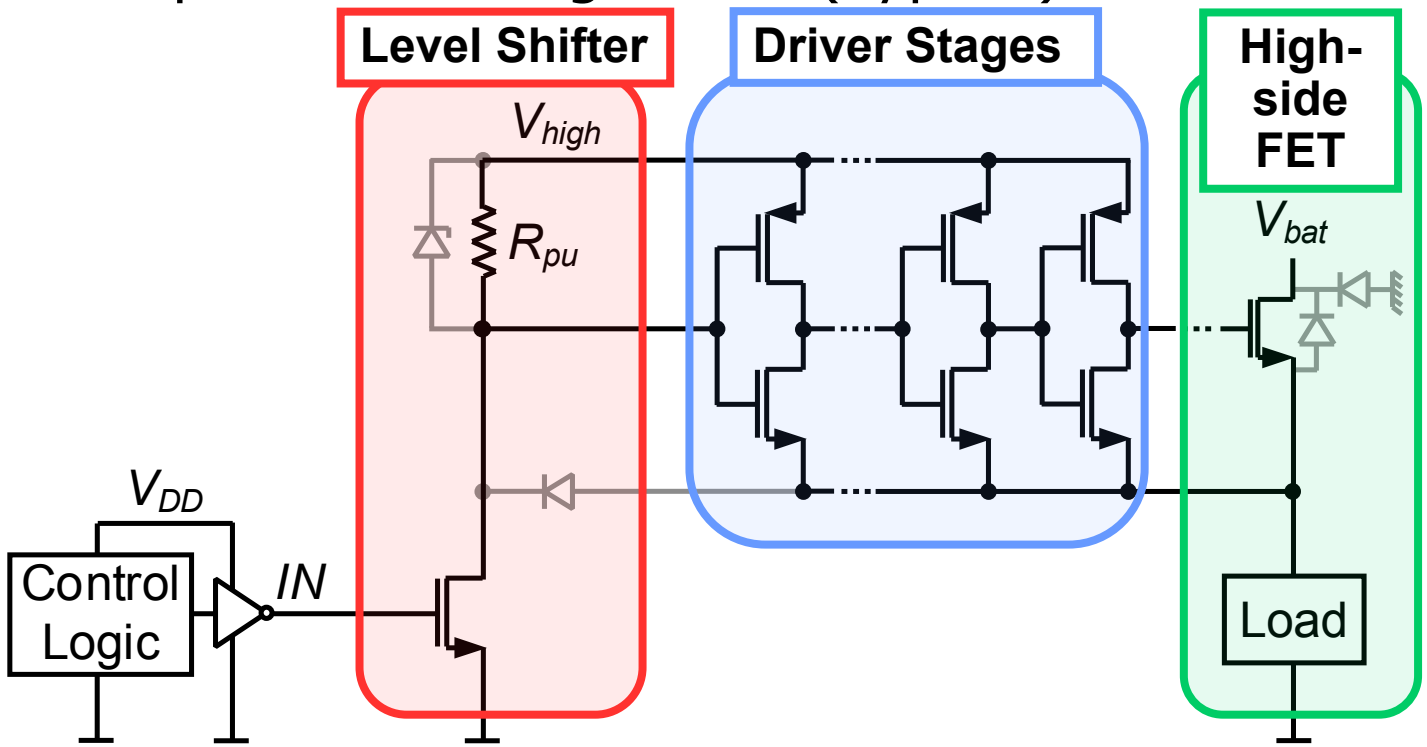
Type 2 Referred to ground



- n-type power switch: Overdrive needed → $V_{high} = V_{bat} + V_{GS}$
- V_{high} from charge pump, bootstrapping or boost converter

High-Side Driver

Example for floating driver (Type 1)

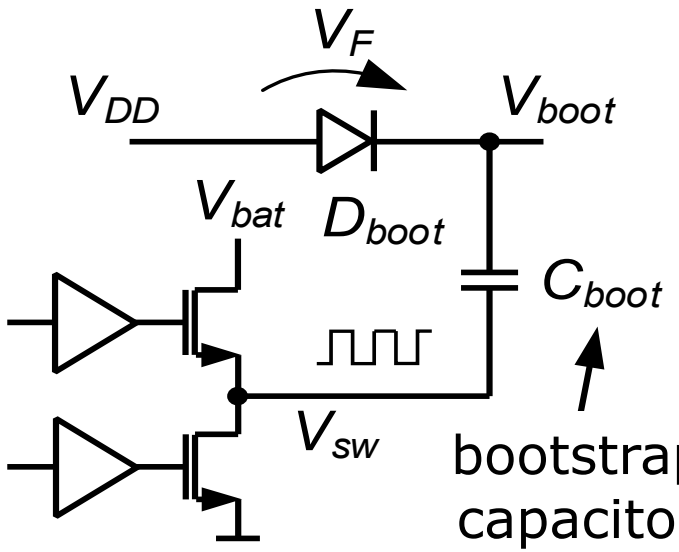


- Driver stage: Low voltage transistors even for large V_{bat}
- R_{pu}: Tradeoff between speed and DC current (typ. 100kΩ)
- Diode(s) to clamp voltage across R_{pu} and limit V_{GS} for driver

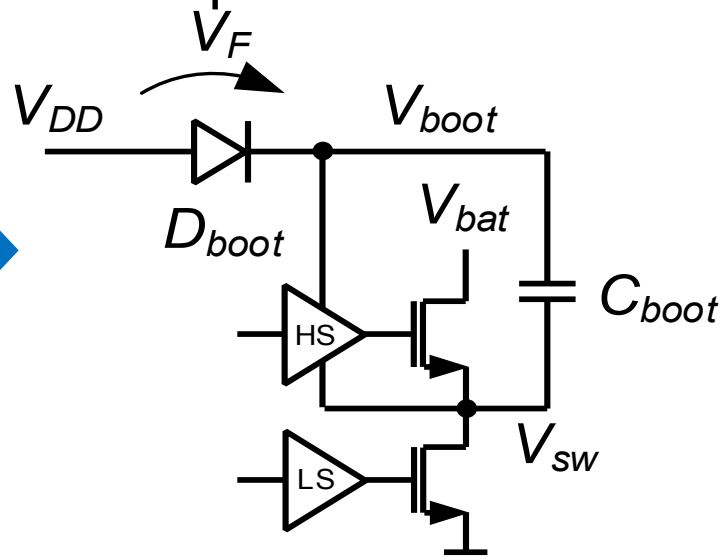
High-Side Gate Supply: Bootstrapping

Similar to charge pump with oscillator replaced by half-bridge (power stage)

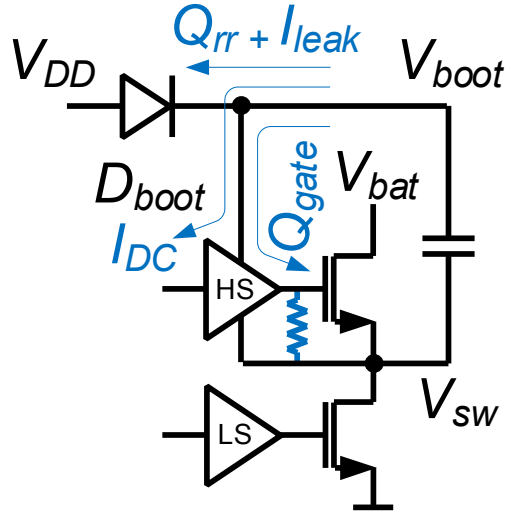
Principle



Circuit Implementation



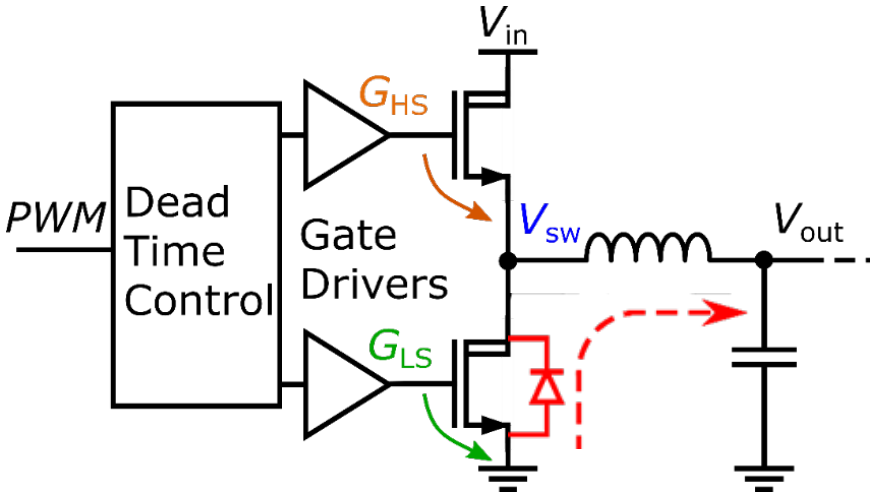
Energy delivered by C_{boot}

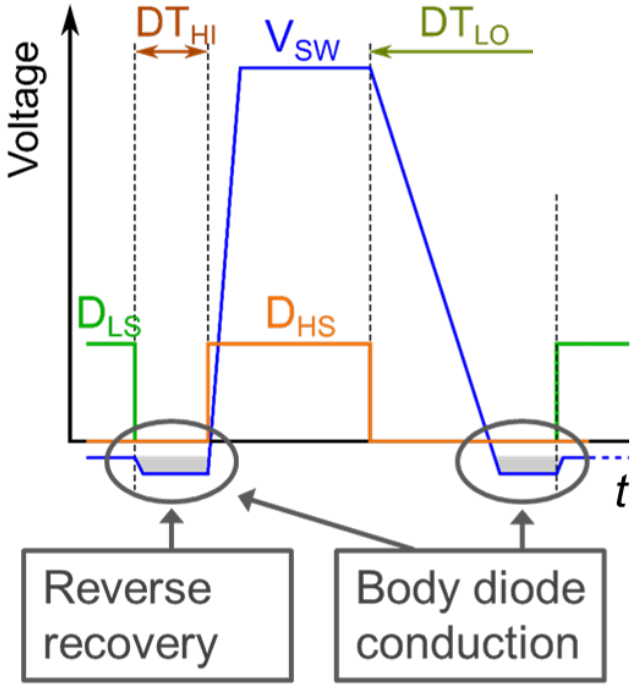


- C_{boot} supplies high-side driver → $V_{boot} = V_{bat}+V_{DD}-V_F$
- C_{boot} gets recharged if high-side is off (low-side on, V_{sw} = 0V) from V_{DD} through bootstrapping diode D_{boot}
- Sizing: $C_{boot} \geq (Q_{gate} + Q_{rr} + I_{boot} / f_{sw}) / \Delta V_{boot}$

Example:
Q_{gate} = 10nC, Q_{rr} = 1nC, I_{boot} = 500µA, ΔV_{boot} = 0.1V @ f_{sw} = 500kHz
→ $C_{boot} \geq$ 120nF

Power Stage Dead Time Control

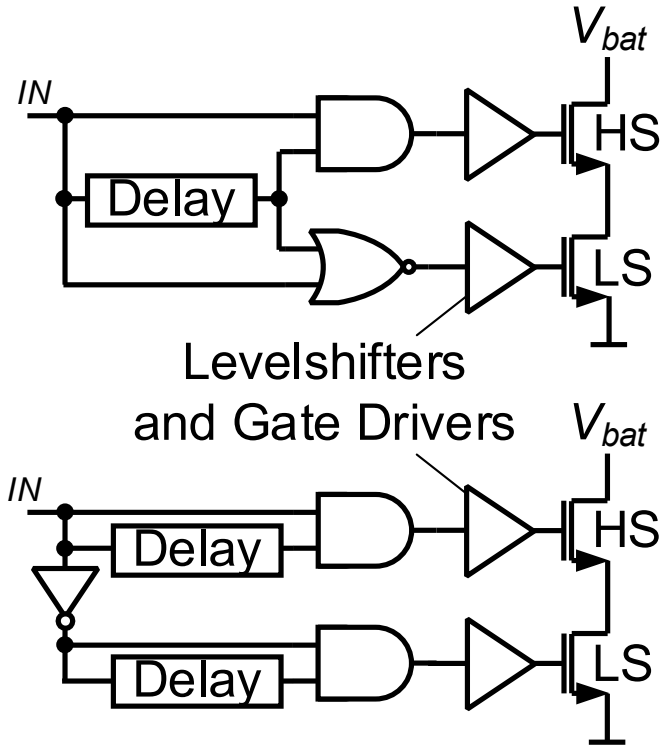




- Turn off one FET → then turn on other FET with dead time in between
- To avoid cross-conduction (damage!) and minimize losses
  - Cross-currents, body-diode (VF, Qrr), zero-voltage switching, >25% loss reduction
- Optimum dead time dependent depends on operating point (V_{in}, load,…)
  - Constant delay (with trimming)
  - Adaptive delay: Sensing of off-state → then turn on other FET
  - Predictive delay: Cycle-by-cycle control, complex

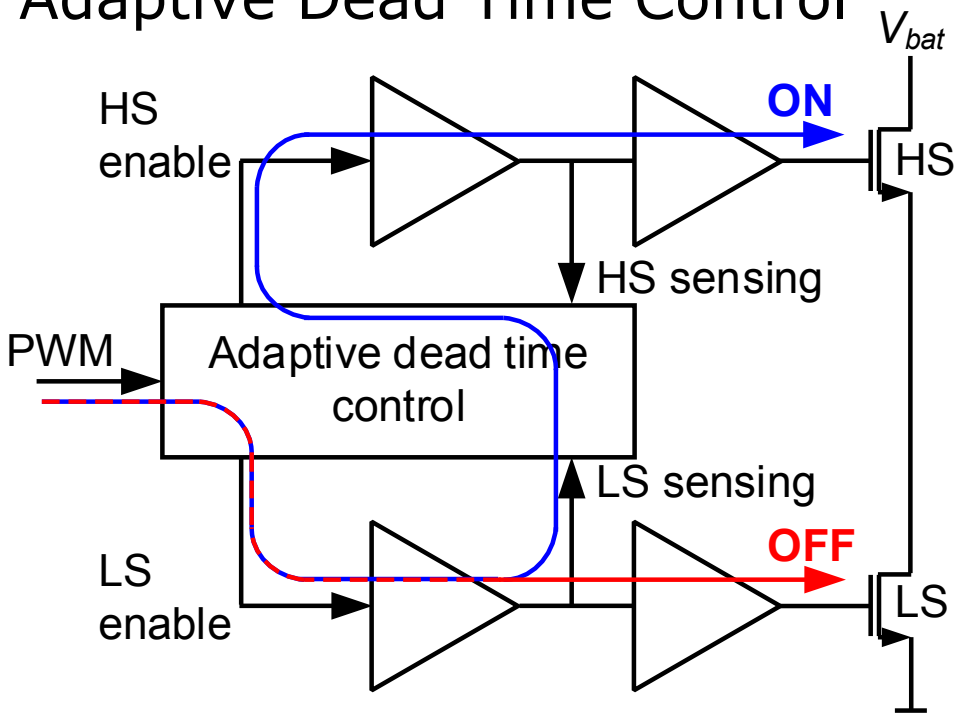
Dead Time Control Concepts (1)

Constant Delay (two examples)



- Worst case margin → large t_{dead}
- delay trimming → length of inverter chain

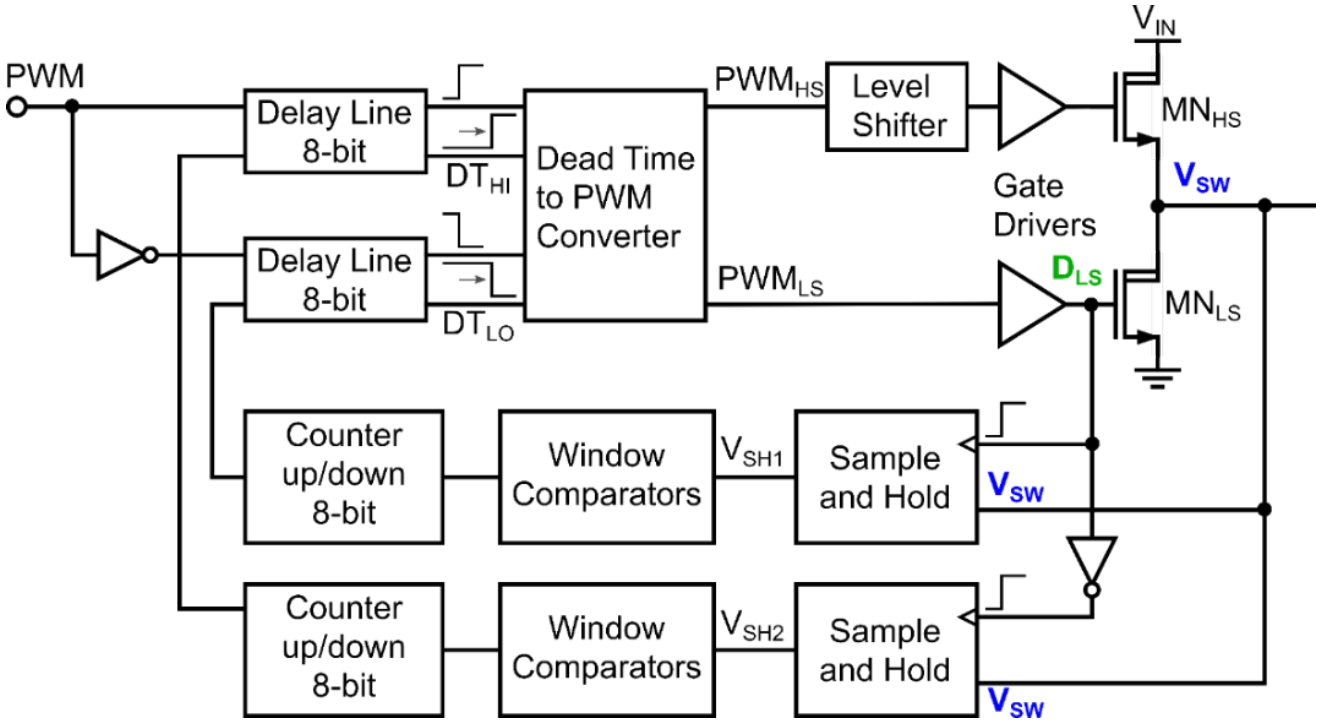
Adaptive Dead Time Control

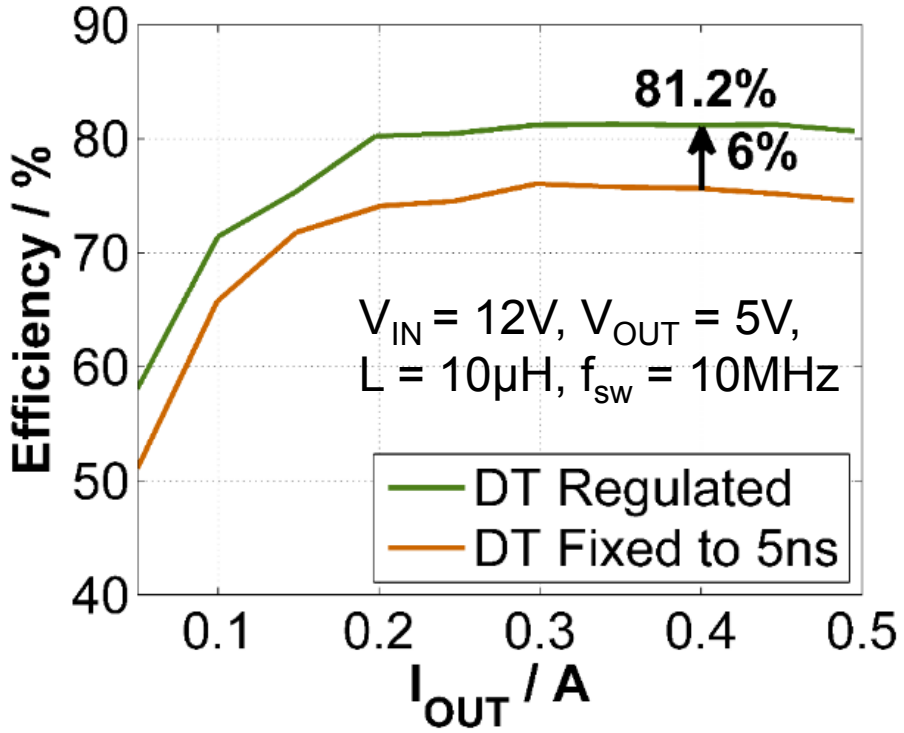


- Off-state detection at cascaded drivers allows shorter t_{dead}
- LS sensing: Simple inverter
  HS sensing: Down-level shifter

Dead Time Control Concepts (2)

Predictive mixed-signal dead time control [Wittmann JSSC July 2016]:





- 10MHz buck converter, 125ps dead time resolution by inverter delay line
- Low-side turn-on if V_{sw}~0V, sensed by S&H, no body diode conduction
- Loss reduction of up to 30% → 6% higher efficiency at 10 MHz

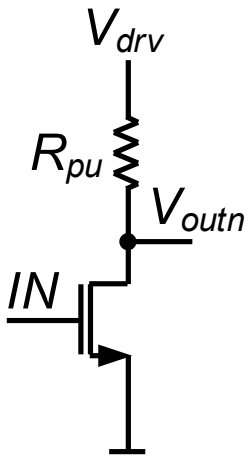
Outline

- Introduction
- Power Transistors
- Gate Drivers
- Level Shifters
- Control Loop
- System Design

Basic Level Shifter Configurations

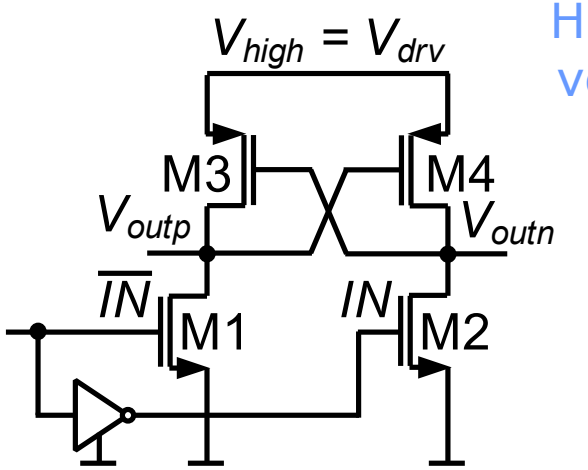
Signal transmission from low side (control) to high side (power stage)

Resistor-based Level Shifter



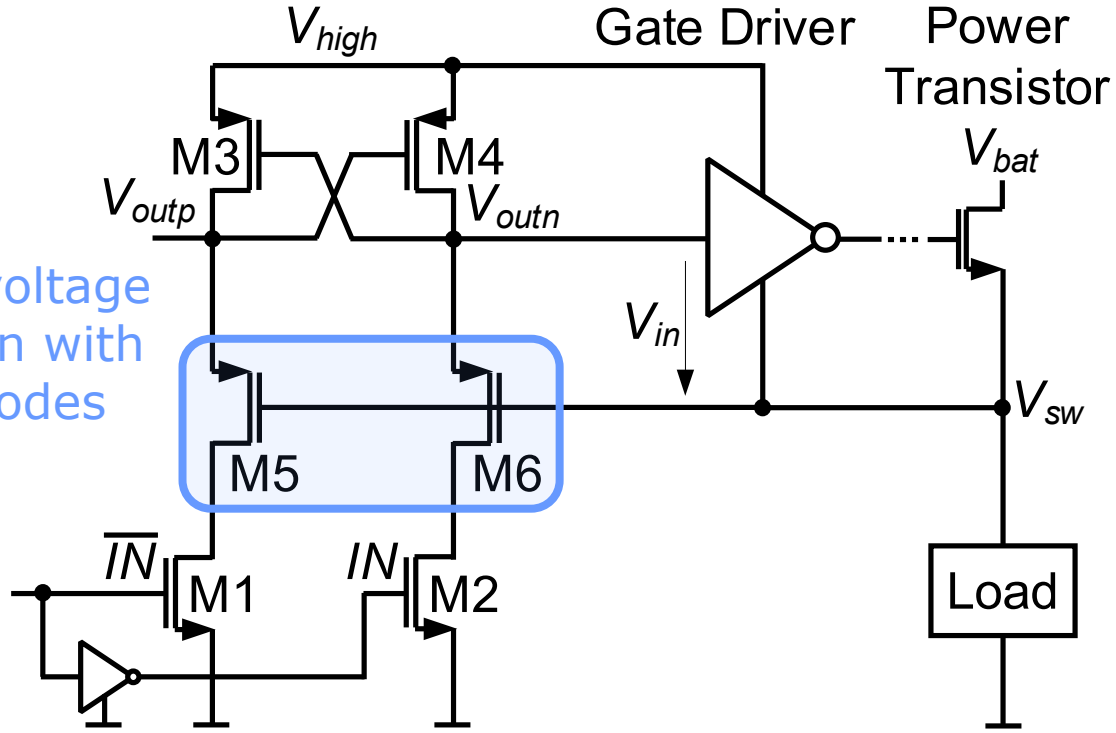
- DC current
+ Simple, small
+ Default state

Cross-coupled Level Shifter



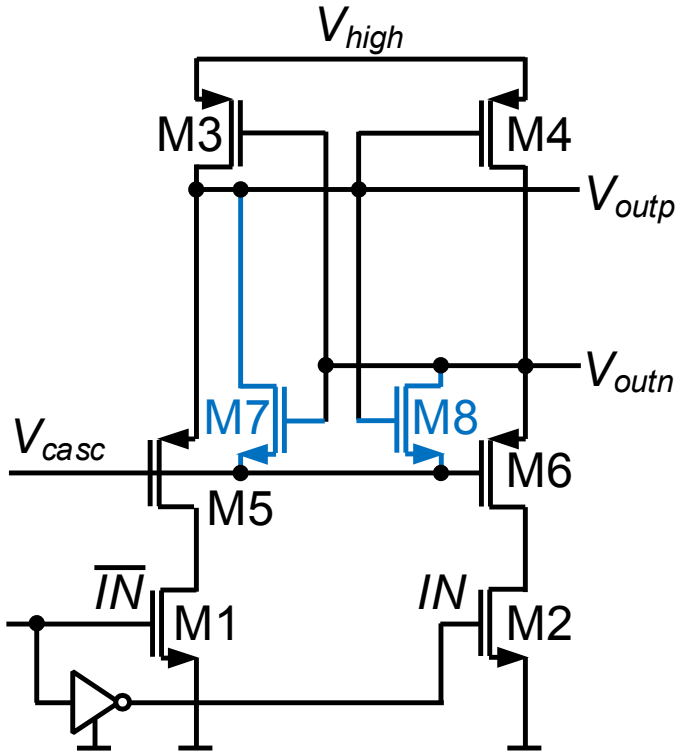
+ No DC current
- Slow and large area
- No default state

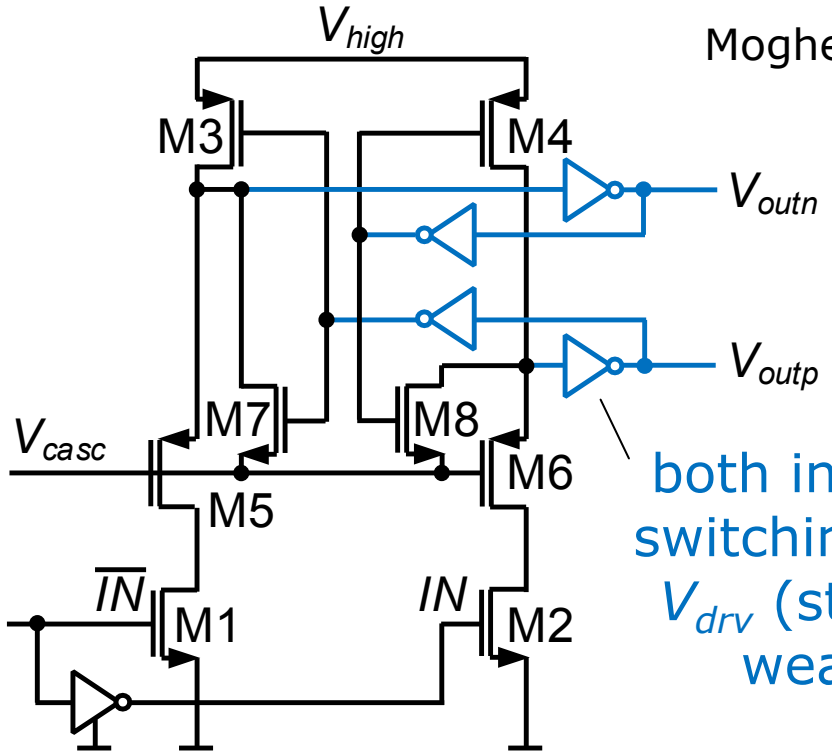
High-voltage version with cascodes



Drawback: $V_{in} \neq V_{sw}$
→ weak '0' level at gate driver input → cross-currents!

Cross-coupled Level Shifter with Full HS Swing





Moghe, JSSC Feb. 2011

both inverters with switching point near V_{drv} (strong pmos, weak nmos)

V_{SG} of cascodes M5, M6 prevents logic '0' level at driver input → full high-side swing achieved by bypass devices M7, M8

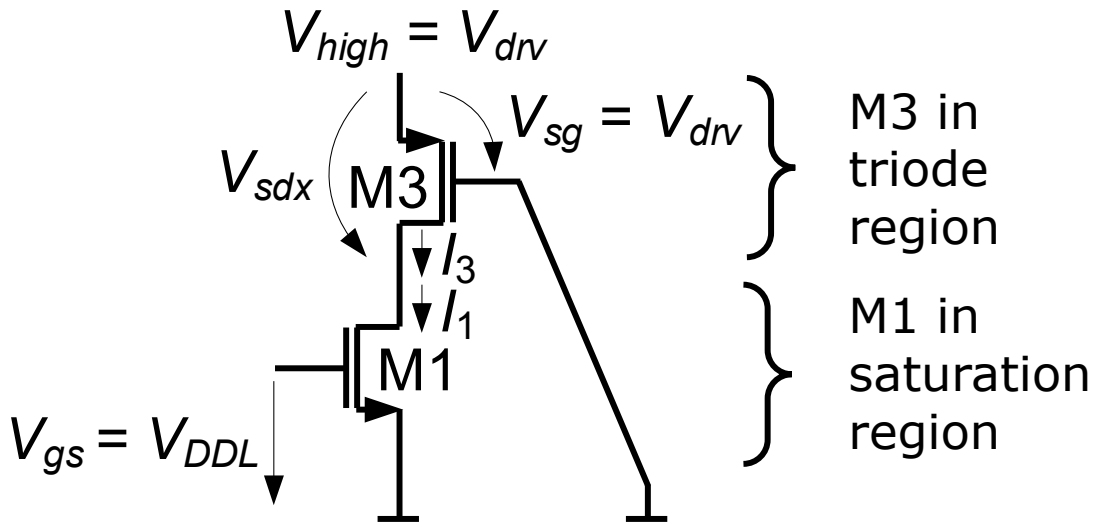
Inverters increase loop gain → faster switching and reduced power consumption → M7, M8 can become minimum size

Sizing of the Cross-coupled Level Shifter (1)

M1 (M2) needs to be strong enough to pull drain of M3 (M4) below V_{drv} by one V_{th} → W/L follows from condition $I_1 = I_3$ (= I_5)

$$\left(\frac{W_1}{L_1}\right) \Big/ \left(\frac{W_3}{L_3}\right) = 2\frac{\mu_{op}}{\mu_{on}}\frac{(V_{drv} - V_{th})V_{sdx}}{(V_{DDL} - V_{th})^2}$$

$$V_{th} = V_{thn} = |V_{thp}|$$



Moghe JSSC Feb. 2011

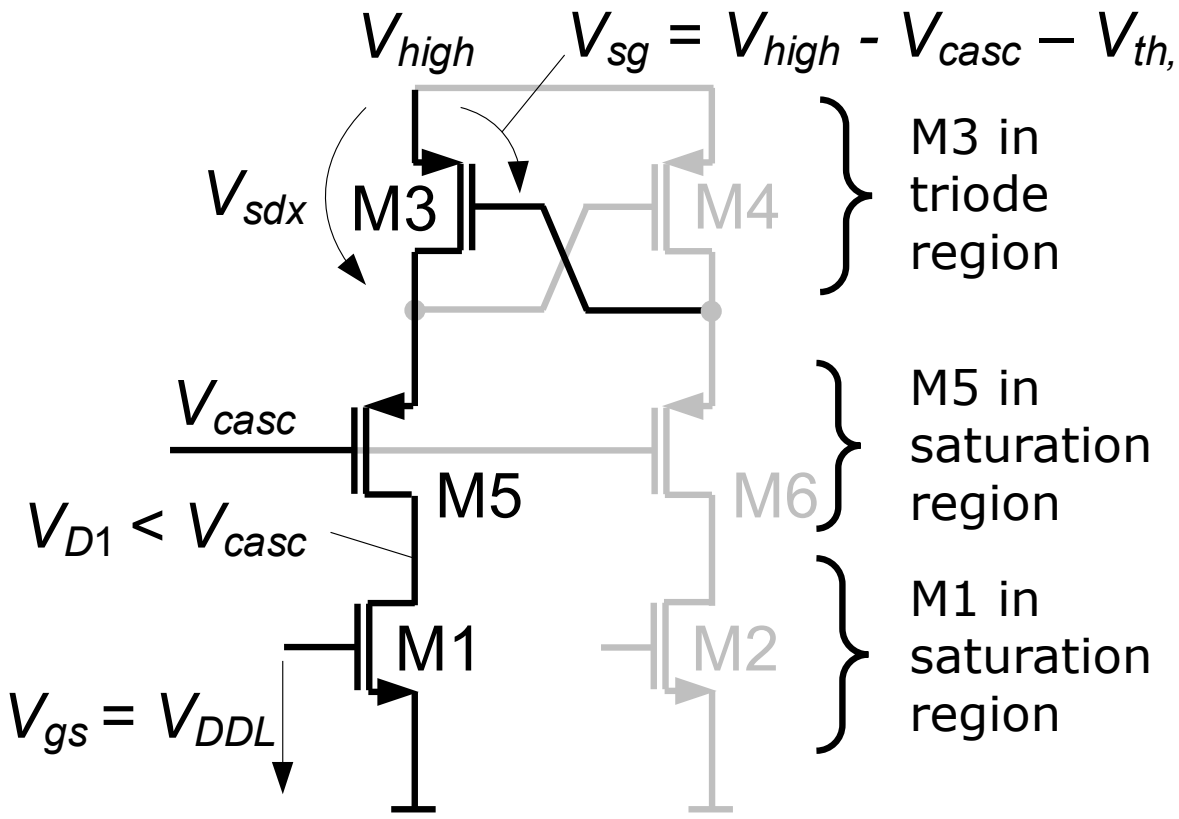
Design guideline:

1. Use minimum L and $V_{sdx} \geq V_{th}$ (higher V_{sdx} gives higher speed)
2. Choose min. W1, W3 (and W5) that fulfill sizing equation(s)
3. Increase W1, W3 (and W5) concurrently to enhance speed
4. W_1 may be set even larger to faster charge parasitic cap at drain of M1, M3

Example: μ_{op}/μ_{on} = 1/3, V_{drv} = 12V, V_{DDL} = 3.3V, V_{th} = 0.8V → Width ratio M1 to M3 = 0.96 ~ 1

Sizing of the Cross-coupled Level Shifter (2)

M1 (M2) needs to be strong enough to pull drain of M3 (M4) below V_{drv} by one V_{th} → W/L follows from condition $I_1 = I_3$ (= I_5)



$$\frac{\left(\frac{W_1}{L_1}\right)}{\left(\frac{W_3}{L_3}\right)} = 2\frac{\mu_{op}}{\mu_{on}}\frac{(V_{drv} - V_{casc} - V_{th})V_{sdx}}{(V_{DDL} - V_{th})^2}$$

$$\frac{\left(\frac{W_5}{L_5}\right)}{\left(\frac{W_3}{L_3}\right)} = 2\frac{(V_{drv} - V_{casc} - V_{th})V_{sdx}}{(V_{drv} - V_{casc} - 2V_{th})^2}$$

$$V_{th} = V_{thn} = |V_{thp}|$$

Moghe JSSC Feb. 2011

Outline

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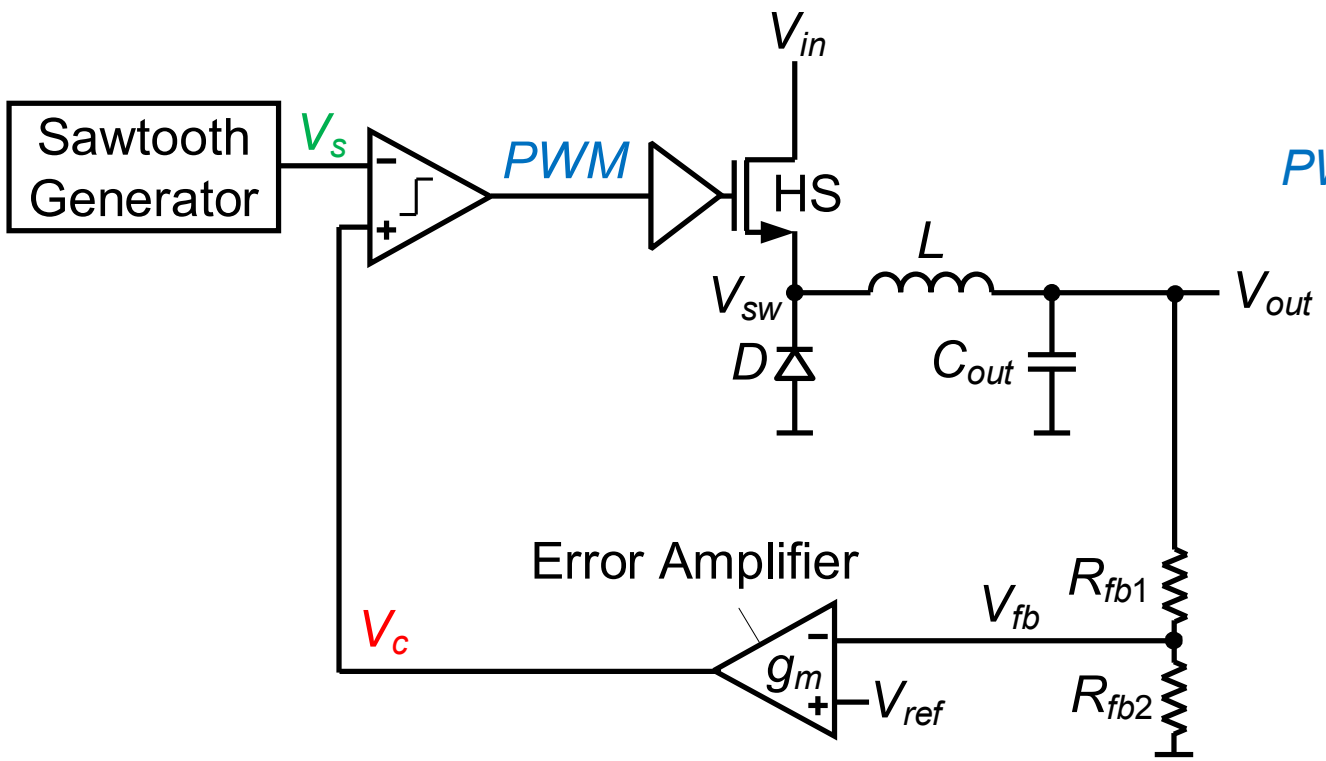
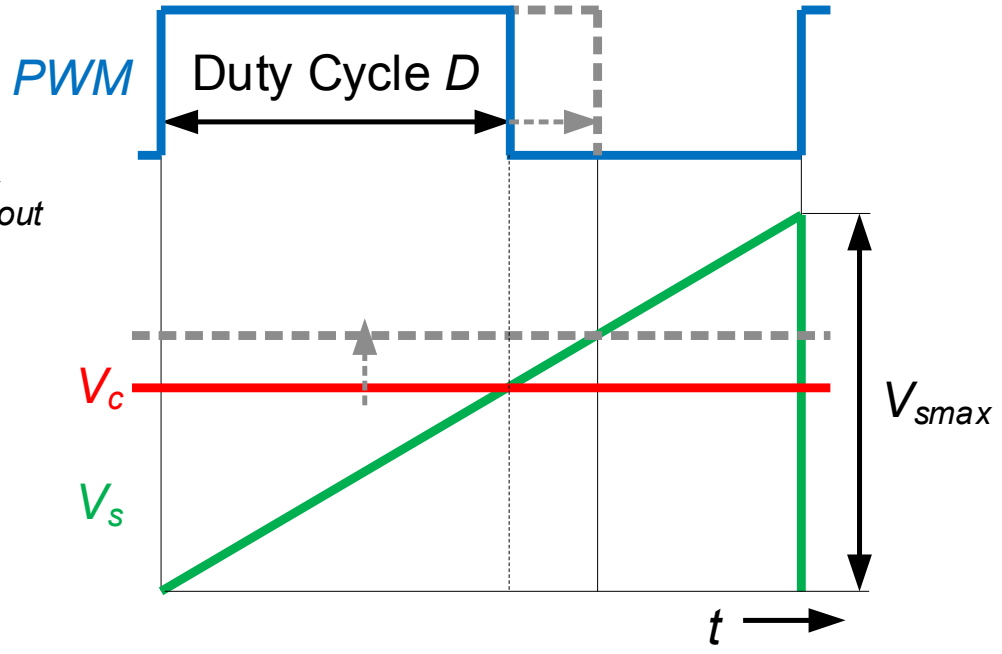
Regulation Schemes: Voltage Mode Control





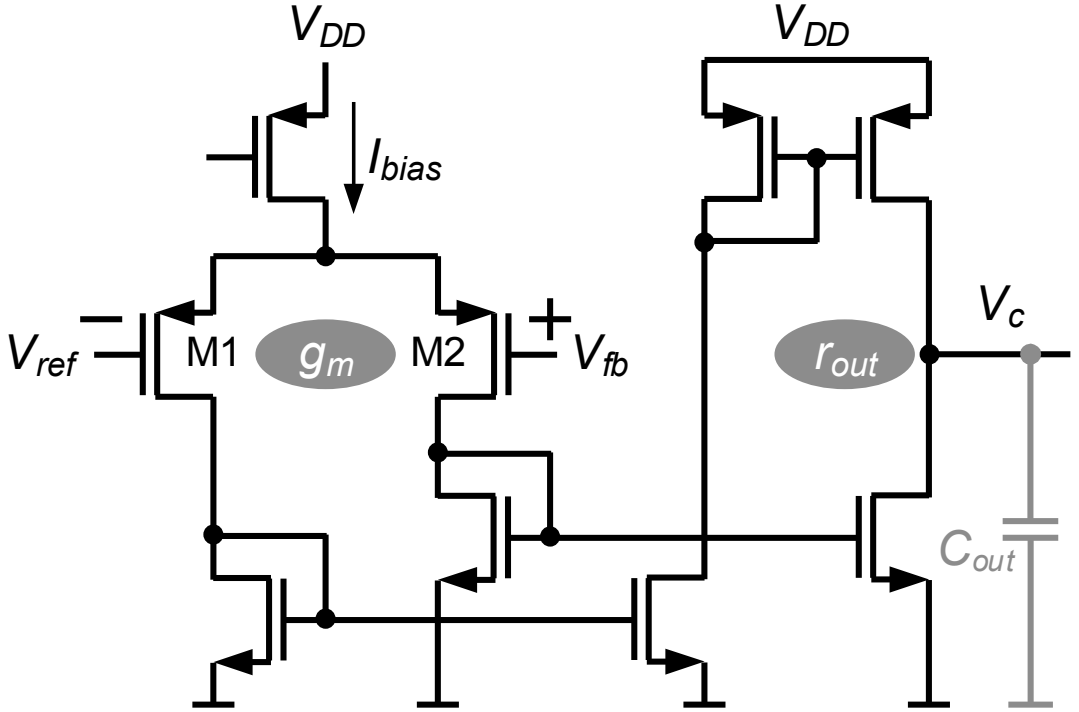
Two-pole plant transfer function: Change in D has L-C_{out} time constant
→ relatively slow, complex loop stabilization

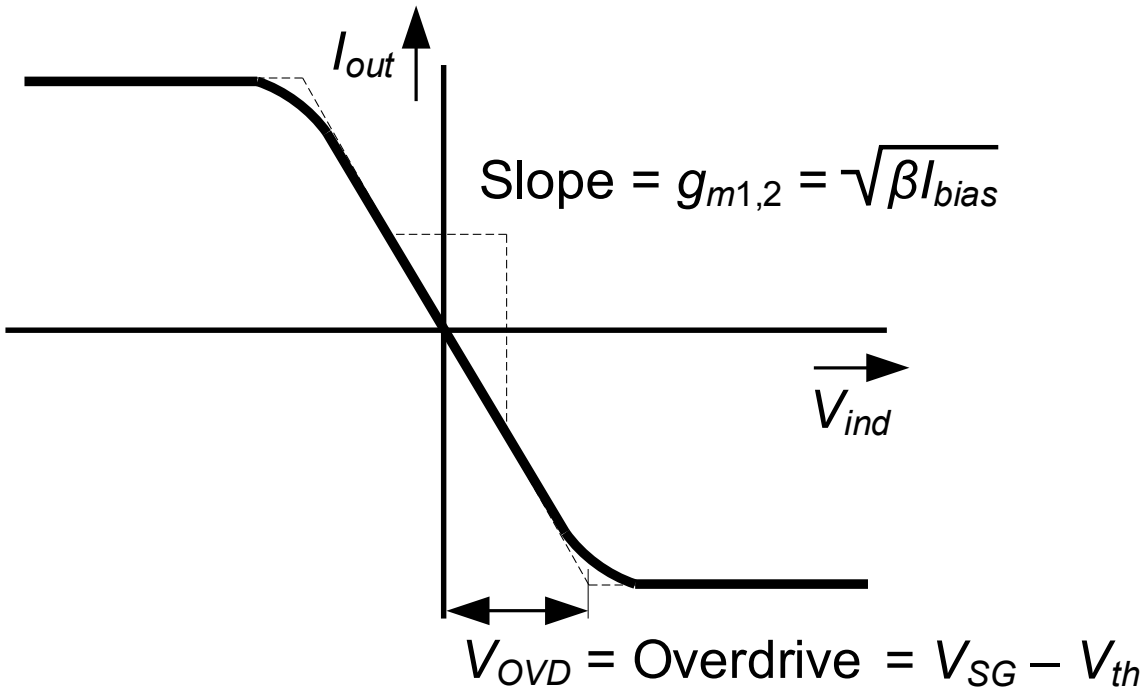
Error Amplifier

Influence on line / load regulation, transient response, etc.

Widely used:
symmetrical OTA, cascode OTA

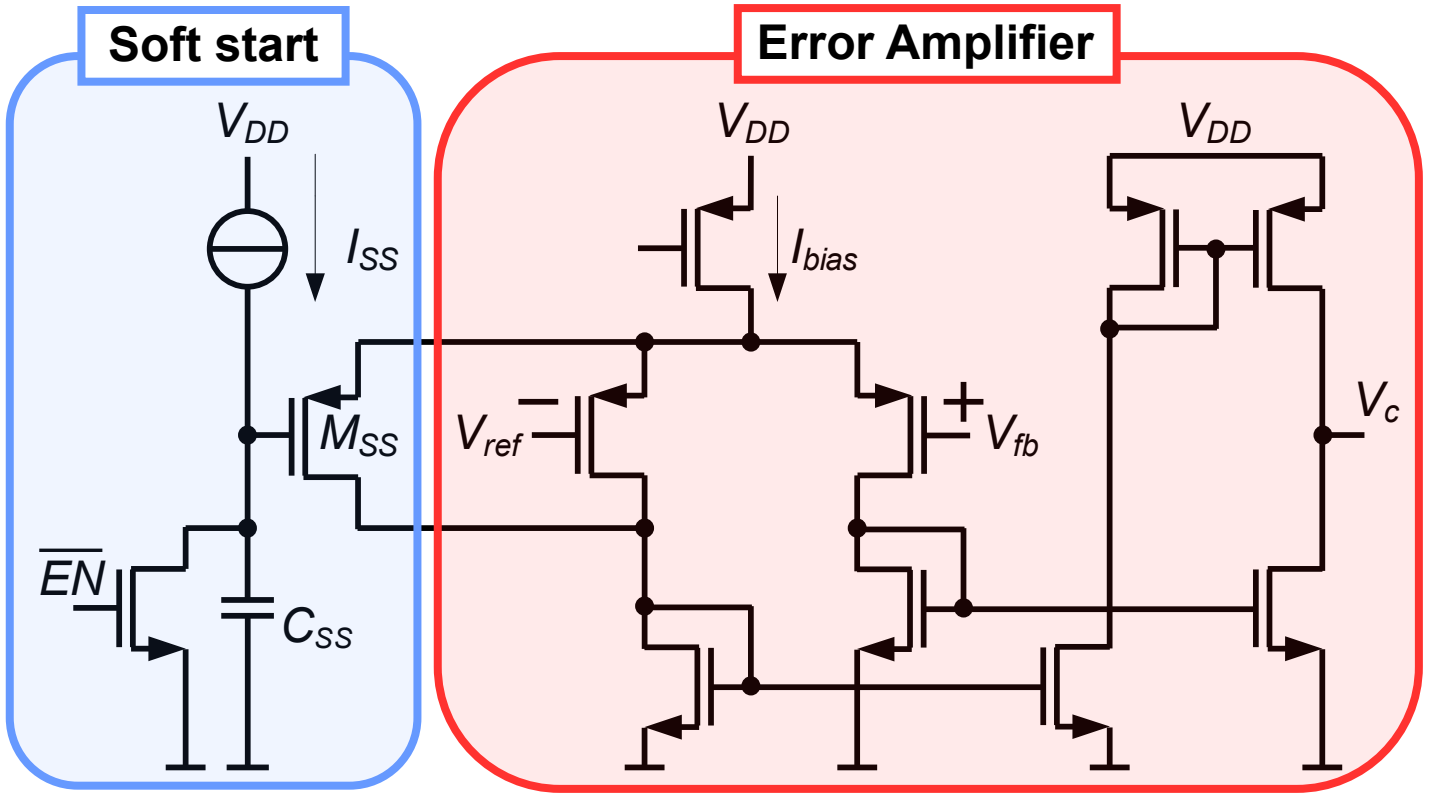
Loop compensation
requires well controlled
$G_m = g_m$ of input pair



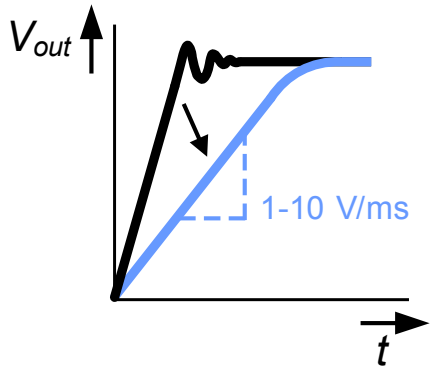


Soft Start

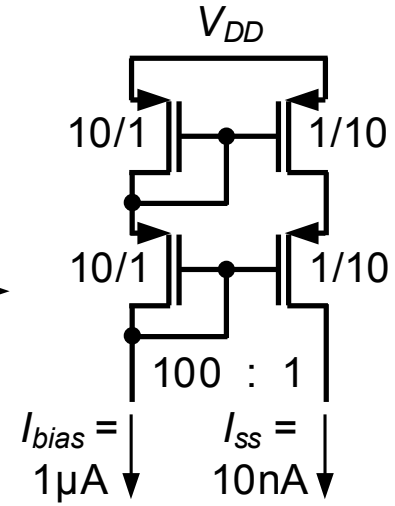
To prevent inrush currents at start-up: Soft start input at error amplifier replaces fixed reference by slowly increasing ramp of ~1-10 V/ms



Converter Output



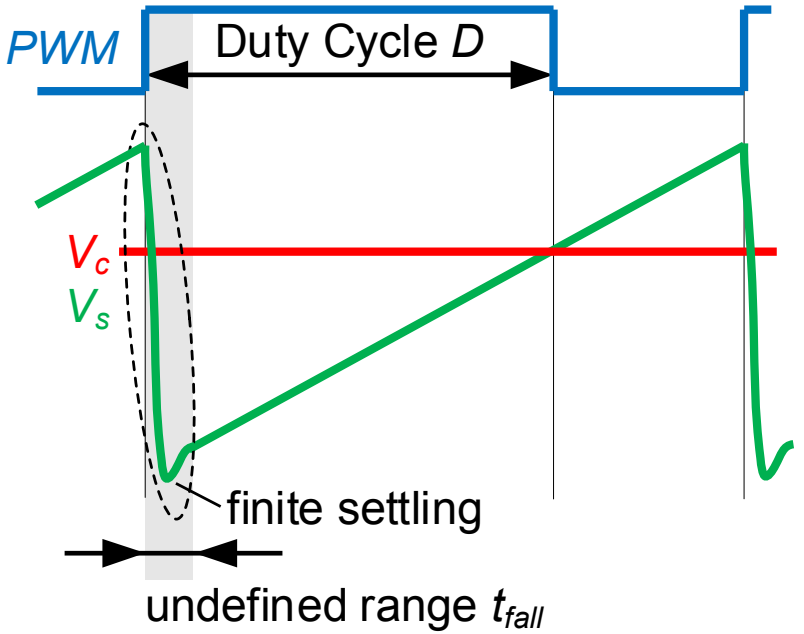
Reasonable capacitance values → I_{ss} in nA range:



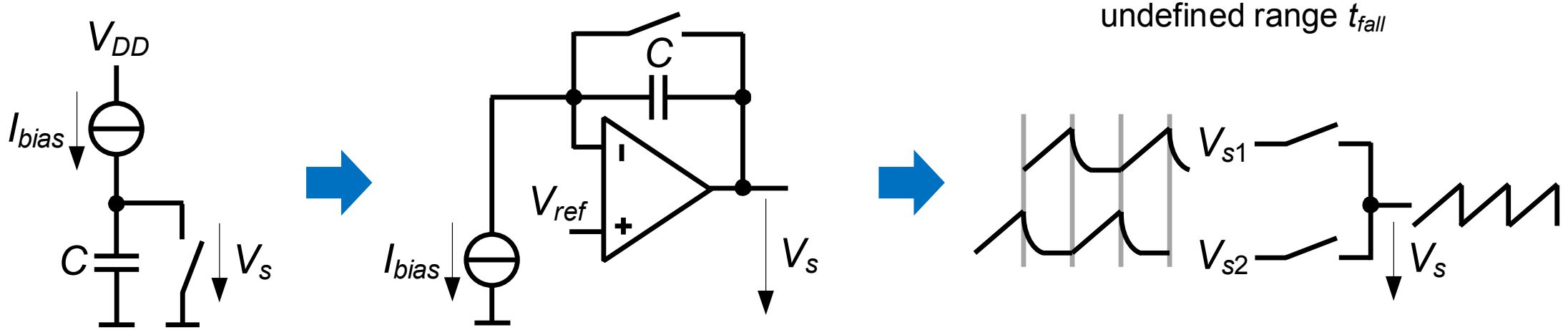
Example: Slope = 2V/ms, C_{ss} = 5pF → I_{ss} = 2V/ms·5pF = 10nA

Sawtooth Generator

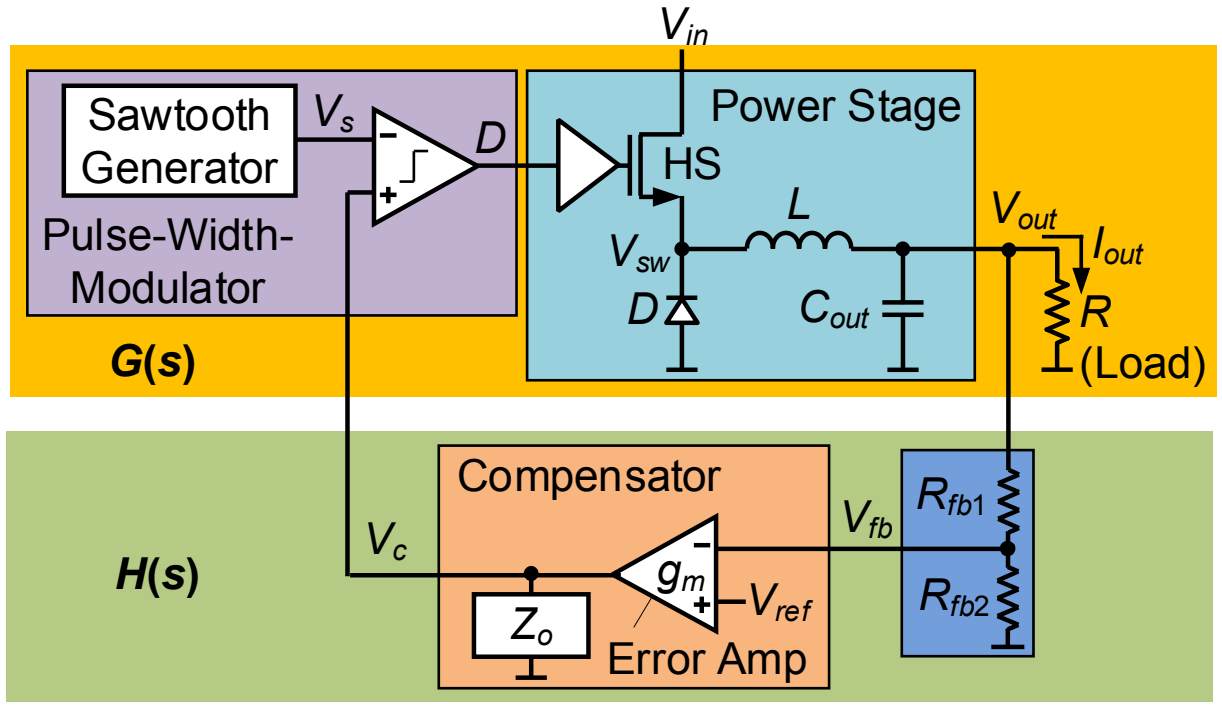
Settling time of falling edge limits duty cycle and switching frequency



Preferred solution: Integrator with fast and precise refresh, saw tooth bias level easily controlled by V_{ref}, can be combined with time-interleaved approach (two integrators)



Control Loop Analysis and Stability



$$\alpha = \frac{R_{fb2}}{R_{fb1} + R_{fb2}}$$

Closed loop transfer function: $\frac{V_{out}}{V_{ref}} = \frac{1}{\alpha} \frac{G(s)H(s)}{1 + G(s)H(s)} \sim \frac{1}{\alpha}$

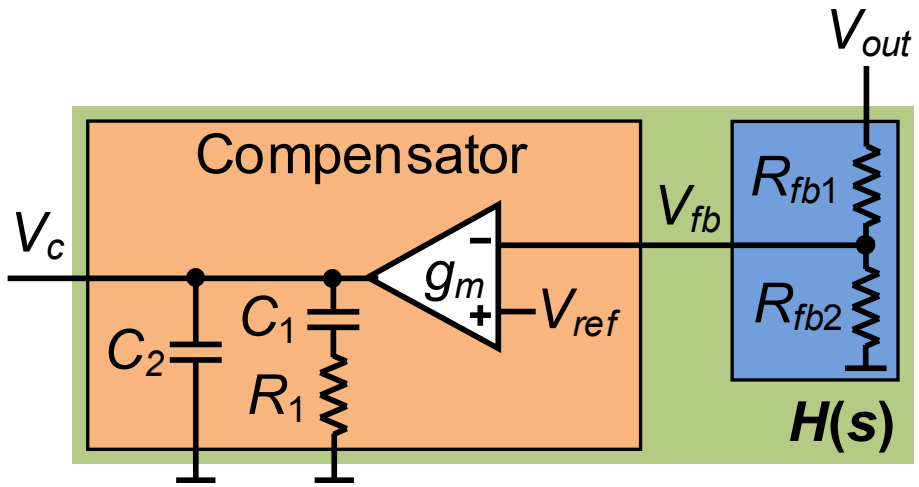
→ Loop gain: $\frac{V_{fb}}{V_{ref}} = G(s)H(s)$

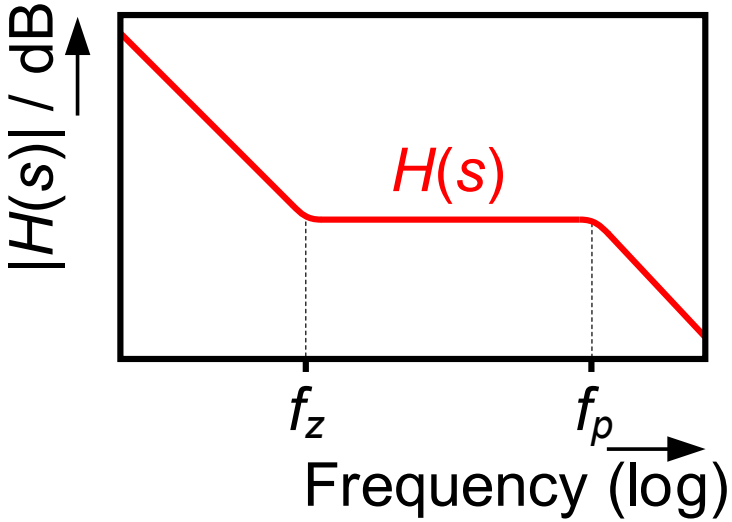
Modulator (plant) transfer function: $G(s) = \frac{D}{V_c} \frac{V_{out}}{D} = \frac{1}{V_{smax}} V_{in} \frac{1}{1 + \frac{sL}{R} + s^2 LC_{out}}$ → double pole

Frequency compensation through $H(s)$ by inserting zeros (and poles) → $Z_o(s)$

Frequency Compensation

Example: Type II compensation → $H(s)$ = two poles, one zero





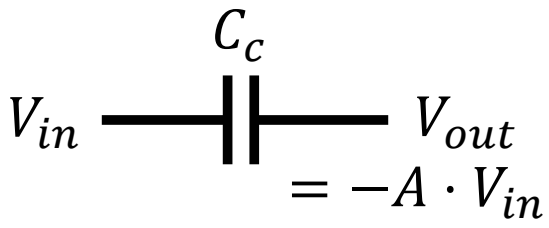
$$H(s) = \frac{V_c}{V_{out}} = -\frac{R_{fb2}}{R_{fb1}+R_{fb2}} \underbrace{\frac{g_m}{sC_1}}_{\text{Integrator (pole at } f=0)} \underbrace{\frac{\overbrace{(1+sR_1C_1)}^{\text{Zero } f_z}}{(1+sR_1C_2)}}_{\text{Pole } f_p}$$

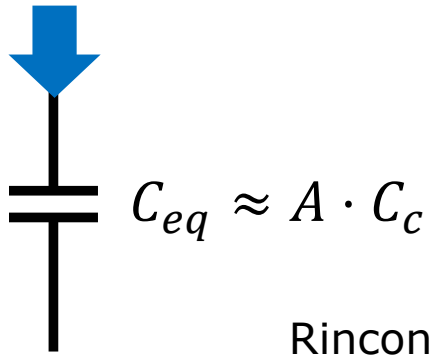
Example: f_z = 10kHz, f_p = 87kHz
→ R_1 = 4kΩ, C_1 = 3.9nF, C_2 = 457pF

→ On-chip integration by means of capacitance multiplier

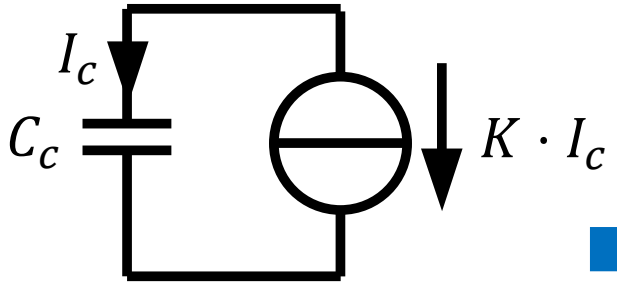
Cap Multiplier: Fully Integrated Compensation

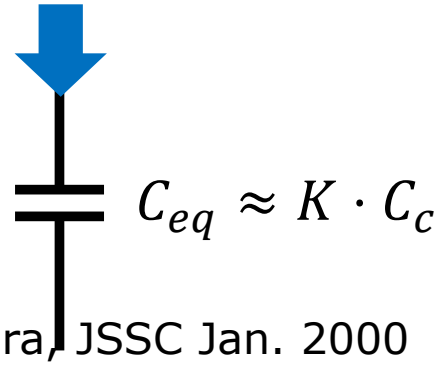
Voltage mode (Miller effect):





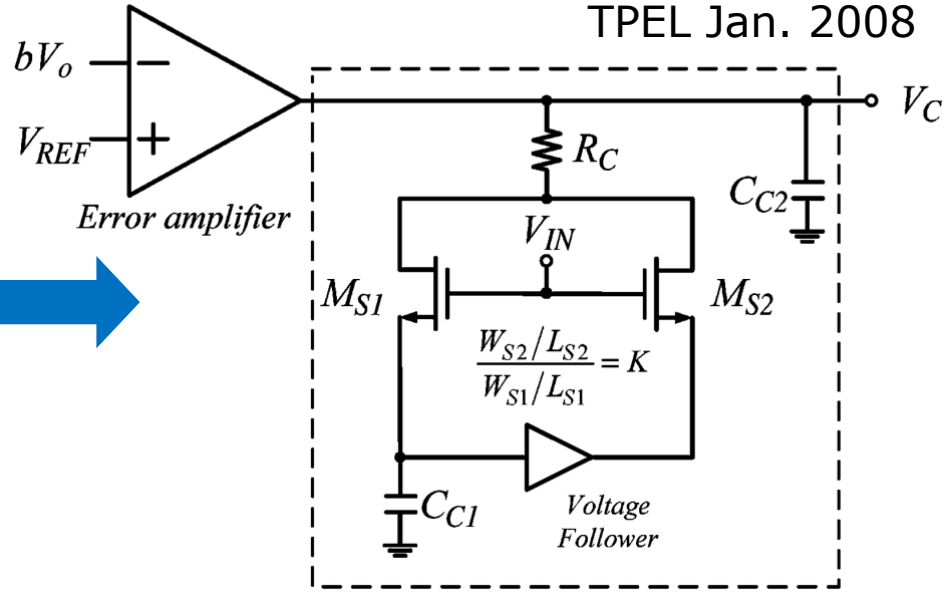
Current mode:





Rincon-Mora, JSSC Jan. 2000

K.-H. Chen, TPEL Jan. 2008

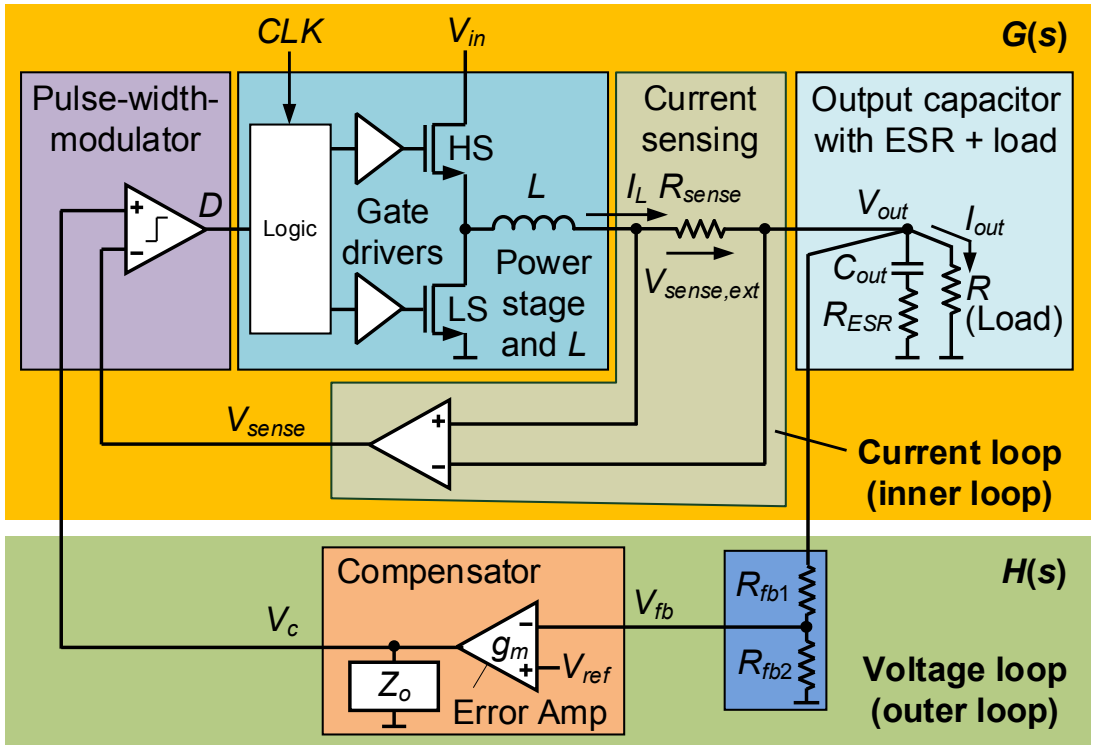


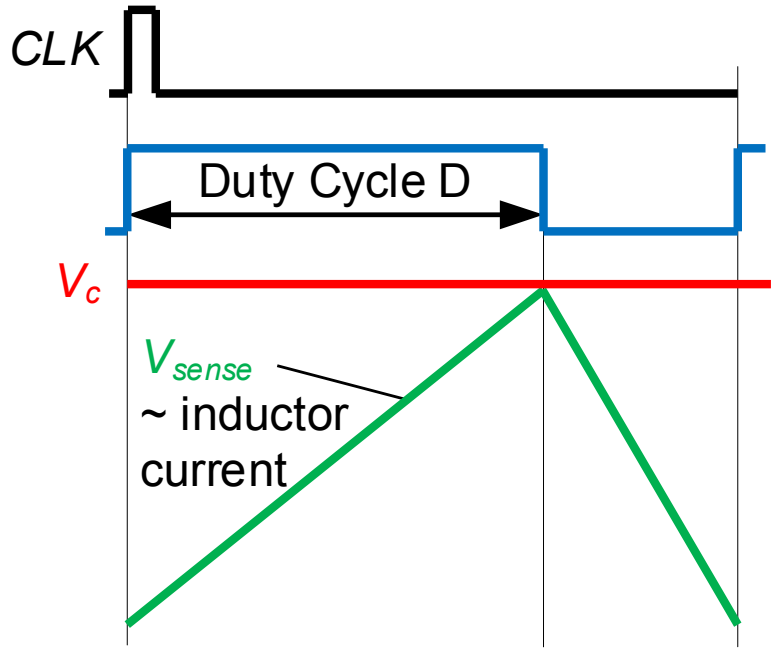
Type II example: R_{MS1} = 4kΩ, R_{MS2} = 80kΩ
C_{C1} = 200pF "equal" to 4nF → 20x smaller

- Area efficient on-chip implementation of large capacitors
- Additional advantage: Can be adaptive → adjust phase margin for fast transient response

Regulation Schemes: Current Mode Control

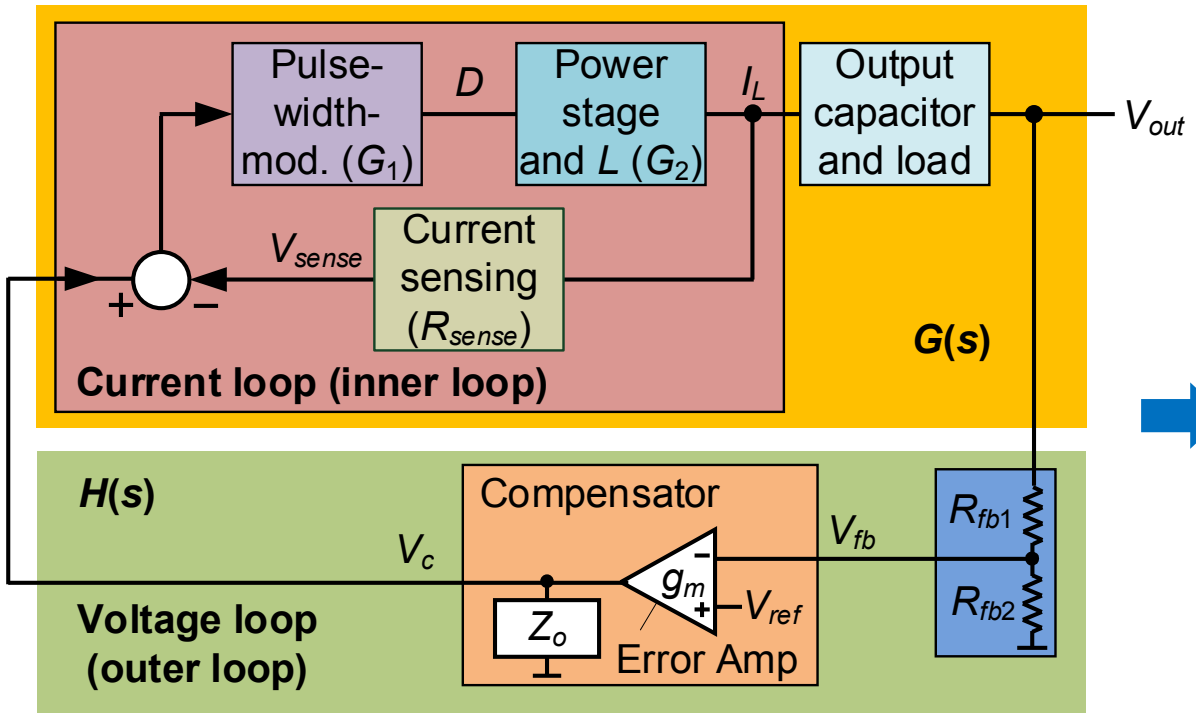
V_c is compared to a ramp voltage V_{sense} derived from the inductor current I_L, forming a second, inner control loop





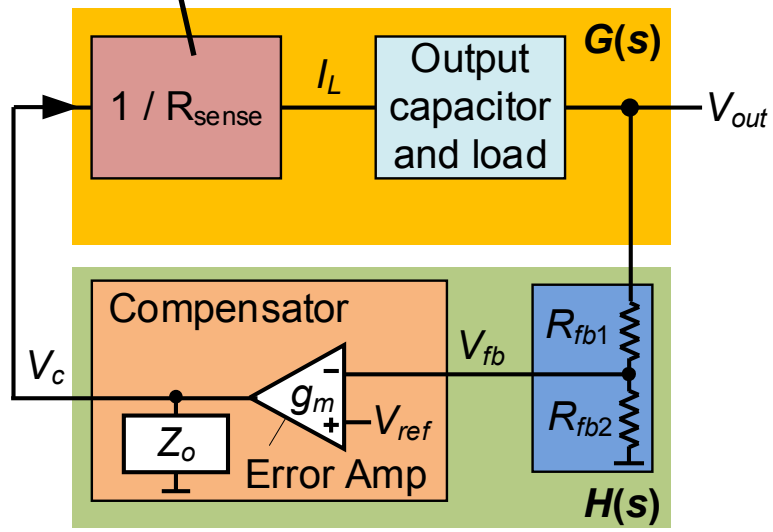
- Excellent line transient response → V_{out} independent of V_{in}
- Inherent I_L current limit (by limiting V_c)

Control Loop Analysis Current Mode Control



Current loop transfer function:

$$\frac{I_L}{V_c} = \frac{G_1 G_2}{1 + G_1 G_2 R_{sense}} \sim \frac{1}{R_{sense}}$$

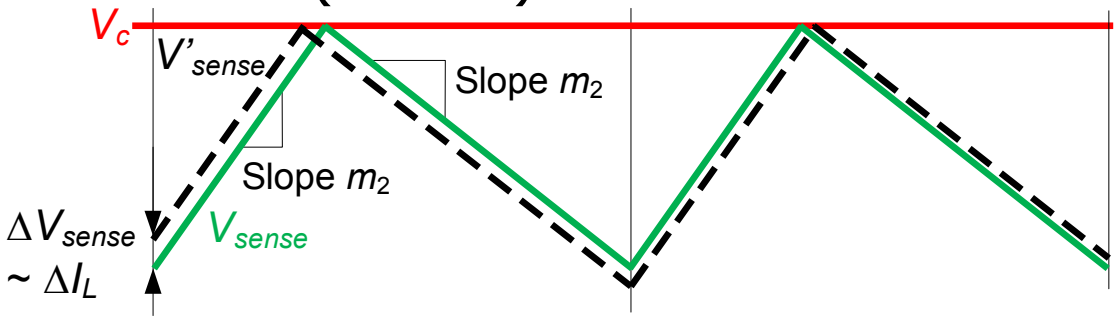


Modulator (plant) transfer function: $G(s) \sim \frac{1}{R_{sense}} \frac{1 + sR_{ESD}C_{out}}{1 + sRC_{out}}$ → 1st order system: much easier stabilization

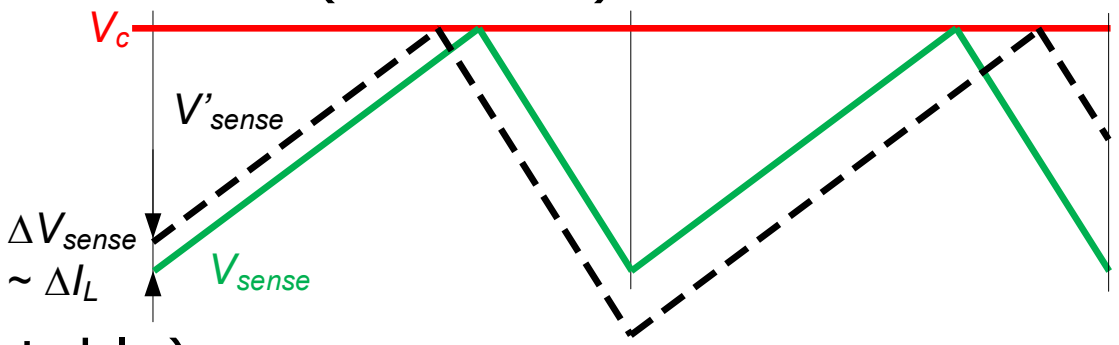
Current Mode: Subharmonic Oscillations

Unconditional instability above 50% duty cycle (step-down)
→ perturbation ΔI_L of inductor current leads to subharmonic oscillations at $f_{sw}/2$

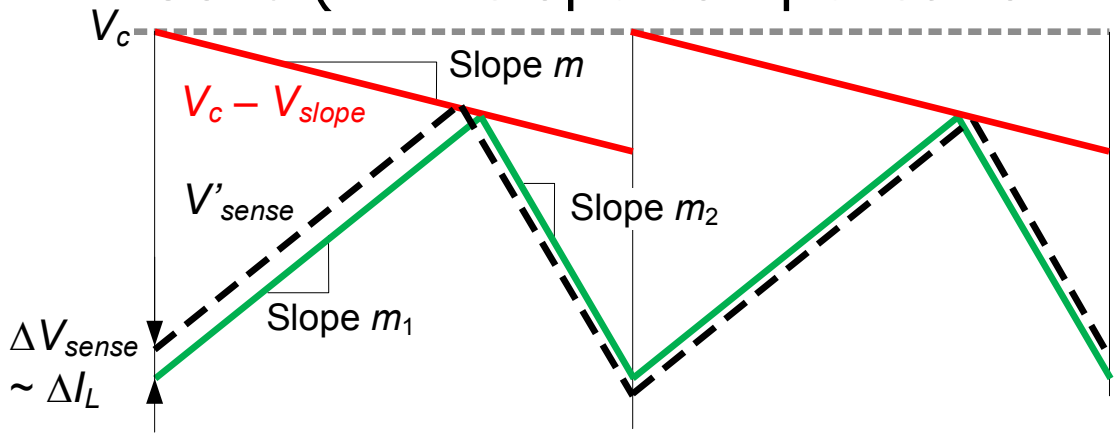
D < 50% (stable)



D > 50% (unstable)



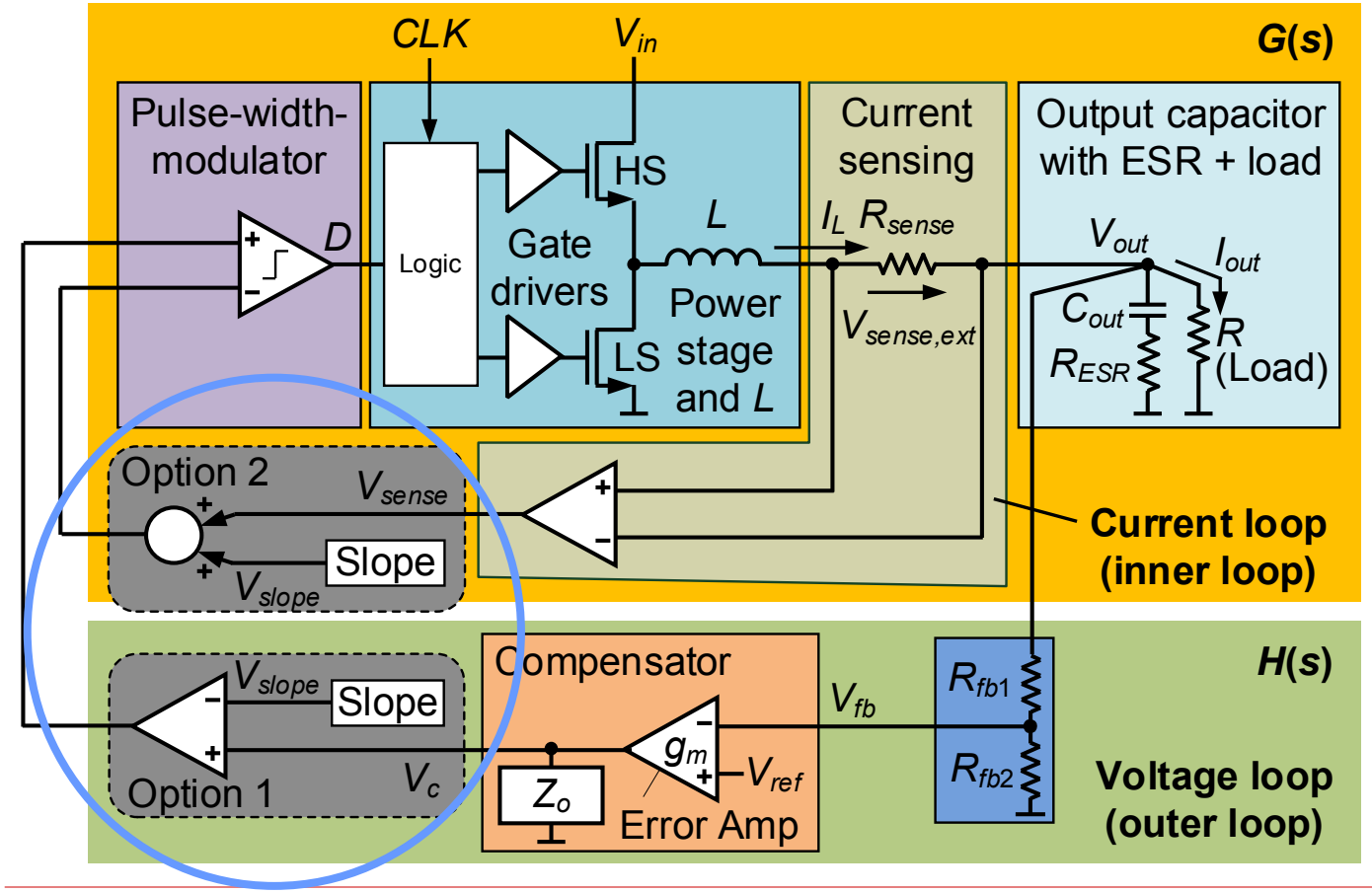
D > 50% (with slope compensation → stable)

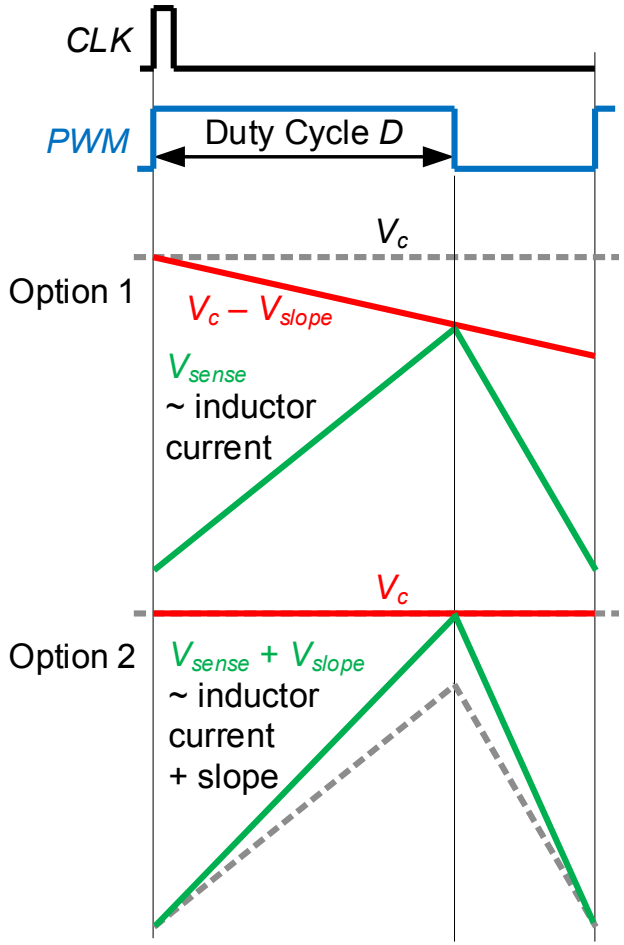


→ stable if $m > \frac{m_2}{2}$

Current Mode Control with Slope Compensation

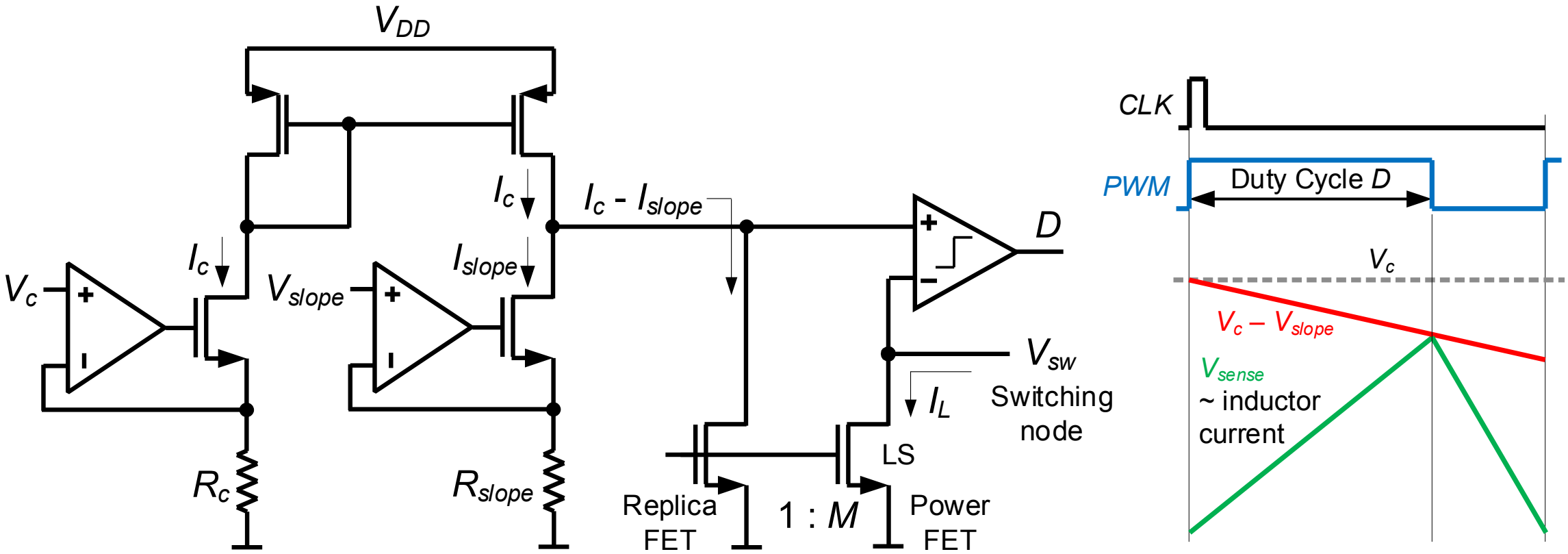
(V_c-V_{slope}) gets compared to a ramp voltage V_{sense} derived from the inductor current → two implementation options





Slope Compensation: Circuit Design (1)

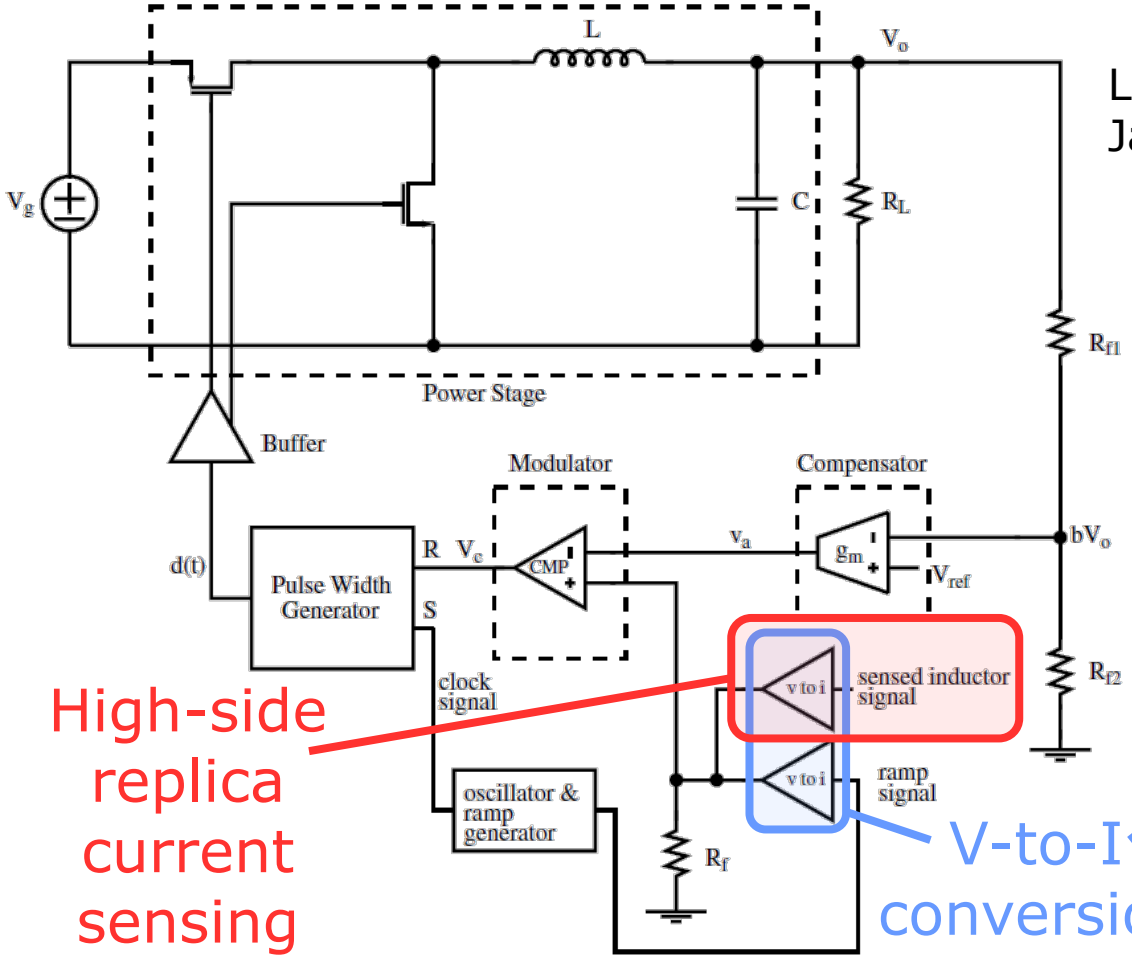
Option 1: Difference (V_c – V_{slope}) is generated in the current domain, fed into replica FET and compared to voltage across power FET = V_{sense} = V_{sw} = R_{DSon}·I_L



Concept can also be implemented on high-side FET (more complex)

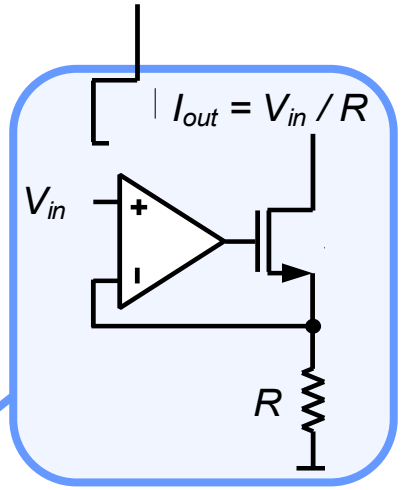
Slope Compensation: Circuit Design (2)

Example for Option 2 with replica current sensing and slope compensation

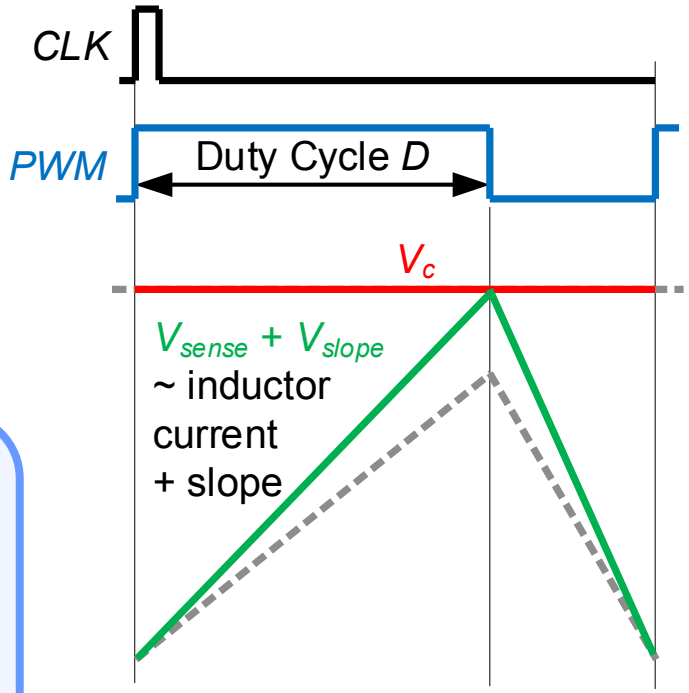


Lee, JSSC
Jan. 2004

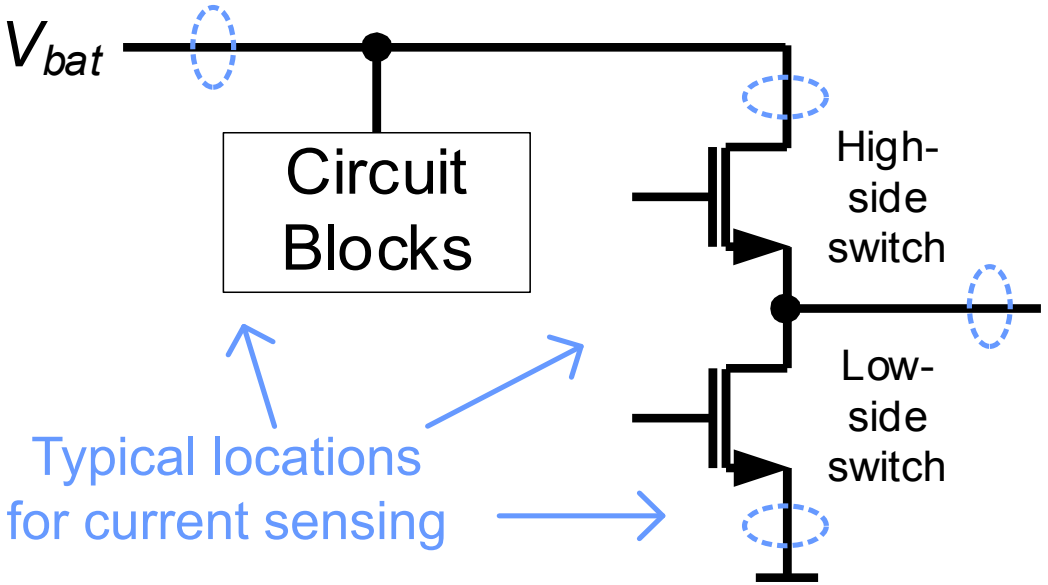
High-side replica current sensing

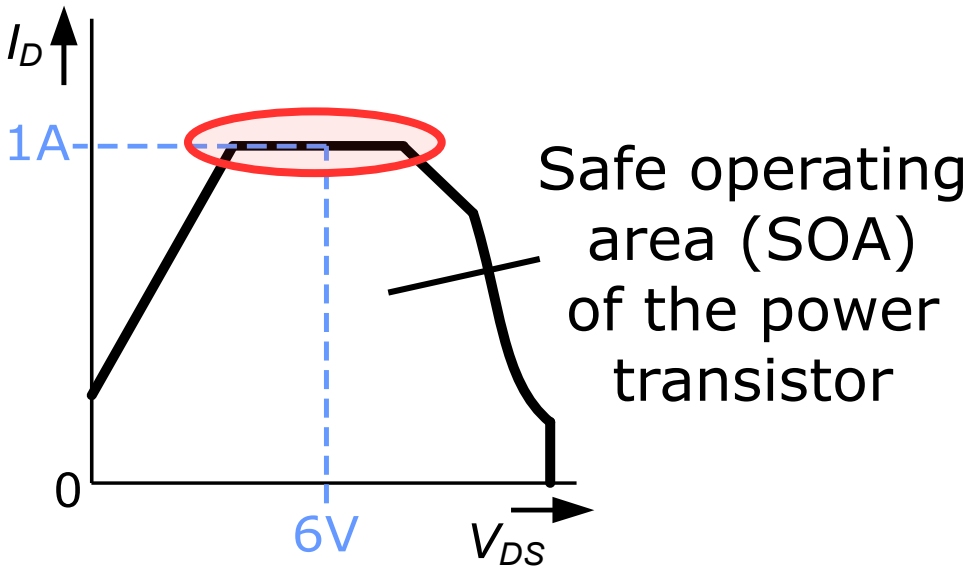


V-to-I conversion



Current Sensing

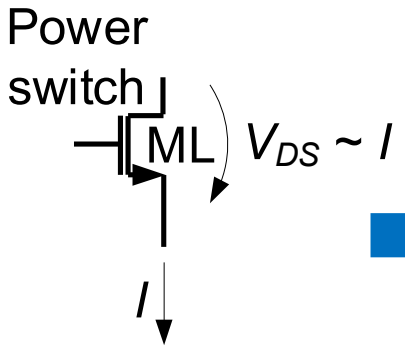




- Open loop:
  - Over-current detection → turn-off power FET
  - Continuous current measurement
- Closed loop:
  - Current limit
  - Current controlled DC-DC conversion

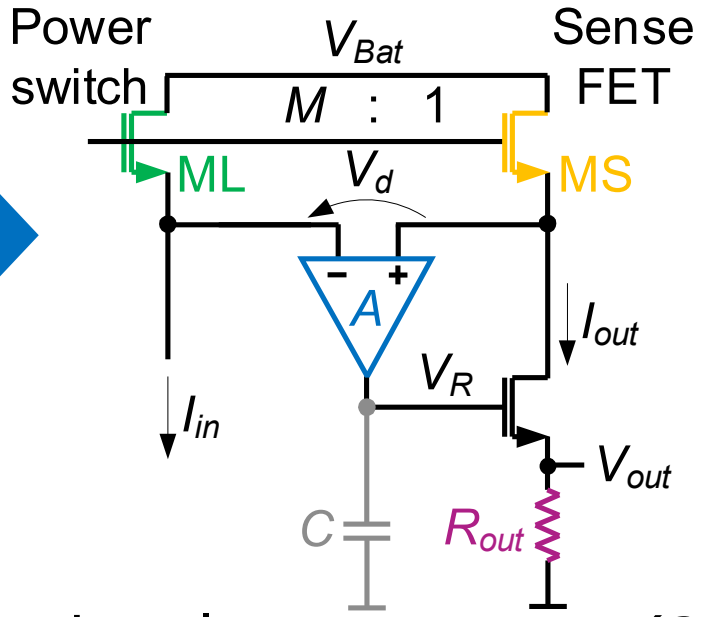
Current Sensing Concepts and Circuits (1)

R_{DS} Sensing

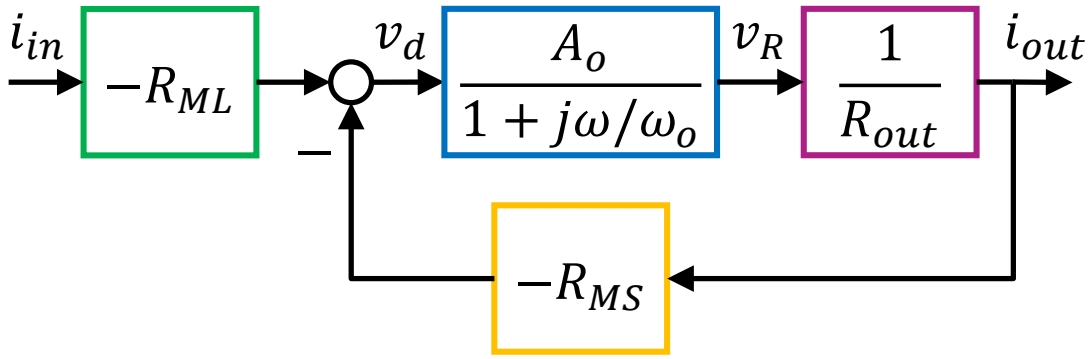


+ Lossless
– Accuracy

Replica Sensing: Sense FET + Sense Amplifier



+ Lossless
+ Good accuracy
– Complexity



$$i_{out} = v_d A / R_{out} \quad (1)$$

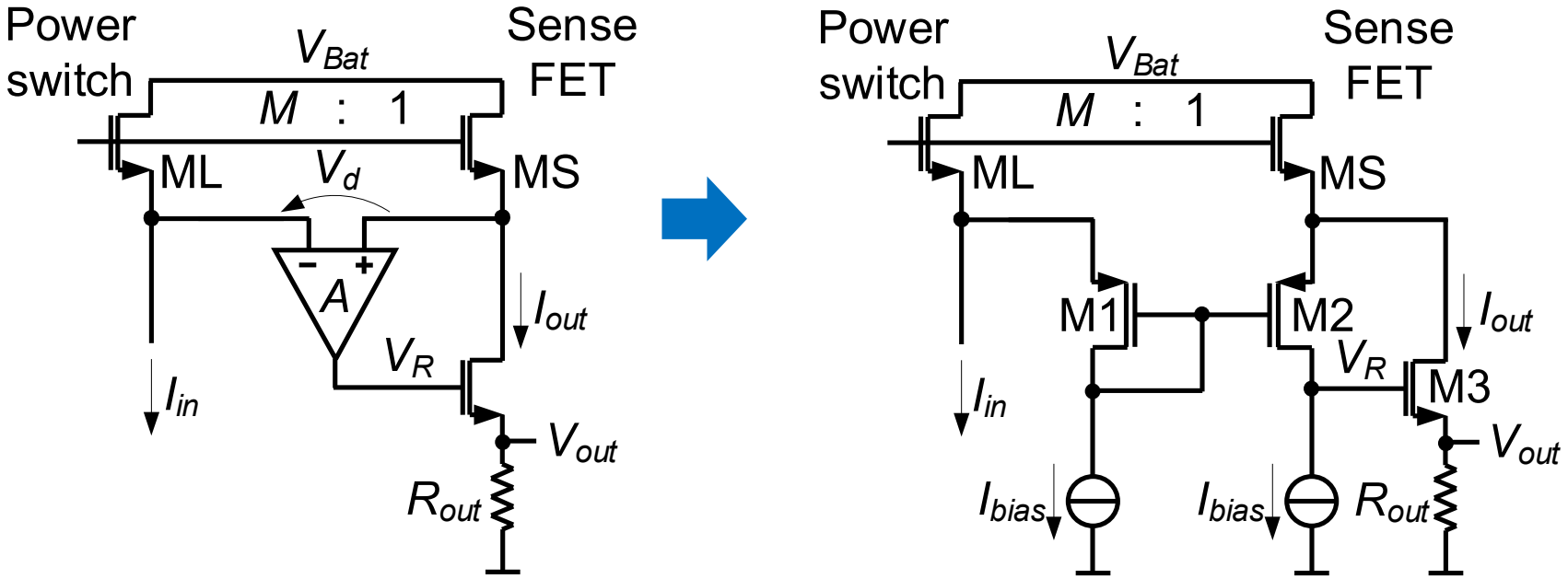
$$v_d = -i_{in} R_{ML} + i_{out} R_{MS} \quad (2)$$

$$(2) \rightarrow (1): \frac{i_{out}}{i_{in}} = \frac{A R_{ML}/R_{out}}{1 + A R_{MS}/R_{out}} \approx \frac{R_{ML}}{R_{MS}} = \frac{1}{M}$$

Loop Gain: $GBW = \underbrace{A_o \omega_o}_{GBW(A)} R_{MS}/R_{out}$ (slow!)

Current Sensing Concepts and Circuits (2)

Sense FET + Sense Amplifier: Practical implementation

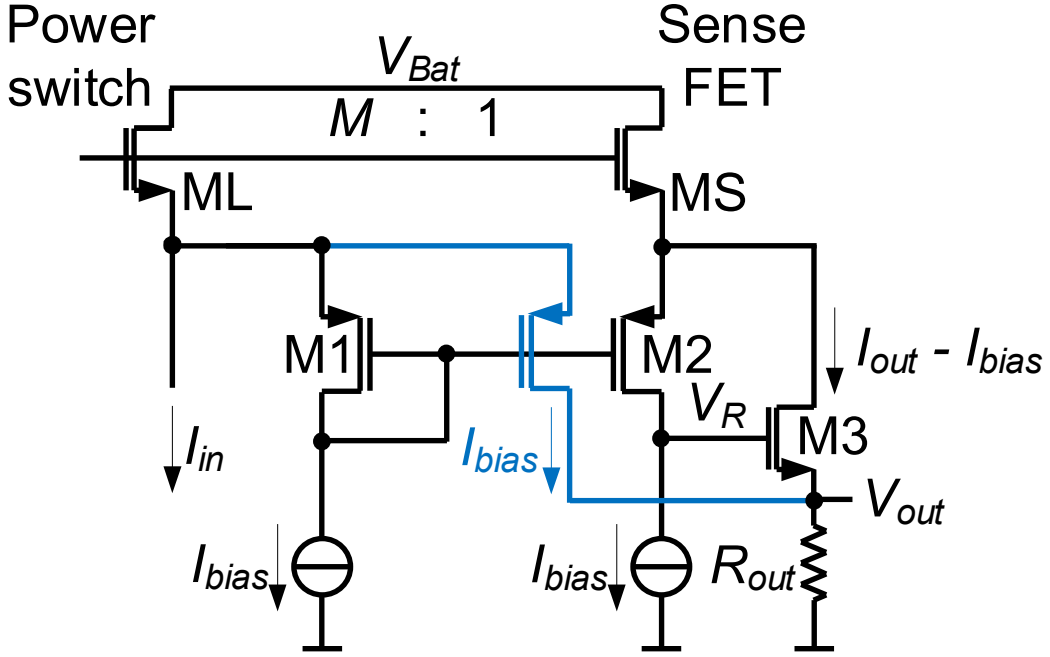


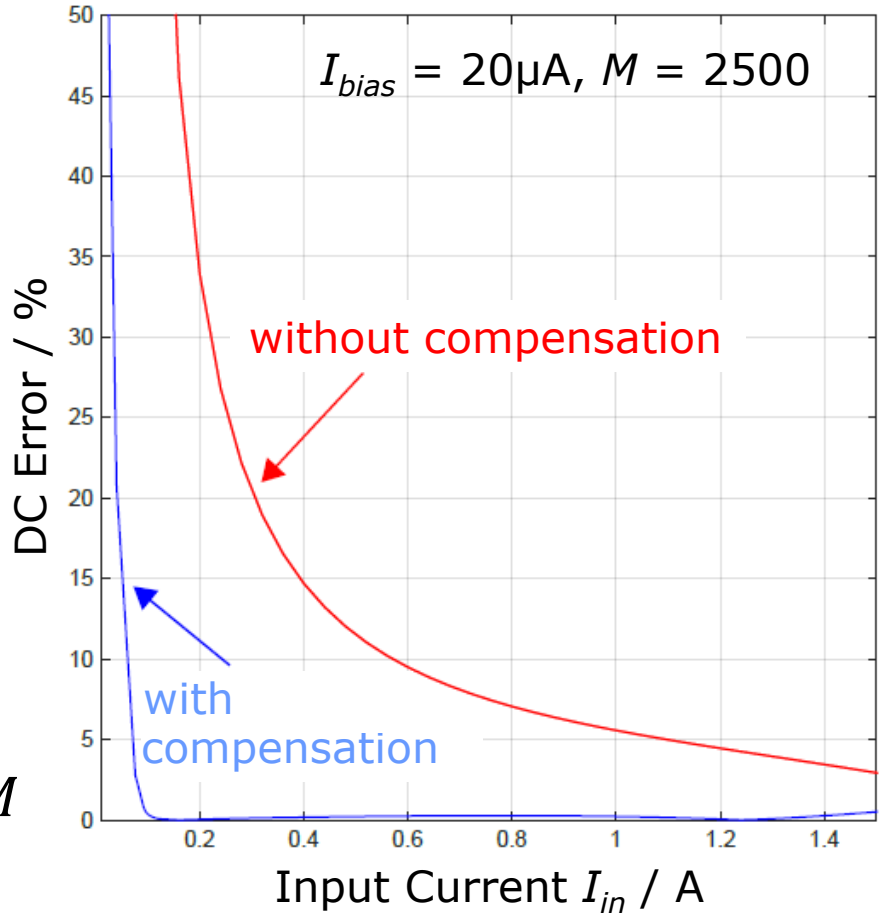
- Accuracy: Mismatch (M, amp offset), variation of R_{out} (trimming), loop gain
- Lower input current limited: $I_{in} \geq MI_{bias}$
- Finite I_{bias} causes a DC error:

$$R_{ML}(I_{in} + I_{bias}) = R_{MS}(I_{out} + I_{bias}) \rightarrow I_{in} = M(I_{out} + I_{bias}) \approx MI_{out} \text{ for } I_{bias} \ll I_{out}$$

Current Sensing Concepts and Circuits (3)

Sense FET + Sense Amplifier: I_{bias} compensation





- With I_{bias} compensation:

  $R_{ML}I_{in} = R_{MS}(I_{out} - I_{bias} + I_{bias}) \rightarrow I_{out} = I_{in}/M$

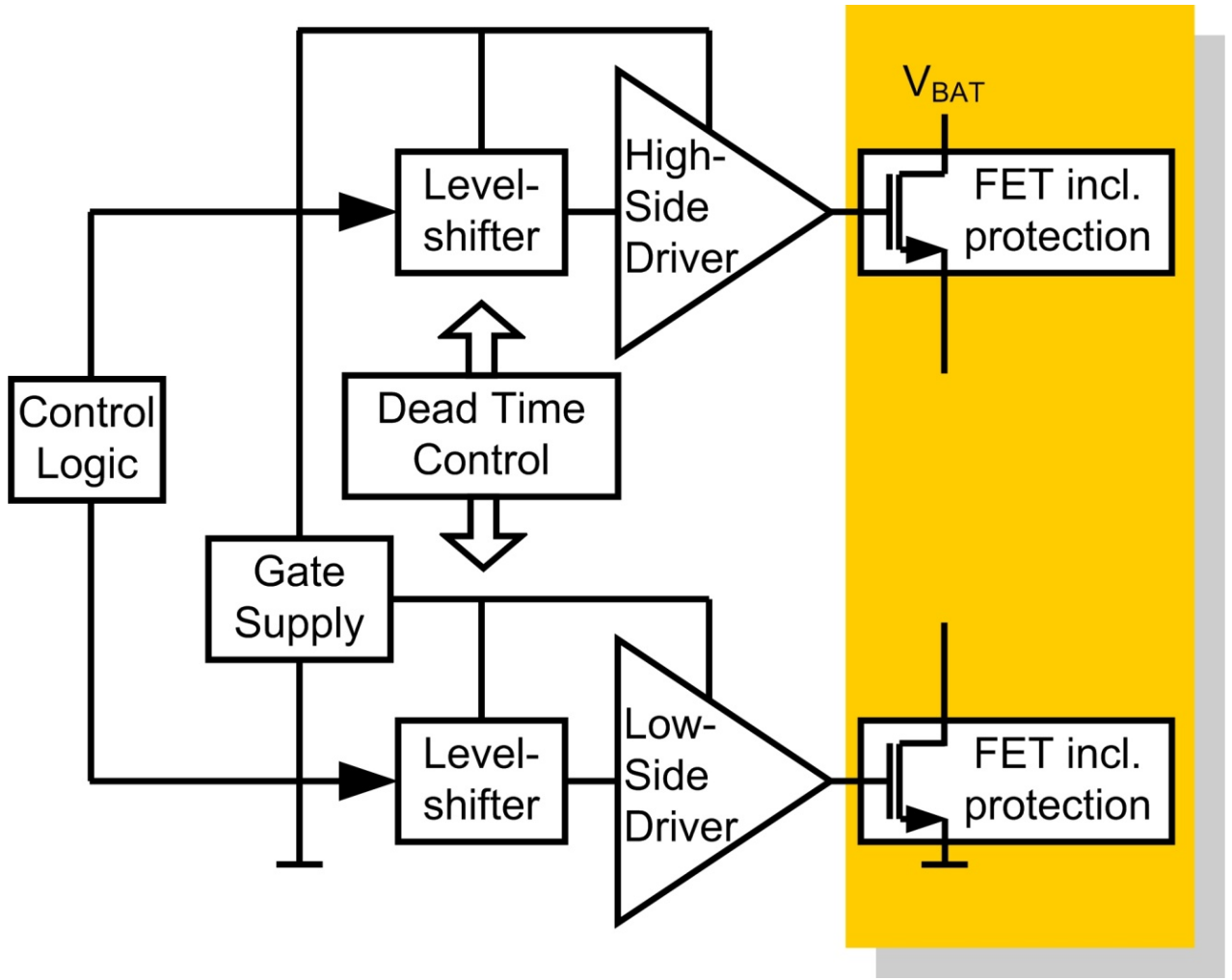
- Input current limit remains: $I_{in} \geq MI_{bias}$

Outline

- Introduction
- Power Transistors
- Gate Drivers
- Level Shifters
- Control Loop
- System Design

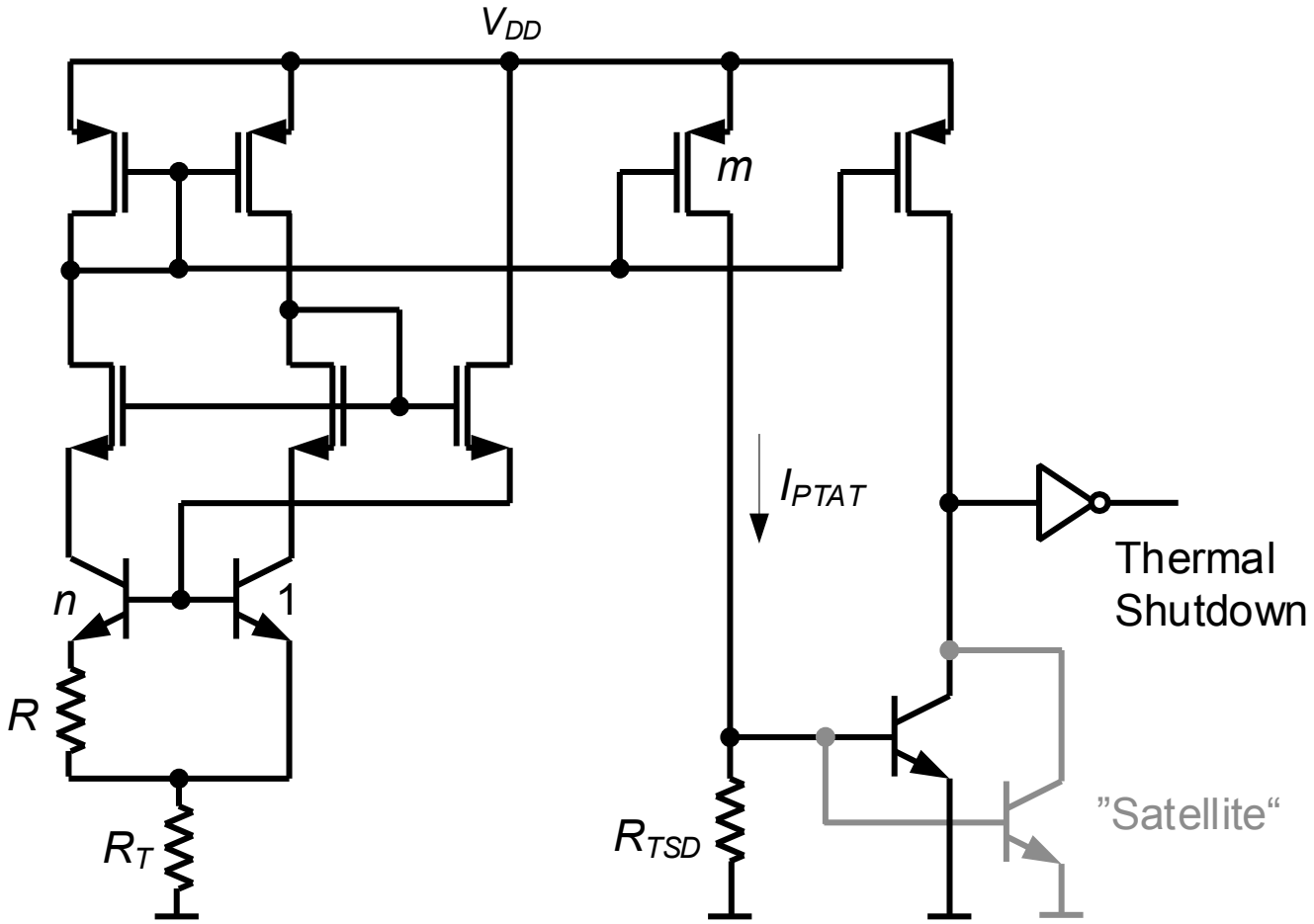
Protection and Diagnostics

- Thermal protection
- Over-voltage (VDS)
- Over-current
- Short-to-ground
- Short-to-battery
- Open load
- Under-voltage (UVLO)



Thermal Protection

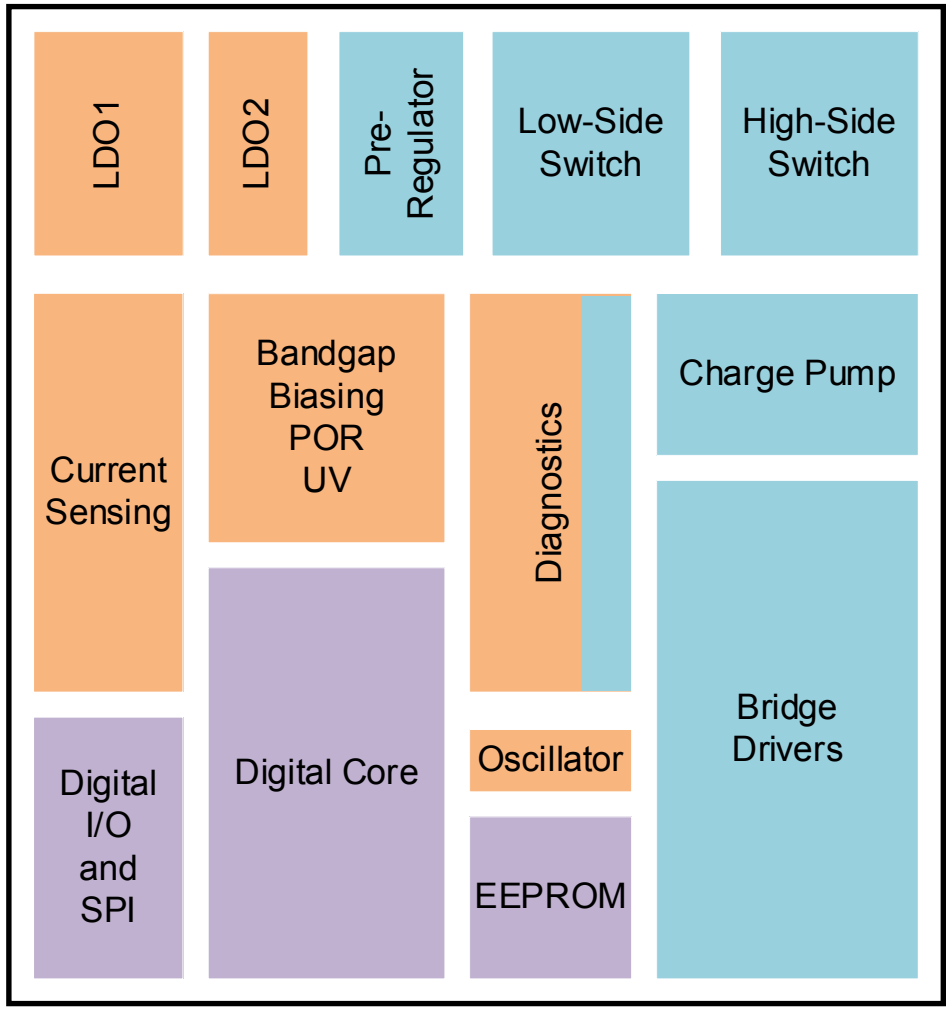
Protects the IC from damage at high temperature



Usually installed as a secondary protection: Indirect limitation of load current in regulators, drivers

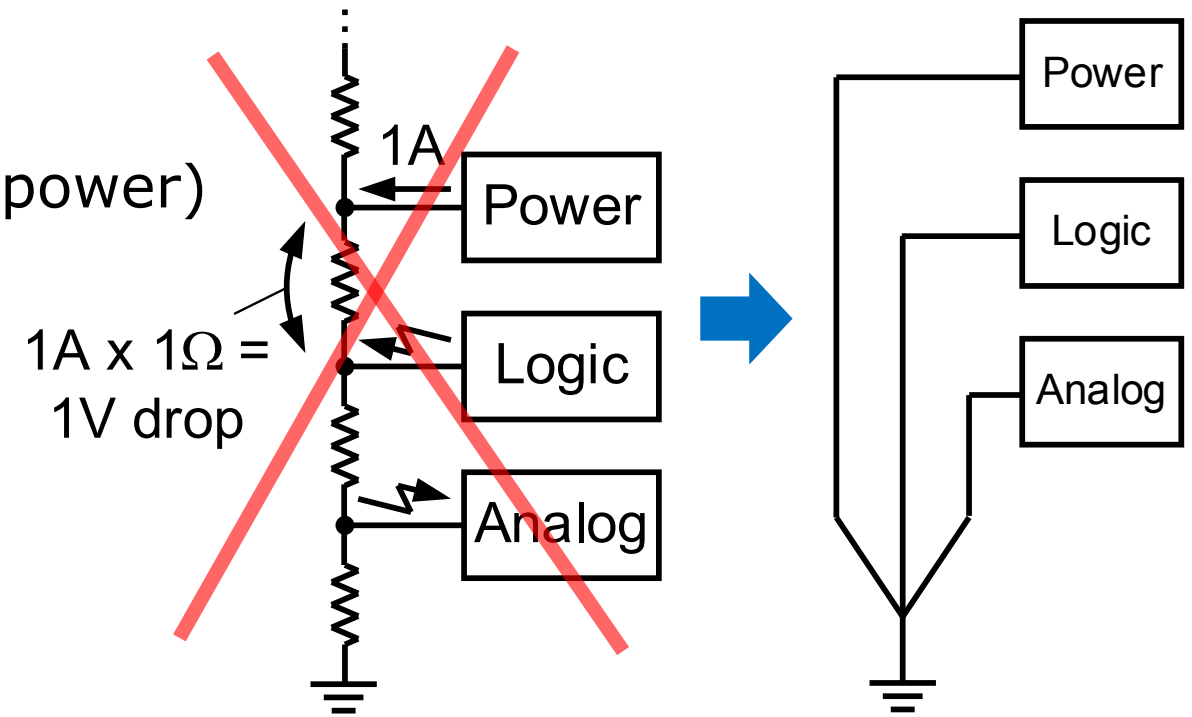
Floorplan

- Rule: Separate high-voltage and low-voltage domains
- Reason: HV-Isolation = Spacing = Chip Area = Cost
- IC level copper metallization
- Thermal analysis
- Mechanical stress: avoid corners / edges for sensitive blocks (bandgap)

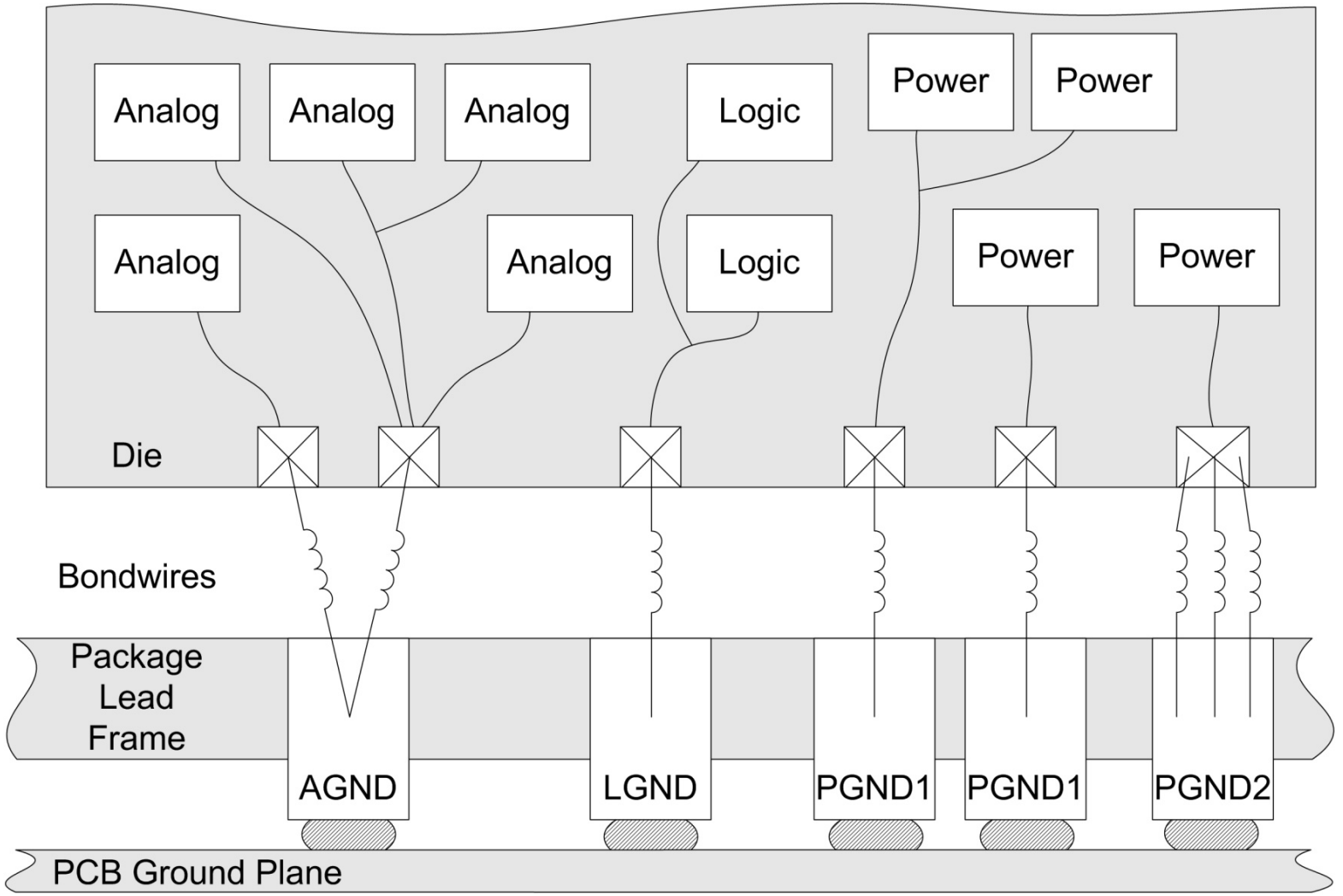


Pinout, Grounding and Supply Guidelines

- Supply and ground pins adjacent, bypass-C placed here close to pins
- Short bond wires for power pins and fast signals (R↓, L↓) → close to the middle of one side of the die, vice versa: corner pins for quite signals
- Use separate bond pads for each domain or at least apply star connections, consider double / tripple-bond
- IC-Level wiring in groups:
  - Noisy lines (digital, switching power)
  - Supply lines (high current)
  - Sensitive lines (analog)



Pinout, Grounding and Supply Guidelines



Conclusion


12/48V

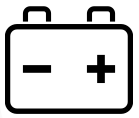

24/36V

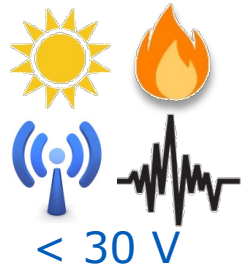

3-15V


12/24/48V


20-75V


5-20V


1-3V

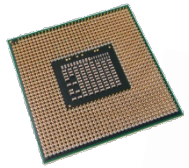

< 30 V


2.5-4.4V

DC-DC Conversion

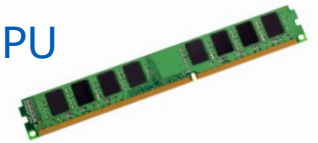
- Power Transistors
- Gate Drivers
- Level Shifters
- Control Loop
- System Design

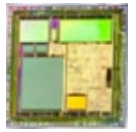

ECUs



Sensors

µC,CPU


RAM,HD,SSD



ICs

Photos: Shutterstock.com

Papers to See This Year

Session 11 “DC-DC Converters” Relevant Papers:

- 11.2: Resonant SC converter with on-chip L-C, level shifter, switch stacking
- 11.3: One-Step 325V-to-3.3–10V DC-DC, bootstrap gate supply
- 11.4: 48 – 80V input 2MHz GaN DC-DC, current sensing (DCR)
- 11.7: Buck-boost DC-DC, 2.5-5V input, adaptive dead time

Session 18 “GaN & Isolated Power Conversion” Relevant Papers:

- 18.2: 400V Offline monolithic GaN IC with control loop
- 18.6: 60A, 48V-to-1V DC-DC, dynamic level shifter

Session 32 “Power Management Techniques” Relevant Papers:

- 32.2: Piezoelectric Energy Harvesting IC

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