Fundamentals of Switched-Mode Power Converter Design

Hoi Lee
Professor
Department of Electrical and Computer Engineering
The University of Texas at Dallas
hoilee@utdallas.edu

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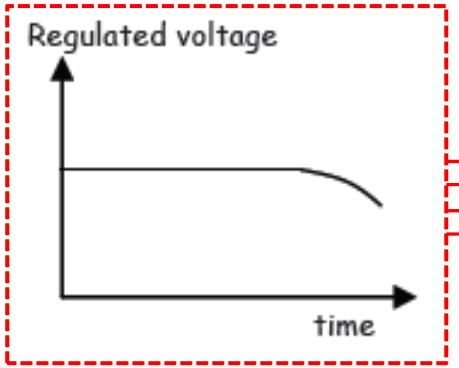
Why DC-DC Converters?

Battery-Operated Portable Electronic Gadgets

Energy Source (Li-Ion: 2.7V – 4.2V)

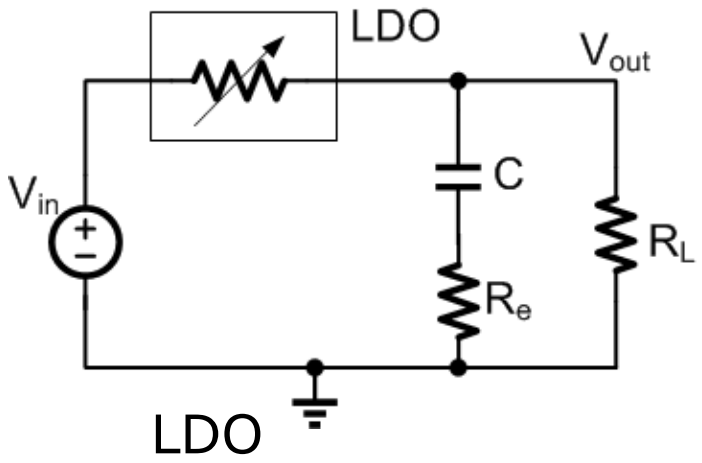


DC-DC Converters ($\eta \rightarrow 1$)

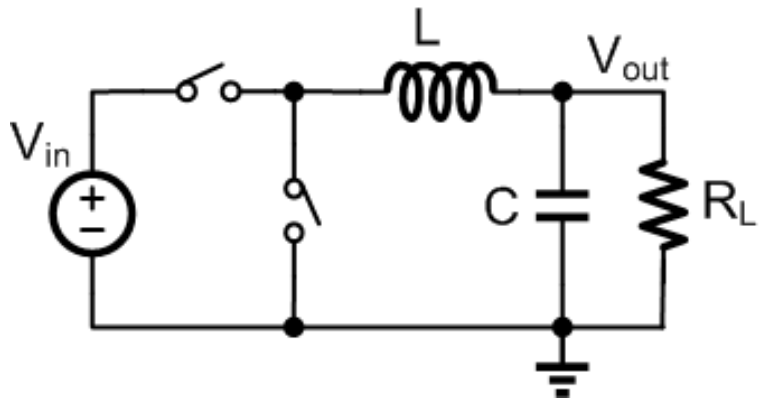
Analog Part (e.g. V_{DD}: 1.8V)	**Digital Part** (e.g. V_{DD}: 0.9V)	**RF Part** (e.g. PA V_{DD}: 5V)	**Interface Part** (e.g. V_{DD}: 1.2V)

- Battery voltage is time-varying.
- DC-DC converters are part of power management to provide regulated voltages.

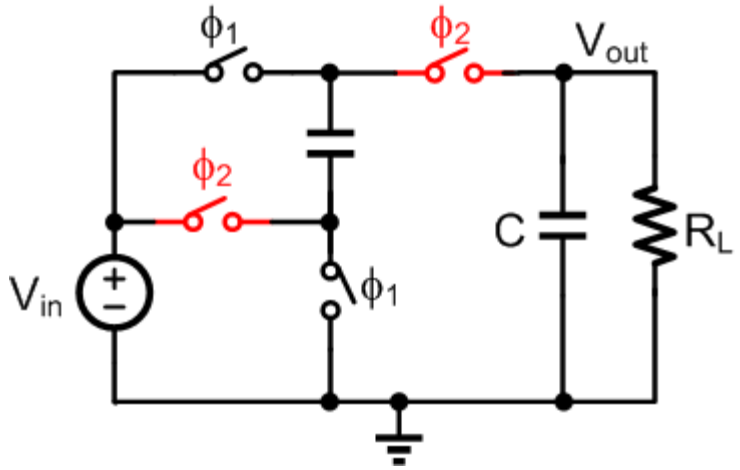
Types of DC-DC Converters



LDO



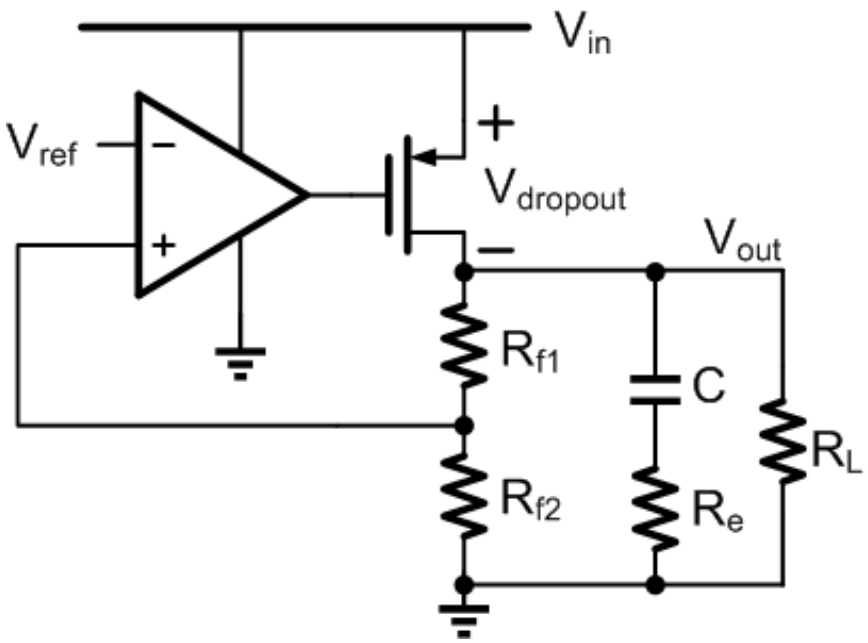
SMPC: Buck Converter

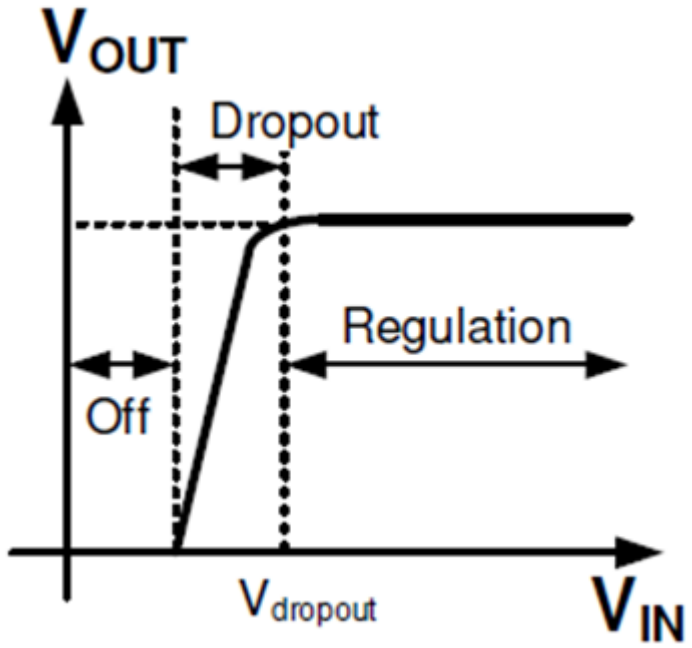


SCPC: Doubler

- **Low Dropout Regulator (LDO)**
  - Continuous-time system with a single power transistor
- **Switched-Mode Power Converter (SMPC)**
  - Sampled-data system using inductor for energy storage
- **Switched-Capacitor Power Converter (SCPC)**
  - Sampled-data system using capacitor for energy storage

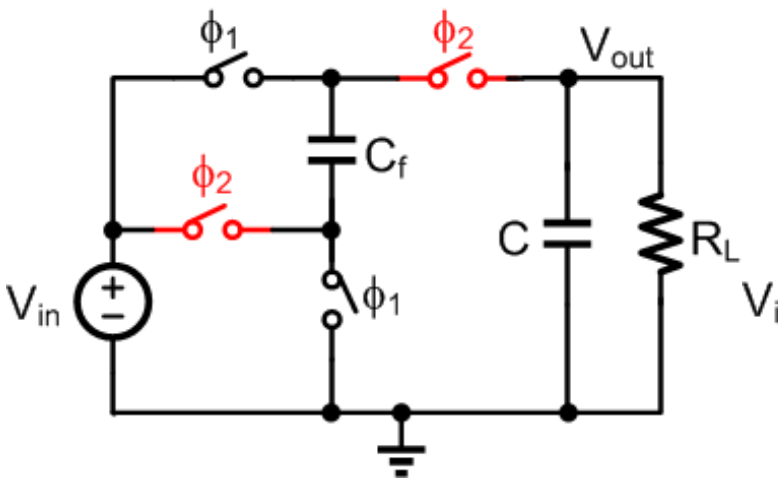
Low Dropout Regulator



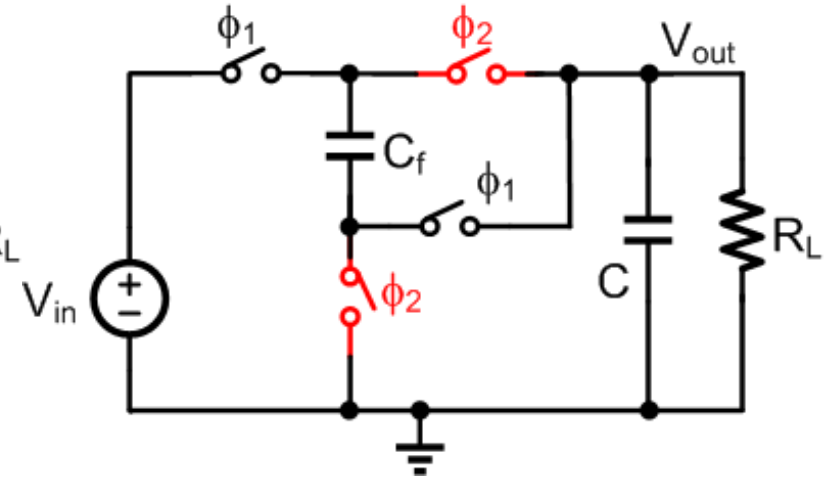


- Based on the LDO structure, V_{out} is always smaller than V_{in}.
- As input current ≈ load current, η approximately equals V_{out}/V_{in} $(=1-(V_{dropout}/V_{in}))$.
- In practice, Power pMOS can reduce $V_{dropout}$ to about 0.1V – 0.2V and is more commonly used than nMOS counterpart for maximizing η.
- Power FET does not switch during operation, so V_{out} is low noise.

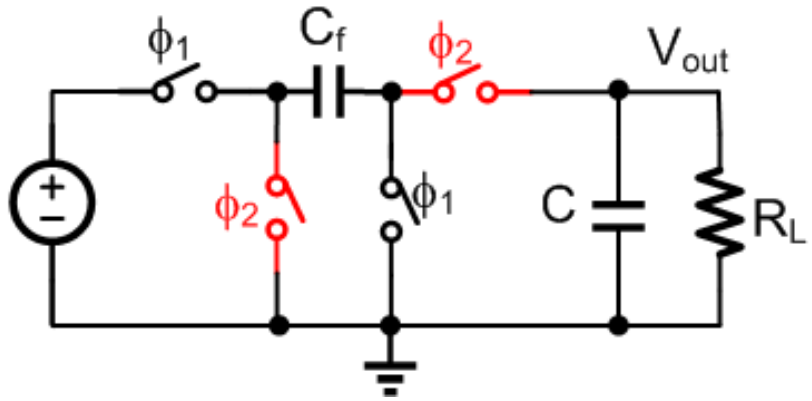
Switched-Capacitor Power Converters (1)



$V_{out} = 2V_{in}$



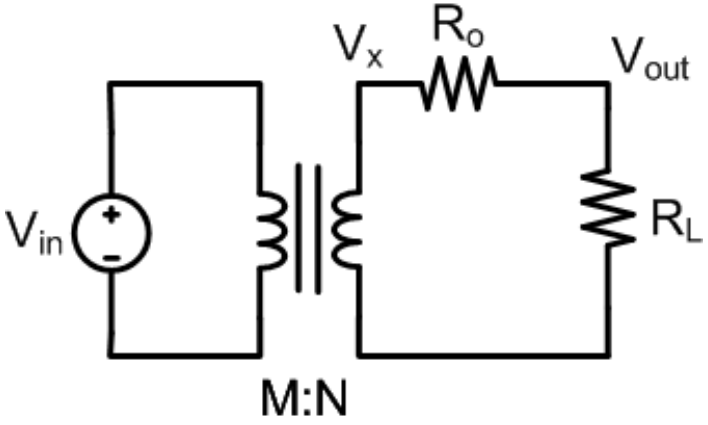
$V_{out} = 0.5V_{in}$



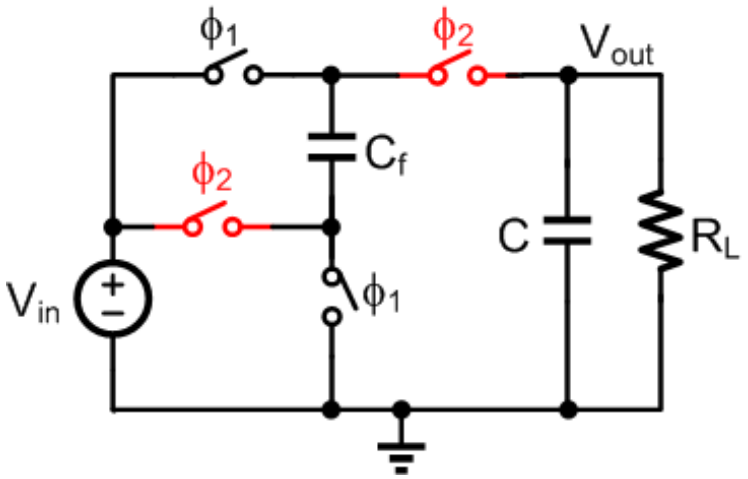
$V_{out} = -V_{in}$

- By changing connections of switches and capacitors, different conversion ratios between V_{in} and V_{out} (step-up, step-down or inverting) can be realized.
- Flying capacitor C_f is used for temporary energy storage.
- V_{out} relates to V_{in} with a fixed conversion ratio via two complimentary clock phases ϕ_1 and ϕ_2.

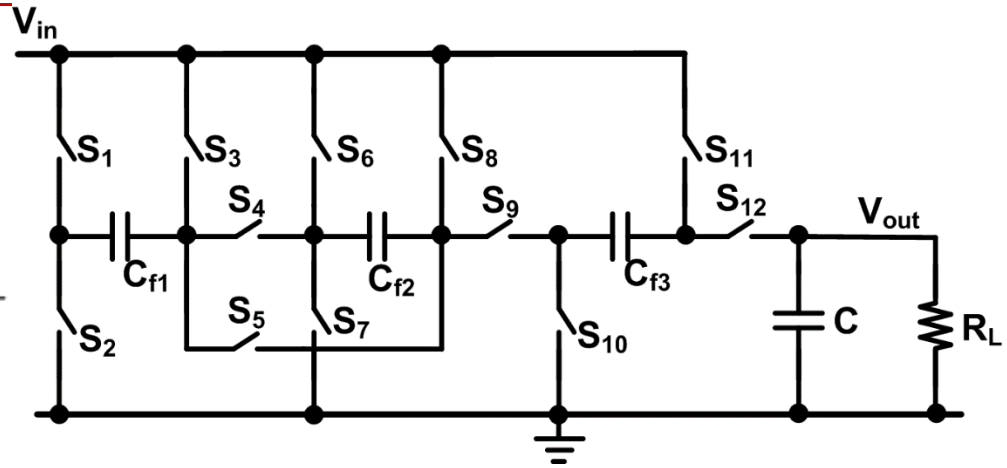
Switched-Capacitor Power Converters (2)



Model of SCPC



$V_{out} = 2V_{in}$

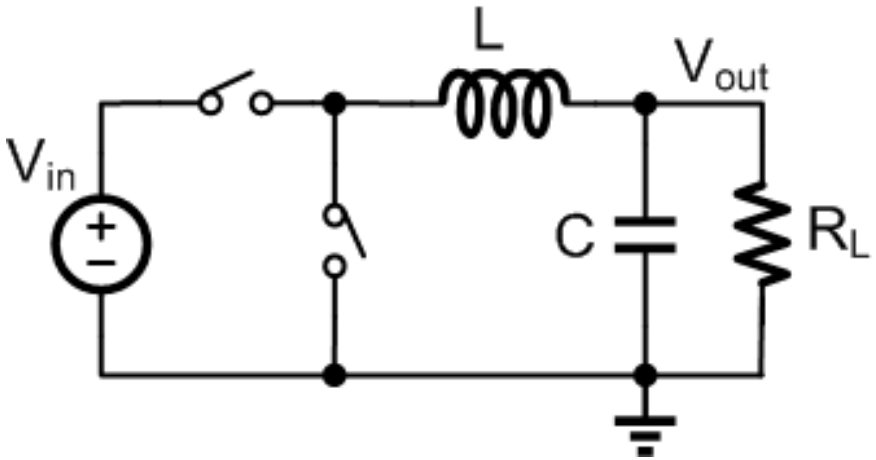


$V_{out} = 2/2.5/3/4V_{in}$

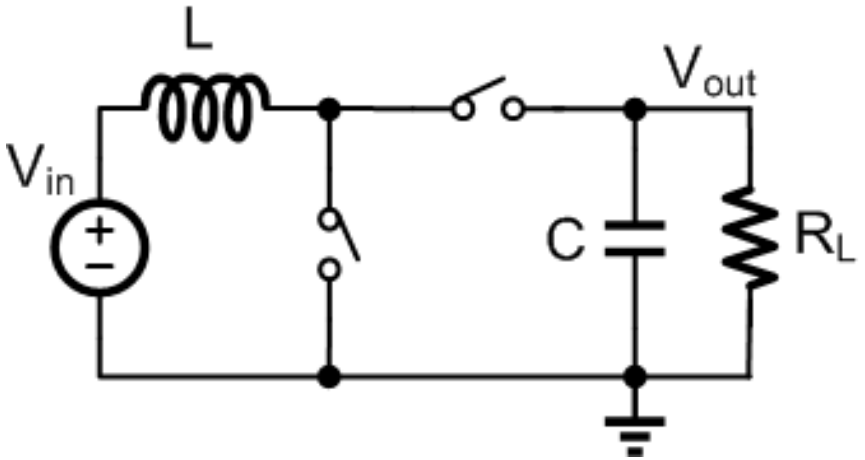
H. Lee et. al., TVLSI, Apr. 2015, pp. 712-722.

- $V_{out}=(N/M)\cdot R_L/(R_L+R_O)\cdot V_{in}$, so V_{out} can be regulated by adjusting output resistance R_O of the power stage; where N/M is the conversion ratio.
- Ideal $\eta=(V_{out}\cdot I_{out})/V_{in}\cdot I_{in}=(V_{out}/V_x)\cdot(V_x/V_{in})\cdot(I_{out}/I_{in})=V_{out}/V_x$ (i.e. η of LDO).
- Lossless V_{out} regulation is to change N/M when V_{in} varies.
- Numbers of flying capacitors and switches however grow rapidly when the resolution of input-output conversion ratio increases.

Switched-Mode Power Converters



Buck Converter



Boost Converter

- With different configurations of L and two switches, two most common topologies: buck (step-down) and boost (step-up) in portable applications are illustrated.
- The converter operates in two complementary phases with an inductor for temporary energy storage.
- The converter provides continuous conversion ratio between V_{in} and V_{out}.

Characteristics of DC-DC Converters

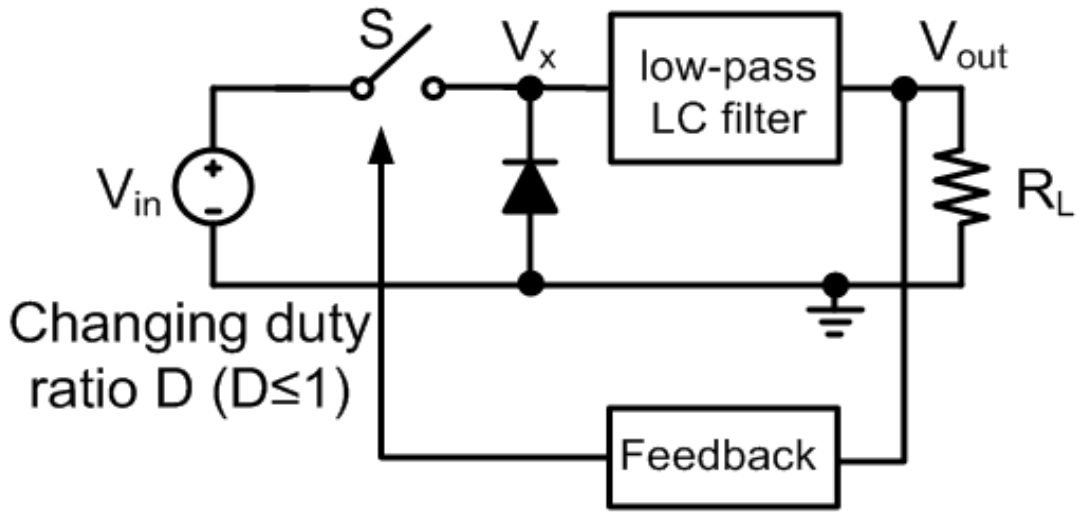
	Types	Pros	Cons
Inductor-less	LDO	▪ Simplest and lowest cost ▪ Low output noise	▪ No step-up conversion ▪ Poor efficiency if the voltage mismatch between input and output is large
	SCPC	▪ Step up / down conversion ▪ Low cost ▪ High energy density	▪ High switch count ▪ Tradeoff between power efficiency and power density
Inductor-based	SMPC	▪ Highest power efficiency ▪ Step up / down conversion	▪ Relatively high cost

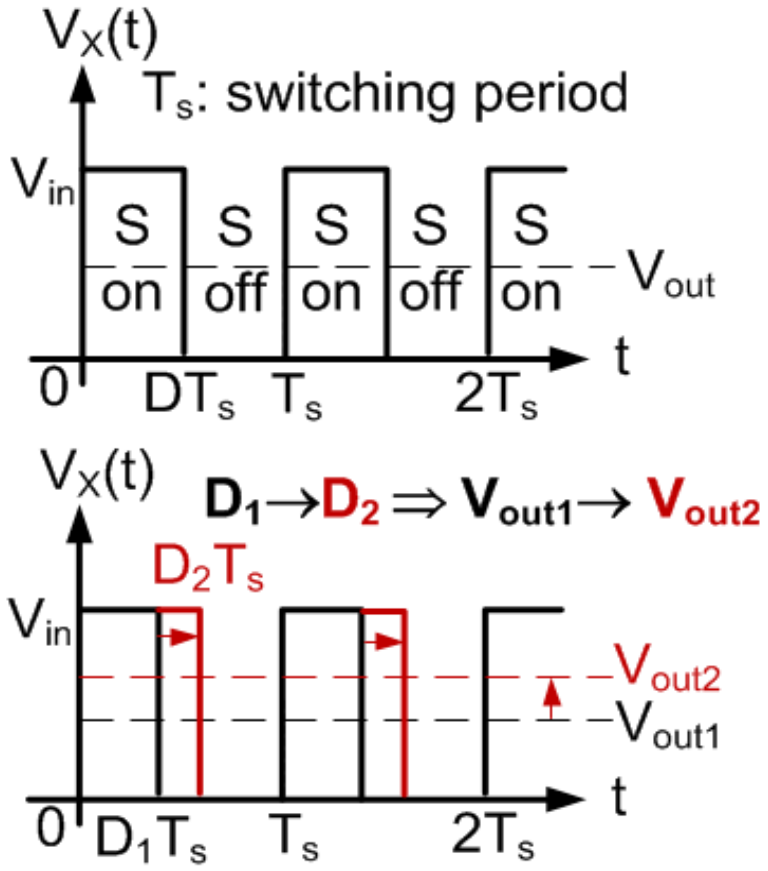
Outline

- SMPC Basics and Design Considerations
- Control Methodologies and Design Issues
  - Voltage-mode PWM and compensator design
  - Current-mode PWM and compensator design
  - Current sensor designs
  - Gate driver designs
  - Hysteretic control
- Advanced Topic
  - Three-Level DC-DC Converter

SMPC Basic

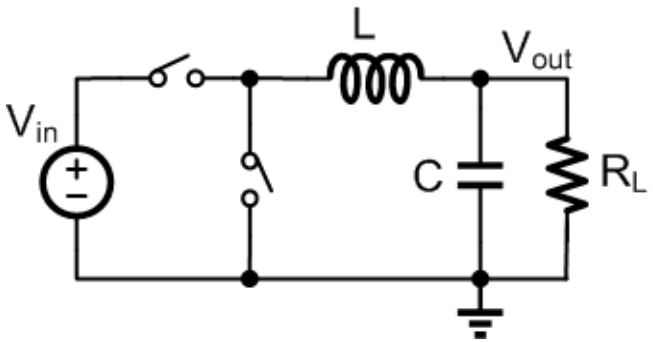
Buck Converter: $V_{out}<V_{in}$



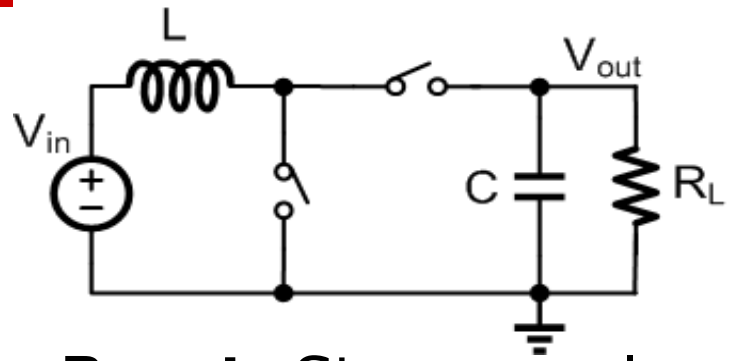


- V_{out} is a function of duty ratio D ($0 \le D \le 1$) and V_{in}.
- Power efficiency (η) = 100% (ideal) with a lossless switch, diode and LC filter.

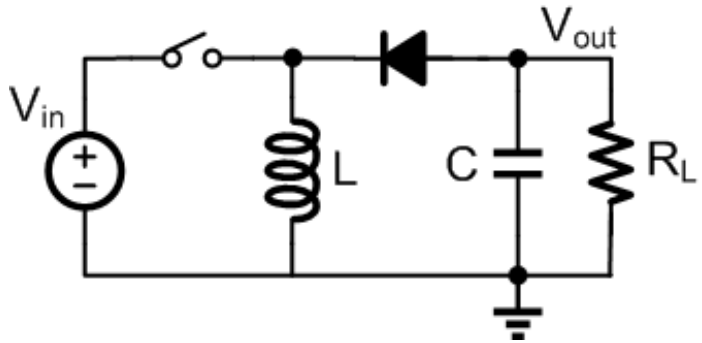
DC-DC Topologies of SMPC



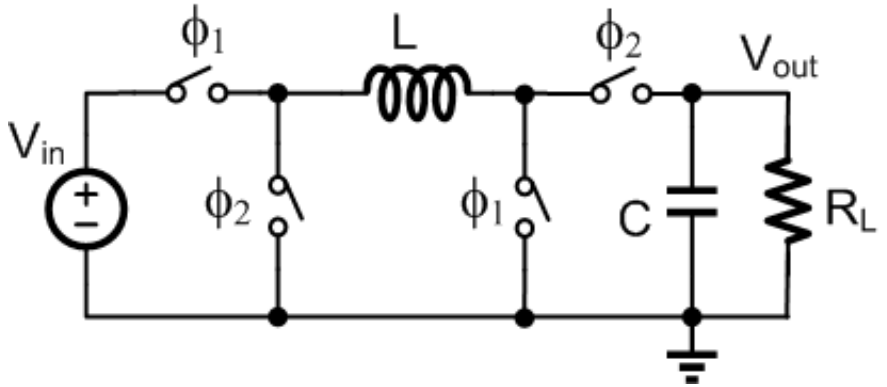
Buck: Step-down only



Boost: Step-up only



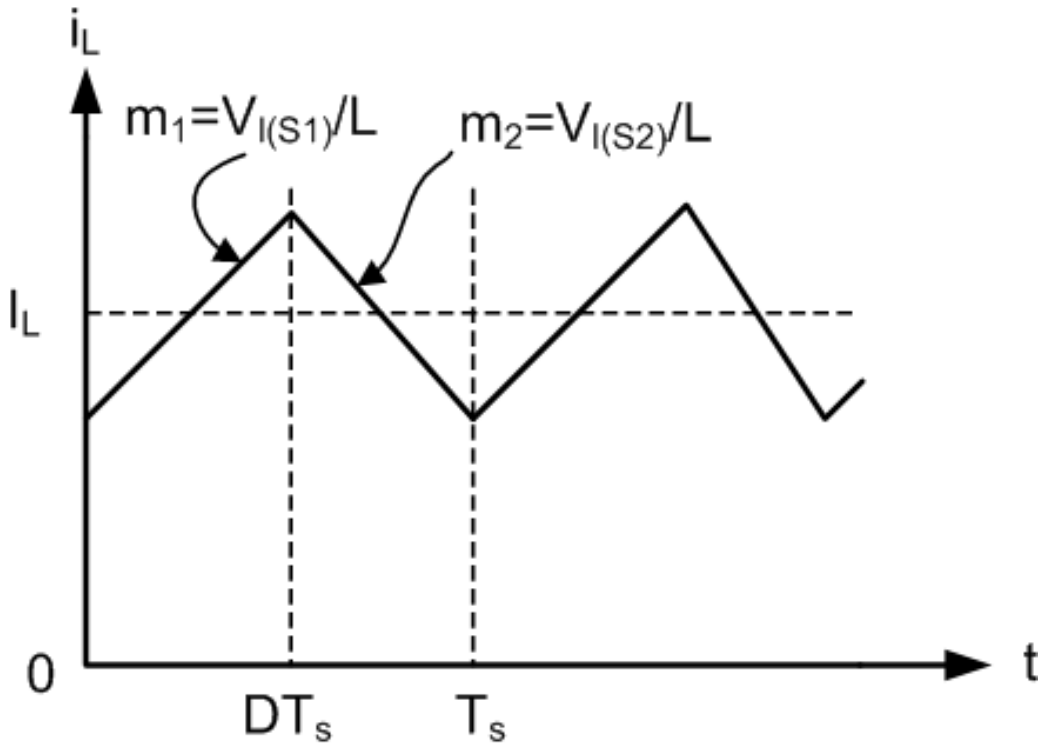
Flyback (buck-boost): Step-up or –down, and V_{out} and V_{in} with opposite polarities



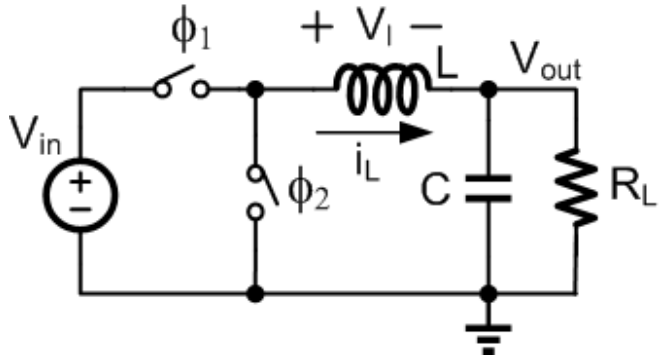
Non-inverting Flyback: Step-up or –down, and V_{out} and V_{in} with the same polarity

Continuous Conduction Mode

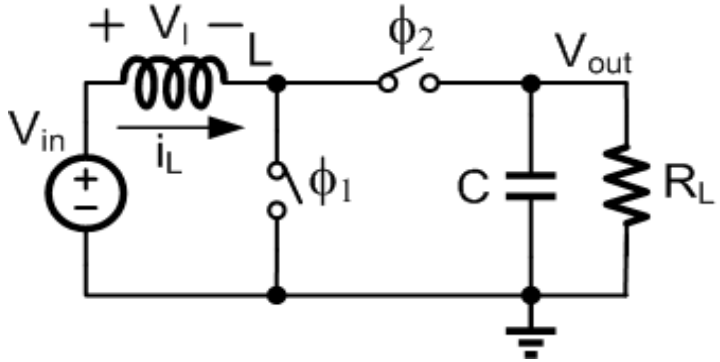
- The converter operates in continuous conduction mode (CCM) if the inductor current is always larger than 0 in the entire switching period T_s.



Buck: Step-down

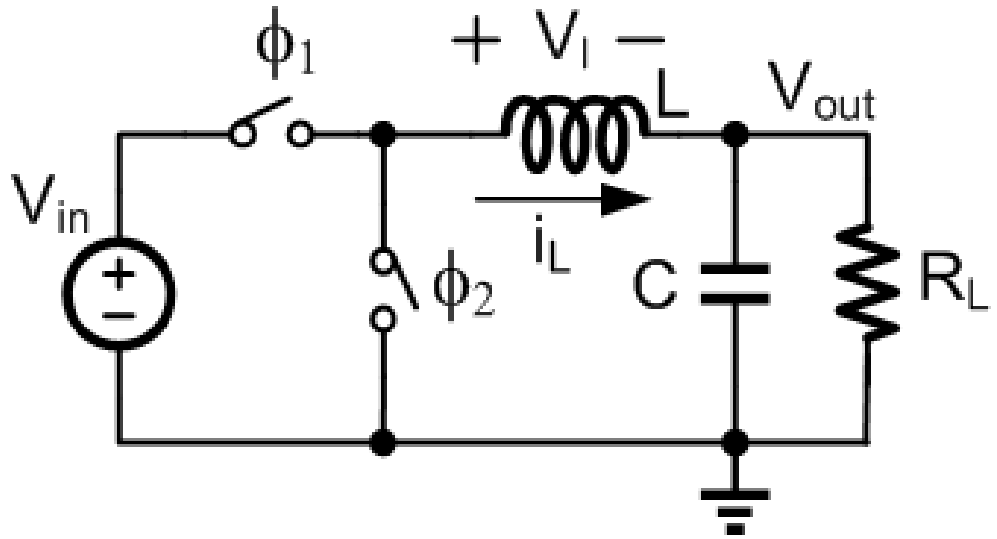


Boost: Step-up



Buck Converter in CCM

- The voltage conversion ratio can be obtained using Volt-Second Balance.
- Note: V_l in state 1 (ϕ_1) = $V_{in} - V_{out}$ and V_l in state 2 (ϕ_2) = $-V_{out}$ assuming ideal switches and inductor.



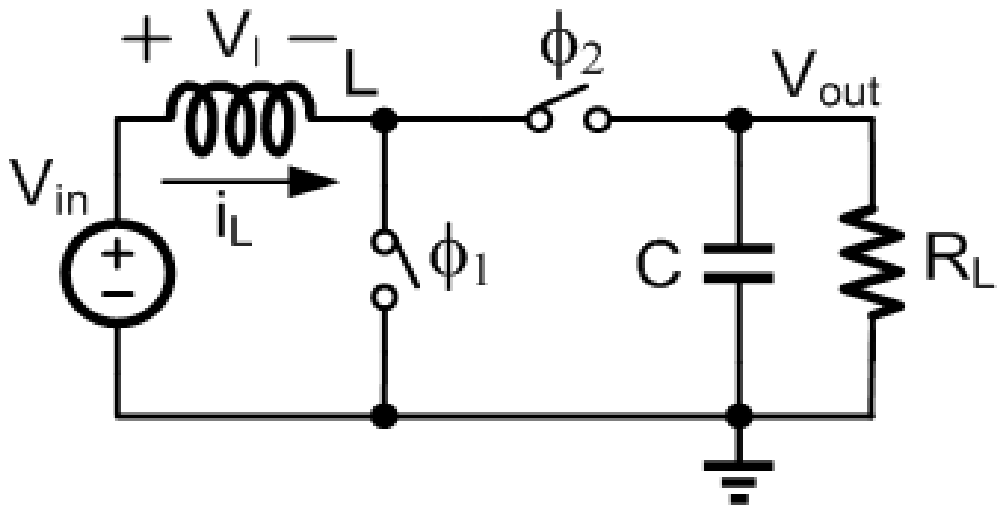
$$m_1 D = m_2(1 - D)$$

$$(V_{in} - V_{out})D = V_{out}(1 - D)$$

$$\frac{V_{out}}{V_{in}} = D$$

Boost Converter in CCM

- The voltage conversion ratio can be obtained using Volt-Second Balance.
- Note: V_l in state 1 (ϕ_1) = V_{in} and V_l in state 2 (ϕ_2) = V_{in} - V_{out} assuming ideal switches and inductor.



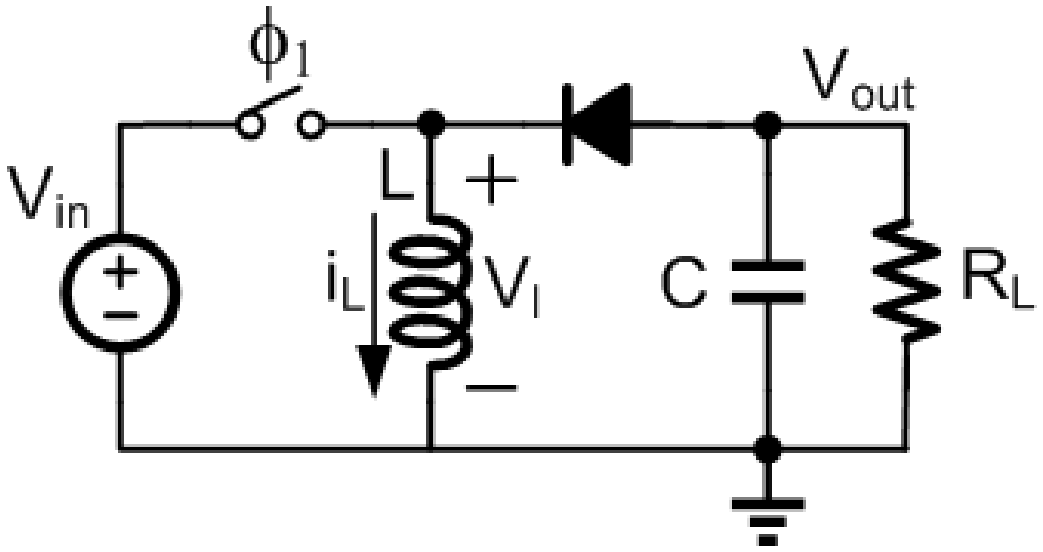
$$m_1 D = m_2(1 - D)$$

$$V_{in} D = (V_{out} - V_{in})(1 - D)$$

$$\frac{V_{out}}{V_{in}} = \frac{1}{1 - D}$$

Flyback Converter in CCM

- The voltage conversion ratio can be obtained using Volt-Second Balance.
- Note: V_l in state 1 (ϕ_1) = V_{in} and V_l in state 2 (T_s- ϕ_1) = V_{out} assuming ideal switch, diode and inductor.



$$m_1 D = m_2(1 - D)$$

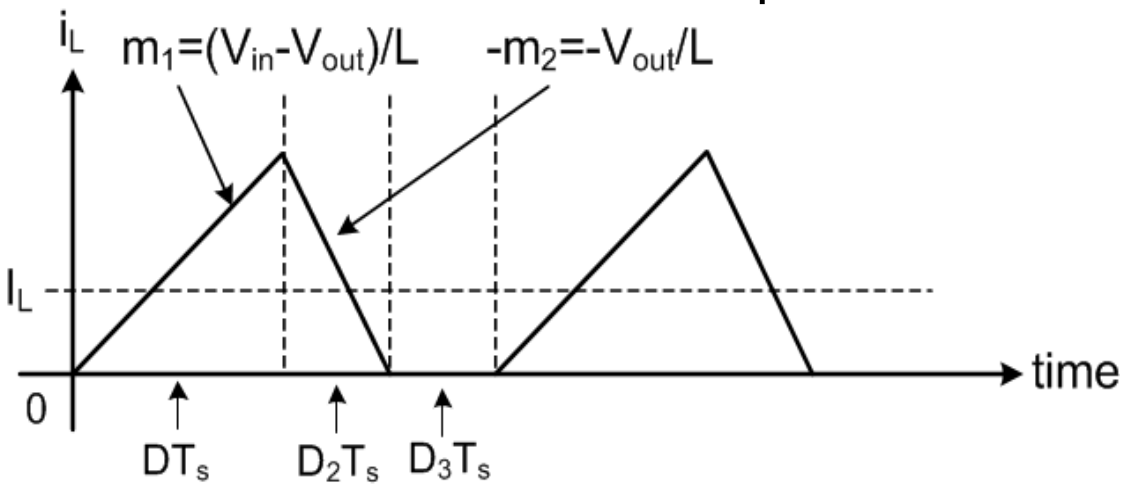
$$V_{in} D = -V_{out}(1 - D)$$

$$\frac{V_{out}}{V_{in}} = -\frac{D}{1 - D}$$

Discontinuous Conduction Mode

- When the output current keeps on decreasing, the inductor current would fall to zero and the converter operates in the discontinuous conduction mode (DCM) with a third state S_3.

Buck converter example



S_1: $nT_s<t<(n+D)T_s$, switch is on & I_L increasing
S_2: $(n+D)T_s<t<(n+D+D_2)T_s$, switch is off & I_L decreasing
S_3: $(n+D+D_2)T_s<t<(n+1)T_s$, both active and passive switches are off, and $I_L = 0$
Note that $D+D_2+D_3=1$

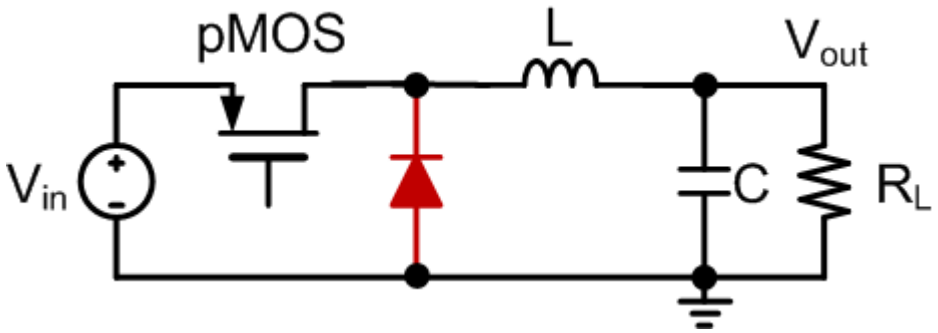
- The volt-second balance becomes

$$m_1 D = m_2 D_2$$

Performance Requirements of SMPC Design

- High Power Conversion Efficiency
  - Minimize power losses in the power stage
- Small Size (High Power Density) and Low Cost
  - Minimize required values of reactive components and off-chip components in the power stage
- High Output Voltage Accuracy
  - Improve both line and load regulations
  - Minimize output voltage ripple relative to the DC output voltage
- Fast Transient Response
  - Improve the speed of the controller
  - Increase the slew rate of the inductor current

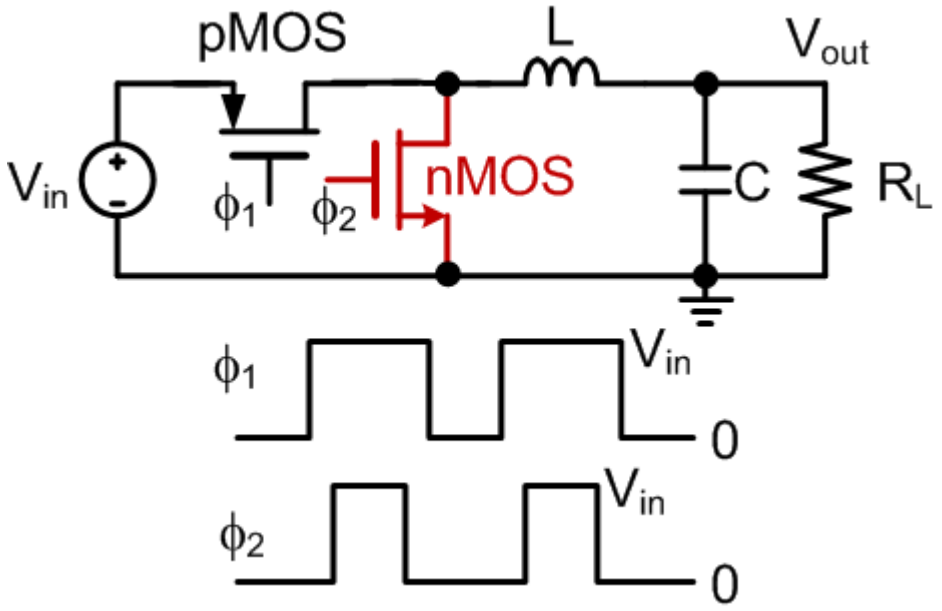
Asynchronous vs Synchronous Power Stage



- Diode provides a current path when the pMOS switch is off.
- Diode voltage drop leads to large conduction power loss, unsuitable for low output-voltage conditions.

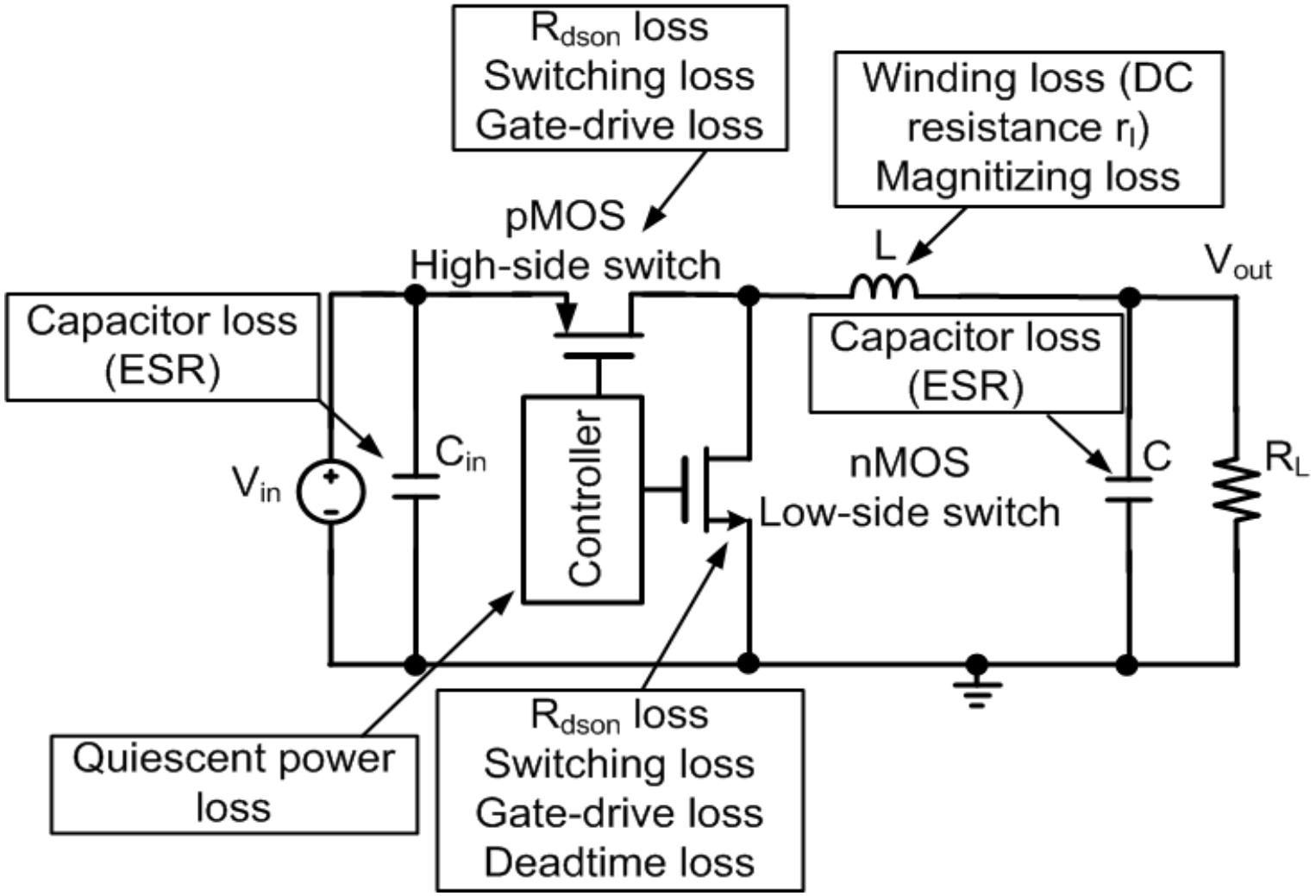
$$\eta_{max} = \frac{V_{out}}{V_{out} + (1 - D)V_d}$$

- If V_{in}=3.6V, V_{out}=1.5V, V_d=0.7V, then η_{max}=78.6%!



- Power nMOS offers much smaller voltage drop than V_d.
- Dead-time is needed for gate driving signals of pMOS and nMOS to avoid short-circuit power loss.

Losses in Synchronous Buck Converters



Example on Conduction Loss Calculation

- Conduction loss is dominated by on-resistance of power FETs and DC resistance (DCR) of the inductor.
- Conduction loss of high-side (HS) power switch

$$P_{L-HS} = I^2_{HS-rms} \cdot R_{dson-HS}$$

$$= I^2_{L,rms} \cdot D \cdot R_{dson-HS} = (I_o^2 + \frac{\Delta i_L^2}{12}) \cdot D \cdot R_{dson-HS}$$

- Conduction loss of low-side (LS) power switch

$$P_{L-LS} = I^2_{LS-rms} \cdot R_{dson-LS}$$

$$= I^2_{L,rms} \cdot (1-D) \cdot R_{dson-LS} = (I_o^2 + \frac{\Delta i_L^2}{12}) \cdot (1-D) \cdot R_{dson-LS}$$

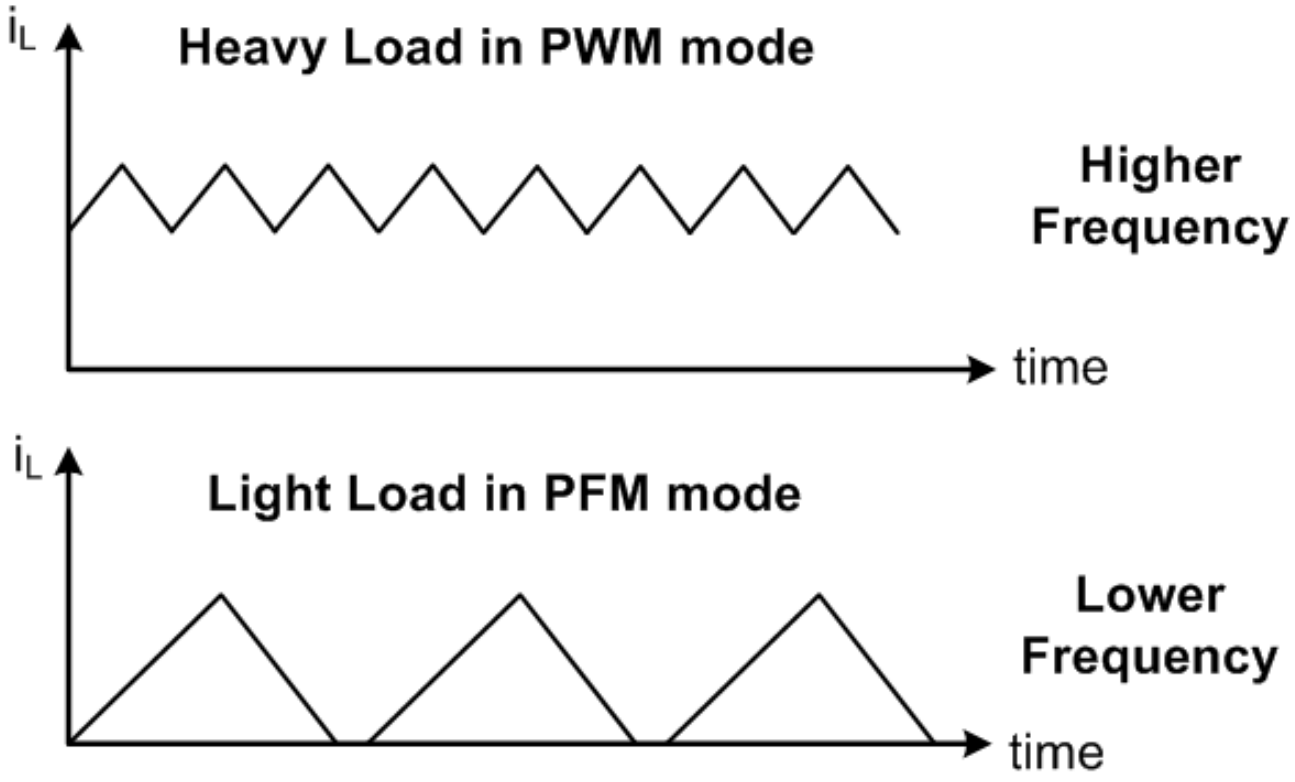
- Conduction loss of inductor DCR

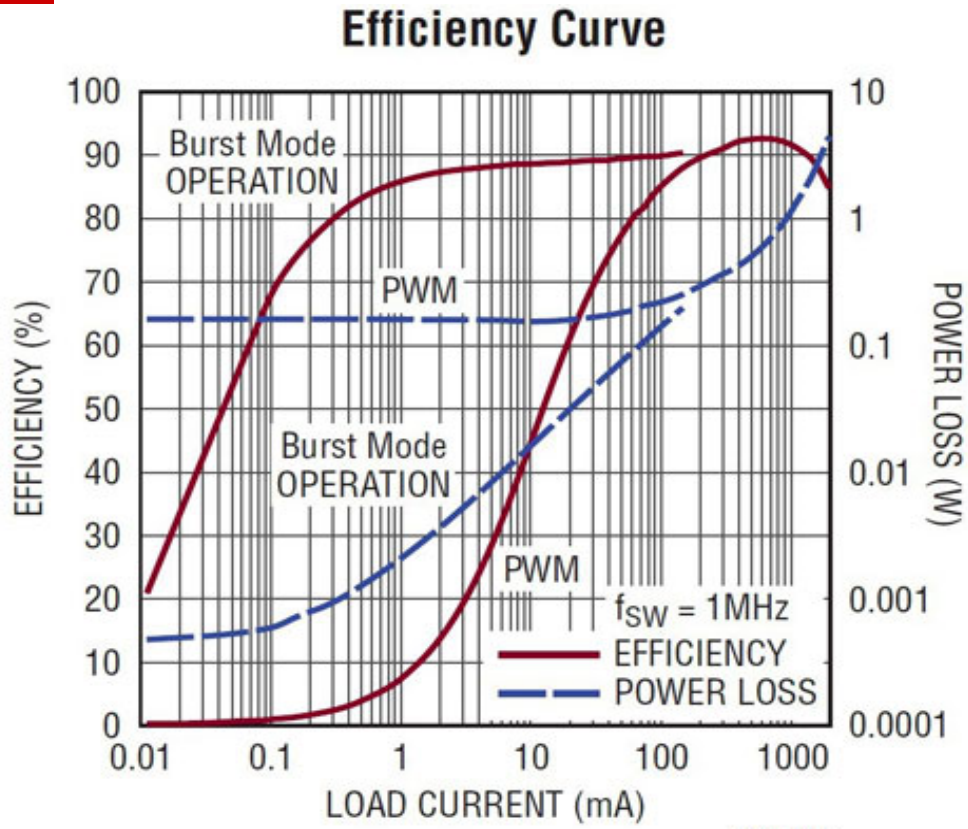
$$P_L = I^2_{L,rms} \cdot r_l = (I_o^2 + \frac{\Delta i_L^2}{12}) \cdot r_l$$

Loss Summary of Synchronous Buck Converter

Conduction Losses	Power FET on-resistance R_{dson}	$(I_o^2 + \frac{\Delta i_L^2}{12})(R_{dson-HS} \cdot D + R_{dson-LS} \cdot (1-D))$
	Inductor Winding Resistance	$(I_o^2 + \frac{\Delta i_L^2}{12})(r_l)$
Dynamic Losses	Power FET Gate Drive Losses	$f_s \cdot V_{in}(C_{g-HS} \cdot V_{g-HS} + C_{g-LS} \cdot V_{g-LS})$
	Capacitive Switching Loss	$\sim 0.5C_x V_{in}^2 f_s$
Static Loss	Converter quiescent current	$I_Q \cdot V_{in}$

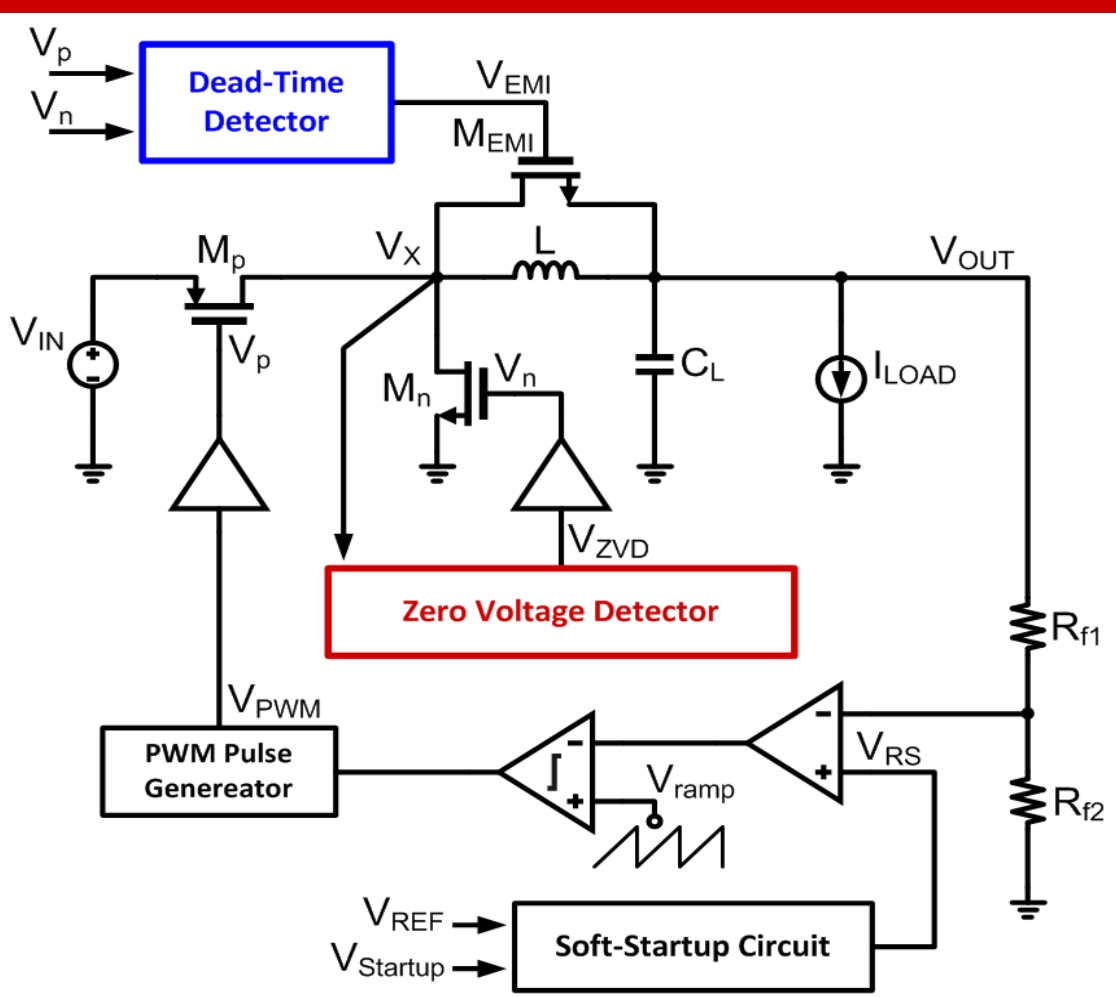
Efficiency Enhancement: PWM-PFM Control

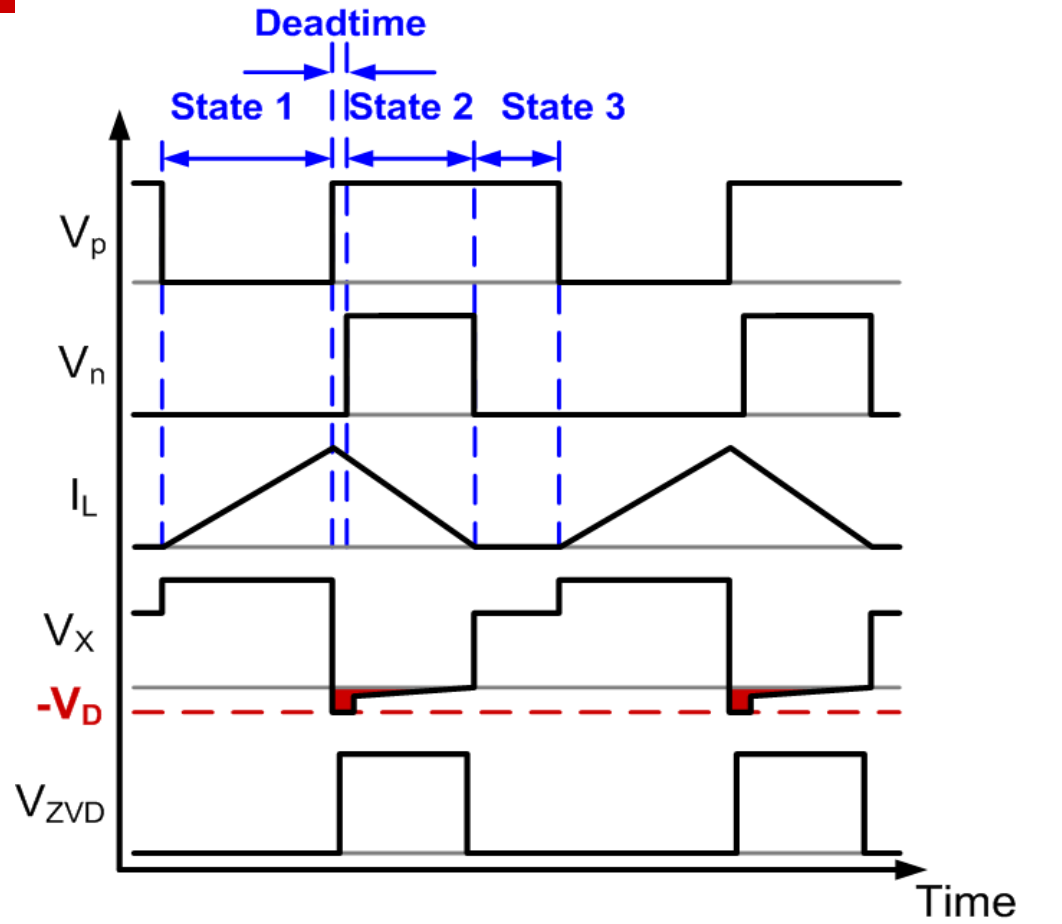




- Dynamic losses (switching and gate-drive losses) become dominant in the light-load condition.
- Reducing switching activities of power transistors in light loads improves converter light-load power efficiency.

Efficiency Enhancement: DCM Operation

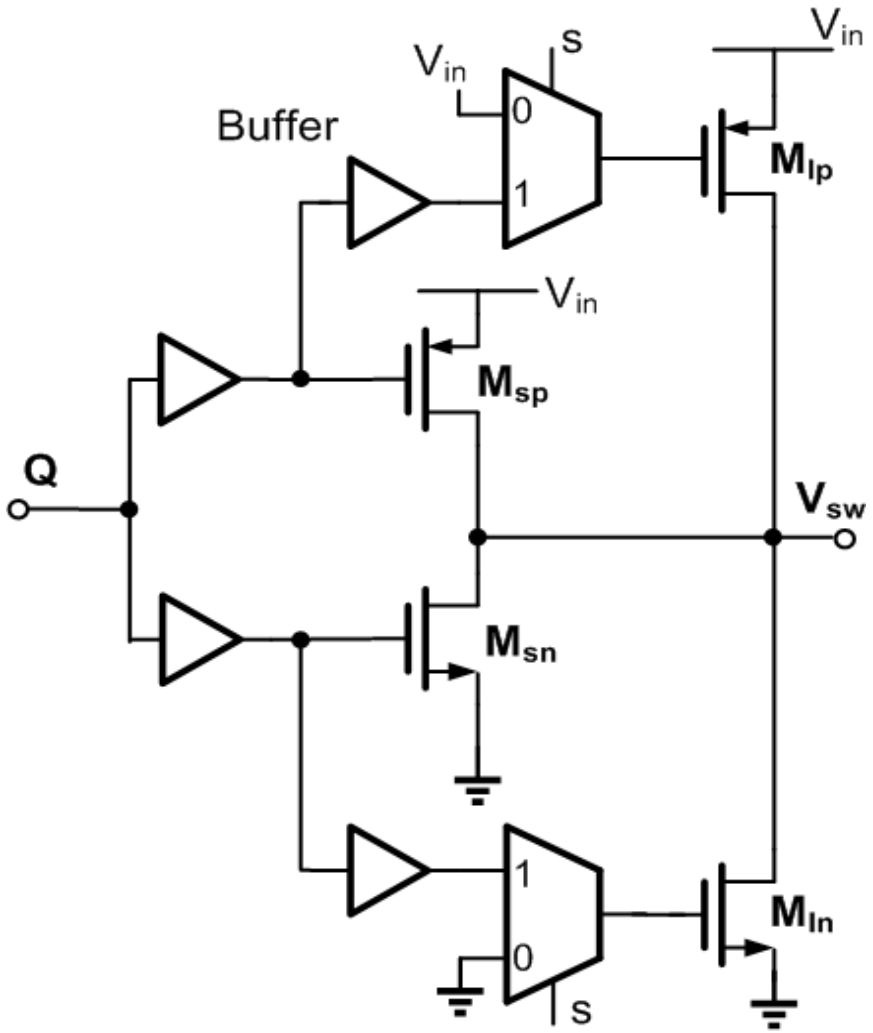




H. Lee et. al., TCAS-II, Mar. 2010, pp. 238-242.

- DCM enables lower frequency operation, reducing the switching power loss.

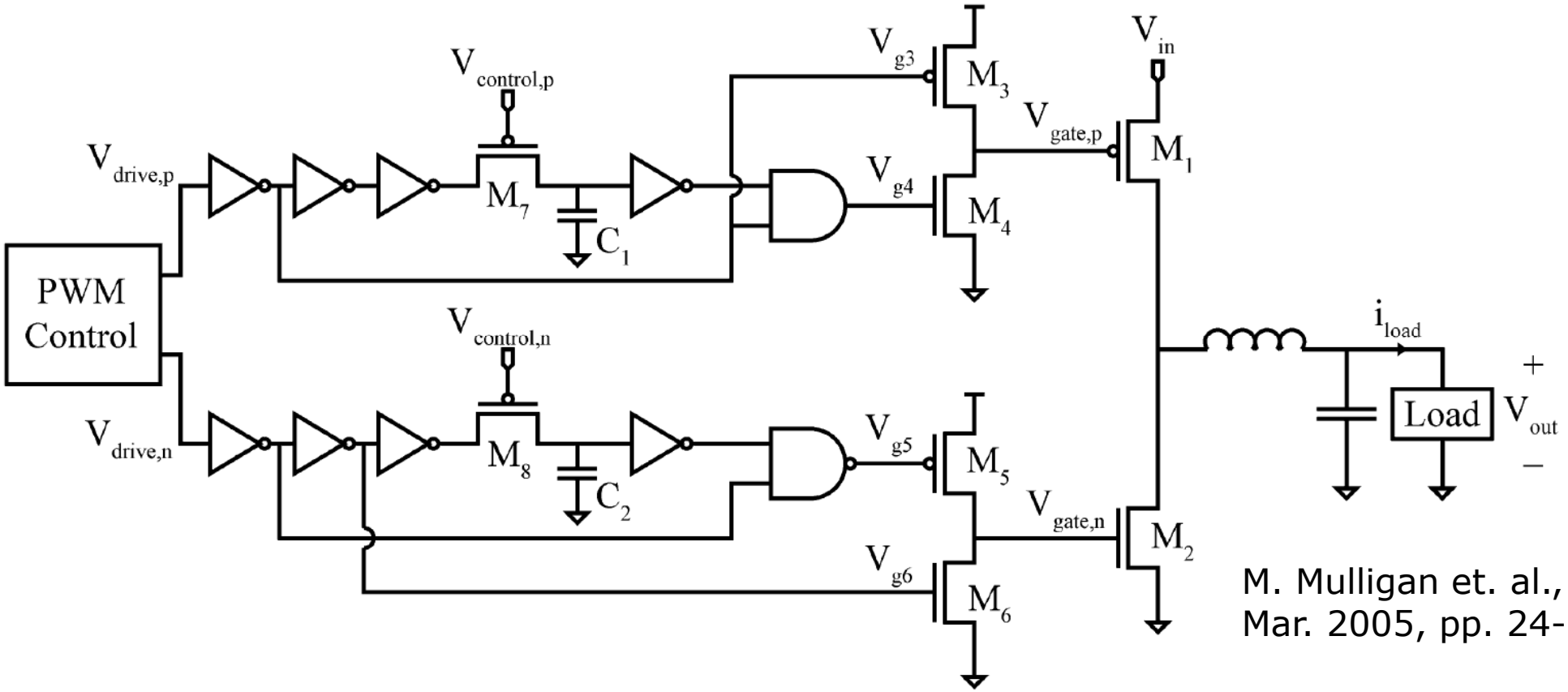
Efficiency Enhancement: Width Switching



- Only smaller-size power transistors (M_{sp}, M_{sn}) are used to reduce the gate drive loss at the light load condition.
- All power transistors (M_{sp}, M_{sn}, M_{lp}, M_{ln}) are used for the full load condition.
- Potential cross conduction of large and small power transistors may occur during switching if buffers are not designed properly.

D. Park et. al., TCAS-II, Aug. 2014, pp. 599-603.

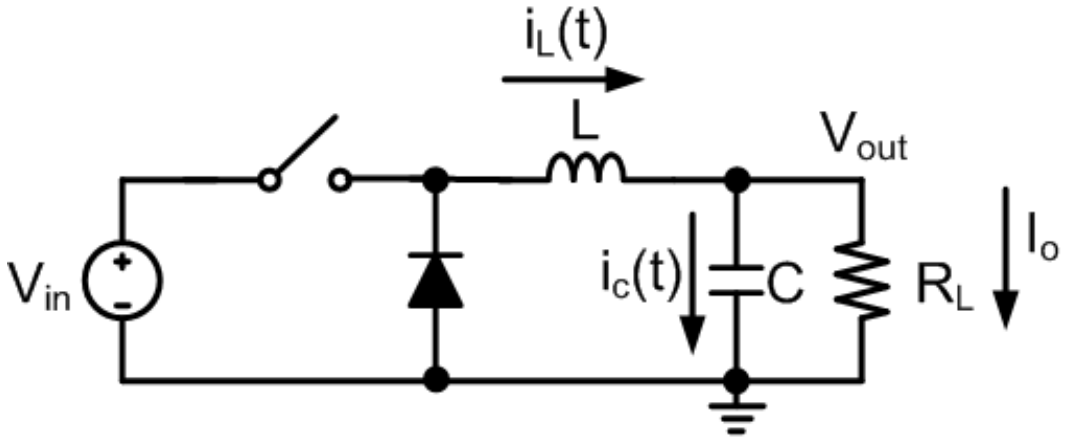
Efficiency Enhancement: Gate Swing Modulation

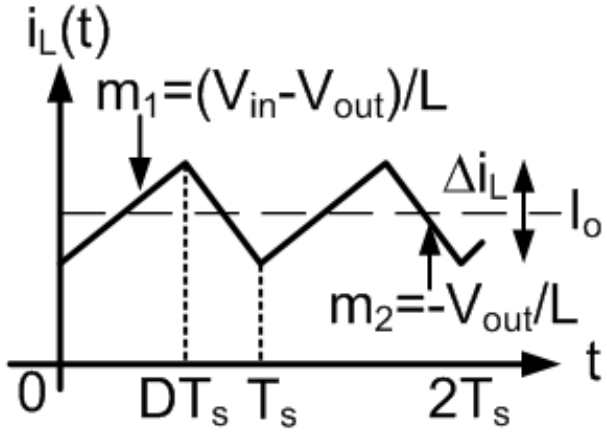


M. Mulligan et. al., PE Letters, Mar. 2005, pp. 24-29.

- This strategy improves light-load efficiency with the fixed switching frequency.
- Control the gate swing of power transistors via modulating the turn-on time of M_4 and M_5 using a voltage-controlled RC delay

Buck Converter: Inductance Selection





- For CCM operation,

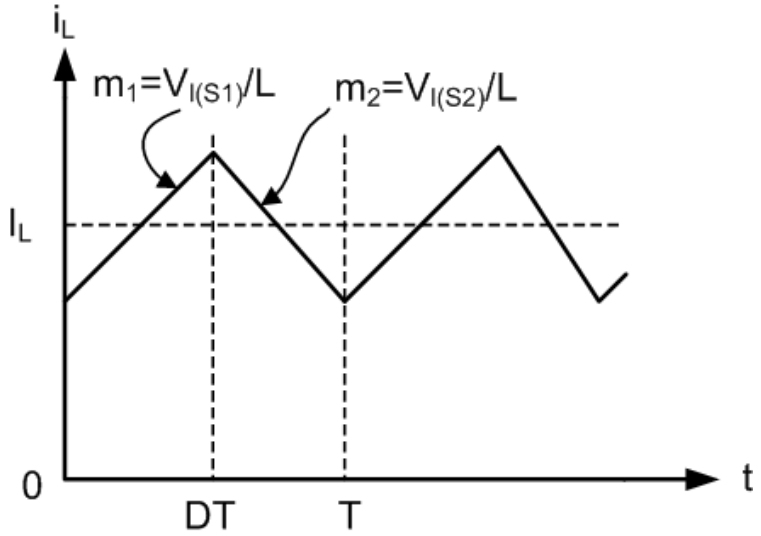
$$L = \frac{(V_{in} - V_{out}) \cdot D}{\Delta i_L f_s} = \frac{(V_{in} - V_{out}) \cdot V_{out}}{V_{in} \cdot \Delta i_L \cdot f_s} = \frac{(V_{in} - V_{out}) \cdot V_{out}}{V_{in} \cdot r \cdot I_{o,max} \cdot f_s}$$

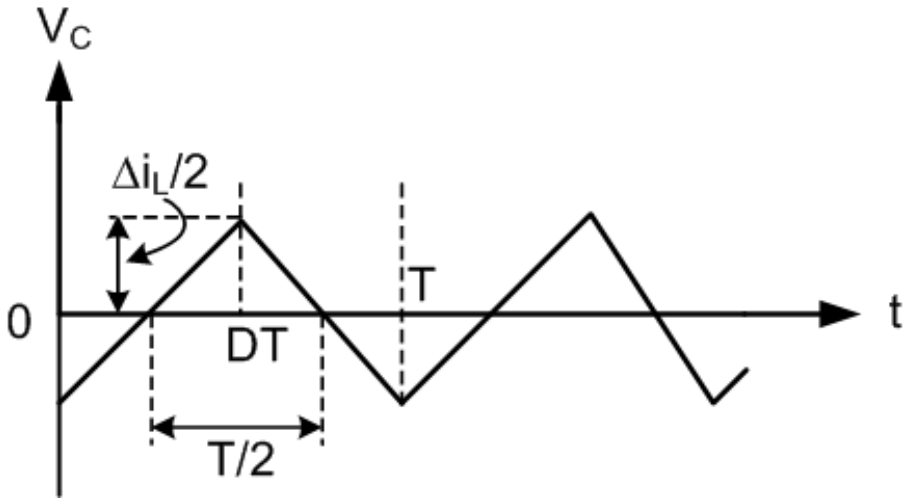
where r is the current ripple ratio of 0.25 – 0.5

$I_{o,max}$: maximum output current

- For given V_{in} and V_{out}, the inductance is determined by the inductor current ripple and switching frequency f_s. Higher switching frequency f_s reduces the required L.

Buck Converter: Output Capacitor Selection





- The output capacitance C is determined by the output ripple and switching frequency

$$C = \frac{0.5 \cdot (\Delta i_L/2)(T/2)}{\Delta V_{out}}$$

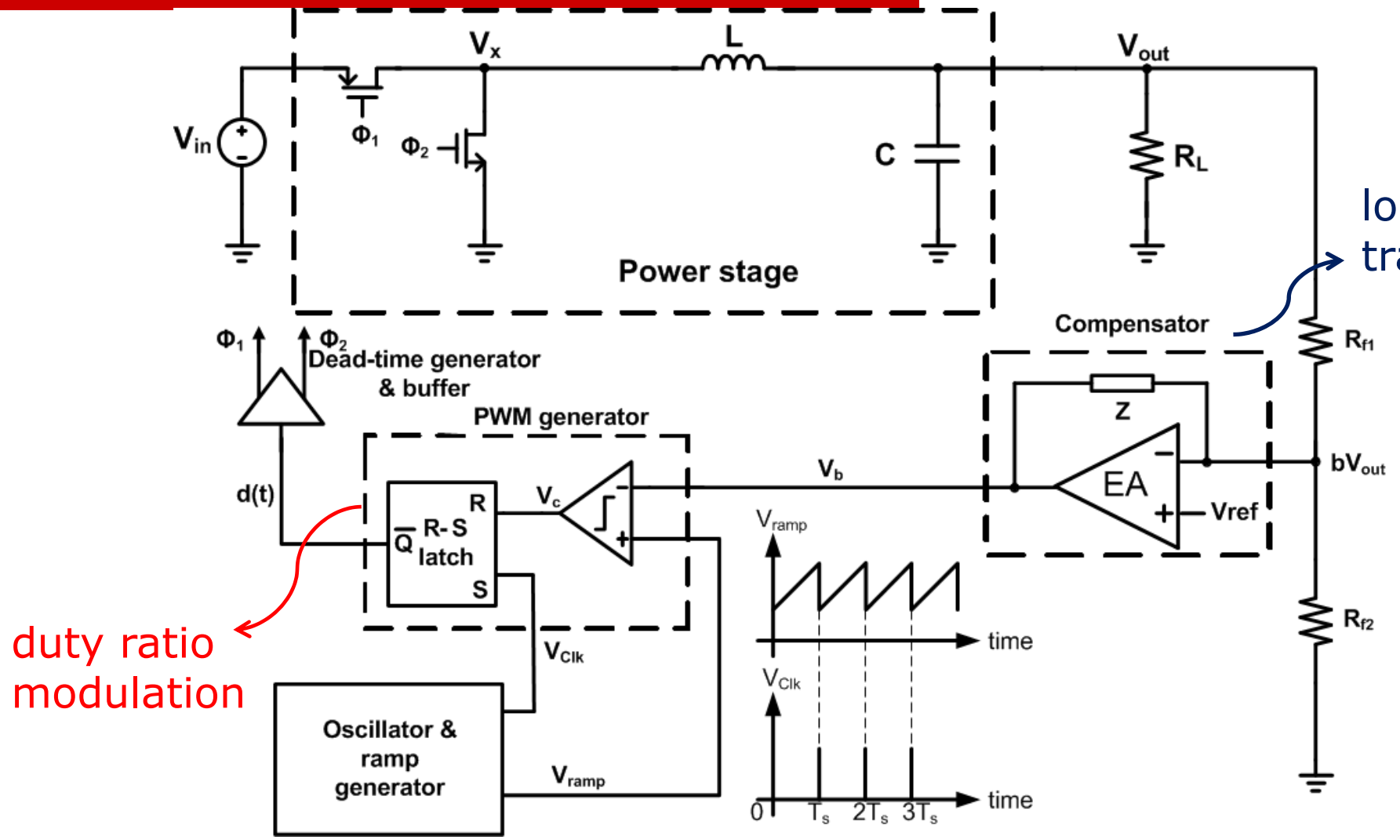
$$= \frac{(V_{in} - V_{out}) \cdot D}{8L\Delta V_{out} f_s^2}, \quad \Delta V_{out} : \text{output ripple voltage}$$

- Higher switching frequency reduces the required value of C for a given ΔV_{out}.

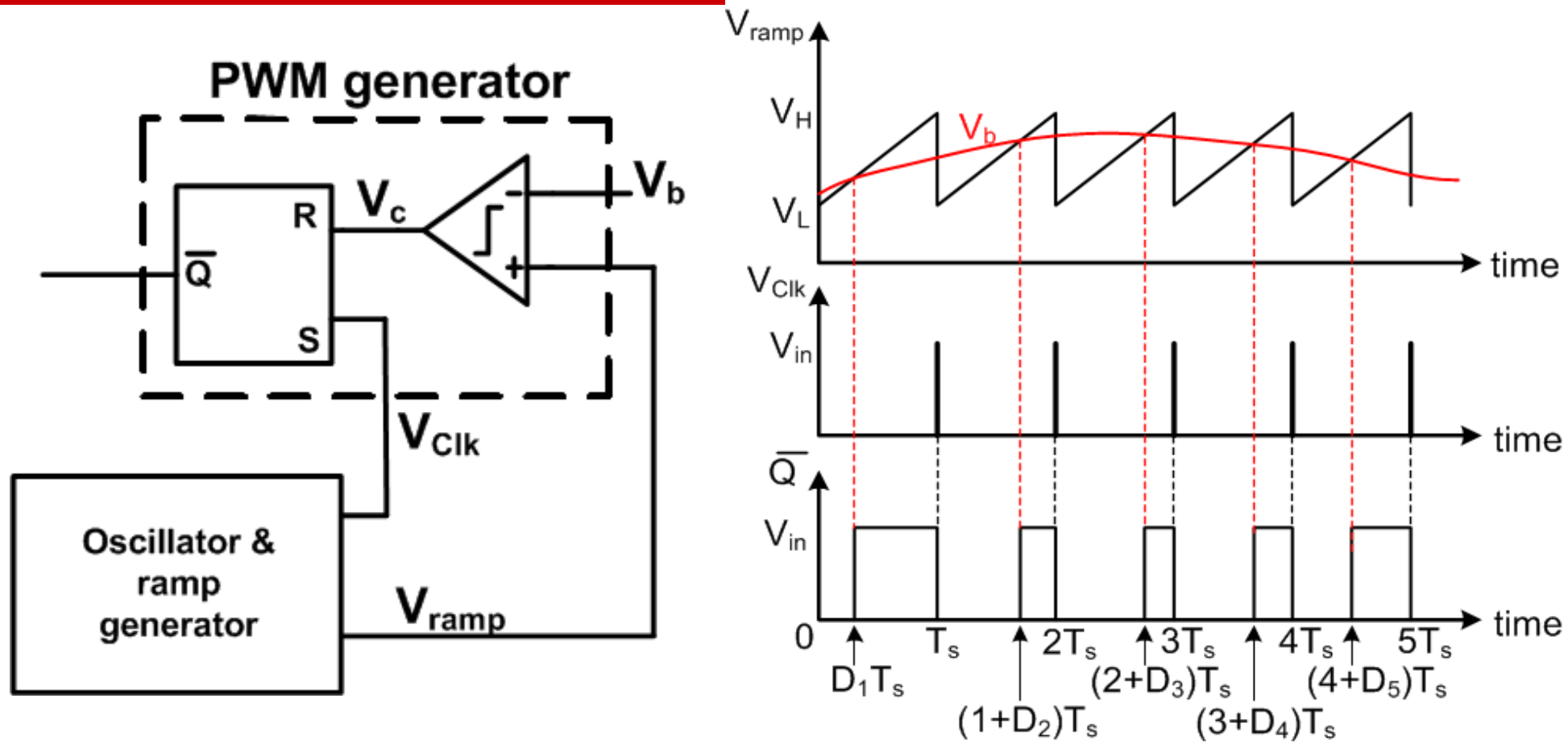
Outline

- SMPC Basics and Design Considerations
- Control Methodologies and Design Issues
  - Voltage-mode PWM and compensator design
  - Current-mode PWM and compensator design
  - Current sensor designs
  - Gate driver designs
  - Hysteretic control
- Advanced Topic
  - Three-Level DC-DC Converter

PWM – Voltage-Mode Control (VMC)



VMC – PWM Generator



- Duty ratio (D) is defined by the crossing of compensator output V_b and the fixed ramp signal V_{ramp}: larger V_b leads to larger D.

VMC – Loop Gain T(s) (1)

- **Loop gain T(s)**

$$T(s) = \frac{R_{f2}}{R_{f1}+R_{f2}} \cdot A(s) \cdot \underbrace{\frac{\Delta D}{\Delta V_b} \cdot \frac{\Delta V_x}{\Delta D} \cdot \frac{\Delta V_o}{\Delta V_x}}_{\mathbf{C(s)}}$$

$$\frac{\Delta D}{\Delta V_b} = \frac{1}{V_M}$$

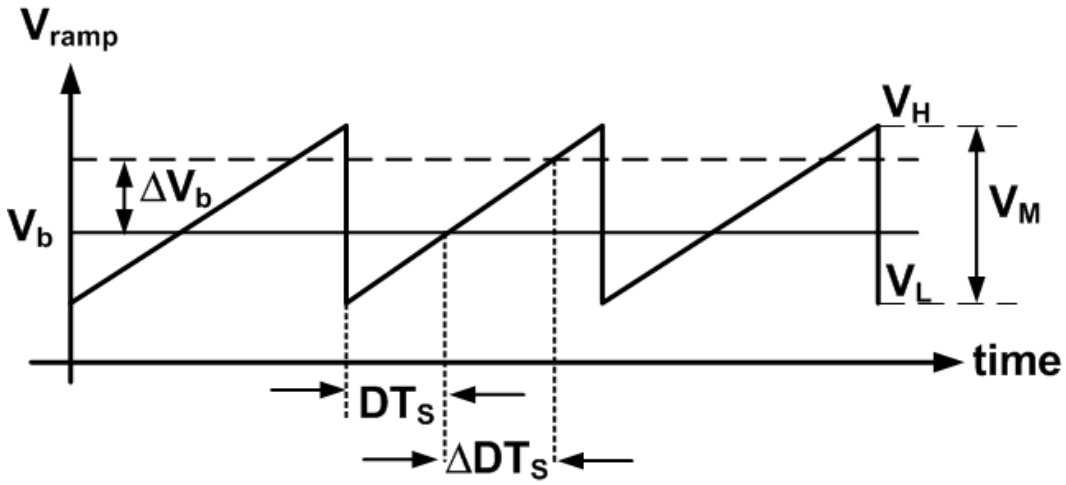
$$\frac{\Delta V_x}{\Delta D} = V_{in}$$

$$\frac{\Delta V_o}{\Delta V_x} = \frac{1+\frac{s}{\omega_z}}{1+\frac{s}{Q\omega_o}+\frac{s^2}{\omega_o^2}} \quad (2^{nd} \text{ order LC filter})$$

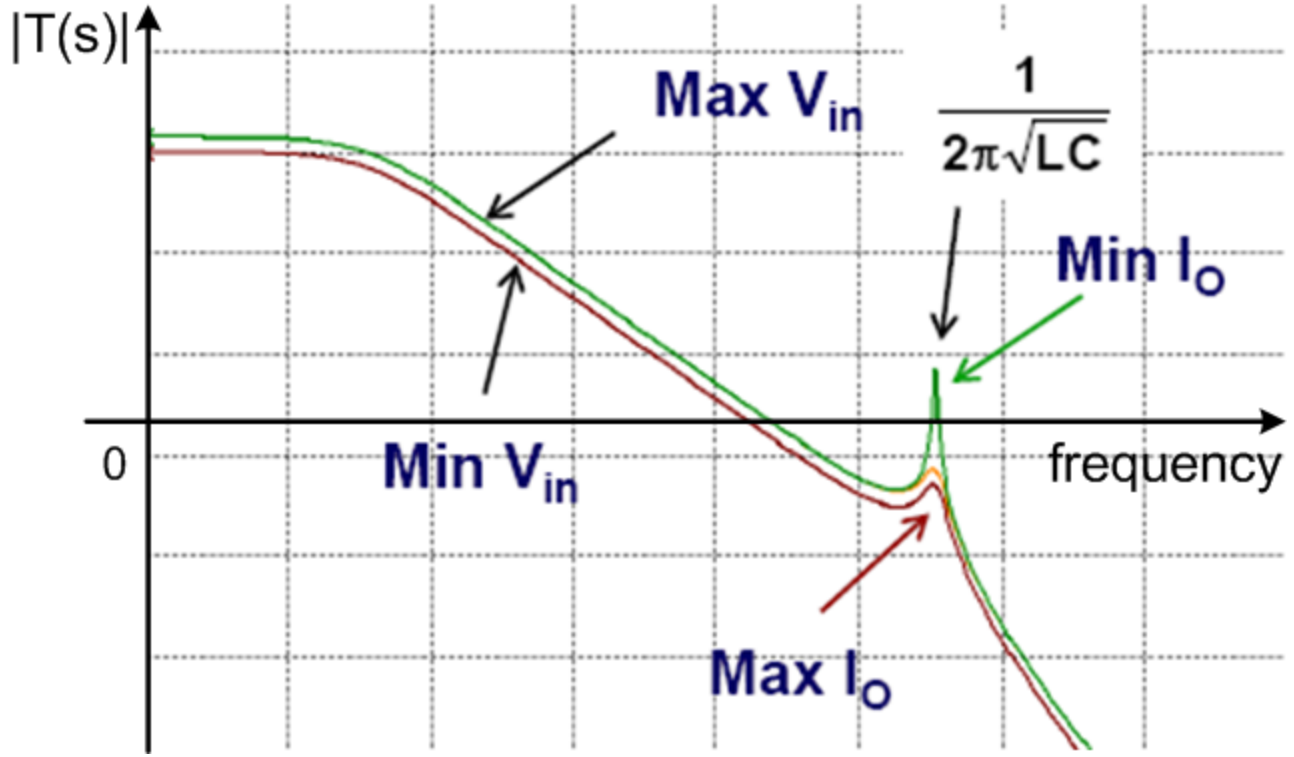
where $\omega_z = \frac{1}{CR_{eC}}$, $\omega_o = \sqrt{\frac{1}{LC}}$, $Q = R_L\sqrt{\frac{C}{L}}$

A(s): Compensator transfer function
C(s): Control-to-output transfer function

PWM generator transfer function ($\Delta D/\Delta V_b$)

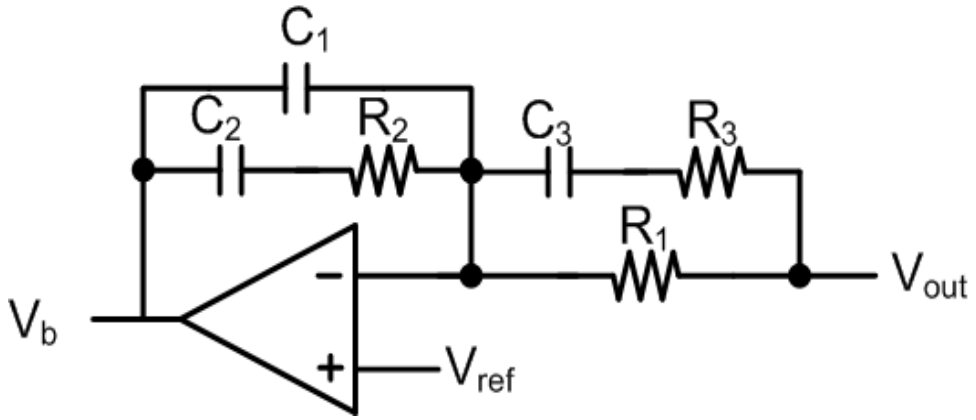


VMC – Traditional Dominant Pole Compensation

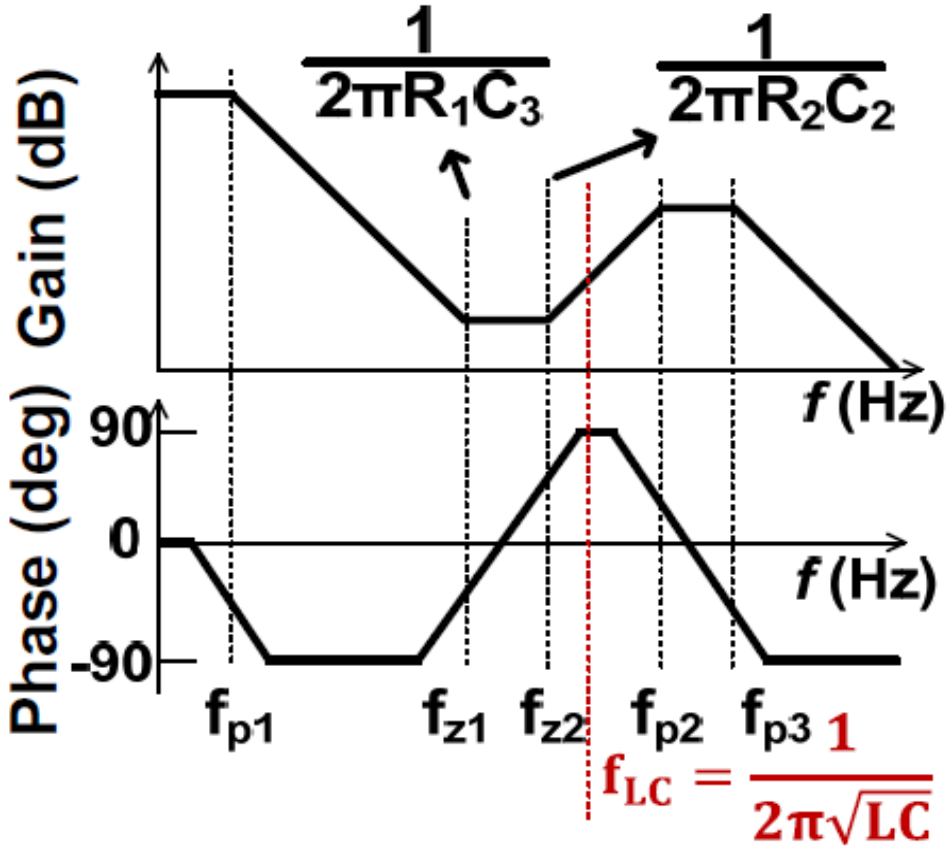


- High Q factor of the complex poles limits the unity-gain frequency of T(s), thereby degrading the converter transient response.
- Worst-case stability (minimum gain margin) occurs at the maximum V_{in} and the minimum I_o due to largest Q value of the complex poles.

VMC – Type III Compensator (1)

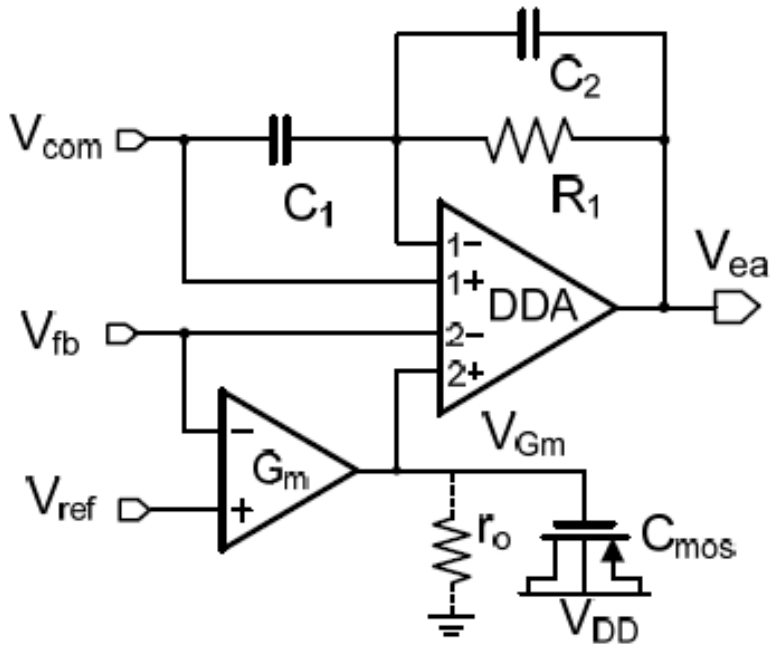


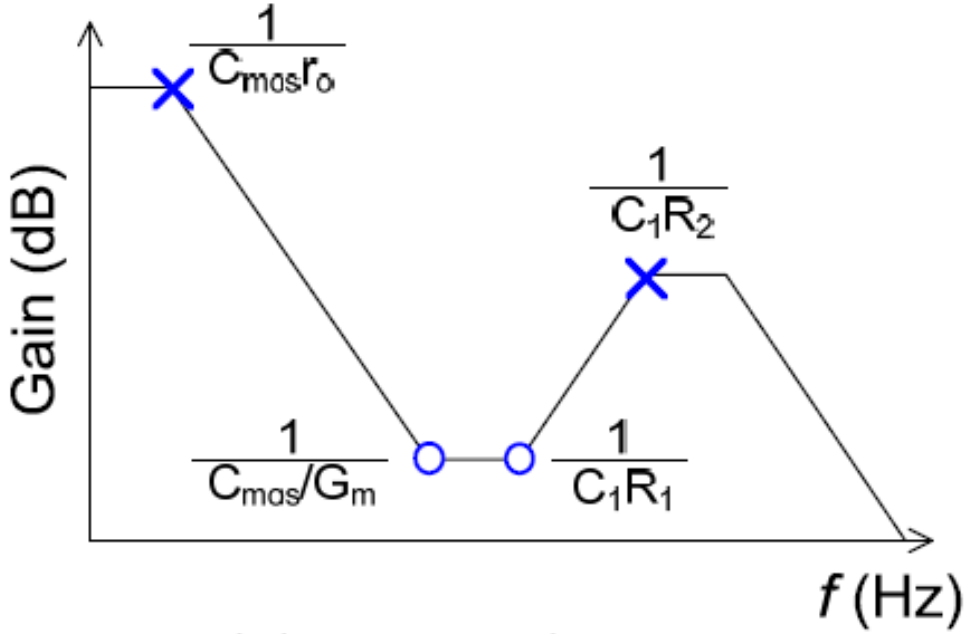
$$A(s) = \frac{R_1 + R_3}{R_1 R_3 C_1} \cdot \frac{(s + \frac{1}{R_2 C_2})(s + \frac{1}{(R_1 + R_3)C_3})}{s(s + \frac{C_1 + C_2}{R_2 C_1 C_2})(s + \frac{1}{R_3 C_3})}$$



- 2 LHP zeros are generated in A(s) to compensate for the negative phase shift of the complex poles in C(s).
- This compensator however requires large area for passive components.

VMC – Type III Compensator (2)



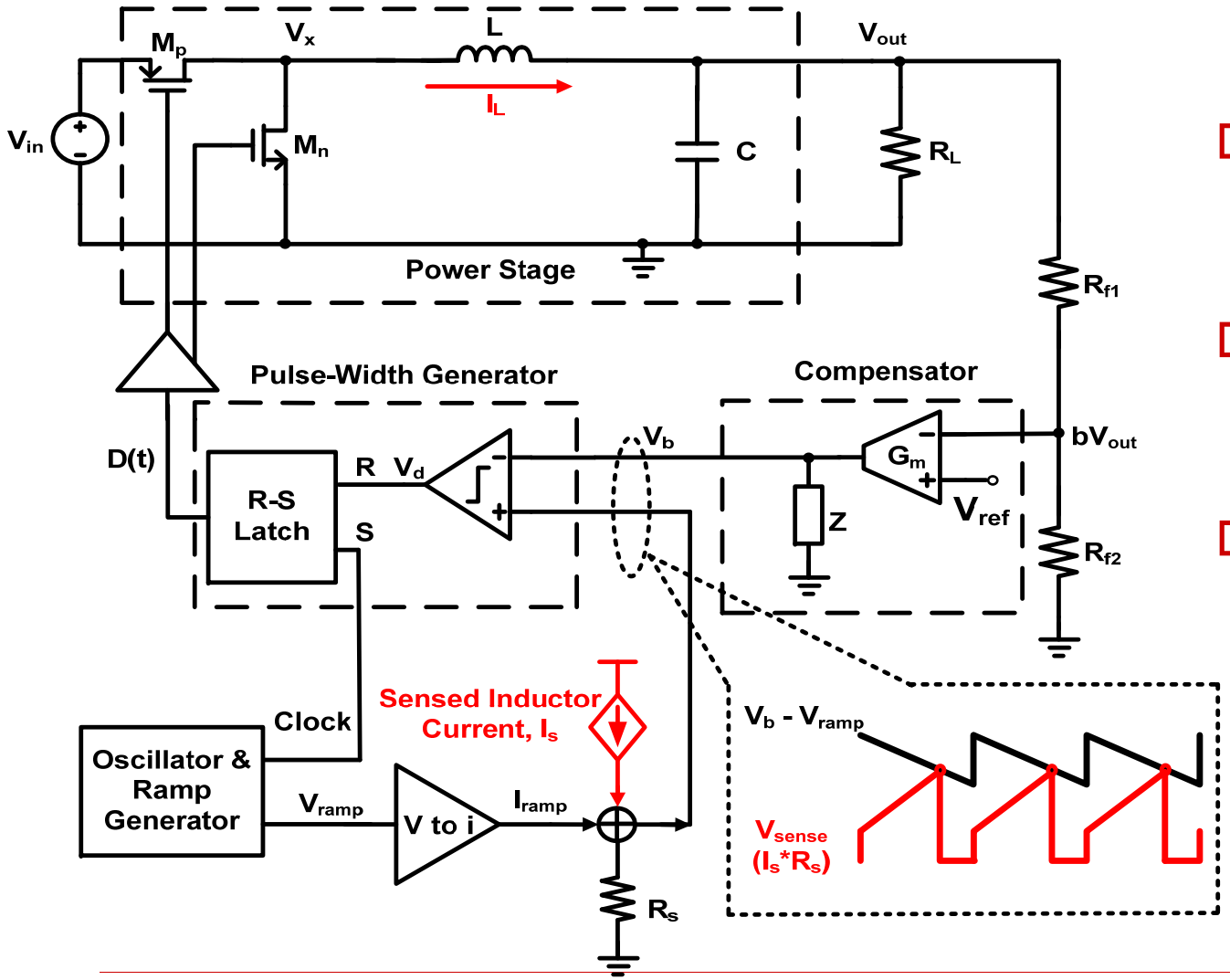


$$A(s) = (1 + G_m r_o)\frac{(1 + sC_{mos}/G_m)(1 + sC_1R_1)}{(1 + sC_{mos}r_o)(1 + sC_2R_1)}$$

- Differential difference amplifier is used to realize the Type-III compensator for reducing the required number of passive components.

L. Chen et. al., ISSCC, Feb. 2014, pp. 84-85.

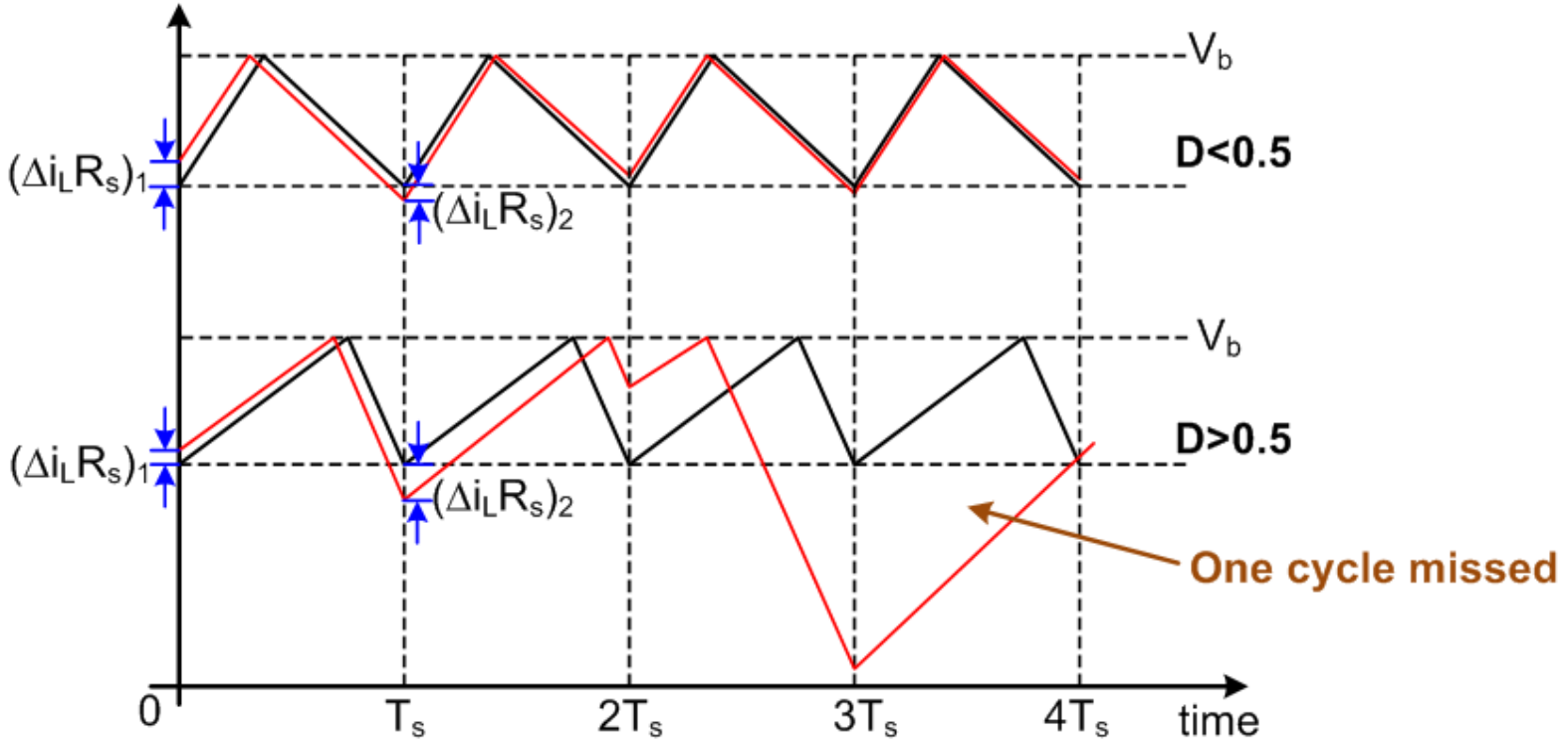
PWM – Current-Mode Control (CMC)



- Both inductor current and output voltage information are used.
- The converter has inherent pulse-by-pulse current limiting and soft start.
- Sensed inductor current is used as a ramp to define D by replacing the fixed voltage ramp.

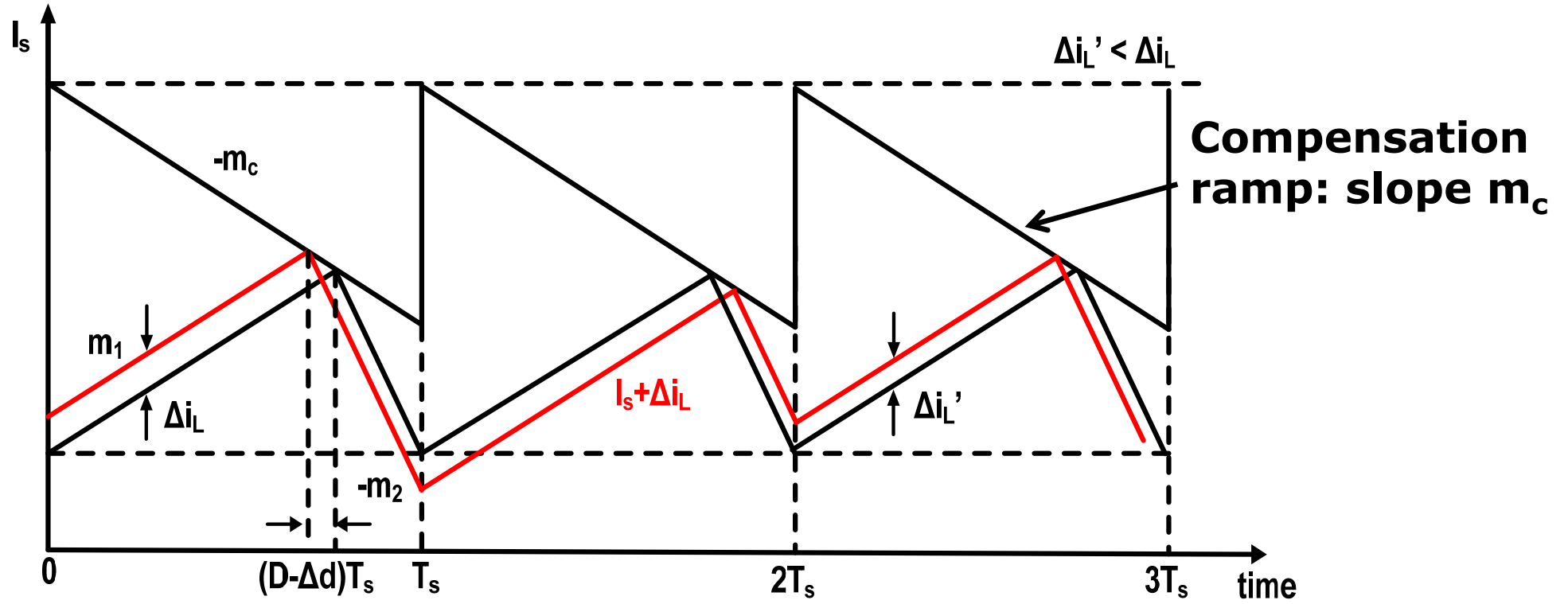
C. F. Lee et. al., JSSC, Jan. 2004, pp. 3-14.

CMC – Sub-Harmonic Oscillations (1)



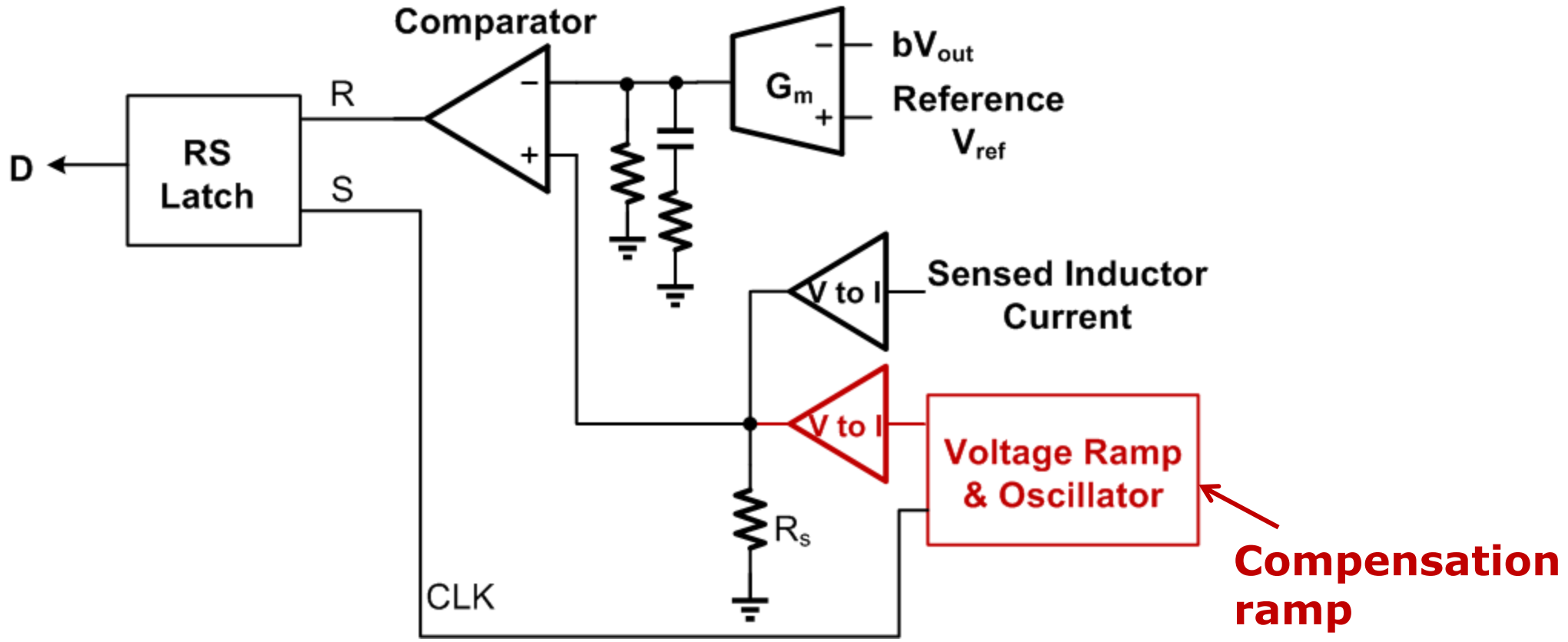
- Current-mode converters will undergo sub-harmonic oscillation (at $f_s/2$, $f_s/4$, etc.) whenever D > 0.5.
- For D < 0.5, $m_1 > m_2$, the perturbation decreases with $(\Delta i_L R_f)_2 < (\Delta i_L R_f)_1$.
- For D > 0.5, $m_1 < m_2$, the perturbation increases with $(\Delta i_L R_f)_2 > (\Delta i_L R_f)_1$.

CMC – Sub-Harmonic Oscillations (2)



- A compensation ramp with slope $m_c \geq m_{2,max}/2 = V_{out,max}/2L$, can suppress the oscillation under D>0.5, where m_2 is the slope of the I_L during $(1-D)T_s$.
- The compensation ramp can be realized by the voltage ramp generator.

Compensation Ramp in Current-Mode Controller



- The compensation ramp with slope m_c is added together with the sensed inductor current signal at the input of PWM generator.

CMC – Loop Gain T(s)

$$T(s) = \frac{R_{f2}}{R_{f1}+R_{f2}} A(s) \frac{R_L // R_a}{R_s} \frac{1+sR_{eC}C}{(1+s/\omega_a)(1+s/\omega_{t1})}$$

$$R_a = \frac{L}{[(1-D)(1+\frac{m_c}{m_1})-D]T_s}$$

$$\omega_a = \frac{1}{C(R // R_a)} = p_1$$

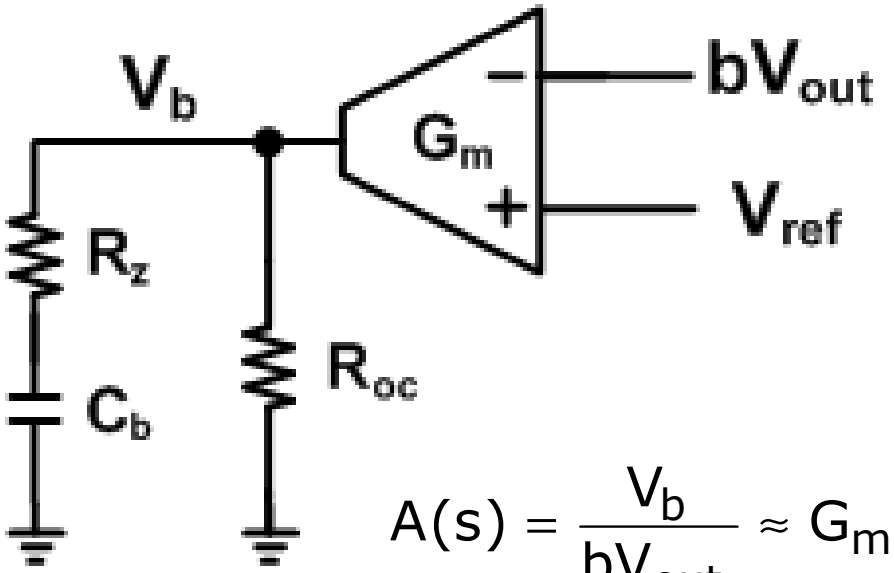
$$\omega_{t1} = \frac{1}{(1-D)(1+\frac{m_c}{m_1})T_s} = p_2$$

R_{eC}: ESR of output capacitor

A(s): transfer function of the compensator

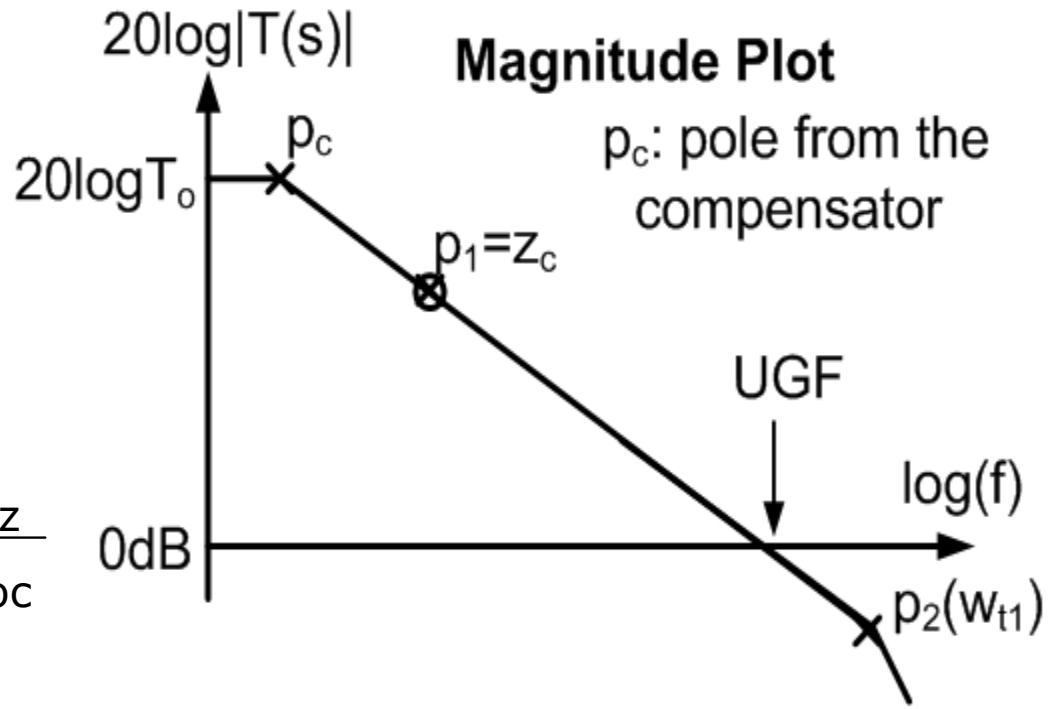
- Two separate poles ω_a and ω_{t1} in T(s) are easier to compensate compared to the complex poles in the voltage-mode counterpart.

CMC – Compensator Design



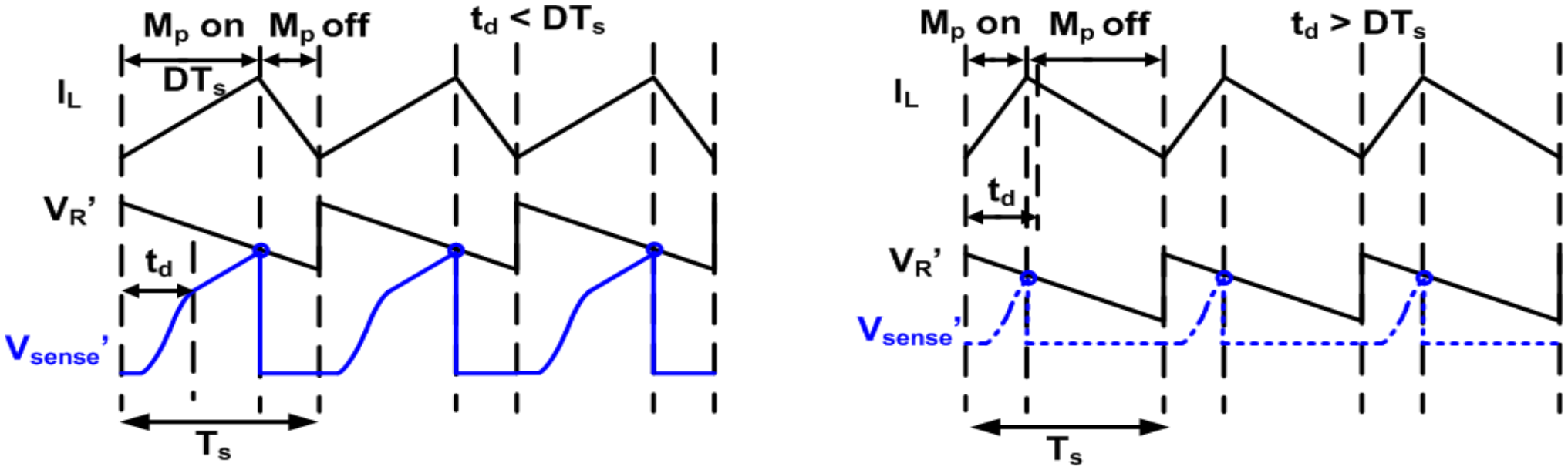
$$A(s) = \frac{V_b}{bV_{out}} \approx G_m R_{oc} \frac{1 + sC_bR_z}{1 + sC_bR_{oc}}$$

for $R_{oc} >> R_z$



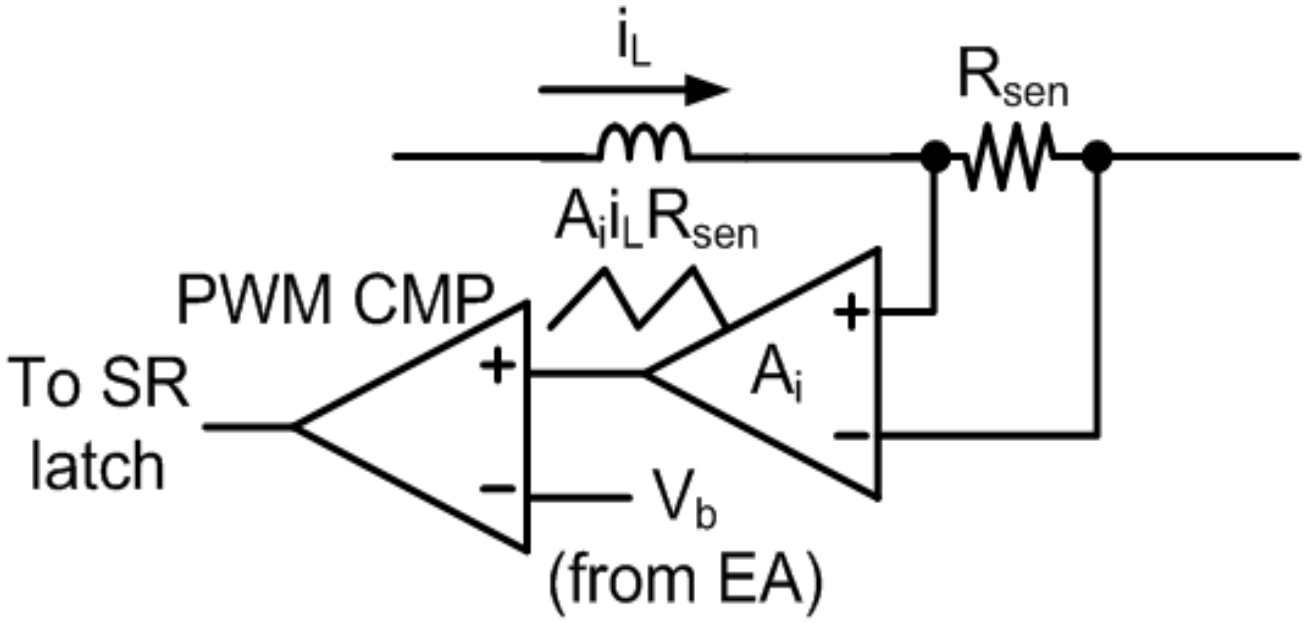
- Compensator LHP zero (z_c) cancels negative phase shift of p_1 (ω_a) in T(s) by positioning z_c at p_1.
- Dominant pole p_c of T(s) is given as $1/R_{oc}C_b$ from the compensator.
- UGF of T(s) is smaller than ω_{t1} and can reach 4 or 5 times less than f_s.

Inductor Current Sensing



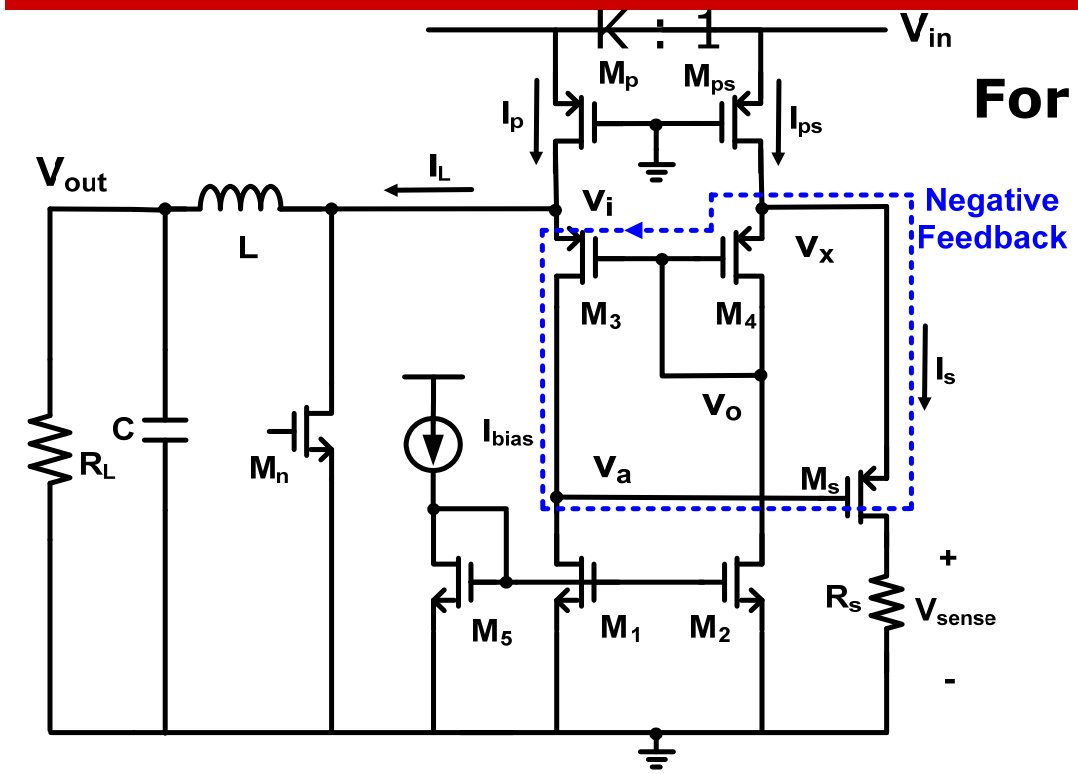
- Speed of inductor current sensing can limit the maximum switching frequency ($f_{s,max}$) and duty ratio range of the converter.
- CMC converter can function properly if the delay (t_d) of the current sensor is smaller than $D_{min} * 1/f_{s,max}$.
- Power dissipation of the current sensor should be minimized.

Sensing Resistor



- Sensing resistor R_{sen} in series with the inductor to provide entire inductor profile.
- If R_{sen} is too small, inductor current cannot be detected in light-load condition.
- If R_{sen} is too large (e.g. 500mΩ), conduction loss of R_{sen} might significantly increase the total power loss.
  - If $i_{L,rms}$ = 1A, the loss due to R_{sen} = 500mW that is not suitable for low-power applications.

Switch Current Sensing for HS Power pMOS



For peak current control in Buck converters

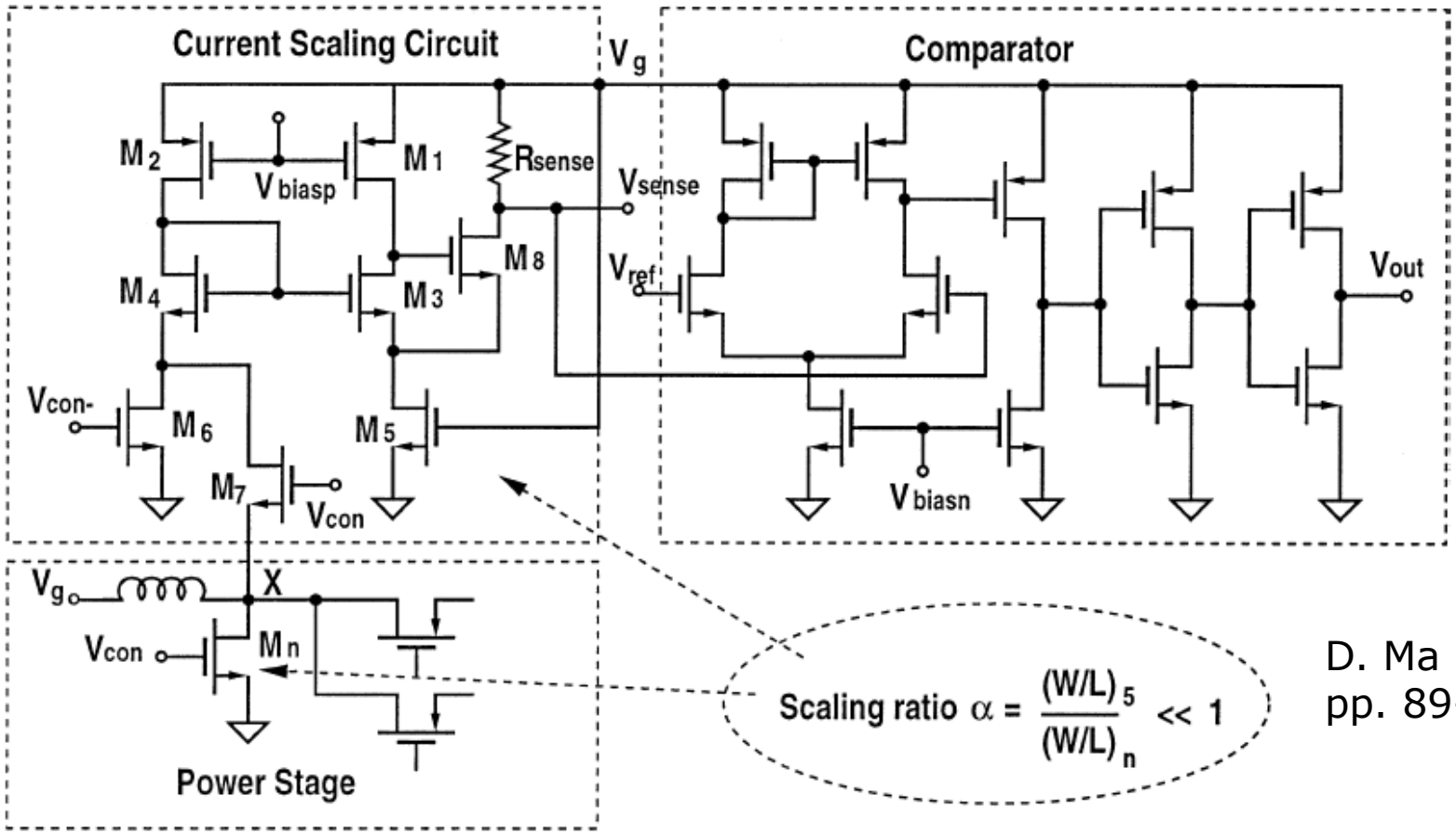
Operation in state DT_s

$$V_{sense} = I_s \cdot R_s \approx \frac{I_p}{K} \cdot R_s = \frac{I_L}{K} \cdot R_s$$

K>>1 and is commonly selected as 1000

- Sensing transistor M_{ps} tracks current through high-side power FET M_P during state 1.
- Since $I_S << I_L$, the switch current sensing is "lossless" compared to the load current.
- The speed of the current sensing is typically limited by the non-dominant pole of the negative feedback loop.

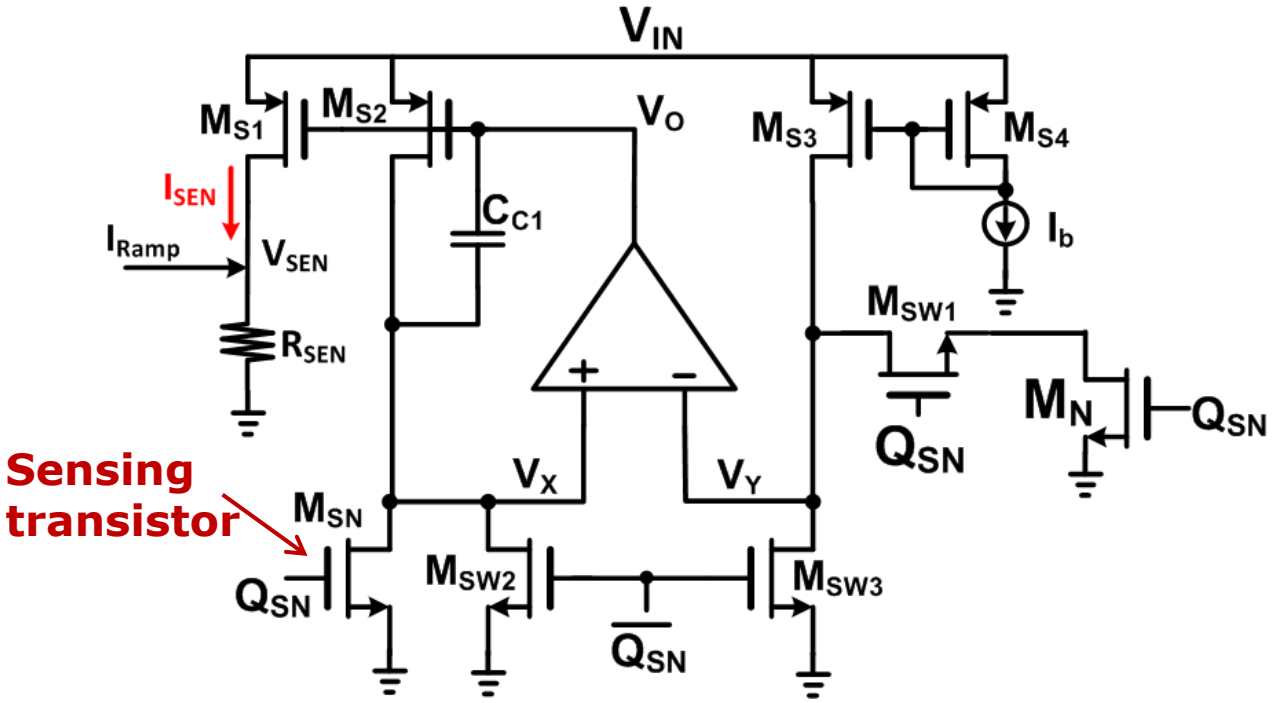
Switch Current Sensing for LS Power nMOS



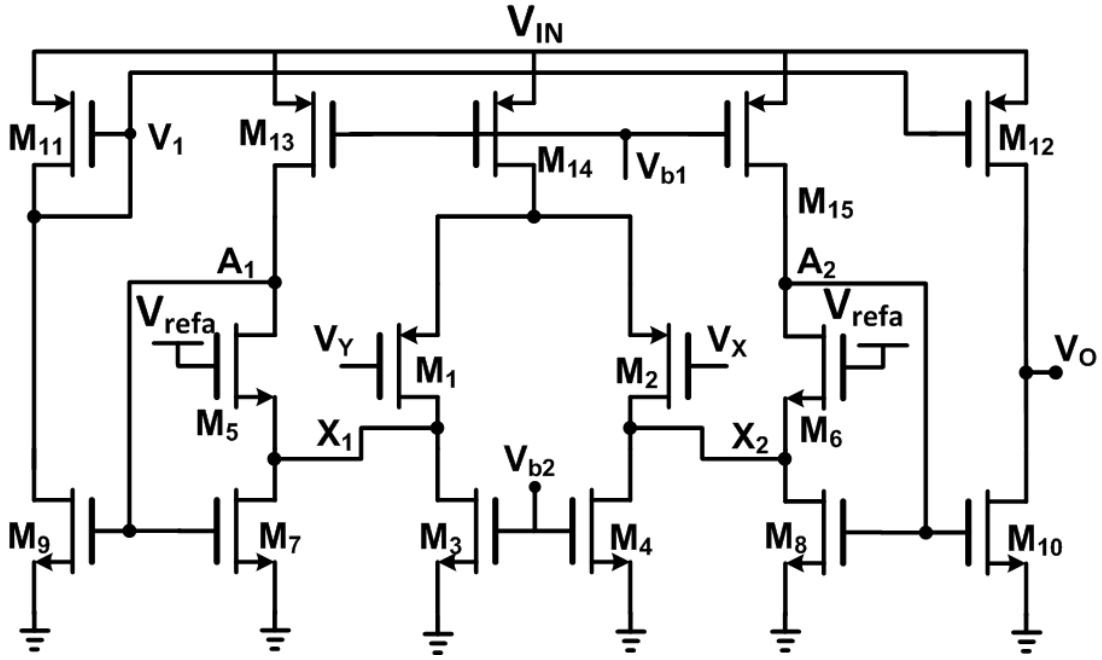
D. Ma et. al., JSSC, Jan. 2003, pp. 89-100.

- Low-side sensing: sensing transistor M_5 tracks current through low-side power nFET M_n during state 1 for the peak current control in Boost converters.

Low-Voltage Switch Current Sensing



Low-voltage current sensor for Boost converters

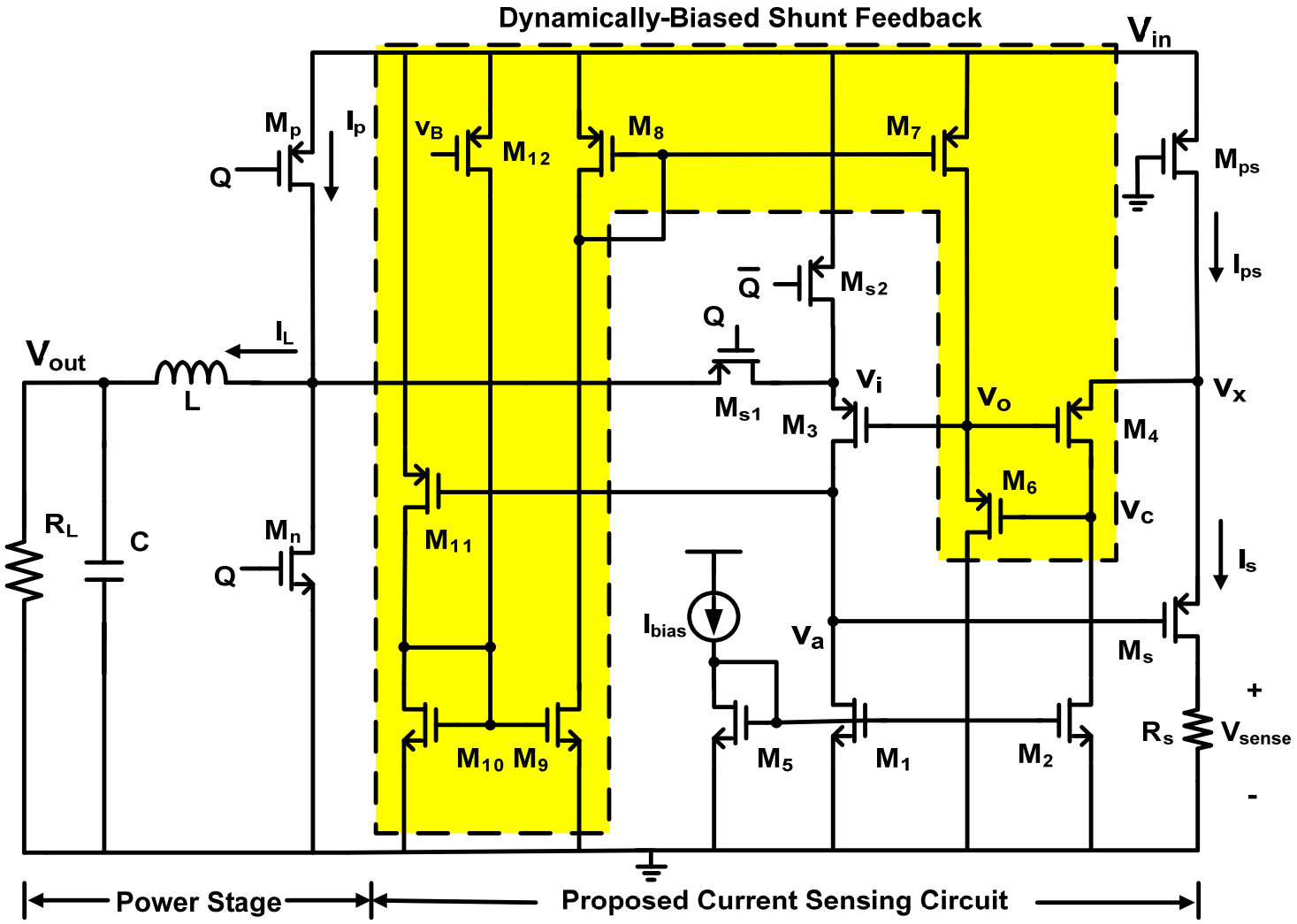


LV error amplifier

- Low-voltage low-side current sensor relies on using a low-voltage error amplifier for obtaining scaled-down sensed current through power nFET M_N.

D. Park et. al., TCAS-II, Aug. 2014, pp. 599-603.

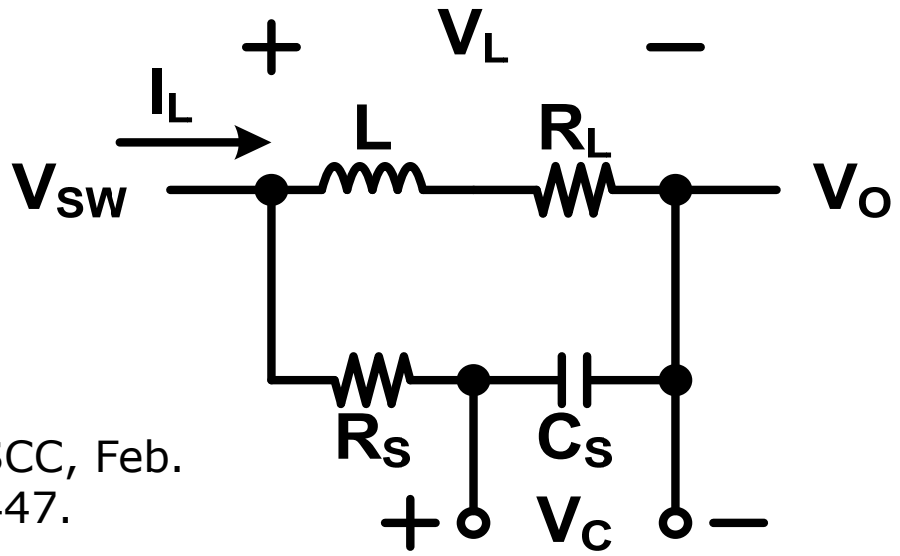
High-Speed Switch Current Sensing



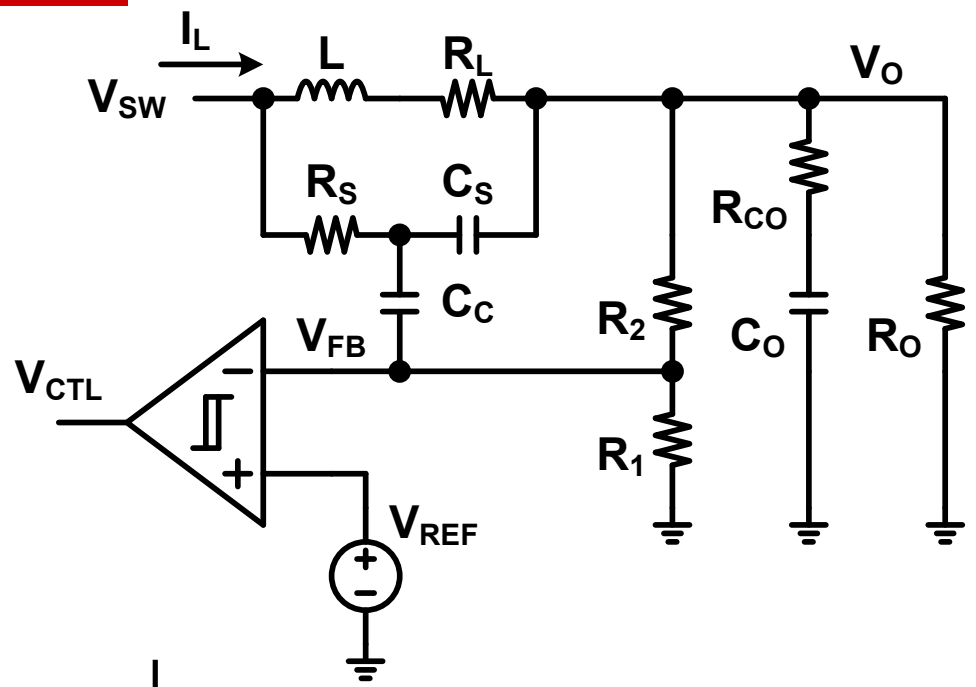
- **Dynamically-biased shunt feedback** uses 7 additional transistors to push the non-dominant pole in the feedback loop to a higher frequency.
- The UGF of the feedback loop is increased, thereby minimizing the sensing delay for higher f_S.

M. Du et. al., TCAS-I, Oct. 2010, pp. 2804-2814.
M. Du et. al., JSSC, Aug. 2011, pp. 1928-1939.

Filter-Based Current Sensing



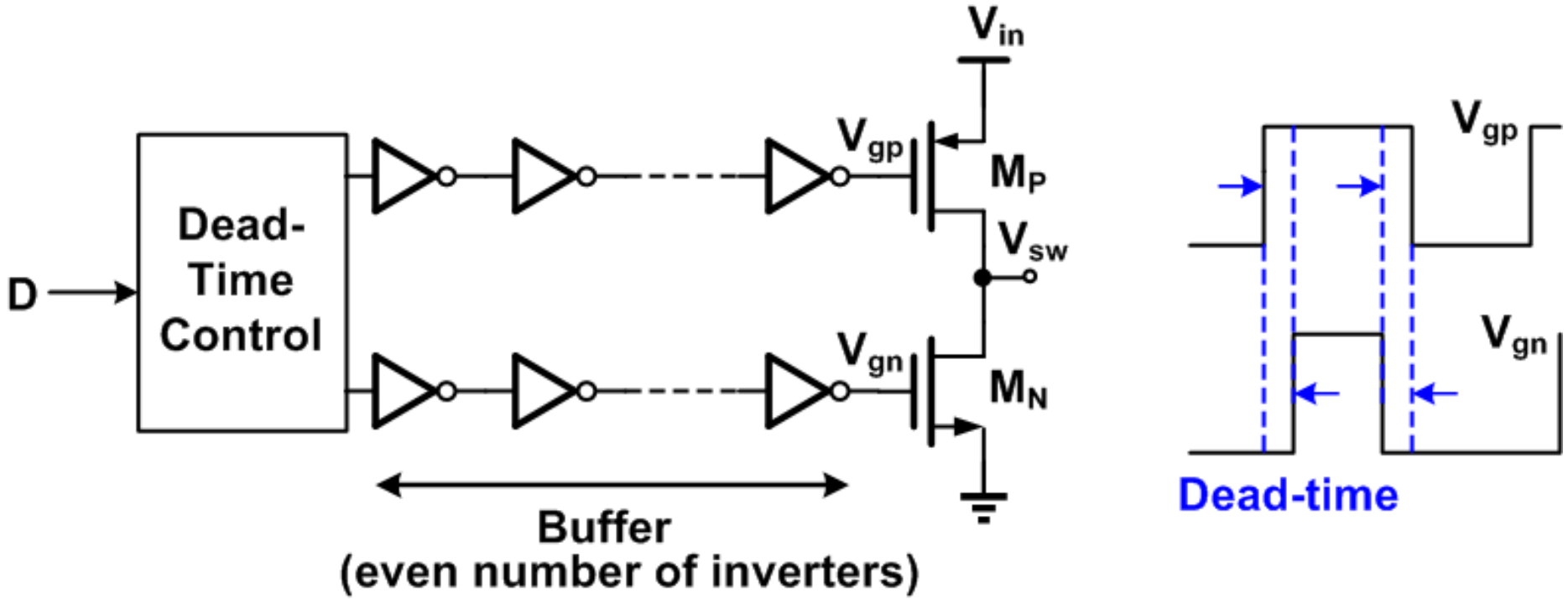
F. Su et. al., ISSCC, Feb. 2009, pp. 446-447.



$$V_C = \frac{V_L}{1+sR_SC_S} = \frac{(R_L+sL)I_L}{1+sR_SC_S} = \frac{1+s(L/R_L)}{1+sR_SC_S}R_LI_L \approx \frac{L}{R_sC_s}I_L \quad \text{if } R_sC_s >> T_s$$

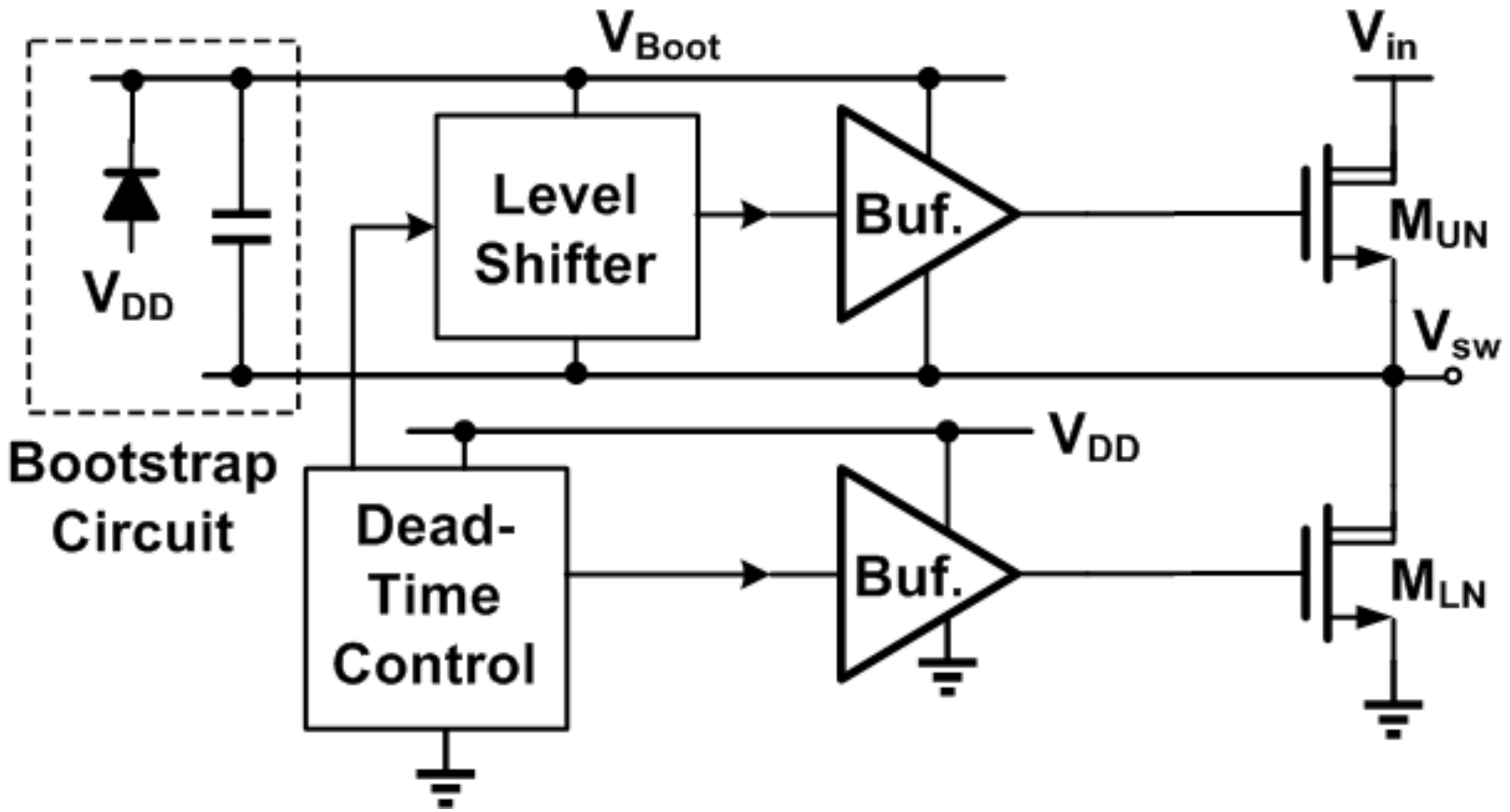
- Capacitor voltage V_C of a lossless low-pass filter formed by R_S and C_S in parallel with the inductor provides inductor current information.
- This current sensor provides high-speed current sensing and is suitable for high-frequency (of over 10MHz) DC-DC converters.

Gate Driver for HS Power pMOS



- Gate driver structure: dead-time control and digital buffers (for LV synchronous converters with a high-side power pMOS and a low-side nMOS).
- Dead-time avoids simultaneous conduction of power transistors during switching transitions, removing the short-circuit loss.

Gate Driver for High-Side Power nMOS (1)

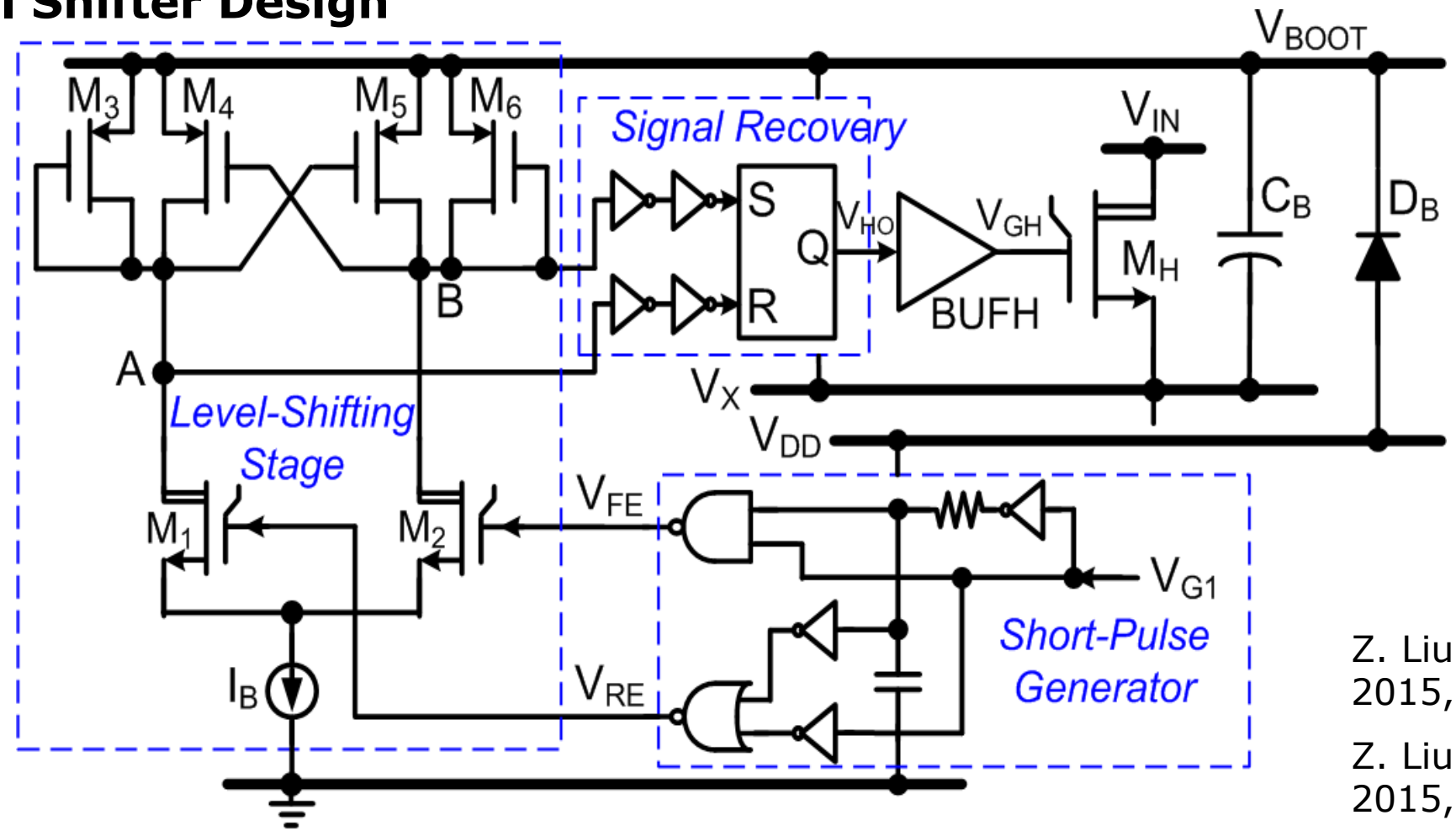


M_{UN} and M_{LN} are HV FETs if V_{in} >> V_{DD}

- With a high-side power nMOS, the gate driver needs to have an additional level shifter and bootstrap circuit.
- Bootstrap supply V_{BOOT} (= V_{IN} + V_{DD}) is realized by a diode and a capacitor.

Gate Driver for High-Side Power nMOS (2)

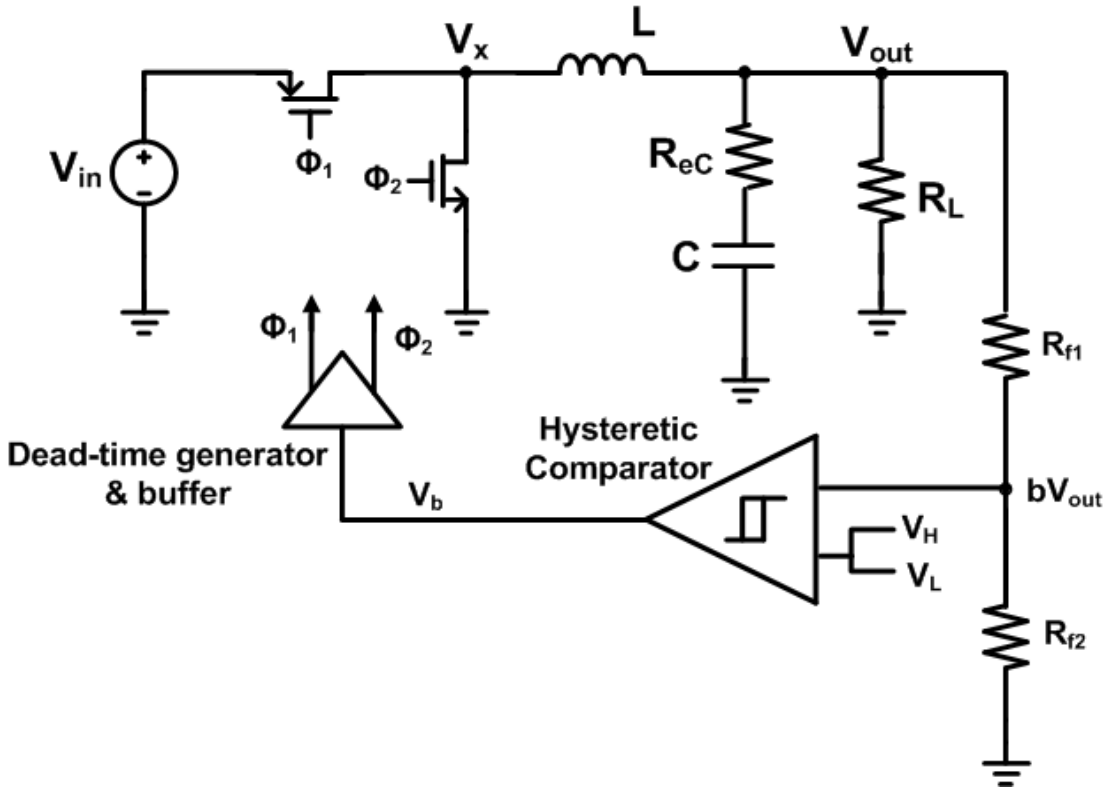
Level Shifter Design

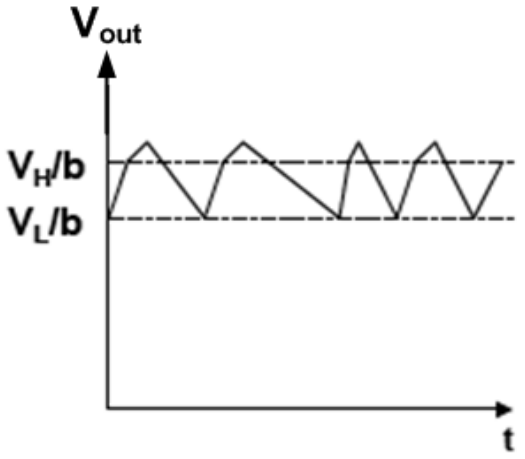


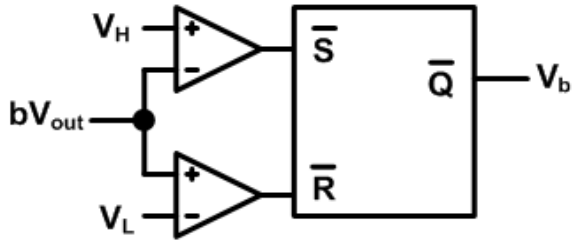
Z. Liu et. al., JSSC, Jun. 2015, pp. 1463-1477.

Z. Liu et. al., JSSC, Sep. 2015, pp. 2174-2187.

Hysteretic Control



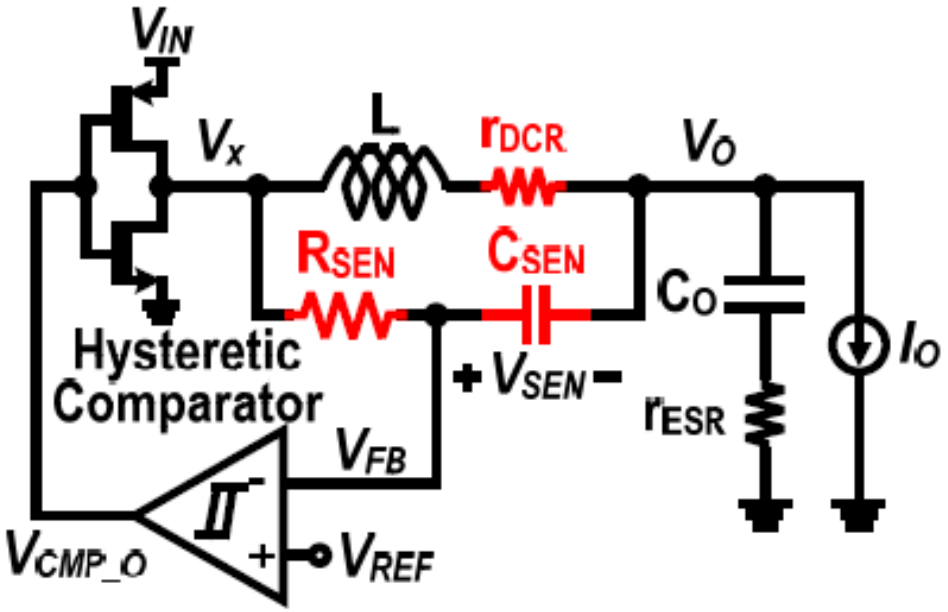




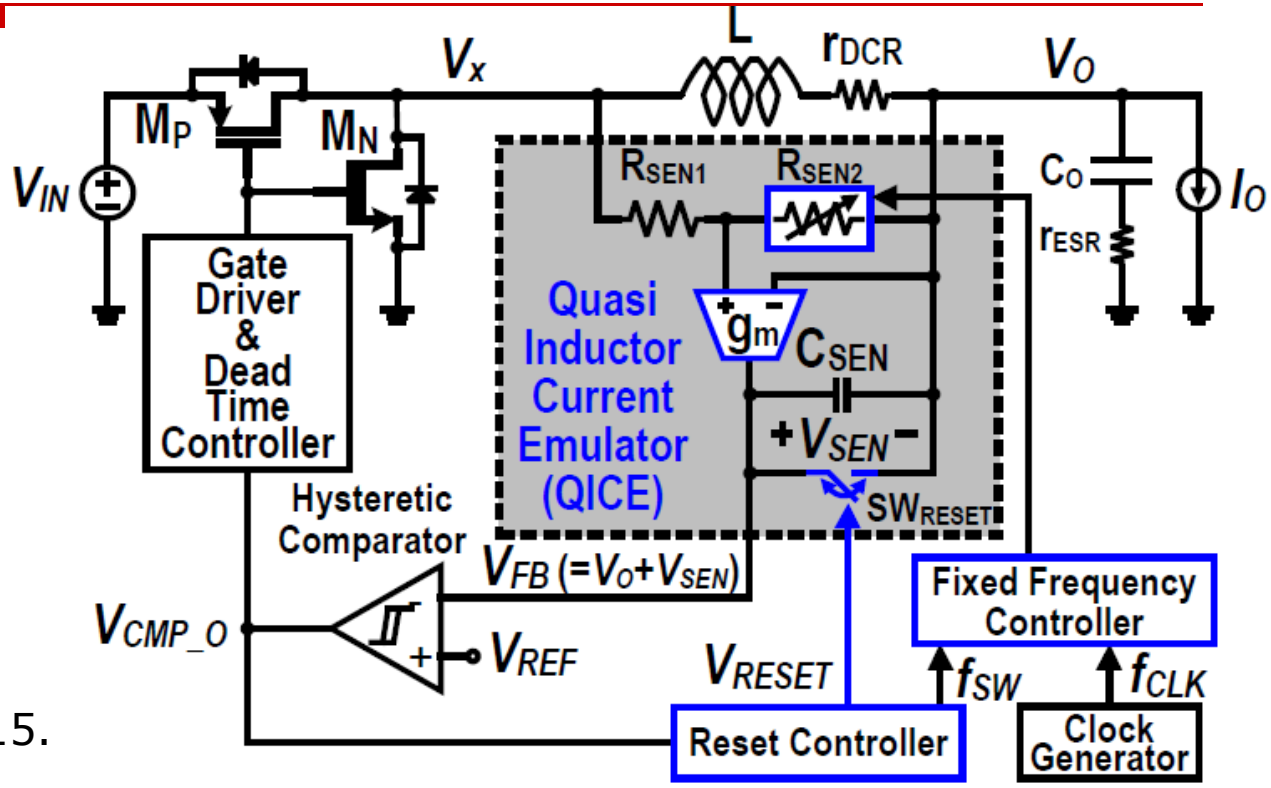
Hysteretic comparator

- Compared to PWM control, hysteretic control improves the converter load transient response without using the bandwidth-limited error amplifier in the controller.
- Cons: large output ripple and unpredictable output noise spectrum with variable switching frequency

Current-Mode Hysteretic Control



S. H. Lee et. al., ISSCC, Feb. 2015, pp. 214-215.



- Current-mode hysteretic control (CMHC) offers smaller output ripple but slower transient response compared to voltage-mode counterpart.
- Quasi-current-mode hysteretic control improves transient response and reduces the required current sensing capacitance C_{SEN} compared to CMHC.

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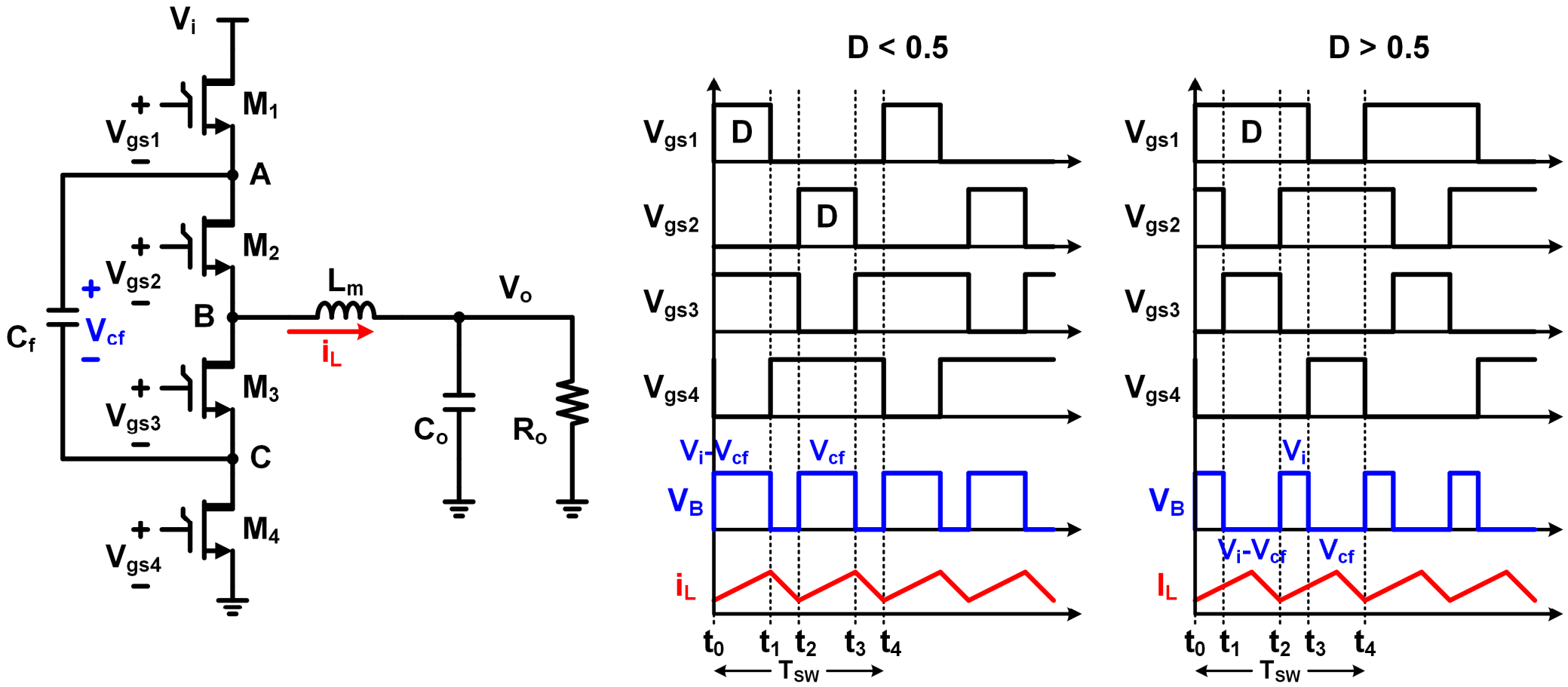
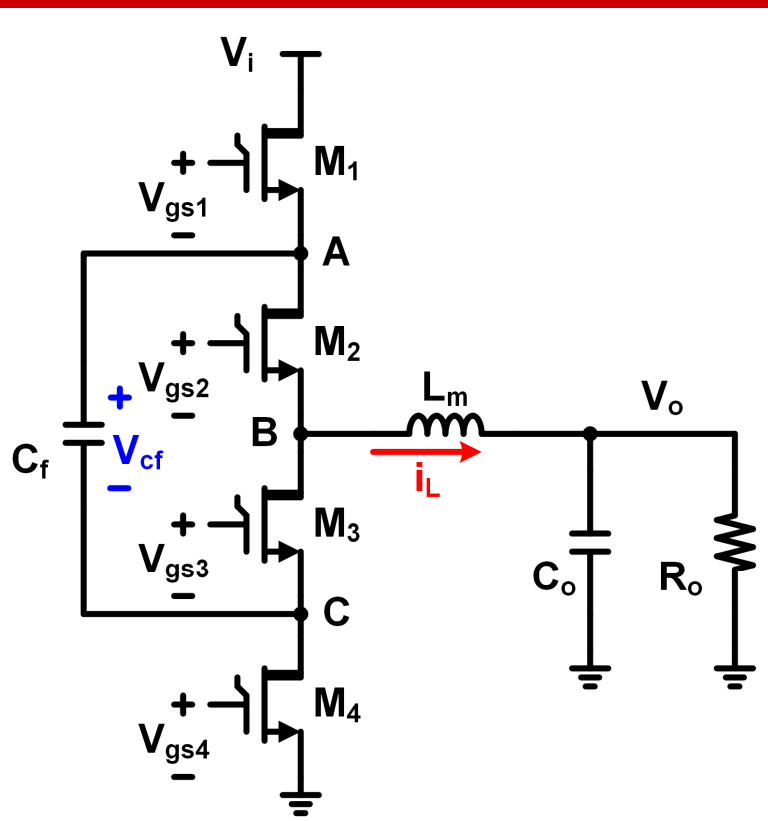
- Advanced Topic
  - Three-Level DC-DC Converter

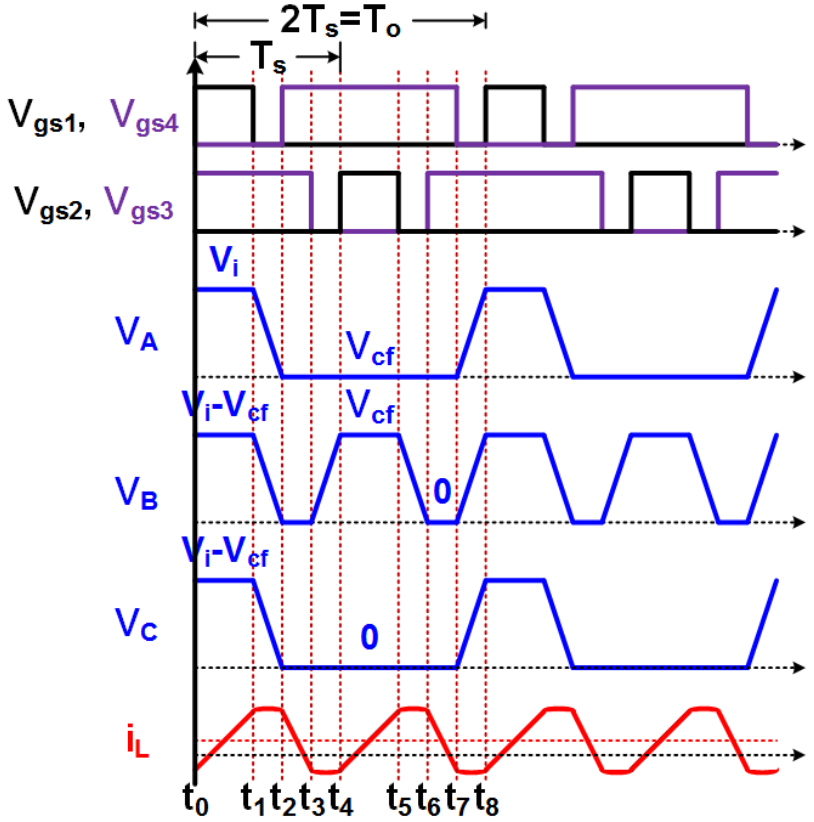
Three-Level DC-DC Converter (1)



- A three-level converter has four power FETs (M_1 – M_4) and a flying capacitor C_f connected between nodes A and C with its voltage $V_{cf} = 0.5V_i$ in the steady state.

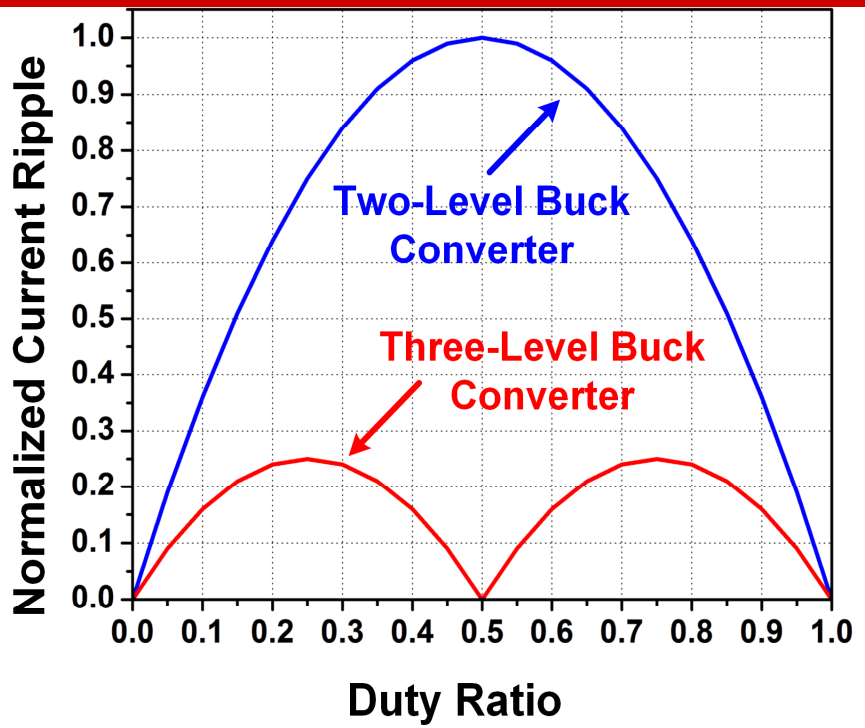
Three-Level DC-DC Converter (2)

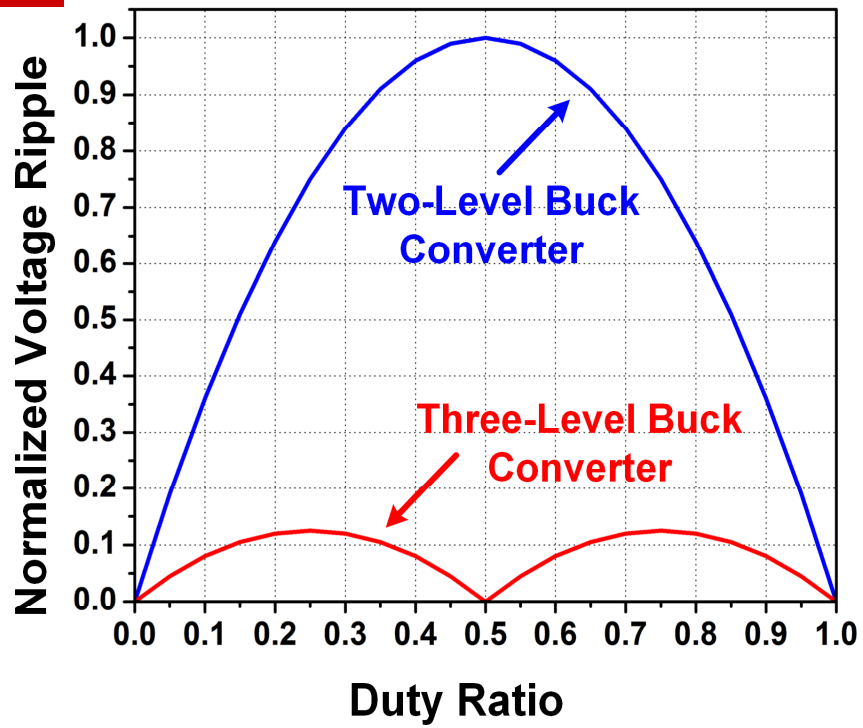




- The frequency of both inductor current and output voltage is 2 times larger than gate drive signals.
- The voltage swing at each switching node is only $V_i/2$ if $V_{cf} = V_i/2$.

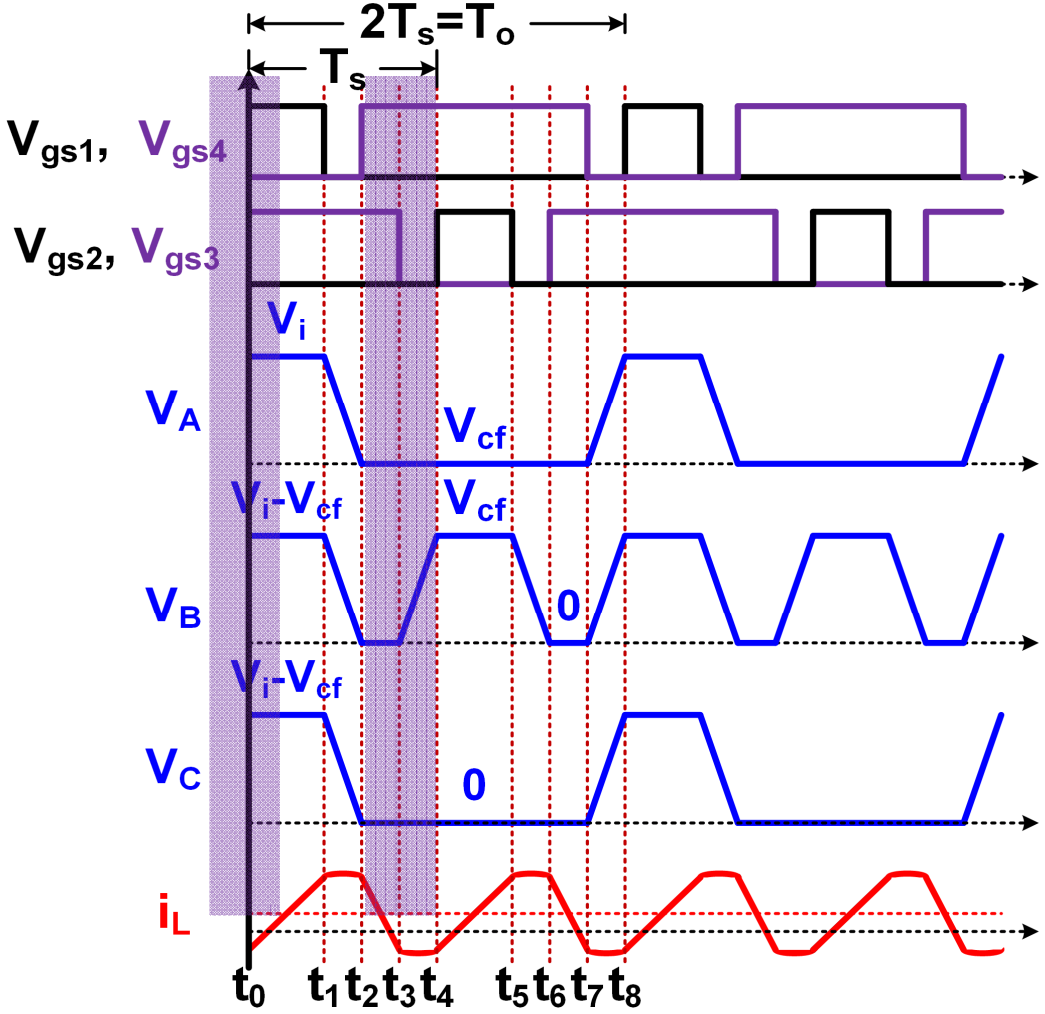
Three-Level DC-DC Converter (3)





- Compared to a two-level converter, the three-level converter
  - reduces the required inductor value by 4 times
  - reduces the required output capacitor value by 2 times
  - reduces the voltage stress across each power switch by 2 times ⇒ smaller-size lower voltage rating power FETs can be used ⇒ suitable for HV applications

Voltage across the Flying Capacitor



- **ΔV_{cf} in charging phase**

$$\Delta V_{cf\_ch} = \frac{I_{L1} \times D_1 \times T_O}{C_f}$$

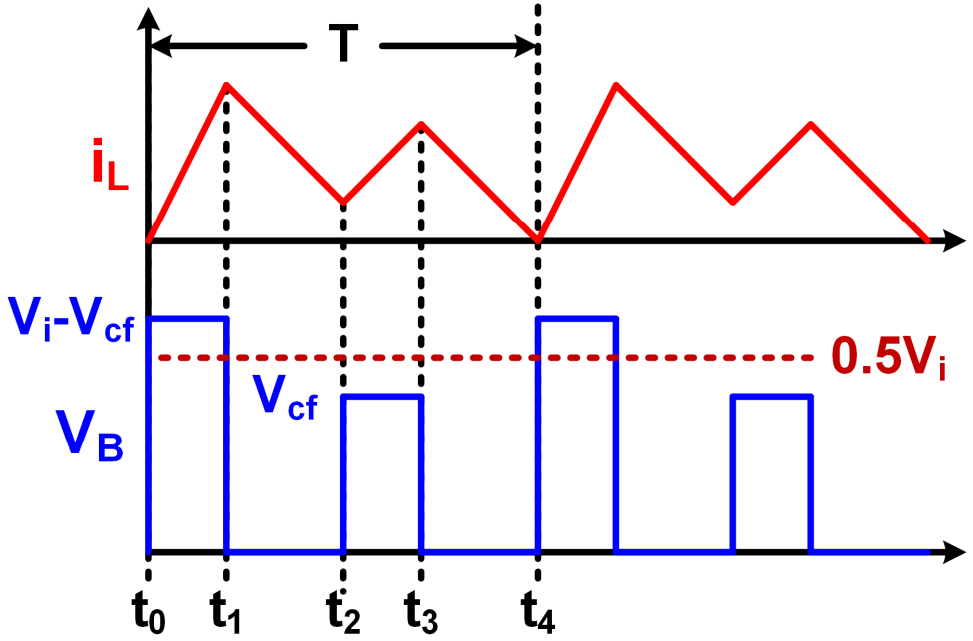
- **ΔV_{cf} in discharging phase**

$$\Delta V_{cf\_dis} = \frac{I_{L2} \times D_2 \times T_O}{C_f}$$

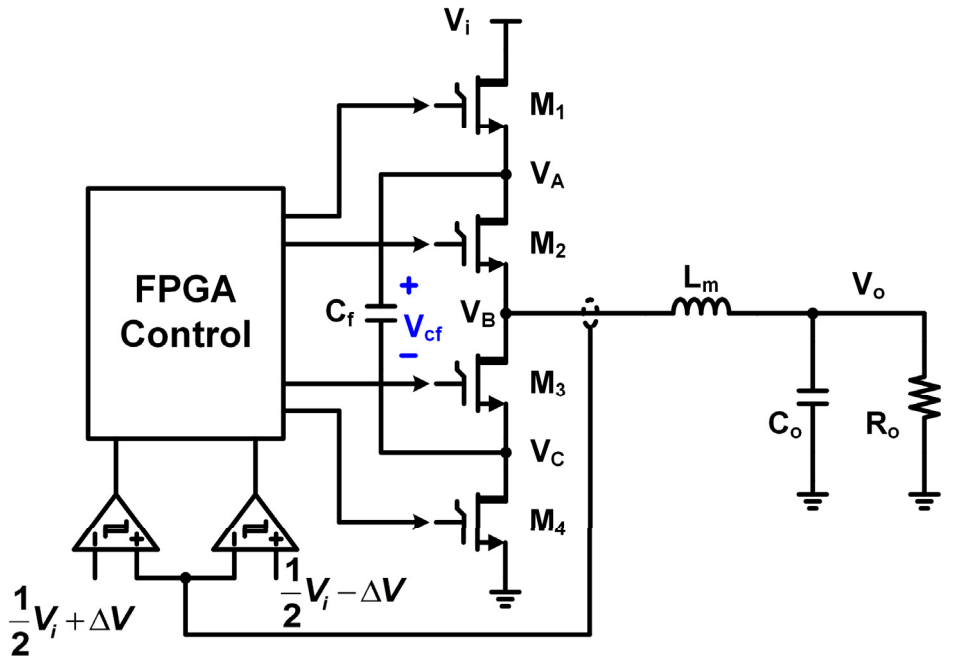
- **ΔV_{cf} in one period T_O**

$$\Delta V_{cf} = \Delta V_{cf\_ch} - \Delta V_{cf\_dis} = \frac{(I_{L1} - I_{L2}) \times D \times T_O}{C_f}$$

Flying Capacitor Balancing



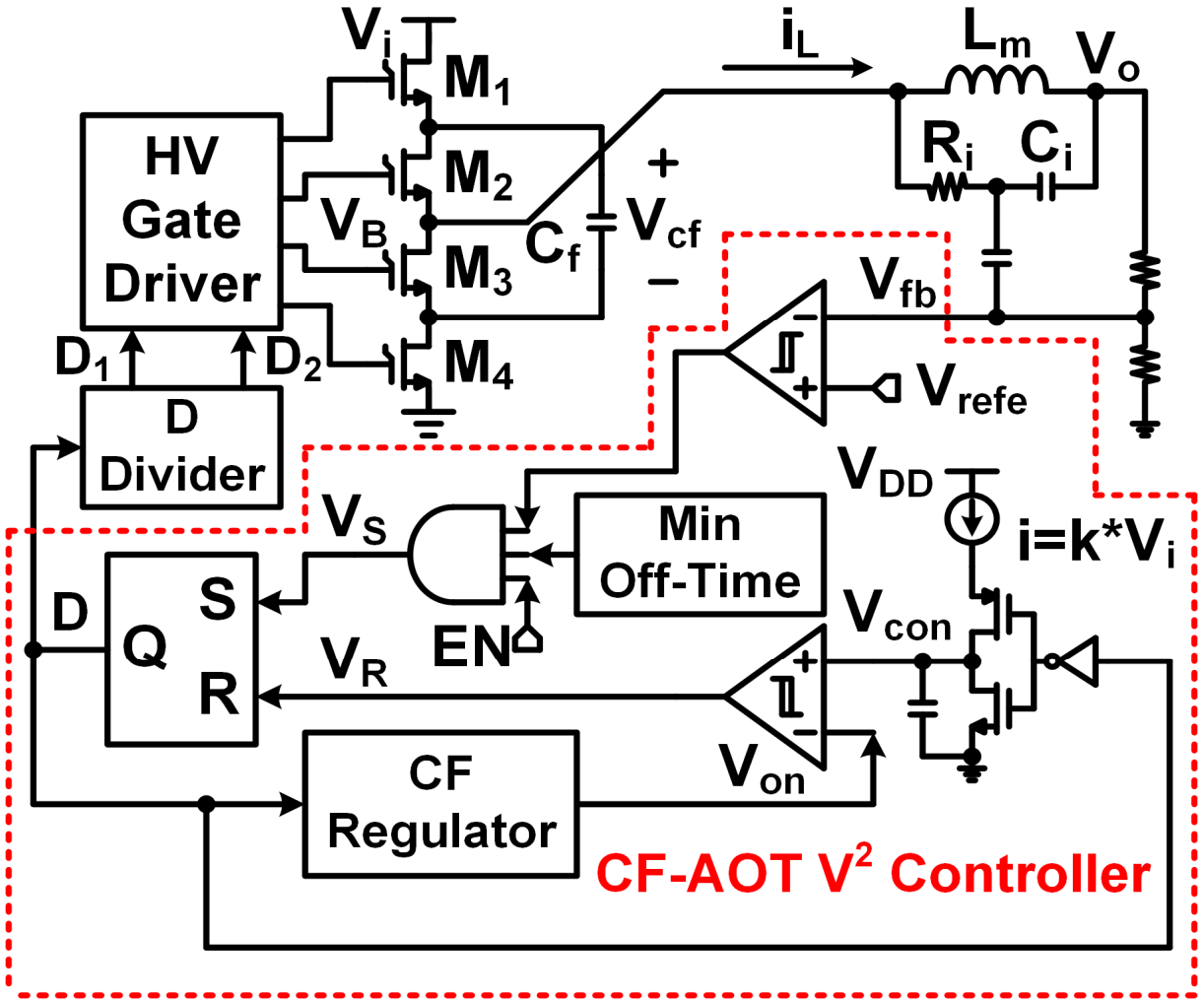
Flying capacitor unbalanced



Control of flying capacitor balancing

- The unbalanced behavior of the flying capacitor would damage the power FETs.
- Comparator-based balancing scheme with two external reference voltages can force V_{cf} close to $V_i/2$, and it is suitable for low-voltage applications.

Flying Capacitor Self Balancing (1)

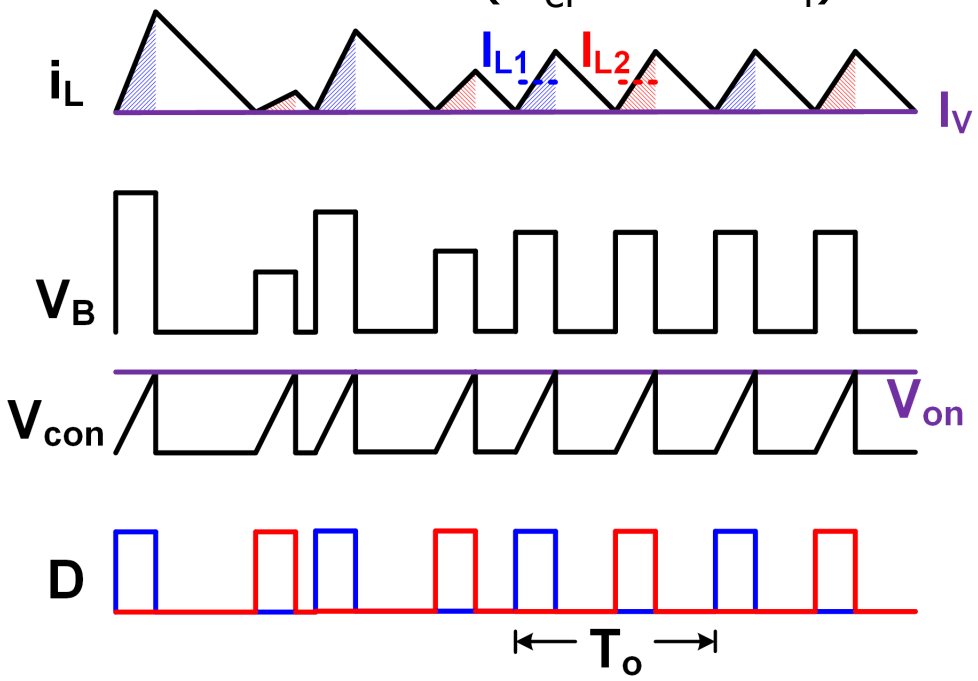


- Self-balancing means that both flying capacitor balancing and output voltage regulation are achieved simultaneously by the same controller.
- By regulating the average inductor current, both V_{cf} and V_o would be regulated automatically.

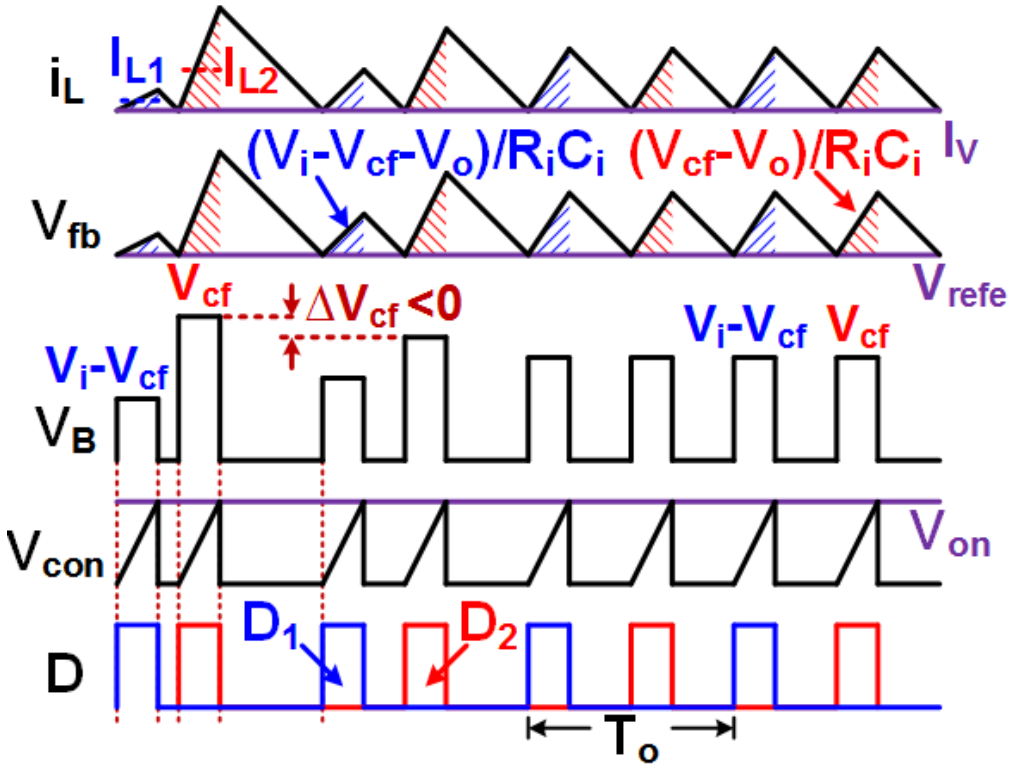
J. Xue et. al., ISSCC, Feb. 2016, pp. 226-227.
J. Xue et. al., JSSC, Dec. 2016, pp. 2854-2866.

Flying Capacitor Self Balancing (2)

- Perturbation ($V_{cf} < 0.5V_i$)



- Perturbation ($V_{cf} > 0.5V_i$)



$$\Delta V_{cf} = \Delta V_{cf\_ch} - \Delta V_{cf\_dis} = \frac{(I_{L1} - I_{L2}) \times D \times T_O}{C_f} = 0$$

- ΔV_{cf} continues to decrease until it equals 0 $\Rightarrow$ the flying capacitor voltage is regulated at $V_{cf} = 0.5V_i$.

Loop Gain of Three-Level Converters

- The loop gain T(s) of the three-level converter

$$T(s) = b \cdot A(s) \cdot \frac{V_{in}}{V_M} \cdot \frac{1}{1 + s\frac{L}{R} + s^2 LC}$$

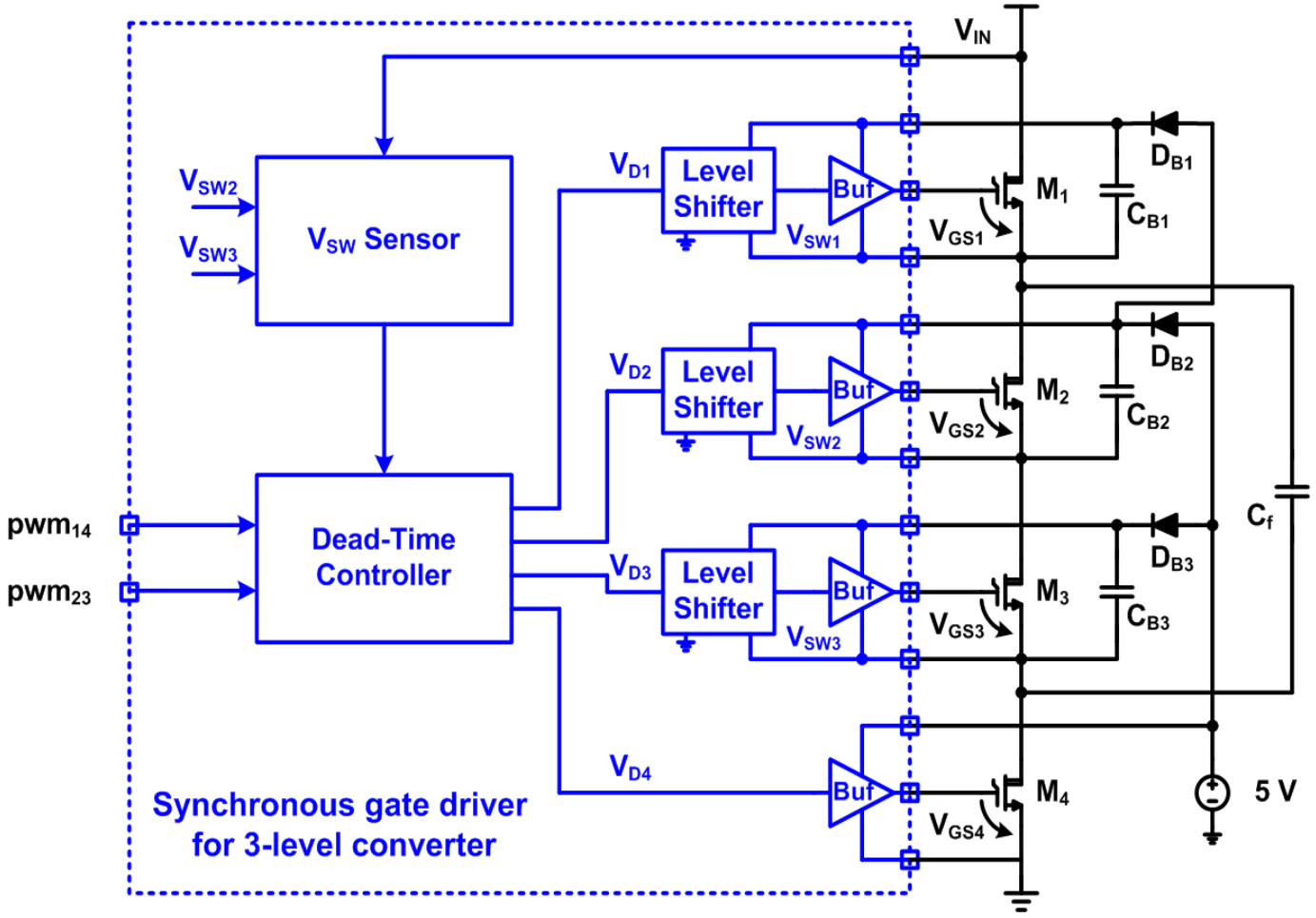
Note: b is the feedback resistor ratio

A(s) is the transfer function of the compensator

V_M is the amplitude of the ramp signal

- The loop gain of the three-level converter is the same as that of two-level converter.
- Same controller type as the two-level converter can be used for the three-level converter.

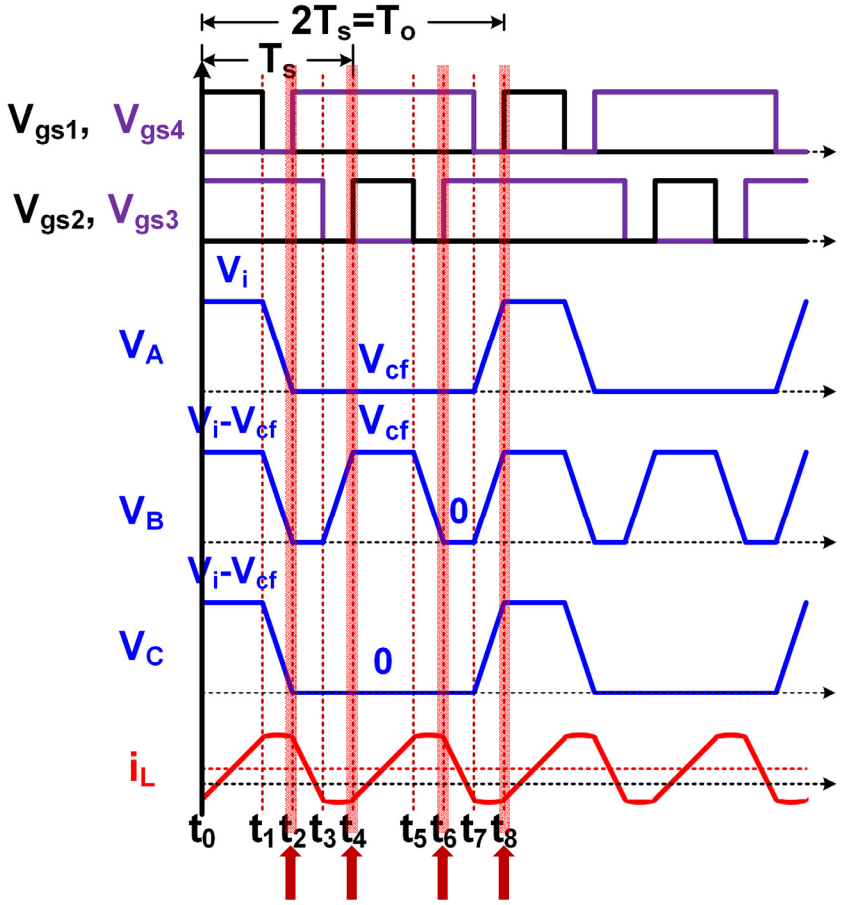
Gate Driver for Three-Level Converters

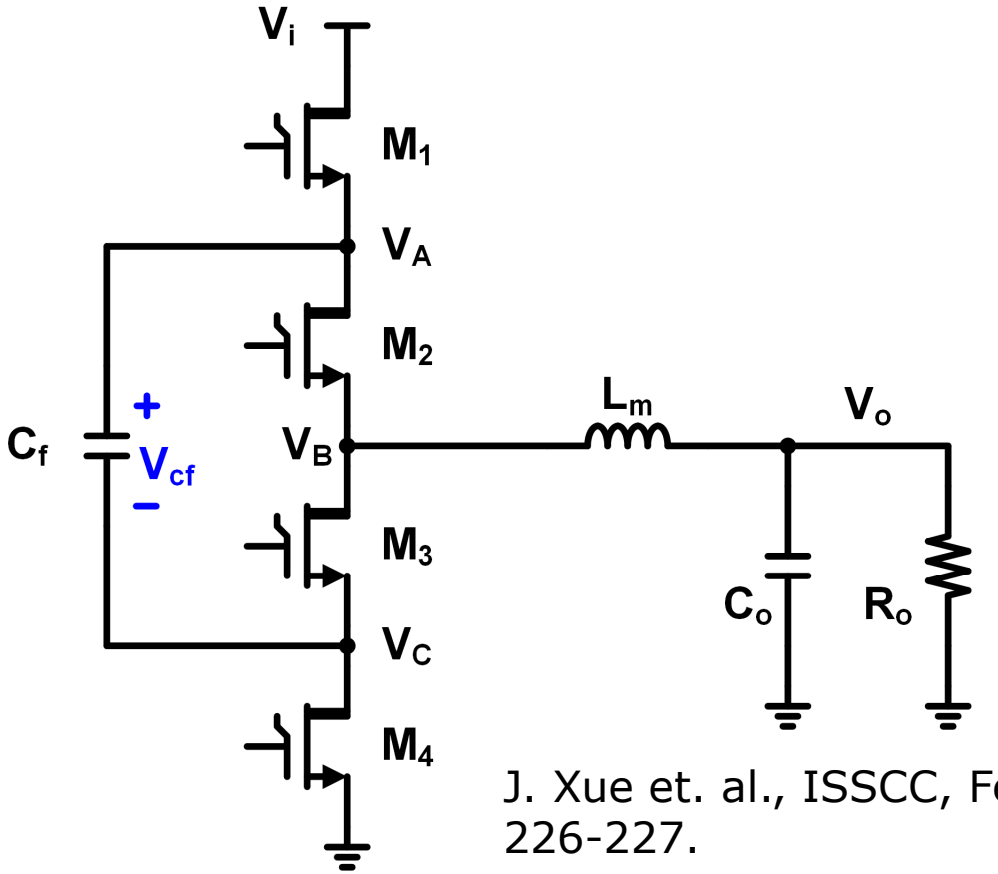


- Driver structure: 3 level shifters, 4 voltage buffers, 3 sets of bootstrap circuitry, and a dead-time controller
- In LV applications, open-loop fixed dead-time is used to remove the shoot-through current of power FETs and V_{SW} sensor is not necessary.

L. Cong et. al., ECCE, Sep. 2015, pp. 1479-1484.
J. Xue et. al., APEC, Mar. 2015, pp. 451-454.

Example: 100V Three-Level DC-DC Converter (1)

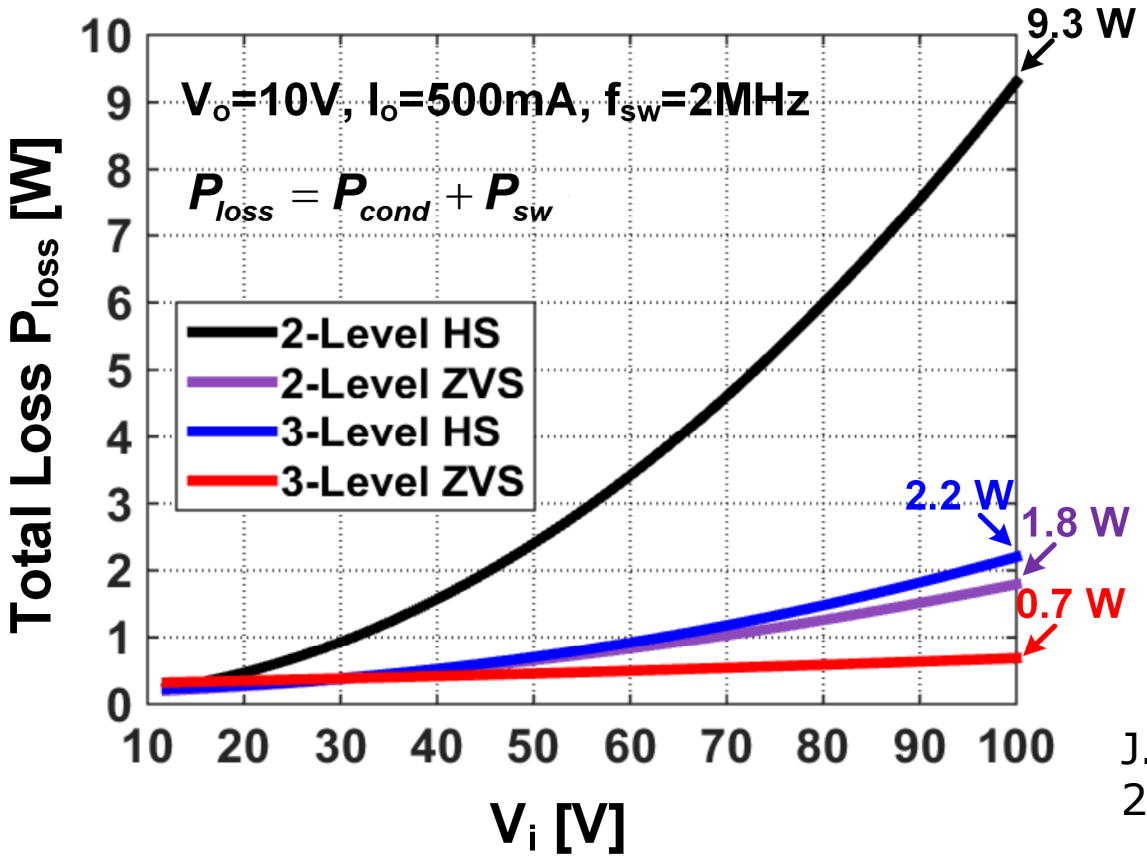




J. Xue et. al., ISSCC, Feb. 2016, pp. 226-227.

- In high-input applications, all power FETs can realize ZVS during turn-on with negative inductor current using a small-size inductor.

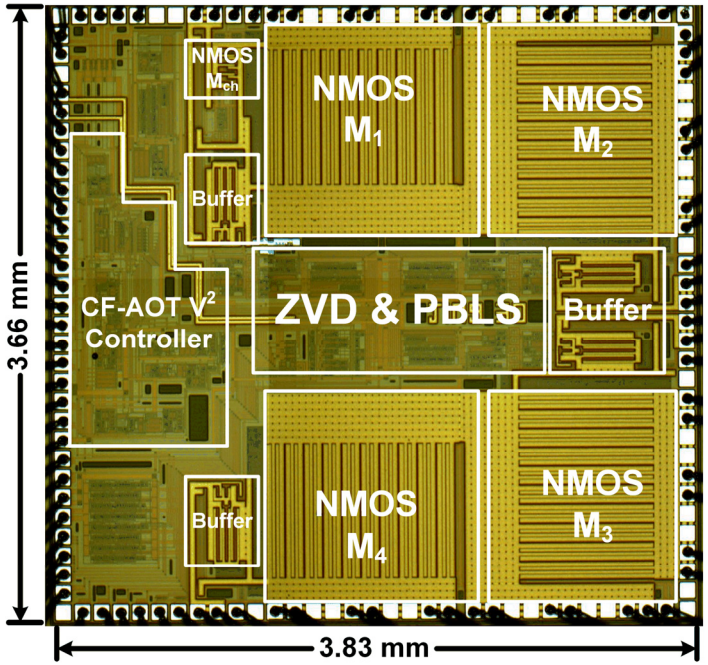
Example: 100V Three-Level DC-DC Converter (2)



J. Xue et. al., JSSC, Dec. 2016, pp. 2854-2866.

- The three-level ZVS converter has the lowest power loss under high inputs
  - 13 times reduction compared to the two-level hard switching converter at V_i = 100V
  - 2.6 times reduction compared to the two-level ZVS converter at V_i = 100V

Example: 100V Three-Level DC-DC Converter (3)



0.5-µm 120-V AMS CMOS process

	TI LM5007	This Work
Process	N. A.	**0.5-µm 120-V CMOS**
Topology	Two-Level, Asyn.	**Three-Level, Syn.**
Power FETs Stress	V_i	**$0.5V_i$ (V_i = 26 V – 100 V)**
Input Voltage (V)	12 – 75	**12 – 100**
Output Voltage (V)	10	**10**
Output Power (W)	4	**5**
Duty Ratio	0.13 – 0.83	**0.11 – 0.83**
Capacitor Balancing	N. A.	**Yes, Self Balancing**
Switching Operation	Hard	**ZVS**
Frequency (MHz)	~ 0.4	**~2**
Frequency Variation	± 3.8%	**± 0.55%**
L	100 µH	**1.5 µH**
C	15 µF (C_o)	**4.7 µF (C_o) + 1 µF (C_f)**
Peak Power Efficiency (Frequency)	86% @ V_i = 50 V, 83% @ V_i = 70 V (0.4 MHz)	**90% @ V_i = 48 V, 86% @ V_i = 72 V, 83% @ V_i = 100 V, (2 MHz)**

Summary

- Switched-mode power converters are the most popular DC-DC converters for high-efficiency voltage conversion
  - Power topology characteristics with CCM vs DCM operation
  - Power loss analysis and efficiency-enhancement techniques
  - Passive selection strategy
  - Voltage-mode PWM control and its frequency compensation strategy
  - Current-mode PWM control and its frequency compensation strategy
  - Current sensor design
  - Hysteretic control
- Advanced material: Three-level DC-DC converter
  - Topology characteristics
  - Flying capacitor balancing and gate driver structure

Related Papers in ISSCC 2018

- **High-voltage DC-DC Converter: Paper 24.1**

L. Cong, H. Lee, "A 2MHz 150-to-400V Input Isolated DC-DC Bus Converter with Monolithic Slope-Sensing ZVS Detection Achieving 13ns Turn-on Delay and 1.6W Power Saving," ISSCC 2018.

- **Low Voltage Ripple Step-Up Converter: Paper 27.5**

S. U. Shin, et. al., "A 95.2% Efficiency Dual-Path DC-DC Step-Up Converter with Continuous Output Current Delivery and Low Voltage Ripple," ISSCC 2018.

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- J. Xue and H. Lee, "A 2MHz 12V - 100V 90%-efficiency self-balancing ZVS reconfigurable three-level DC-DC regulator with constant-frequency adaptive-on-time V^2 control and nanosecond-scale ZVS turn-on delay," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 12, pp. 2854 – 2866, Dec. 2016.
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