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Tutorial 8

Fundamentals of Switched-Mode Power-Converter Design

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1. (Slide 1) Introduction

Good afternoon everyone, I'm glad to be here to present you with the fundamentals of the switched-mode power converter design.

2. (Slide 2) Why DC-DC Converters?

DC-DC converters are essential in today's portable devices like smartphones, DVD players, and notebooks. The energy source in the portable devices is mainly battery, like the lithium-ion battery, the voltage will change from 2.7V to 4.2V.

At the same time, there are different electronic subsystems in the portable devices. Those electronics subsystems also have their own supply voltage requirements. For example; the analog subsystems may require the V_{DD} to be 1.8V, the digital part may need to have the supply voltage to be 0.9V, the RF part needs to have the supply to be 5V, and the interface part will need the 1.2V supply.

DC-DC converters convert the time varying battery voltage to different regulated voltages to satisfy the supply voltage requirements of different electronic subsystems. So while doing the voltage conversion, the DC-DC converters will also need to be power efficient.

To quantify this metric, we like to use power efficiency. The power efficiency is defined as the output power over input power. So the power efficiency of an ideal DC-DC converter will be 1 or 100 %.

3. (Slide 3) Types of DC-DC Converters

There are three different types of the DC-DC convertors: the LDOs, the switched-mode power converters, and the switched-capacitor power converters. In the LDO, there exists a power transistor. It is modeled as variable resistor, on the left diagram, connected between input and output.

During the operation, the power transistor is always on, so the LDO is a continuous-time system.

Switched-mode power converters use power switches and inductors for voltage conversion. The inductor is used to store energy, the power switches will turn on and off during a switching period; therefore the switched-mode power converter is a sampled-data system.

Similarly, the switched-capacitor power converter is also a sampled-data system, by using the power switches and the capacitor for voltage conversion.

The capacitors in the switched-capacitor power converters are used to store energy.

4. (Slide 4) Low Dropout Regulator

The left diagram shows the structure of an LDO; it consists of a power transistor PMOS; two feedback resistors, R_{f1}, R_{f2}, output capacitor C, the load resistor R_L, and the error amplifier.

The error amplifier compares the scale down output voltage with the reference V_{ref} to adjust the on-resistance of the power transistor, such that the output voltage can be regulated to a fixed value.

The selection of the power transistor in the LDO is important to the power efficiency, since the output current in the LDO is approximately equal to input current, so the power efficiency can be expressed using this equation which is approximately equal to output voltage divided by the input voltage. So in other words, the smaller the difference between the output voltage and the input voltage, the better the power efficiency will be.

The selection of the PMOS in the LDO can minimize the voltage difference between the output voltage and the input voltage; therefore the power efficiency of the LDO can be maximized.

As mentioned before, the LDO is a continuous-time system, so the output voltage has no noise, and also the only potential limitation on the application for the LDO is that the output voltage is always smaller than the input voltage.

5. (Slide 5) Switched-Capacitor Power Converters (1)

Switched-capacitor power converters on the other hand, can provide the generator output that is higher, lower, or opposite polarity as compared to the input voltage. These three diagrams illustrate three specific examples that can generate an output voltage that is two times the input voltage, half the input voltage and the negative of the input voltage. This is done by different connections of the power switches and the capacitors.

This is actually done by using the power switch and capacitor as well as the two phase non-overlapping clock signals.

6. (Slide 6) Switched-Capacitor Power Converters (2)

To understand the operation of the switched-capacitor power converter, we can use a circuit model as shown on the left hand side. It consists of a transformer with the turn ratio N:M. The term ratio N:M represents the conversion ratio from input to output with the conversion ratio as N over M. The model also consists of R_0 which is the effective output resistance in the power stage. R_L is the load resistance of the converter. With this model, we can derive the output voltage which is given by this equation.

In order to do the output regulation, we can adjust the output resistance R_0 by using a controller. However if we consider the power efficiency of the switched-capacitor power converter, we can find out that the ideal power efficiency can be expressed as V_{out} over V_x. V_x is the node in this part (model of SCPC); therefore the power efficiency also depends on the output resistance. If you adjust the output resistance to regulate the output voltage, the power efficiency of the switched-capacitor power converter will suffer. The only way to achieve the lossless output regulation is through adjusting the turn ratio or the conversion ratio N/M in the power stage.

The two diagrams to the right, shows that the number of power switches and capacitors for realizing four conversion ratios is much larger than the number of power switches and capacitors for simply realizing a single fixed ratio converter.

Therefore, there is a trade-off between the power efficiency and the converter area for achieving the output regulation. This is a very hot research topic in switched-capacitor power converters, developing area and power efficient power stages.

7. (Slide 7) Switched-Capacitor Power Converters
Switched-mode power converters use power switches and inductors for voltage conversion. These two diagrams illustrate the two most commonly used topologies for portable applications. The buck converter is for step-down voltage conversion. The boost converter is for step-up voltage conversion.

The switched-mode power converter can provide a continuous conversion ratio between input and output by simply controlling the timing of the power switches; therefore the required number of power switches in the switched-mode power converter will be much smaller than that in the switched-capacitor power converter.

8. (Slide 8) Characteristics of DC-DC Converters
This table provides the advantages and the disadvantages of different types of DC-DC converters.

For example, the switched-mode power converter can provide the highest power efficiency and different types of the voltage conversion; however the inductor cost would be slightly higher than the cost of the capacitors.

9. (Slide 9) Outline
After this slide, we will only focus on the switched-mode power converters. The first part we will talk about is mainly the switched-mode power converter basics and some of the design considerations in the power stage.

10. (Slide 10) SMPC Basics
This shows the basic operation of the switched-mode power converter using the buck converter for illustration. In the buck converter, there are two power switches: the high-side power switch, S, and the low-side power switch realized by a diode. So when the high-side switch is on, V_x , the switching node voltage, equals to the input voltage.

When the switch is off, the switching node voltage equals to 0, so we can draw the switching node voltage versus time in this diagram. There is also a low-pass LC filter connected between the switching node, $V_{x,}$ and the output. The function of the low-pass filter is to try to get the average value of the switching node voltage to become the output voltage.

The larger the turn on time of the high-side switch or the larger the duty ratio, the higher the output voltage. I should mention that the duty ratio in the switched-mode power converter is defined as the turn on time of the high-side switch divided by the switching period.

11. (Slide 11) DC-DC Topologies of SMPC
There are four different converter topologies in switched-mode power converters. If the output voltage is always lower than the input voltage, we can implement the buck converter with only two power switches and one inductor. If the output voltage is higher than the input voltage, we can implement the boost converter. If the output voltage needs to have an opposite polarity to the input voltage, we can use the flyback converter. If the system requires a output voltage that is within the input voltage range, for example, if the output voltage needs to be 3.5V for an input voltage varying from 2.7 to 4.2V. In this case, we have to use the non-inverting flyback converter. The non-inverting flyback converter has two additional power switches compared to the buck or boost topology.

12. (Slide 12) Continuous Conduction Mode

In switched-mode power converters, since the inductor is used to store energy, the inductor current profile is a very good indicator, reflecting the operational state of the converter. Continuous conduction mode means that the varying conductive current is always larger than 0. The inductor current in the existing switching period will be continuously connected to the next switching period.

The continuous conduction mode occurs when the average inductor current is larger than two times the current ripple, and CCM can apply to all the different topologies in the switched-mode power converters.

13. (Slide 13) Buck Converter in CCM

Now we will use the volt-second balance to derive the voltage conversion ratio of the buck converter in CCM. The volt-second balance is essentially the conservation of the magnetic flux, flux change associated with the inductor in the two operation states.

In state 1, when ϕ_1 equals to 1, the high-side switch is turned on, so the voltage across the inductor equals to (V_{in} - V_{out}), so the volt-second in state 1 is equal to [(V_{in} - V_{out}) * DT].

In state 2, when ϕ_2 equals to 1, the voltage across the inductor equals to -V_{out}, so the volt-second magnitude in state 2 equals V_{out} * (1-D) * T. Based on volt-second balance, we find the voltage conversion ratio, V_{out}/V_{in}, is D.

14. (Slide 14) Boost Converter in CCM

Similarly, we can also use the volt-second balance to find out the voltage conversion ratio in the boost converter. The volt-second balance in state 1 of the boost converter, equals to (V_{in} * D) and the volt-second in state 2 equals to [(V_{out} - V_{in}) * (1-D) * T].

So from here, we find that V_{out}/V_{in} the boost convertor equals to 1/(1-D). Because D is a number between 0 to 1, so with this conversion ratio, we know that V_{out}/V_{in} is always larger than 1, which means the boost converter can provide step-up voltage conversion.

15. (Slide 15) Flyback Converter in CCM

Similarly, we can use in a volt-second balance to find out the voltage conversion ratio for the flyback converter, and that is given as -D/(1-D).

The negative sign means that V_{out} and V_{in} will be opposite in polarity. We will simply focus on the magnitude. When the duty ratio D is less than 0.5, we find that V_{out}/V_{in} is larger than 1, meaning that it provides a step-up conversion. When the D is larger than 0.5, then the V_{out}/V_{in} magnitude will be less than 1, and the converter provides a step-down conversion.

16. (Slide 16) Discontinuous Conduction Mode

When the load current of the converter decreases, the average inductor current also decreases, so the whole inductor current profile will shift down.

When the average inductor current is smaller than two times the inductor current ripple, the converter will enter DCM, discontinuous conduction mode. In DCM, there's a third state within the switching period.

In S3, both power transistors will be turned off and the inductor current equals 0. We can still use the volt-second balance to derive the voltage conversion ratio of the converter in DCM, but the volt-second balance can

only be appled in the first two states when the inductor current is larger than 0, because of that reason, the voltage conversion ratio is not only a function of the duty ratio, but also a function of the inductance, load resistance, as well as the switching period.

17. (Slide 17) Performance Requirements of SMPC Design

This slide provides the performance requirements of the switched-mode power converter design. In order to have high power efficiency, we need to minimize all the power losses in the power stage, because the power stage handles a large current.

For reducing the converter size and achieving a low-cost, we can implement all the power transistors on-chip, and also minimize the required values of the passive components, inductors and capacitors, by increasing the switching frequency of the converter.

In order to achieve high output voltage accuracy, we can improve both line and load regulation, as well as minimize the output voltage ripple relative to the DC output voltage.

For achieving fast load transient response of the converter, we need to improve the speed of the controller and increase the slew rate of the inductor current.

18. (Slide 18) Asynchronous vs Synchronous Power Stage

For power efficiency optimization, the first question we need to consider is whether we need to be using the asynchronous or the synchronous power stage. The left diagram shows the asynchronous power stage. It has a low-side power switch implemented by a diode.

The advantage of the asynchronous power stage is that when the high-side power switch is turned off, the diode will be automatically turned on. However if you consider the power efficiency by including the losses of the diode only, we find that the maximum achievable efficiency of the converter, is given by this equation.

If we simply focus on the denominator, we will find that if the diode voltage occupies a significant portion of the output voltage, the maximum power efficiency will drop.

For example, if the V_{in} is 3.6V, V_{out} is 1.5V, and the diode drop is 0.7V, the maximum achievable power efficiency is only 79%.

In order to improve the power efficiency, we have to use the synchronous power stage. The synchronous power stage implements the low-side power switch by using a NMOS transistor.

The idea is that we need to design a very large sized NMOS transistor, such that the
voltage drop across the NMOS transistor will be much smaller than the diode voltage drop.

The challenge of using the synchronous power stage is the requirement of dead time. The dead time is necessary to prevent both power transistors from turning on simultaneously during the switching transition, so the converter can be free of short circuit power loss.

19. (Slide 19) Losses in Synchronous Buck Converters

This diagram summarizes all the power losses in the synchronous buck converter. Regarding the power loss for each power transistor, there are three losses.

Conduction loss is due to the on-resistance of the power transistor. The switching loss is due to charging and discharging the drain capacitance of the power transistor at the switching node.

The gate drive loss is due to charging and discharging the gate capacitors of the power transistor during switching transition.

Also, there are two losses associated with the inductor: the winding loss and the magnetizing loss. The winding loss is associated with the DC resistance of the winding wire inside the inductor. The magnetizing loss is sometimes called AC loss. This is mainly caused by the hysteresis of the core inside the inductor.

The magnetizing loss increases with the inductor current ripple and the switching frequency. The calculation of the magnetizing loss is typically specified in the datasheet of the inductor.

20. (Slide 20) Example on Conduction Loss Calculation

This slide provides the example of calculating the conduction power losses of the power switches and the inductor. The conduction power losses are equal to the RMS current times either the on-resistance of the power switch or the DC resistance of the inductor.

When we use the RMS current, that means both the average inductor current and the inductor current ripple, will contribute to the conduction power loss.

21. (Slide 21) Loss Summary of Synchronous Buck Converter

This table summarizes all different losses of the buck converter. In addition to the conduction losses, there are also dynamic losses and static loss.

The dynamic losses consists of the gate drive losses and the switching loss. Both the gate drive losses and the switching loss are proportional to the voltage swing, the switching frequency, and the corresponding capacitance.

The static loss is determined by the controller, so the static loss is equal to the current consumed by the controller times the supply voltage of the controller.

22. (Slide 22) Efficiency Enhancement: PWM-PFM Control

Tor the next four slides, we will start to talk about some of the power efficiency enhancement techniques in the switched-mode power converter.

In the switched-mode power converter, it is very important to achieve high power efficiency over a wide load current range. In the portable applications, the low current range can vary by 1000 times easily. It can vary from 1mA all the way to 1A, and it is very challenging to maintain high power efficiency over such a wide low current range.

One of the techniques to achieve that is to operate the converter with PWM control with fixed switching frequency in the heavy load condition, and then change it to PFM mode with much lower switching frequency in the light load condition.

With much lower switching frequency, the switching activity of the power transistor can be significantly reduced. This will reduce the gate drive loss, then the light-load power efficiency can be improved.

23. (Slide 23) Efficiency Enhancement: DCM Operation
When the load current becomes small, and the average inductor current is less than two times the inductor current ripple, we have to let the synchronous converter go into the DCM effectively.

In other words, we have to turn off both power transistors when the inductor current equals 0. Instead of sensing the inductor current, we can use a zero voltage detector to detect the switching node voltage. When the switching node voltage increases from a
negative value to zero, this voltage can trigger a logic signal to turn off the low-side NMOS. Then the converter can effectively enter state 3, in other words the converter can go into DCM operation.

This paper reports using a high speed comparator with low input offset to realize the zero-voltage detector.

24. (Slide 24) Efficiency Enhancement: Width Switching
Another way to improve the light-load power efficiency is to use the width switching technique. For example, we can break down the large power transistors into different portions.

In this example, in the diagram we are breaking down each power transistor into two portions. For the high-side power transistor, we separate it into a smaller sized M_{sp} and larger sized M_{lp}. Similarly for the NMOS transistor, we separate it into a smaller sized M_{sn} and a larger sized M_{ln}.

So in the light-load condition, only the smaller sized transistor M_{sp} and M_{sn} will be used,
while the M_{lp} and M_{ln} will be turned off. With only the smaller transistor used, this can reduce the gate capacitance of the power transistor during switching, so the gate drive loss can be reduced to improve the light-load power efficiency.

One thing I should note is that during the operation, it is possible in the heavy load condition that there will be an issue of cross conduction. The cross conduction problem happens when the large sized transistors, M_{lp} and M_{sn}, are turned on simultaneously during switching transition in the heavy load condition.

There is conduction between M_{sp} and the M_{ln}, so a special gate driver needs to be designed to prevent this cross conduction issue when we use the width switching technique.

25. (Slide 25) Efficiency Enhancement: Gate Swing Modulation
The light-load power efficiency of the converter can also be improved by using the gate swing modulation.

The idea of the gate swing modulation is to limit the voltage swing at the gate terminal of the power transistors, such that the gate drive power loss can be reduced to improve the light-load power efficiency.

This paper reported a voltage controlled RC delay element in each of the buffers for the power transistors such that when we try to turn on the power transistor, it can turn on the transistor much slower to limit the voltage swing at the gate terminal of power transistor during its turn on.

26. (Slide 26) Buck Converter: Inductance Selection
Minimizing the inductance is very important to the converter size and the system cost. We will use the buck converter in CCM as a design example to discuss how we can select an appropriate size for the inductance.

The inductance is given by this equation. It is inversely proportional to the inductor current ripple and the switching frequency. Since the inductor current ripple is a portion of the maximum output current and the

maximum output current is typically specified for a particular example, the only way to reduce the required inductance in the power stage is to increase the switching frequency.

27. (Slide 27) Buck Converter: Output Capacitor Selection
Regarding the output capacitor selection, the output capacitor is given by this equation. It is inversely proportional to output voltage ripple and the square of the switching frequency.

Similar to the previous approach, we can increase the switching frequency to reduce the required output capacitance in the power stage.

28. (Slide 28) Outline – Control Methodologies and Design Issues
Next I will move on to talk about the control methodologies in the switched-mode power converters.

29. (Slide 29) PWM – Voltage-Mode Control (VMC)
This slide shows the structure of a voltage mode control buck converter. The voltage mode control uses the output voltage information for output voltage regulation.

As shown in this diagram, there exist three major blocks in the controller: the compensator, the PWM generator, as well as the gate driver.

The compensator takes the scaled down output voltage to generate an output V_b, and then the PWM generator uses the V_b information, the system clock information, and the fixed voltage ramp to generate the duty ratio. The duty ratio will be used to control the switching of the power transistors such that the output voltage can be regulated. The compensator in the controller is used to determine the loop stability of the converter.

The compensator also controls the unit gain frequency of the loop gain transfer function in the converter, so that you can determine the transient response of the converter.

30. (Slide 30) VMC - PWM Generator
The left diagram here shows the structure of the PWM generator. It consists of a comparator and a RS latch. As I mentioned before, the function of the PWM generator is to generate a duty ratio for the power transistors, so the leading edge of the duty ratio as we can see from the right diagram is determined by the clock signal, and the trailing edge of the duty ratio will be determined by the crossing between V_b and the fixed ramp signal.

A higher V_b voltage will generate a larger duty ratio, so the output voltage will be larger.

31. (Slide 31) VMC – Loop Gain T(s) (1)
For the stability of the converter, we have to study the loop gain transfer function, T(s). T(s) is given by this equation. It consists of the compensator transfer function, A(s), and also the control to output transfer function, C(s).

C(s) consists of three components: the PWM generator, which is given by $\Delta D/\Delta V_b$, the duty ratio going to the switching node, which is given by $\Delta V_x/\Delta D$, and the switching node going to the output, which is given by $\Delta V_{out}/\Delta V_x$.

Since there is a low-pass filter that exists between V_x and the output, implemented by the inductor and the capacitor, $\Delta V_{out}/\Delta V_x$ can be given by a standardized second-order equation.

It consists of a complex pole, where the Q value of the complex pole is proportional to the load resistor, and where the location of the complex pole, $\omega_{0,}$ is proportional to the square root of the inductance and the capacitance in the power stage.

32. (Slide 32) VMC – Traditional Dominant Pole Compensation

The conventional way to stabilize the voltage mode control is to use a dominant pole compensation. In the dominant pole compensation, there is only a single pole located at the output of the compensator.

That single pole will act as the dominant pole of the loop gain. Here is the magnitude plot of the loop gain transfer functions under different conditions. As we can see, there is a peaking that occurs at the complex pole location.

A larger peaking or Q value will decrease the gain margin of the loop gain transfer function. You will make the converter become more unstable. The worst-case stability occurs when the load current is the minimum. In that case, you have the largest Q value, and the smallest gain margin.

To ensure the stability of the loop gain transfer function, we have to leave at least 20 dB gain margin at the location of the complex pole. In this way, we have to design a very, very low frequency dominant pole. As a result, the unity-gain frequency of the loop gain transfer function is also very low. This will significantly degrade the load transient response of the converter.

33. (Slide 33) VMC – Type III Compensator (1)

To address this issue, we can use a type III compensator. Here shows the structure of a type III compensator. The type III compensator generates two separate left half plane (LHP) zeros.

The idea is that we are using the positive phase shift from the LHP zeros to cancel out the negative phase shift coming from the complex pole.

The right diagram shows how we place the LHP zero. The first LHP zero should be placed a few times smaller than the location of the complex pole. The second LHP zero will be placed approximately equal to the location of the complex pole.

After the pole-zero cancellation, the unity gain frequency of the loop gain transfer function, can be located at a frequency higher than the complex pole. This can significantly improve the load transient response of the converter as compared to the previous case.

34. (Slide 34) VMC – Type III Compensator (2)

However, in the previous type III compensator, there are so many passive components. These passive components are generally off-chip, and you will occupy a large board area.

This research work reported at 2014 ISSCC, reported a new way to design the type III compensator with a much smaller number of passive components using a differential difference amplifier to generate two LHP zeros.

So you can still enjoy the fast transient response of a type III compensator with much less passive components.

35. (Slide 35) PWM – Current-Mode Control (CMC)
Next, I will switch the gear to talk about the current-mode control. This shows the structure of the current-mode control PWM buck converter. Compared to the previous controller, it uses both the output voltage information and the inductor current information for output regulation. Also, instead of using the fixed voltage ramp to define the duty ratio, the current-mode control uses the sensed inductor current to define the duty ratio by the PWM generator.

36. (Slide 36) CMC – Sub-Harmonic Oscillations (1)
Soon after the discovery of the current-mode control, researchers found that there is a system stability problem when the duty ratio of the converter is larger than 0.5. As I mentioned before, the PWM generator is used to define the duty ratio by comparing V_b and the sensed inductor current.

In the case where there are any kind of perturbation in the sensed inductor current and the duty ratio is less than 0.5, the perturbation will become smaller after one switching period. After several switching periods, the perturbation disappears, and the converter can be free of stability issues.

However, for the case of duty ratio larger than 0.5, we can see that the perturbation amplitude increases after one switching period. After two switching periods, the converter will not have the accurate duty ratio information.

This issue happens at two times the fundamental switching period; therefore we call the problem a sub-harmonic oscillation.

37. (Slide 37) CMC – Sub-Harmonic Oscillations (2)
To eliminate the sub-harmonic oscillation, we can introduce a compensation ramp as shown in this diagram with the slope of m_c. The idea of this compensation ramp is to limit the peak value of the sensed inductor current such that after one switching period, the perturbation amplitude can be smaller compared to the initial value, and the converter would be free of sub-harmonic oscillations.

I should mention that compensation ramp can be realized by the same voltage ramp generator in the voltage mode controller.

38. (Slide 38) Compensation Ramp in Current-Mode Controller
This slide shows how we can combine the compensation ramp, sensed inductor current, and the compensator output together in the controller. We can combine the current information of the sensed inductor current and the compensation ramp together.

The combined current will be converted back to the voltage domain using a resistor R_s, and this voltage will fit into the non-inverting terminal of the comparator.

39. (Slide 39) CMC – Loop Gain T(s)
Regarding the stability of the current-mode control, the control-to-output transfer function this time only has two separate LHP zero. The two separate LHP zero will be much easier to compensate, and the compensator will be much easier to implement as compared to the type-III compensator in a voltage mode controller.

40. (Slide 40) CMC – Compensator Design

The left diagram shows the design of the compensator for the current-mode control. The compensator is used to generate one pole and one zero. It can be realized by the single pole transconductance amplifier, loaded with a resistor, R_z, connected with an output capacitor, C_b.

The series connection of the R_z and C_b will generate a LHP zero. The output resistance of the amplifier R_{oc} and C_b will be the pole of the compensator. The pole of the compensator is also the dominant pole of the loop gain transfer function.

The LHP zero is used to cancel out the first pole from the control-to-output transfer function in the loop gain transfer function here.

41. (Slide 41) Inductor Current Sensing

Next we will move on to talk about the inductor current sensing. Inductor current sensing is very important because the current-mode control relies on the accurate inductor current information.

For peak current sensing, we have to minimize the detection delay of the inductor current sensing. In fact, the detection delay should be smaller than the minimum turn-on time of the high-side power transistor.

If this is the case, then the peak inductor current can be accurately sensed to define the duty ratio. However if the detection delay is too long, and longer than the minimum turn-on time of the power transistor as shown on the right hand side, the duty ratio cannot be accurately defined in the controller and the converter cannot work.

Since the turn on-time is proportional to the switching period, so the speed limit of the current sensor will affect the maximum achievable frequency of the converter.

42. (Slide 42) Sensing Resistor

The simplest way to implement the current sensing is to place a resistor next to the inductor. The voltage across this sensing resistor will consist of the entire inductor current profile.

However, it is challenging to determine the resistance of the sensing resistor. If the resistance is too small, the inductor current will not be accurate in the light load condition.

If the resistance is too large, the power loss associated with the sensing resistor will degrade the power efficiency, especially in low power applications.

43. (Slide 43) Switch Current Sensing for HS Power PMOS

In fact, in the current-mode control, we actually do not need to use the entire inductor profile, only the peak and valley inductor current will be necessary to determine the accurate duty ratio.

This shows a switch current sensor for the peak current control buck converter. In this circuit, M_{ps} is the sensing transistor, and M_p is the power transistor.

We design the sensing transistor, M_{ps}, K times smaller than M_p. In practice, K is typically 1000. In this case, the current passing through the sensing transistor can be significantly smaller than the current going to the power stage.

However, during operation the power transistor is operating in the deep triode region. In order to get the accurate copy of the inductor current, or the current passing through the power transistor, we have to make sure that the drain voltage of the power transistor and the sensing transistor is the same.

This is achieved by using the voltage mirror M_3 and M_4. When we have the same current passing through M_3 and M_4, M_3 and M_4 will have the same V_{gs} because the gate voltage of M_3 and M_4 are tied together, so the drain voltage of the sensing transistors will be forced to be the same as the drain voltage of M_p.

44. (Slide 44) Switch Current Sensing for LS Power NMOS

In order to realize the peak current sensor for the boost converter, we can use the exact same concept of the switch current sensor discussed in the previous slide, except that we have to change all the PMOS transistors in the previous slide to NMOS transistors and vice versa, because in the boost converter, the peak current occurs in the low-side NMOS power transistor here.

45. (Slide 45) Low-Voltage Switch Current Sensing

In the low-voltage current-mode control converter, we have to design a low-voltage switch current sensor. So instead of using the voltage mirror, M_3 and M_4, in the previous slide, this paper reported using a low-voltage error amplifier to enforce the drain voltage of the sensing transistor to be the same as the drain voltage of the power transistor. In this case, the converter can operate with a low-voltage.

If I remember correctly, according to this paper, the converter signal can operate down to 1.1V with the 0.35μm CMOS process with the typical threshold voltage as high as 0.75V.

46. (Slide 46) High-Speed Switch Current Sensing

If the converter needs to operate in the few megahertz range, and support a wide duty ratio range from 0.2 to 0.9, we have to improve the speed of the current sensor. These two papers reported a technique called the dynamic bias shunt feedback, which has an additional 7 transistors compared to the first version of the switch current sensor.

The function of this shunt feedback technique is to push the non-dominant pole of the negative feedback loop in the current sensor to much higher frequencies. This will move the unity gain frequency of the loop to a much higher frequency, such that the transient response can be improved.

47. (Slide 47) Filter-Based Current Sensing

If the converter needs to operate at 10MHz or above, the switch current sensor will not be fast enough, and then we have to change to the filter-based current sensor.

In the filter-based current sensor, we have a sensing resistor, R_S, and capacitor, C_S, connected in parallel with the inductor. We can take the voltage across the sensing capacitor, C_S, and this voltage will be proportional to the inductor current if the time constant of R_S and C_S is much larger than the switching period.

48. (Slide 48) Gate Driver for HS Power PMOS

The next important block in the controller is the gate driver. Here is the structure of the gate driver for driving the complementary power transistors. It happens in the low-voltage. The high-side power transistor is a PMOS. The use of PMOS is mainly because we can use the gate signal swing of the PMOS, which is only from 0 to Vin, and does not require any extra supply for controlling the power transistor.

The gate driver consists of two blocks: a dead-time controller and two digital buffers. The dead-time controller tries to minimize or eliminate the short circuit power loss by preventing the simultaneous conduction of the power transistors during switching.

Each digital buffer will consist of a chain of digital inverters with a growing aspect ratio. The purpose of having this is to drive the large gate capacitance of the power transistors with the minimum propagation delay.

49. (Slide 49) Gate Driver for High-Side Power NMOS (1)

In the case of high input voltage, it is very common that we implement the high-side power transistor using NMOS. The reason for using NMOS is due to its advantage in mobility. The size of the NMOS transistors can be a few times smaller than the PMOS transistors for the same on-resistance.

In this gate driver, there consists of two additional blocks as compared to the previous version. There is a level shifter and a bootstrap circuitry. The level shifter is to up-shift the duty ratio information from the low-voltage domain to the high-voltage domain for driving the high-side power NMOS.

The bootstrap circuitry is used to generate an auxiliary supply, V_{Boot}. V_{Boot} is actually equal to the sum of V_{in}, the supply of the converter, and V_{DD}, the maximum voltage of the gate terminal.

By having V_{Boot}, the high-side circuitry can properly turn on the high-side power NMOS transistor.

50. (Slide 50) Gate Driver for High-Side Power NMOS (2)

The design of the level shifter in the previous gate driver is very important because it could determine the power dissipation, as well as the speed of the whole gate driver.

Here shows the structure of a low power dynamic level shifter. It consists of three blocks: a short-pulse generator, a level-shifting stage, and a signal recovery circuitry. The short-pulse generator is to convert the input signal, V_{G1}, to become two short-pulses according to the rising and the falling edges of the input signal.

The level shifting stage will convert the short-pulses at the input to the high-voltage domain. Since the level-shifting stage only turns on for a very short period of time during the pulse wave of the input short-pulses, so the average current consumption of this level shifting stage can be significantly reduced. This will lower the power consumption of the level-shifting stage, as well as the level-shifter.

The signal recovery circuit will convert the up-shifted short-pulses at nodes A and B to the output, V_{HO}. V_{HO} will have the same pulse-width as the input signal, V_{G1}.

51. (Slide 51) Hysteretic Control

In the next two slides, we will discuss a new control scheme, the hysteretic control. In the PWM control, the transient response of the output voltage is typically limited by the bandwidth limited error amplifier and the unit gain frequency of the loop gain transfer function.

The hysteretic control only has a hysteretic comparator in the controller. The hysteretic comparators use two reference voltages, V_H and V_L, to define the output voltage.

With this architecture, the propagation delay of the controller can be significantly reduced in order to improve the transient response of the output. However, there is a disadvantage in using the hysteretic controller. The input offset voltage of the comparator together with the resistor feedback network will lead to the output voltage

having a very large output voltage ripple. In fact, the output voltage ripple using the hysteretic controller would be much larger than that of the PWM controller.

52. (Slide 52) Current-Mode Hysteretic Control

To reduce the output voltage ripple in the previous voltage mode hysteretic controller, we can use current-mode hysteretic control as shown on the left diagram. In the current-mode hysteretic controller, the voltage in the middle of the inductor current emulator will be fed into the hysteretic controller.

In this way, the output ripple voltage can be significantly reduced. However, there exists a DC offset across this sensing capacitor, and that will slow down the output transient response.

A couple of years ago, there was a piece of research work reporting a revised filter-based current sensor. They called it the quasi current-mode hysteretic control. In this controller, there is a reset switch to try to minimize the offset voltage across the sensing capacitors such that the transient response can be improved.

They also have a transconductance amplifier in the sensor that can reduce the required value of the sensing capacitor. In this way, the area occupied by this sensor will be much smaller compared to previous case.

53. (Slide 53) Outline – Advanced Topic

Finally, I will start to talk about the advanced topic of the three-level DC-DC converter.

54. (Slide 54) Three-Level DC-DC Converter (1)

The left diagram shows the structure of the three-level DC-DC converter. Compared to the two-level buck converter, it has two additional power switches, and one flying capacitor, C_f, connected between two switching nodes A and C.

If you try to compare the voltage conversion ratio, the voltage conversion ratio of the three -converter would be the same as the two-level buck converter. The two timing diagrams on the right is used to describe the operation of the three-level converter under different duty ratios.

We will discuss the case where the duty ratio is less than 0.5 to illustrate operation of the three-level converter.

For the duration from t_0 to t_1, the power transistors M_1 and M_4 are turned on. In this case, the voltage at node B or V_B equals to half the input voltage.

Since V_B is larger than V_{out}, the inductor current increases. In this duration, the current is actually flowing into the flying capacitor, so we call this duration the charging phase of the flying capacitor.

For the duration from t_1 to t_2, M_3 and M_4 are turned on so that V_B equals to 0, and the voltage across the inductor is a negative value, so the inductor current decreases.

From t_2 to t_3, the transistors M_2 and M_4 are turned on. In this case, V_B is charged back to $0.5V_{in.}$ During this operation, the current is pulling out from the flying capacitor, so we are calling this is the discharging phase of the flying capacitor.

Since V_B is larger than V_{out}, so the inductor current increases again. From t_3 to t_4, M_3 and M_4 are turned on again, so V_B is reset to zero, and the inductor current decreases.

When we are looking at the inductor current profile, we will find out that the frequency of the inductor current is actually two times the frequency of the gate drive signal.

55. (Slide 55) Three-Level DC-DC Converter (2)

With the two times increase in the switching current profile, the output voltage in the three-level converter, the frequency of the output voltage waveform is also increased by two times compared to the gate drive signal.

Also, the voltage swing at each switching node is reduced to half the input voltage. This is very important because in high voltage applications, we can use the power transistors with a much lower voltage rating. The power transistors with a lower voltage rating can have a much smaller converter area.

56. (Slide 56) Three-Level DC-DC Converter (3)

The left diagram is a comparison of the inductor current ripple between the two-level buck converter and the three-level buck converter. As we can see, the inductor current ripple has been reduced by 4 times in the three-level converter; therefore, the required inductance in the three-level converter is also reduced by 4 times.

On the right diagram, this is a diagram to show a comparison of the output voltage ripple between the three-level converter and the two-level converter. We can see that the output ripple in the three-level converter is 8 times smaller.

Of this 8 times, 4 times is coming from the internal current ripple reduction; therefore, by using the three-level converter, the required capacitance can still be reduced by two times.

57. (Slide 57) Voltage across the Flying Capacitor

In the three-level converter, it is very important to ensure the voltage across the flying capacitors are maintained at half the input voltage. So, we have to evaluate the voltage change across the flying capacitor, $\Delta V_{cf.}$ ΔV_{cf} in one period is equal to the difference of ΔV_{cf} in the charging phase, and ΔV_{cf} in the discharging phase.

If you go back to the diagrams, you will see that ΔV_{cf} in the charging phase is proportional to the average inductor current in the charging phase.

Similarly, ΔV_{cf} in the discharging phase would be proportional to the average inductor current in the discharging phase, I_{L2}. Therefore, the total voltage change across the flying capacitor will be proportional to the difference between I_{L1} and I_{L2}.

If I_{L1} is equal to I_{L2}, ΔV_{cf} equals 0, that means the voltage across the flying capacitor is successful maintained at half the input voltage.

58. (Slide 58) Flying Capacitor Balancing

During the operation of the three-level converter, there are always some perturbations which will affect the voltage across the flying capacitors different from the $0.5V_{in}$. It is very common that in addition to the controller for output regulation, we also need to have a separate controller to regulate the voltage across the flying capacitor such that the voltage across a flying capacitor will be exactly equal to $0.5V_{in}$.

Now if the voltage is different from $0.5V_{in}$, the voltage stress across the power transistor may be higher than the allowable voltage rating, and that will damage the power transistors, and the converter may not work.

59. (Slide 59) Flying Capacitor Self Balancing (1)
Instead of using two separate controllers to perform the regulation of the flying capacitor voltage and the output voltage, we can use the self-balancing technique. The self-balancing technique means that we can use the same controller to perform the flying capacitor balancing and output voltage regulation.

The idea behind this is that the voltage change across the flying capacitor, as mentioned before, is related to the average inductor current.

The output voltage of the three-level converter is also proportional to the average inductor current. If we can regulate the average inductor current by using the controller, then both the flying capacitor balancing, as well as the output regulation can be achieved simultaneously.

This work reported in 2016 ISSCC, talked about the adaptive on-time V^2 controller that can detect the inductor current information and regulate the inductor current information to achieve both flying capacitor self-balancing and output voltage regulation simultaneously.

60. (Slide 60) Flying Capacitor Self Balancing (2)
These slides basically illustrate the self-balancing scheme under different perturbations when the voltage across the capacitors is less than half of the input voltage or larger than half of the input voltage.

As we can see from these diagrams, if we can regulate I_{L1} and I_{L2} in the charging phase and discharging phase correctly by using the controller, after several cycles these two values will be equal to each other; therefore, the flying capacitor can be successfully balanced.

61. (Slide 61) Loop Gain of Three-Level Converters
This equation is the loop gain transfer function of the three-level converter. We can find out that this equation is exactly the same transfer function as the two-level buck converter. Therefore, the controller using the two-level converter can be successfully applied to control the output of the three-level converter.

62. (Slide 62) Gate Driver for Three-Level Converters
This diagram shows the structures of the gate driver for the three-level converter. In the
three-level converter, there are three high-side power transistors: M_3, M_2 and M_1. Therefore, we need to have three level-shifters and three sets of bootstrap circuitry to generate the appropriate auxilary supplies for the different high-side circuitries.

In the gate driver, we still have a dead-time controller to prevent the simultaneous conduction of the power transistors during switching transition. This can make the converter have a higher power efficiency because there is no short circuit power loss.

63. (Slide 63) Example: 100V Three-Level DC-DC Converters (1)
Now I would like to discuss specific design examples of the three-level DC-DC converter which is used for high voltage applications.

This three-level converter can be used to support the supply voltage up to 100V. In high voltage applications, the switching power loss is dominant, so we have to effectively eliminate the switching power loss in order to allow the converter to achieve high power efficiency.

In this design, a very small value inductor is used to generate the transient current. The transient current will be used to charge and discharge the different switching nodes: V_A, V_B, and V_C, in order to realize zero voltage switching (ZVS) of the power transistor, and then the power transistor can then turn on.

In particular, as shown in the timing diagram here, M_2 and M_4 are turned on with ZVS at the time instances t_4 and $t_{8,}$ respectively. Similarly, the power transistors M_4 and M_3 are turned on with ZVS at the time instances t_2 and $t_{6,}$ respectively.

64. (Slide 64) Example: 100V Three-Level DC-DC Converters (2)
This diagram provides the power loss of 4 different converters: the two-level hard switching, the two-level ZVS, the three-level hard switching, and the three-level ZVS.

Under a supply voltage of 100V, we can see the power loss of the three-level ZVS has a 13 times reduction compared to the two-level hard switching converter. The power loss is also reduced by 2.6 times compared to the two-level ZVS.

65. (Slide 65) Example: 100V Three-Level DC-DC Converters (3)
The three-level ZVS converter was implemented in the 0.5μm 120V CMOS process, and here shows the micrograph.

This table provides the performance comparisons of the three-level ZVS with an industry product using the architecture as a two-level hard switching converter.

These two converters have similar input voltage range, output voltage, and output power. With the ZVS scheme, the required inductance of the three-level ZVS can be reduced by 66 times.

The total capacitance can also be reduced by 2.6 times. The switching frequency can operate at 2MHz which is 5 times higher than the two-level hard switching case.

Even with the highest switching frequency, the peak power efficiency of the three-level ZVS converter is always higher than the peak power efficiency in the two-level converter under different input supply voltages.

66. (Slide 66) Summary
In summary, today we have talked about the fundamentals of the switched-mode power converters, including different kinds of topics related to topology, power loss, different control schemes, current sensor design, as well as hysteretic control. We also had time to talk about the three-level DC-DC converter, the basic operation together with the flying capacitor balancing.

67. (Slide 67) Related Papers ISSCC 2018
There are two papers in ISSCC 2018 that are relevant to the material that I have discussed. One is paper 24.1 which is on the high voltage DC-DC converter. The other paper is paper 27.5 which is about the low-voltage ripple step-up converter.

68. (Slide 68) References
You also can find more materials relevant to what we discussed today based on the reference list here. With that, I would like to thank you all for your attention, and I can take any questions you may have. Thank you!