ADC-Based Serial Links: Design and Analysis

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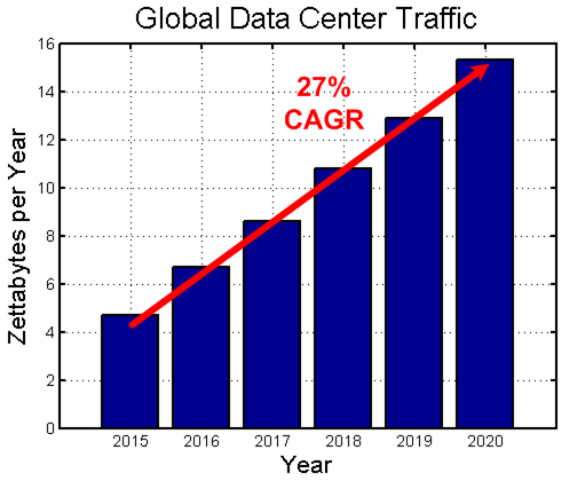
We Need More Data Bandwidth

Human-driven traffic growth

Hi definition video conference

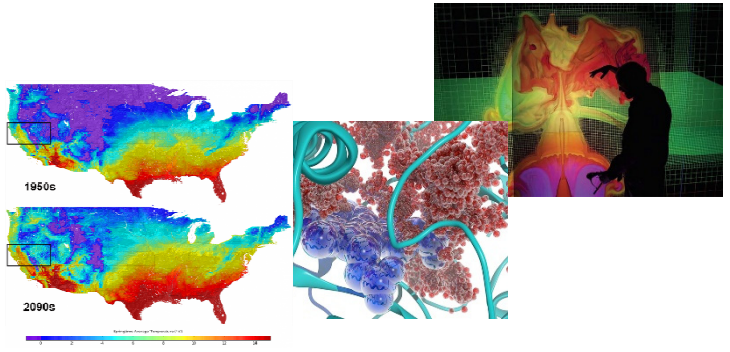


[Cisco Global Cloud Index 2016]

Machine-driven traffic growth

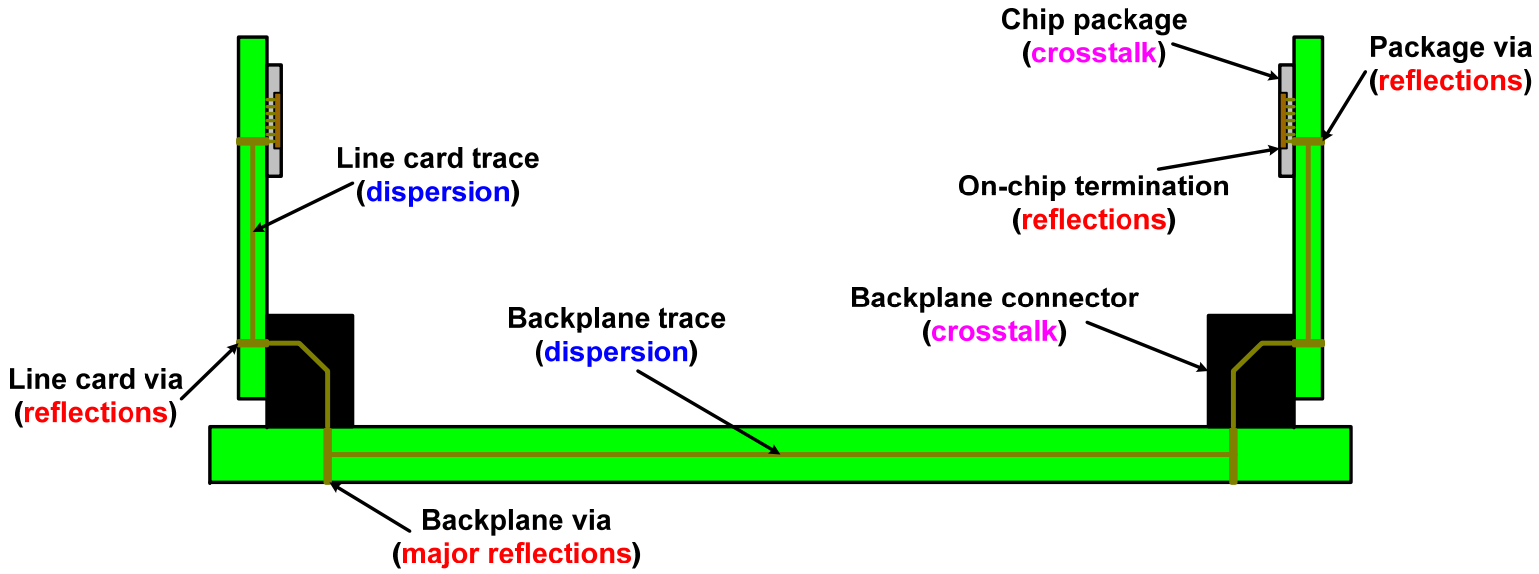
Cloud service, big data, IoT

Enterprise service

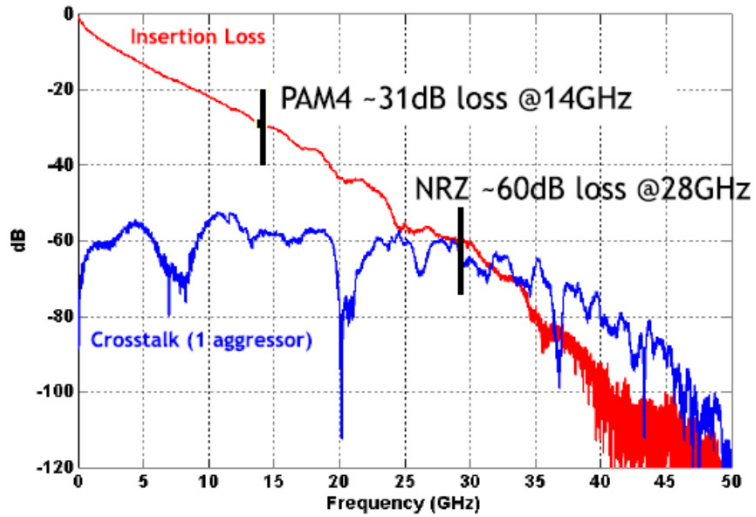


Supercomputer

Electrical Channel Bandwidth Limitations



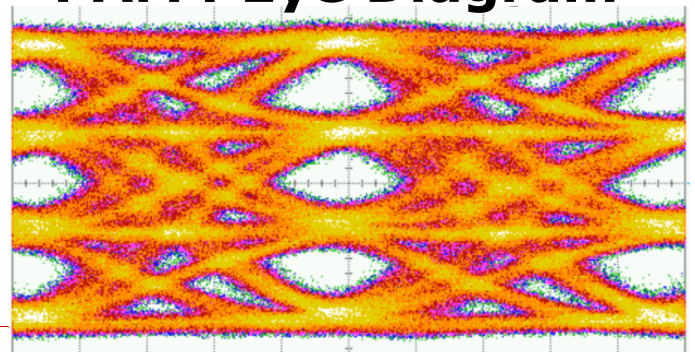
56Gb/s Legacy Backplane Channel



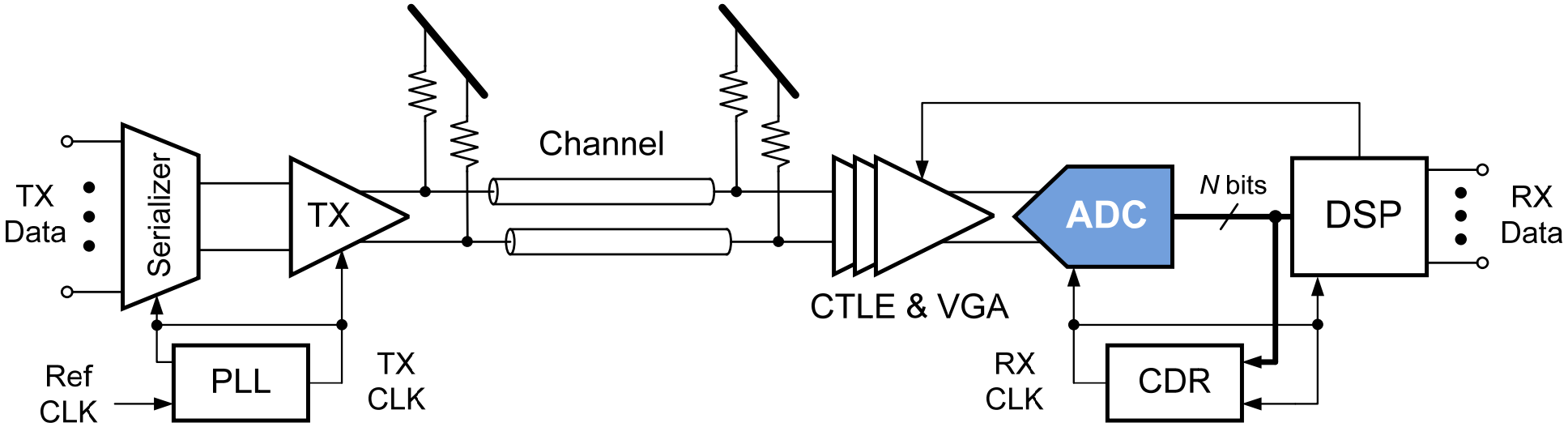
[Frans JSSC 2017]

- Electrical channel bandwidth has not scaled to match I/O bandwidth demands and the CMOS technology speed
- Motivates more spectrally-efficient modulation schemes (PAM4)

PAM4 Eye Diagram



ADC-Based Receiver Front Ends



- ADC-based receivers perform ISI cancellation in digital domain, allowing for flexible advanced equalization and symbol detection
- Well suited for more spectrally-efficient modulation schemes (PAM4)
- Benefit from improved area and power with CMOS scaling
- Power dissipation of both the ADC and digital equalizer is a major issue

Outline

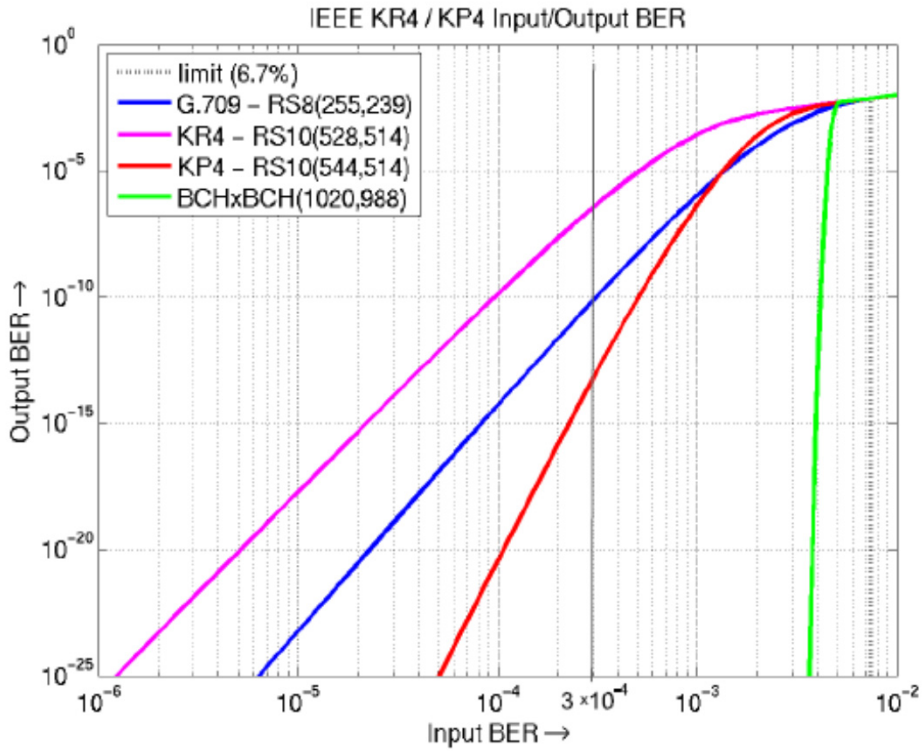
- ADC Resolution Requirements & Topologies
- Key ADC Circuits
- ADC Calibration Techniques
- Digital Equalization
- Analog Front-End
- Conclusion

ADC Resolution Requirements

- The required ADC resolution is a function of
  - Channel loss
  - Amount of TX and RX front-end analog equalization
  - Modulation scheme
  - Required BER (FEC)

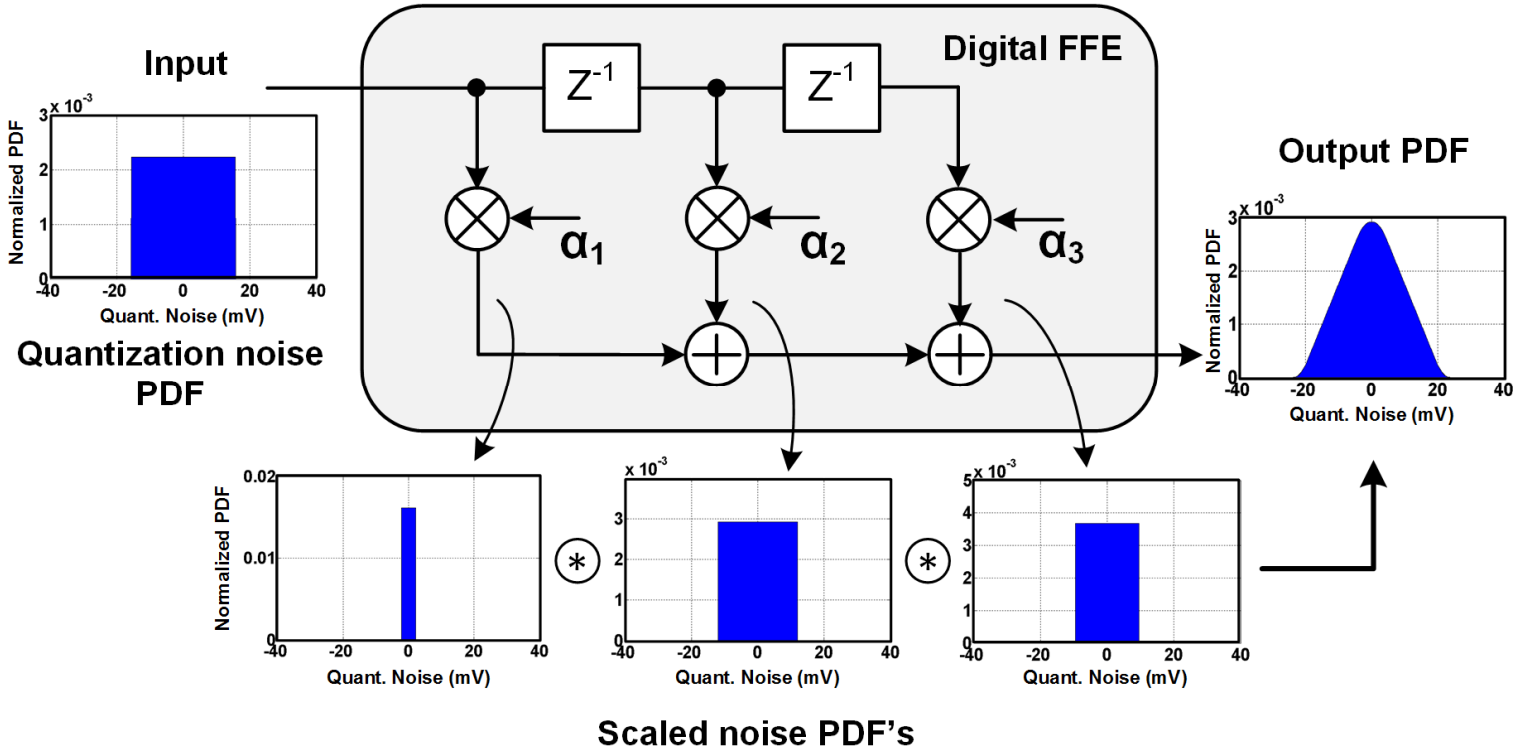
- Quantization noise must be accurately modeled to select the necessary ADC resolution

Impact of FEC on RX Front-End Raw BER



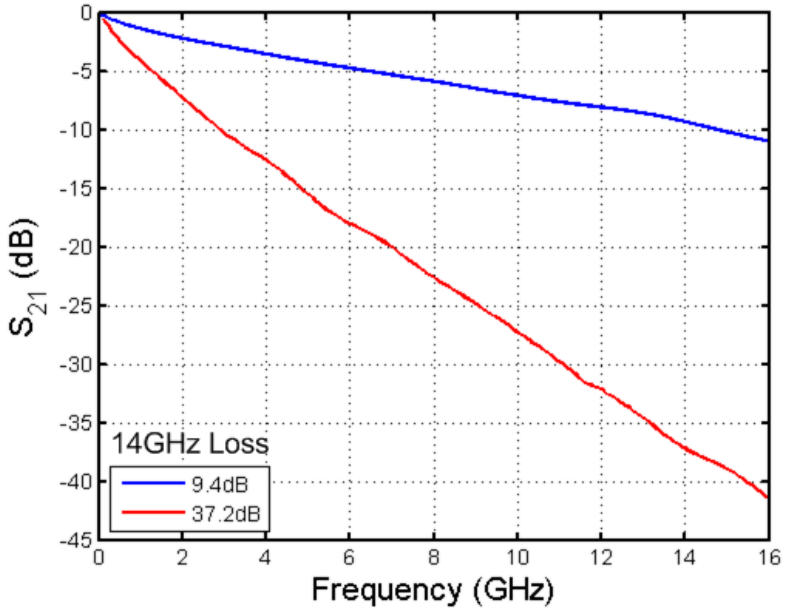
[Frans JSSC 2017]

Quantization Distortion Modeling

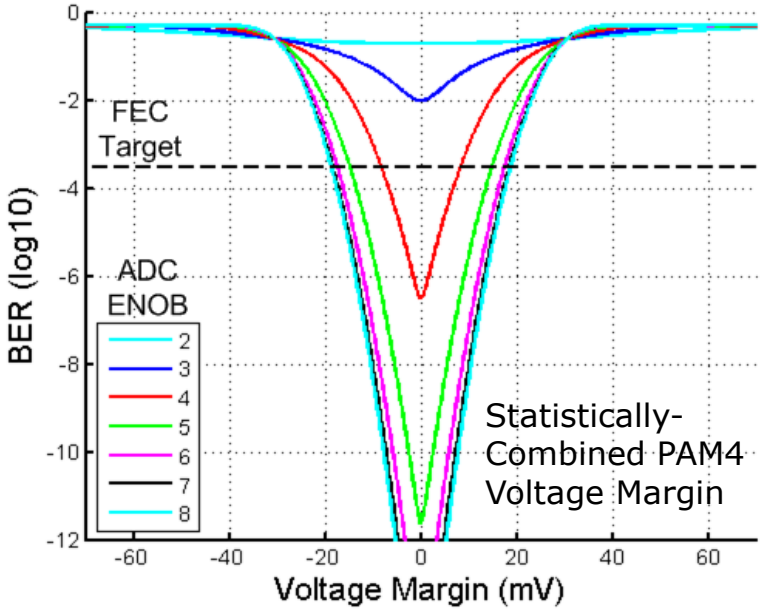


- Quantization noise is shaped by RX-side digital FFE
- Allows for direct convolution w/ other noise/distortion PDFs
  - Assuming small INL/DNL and front-end non-linearity

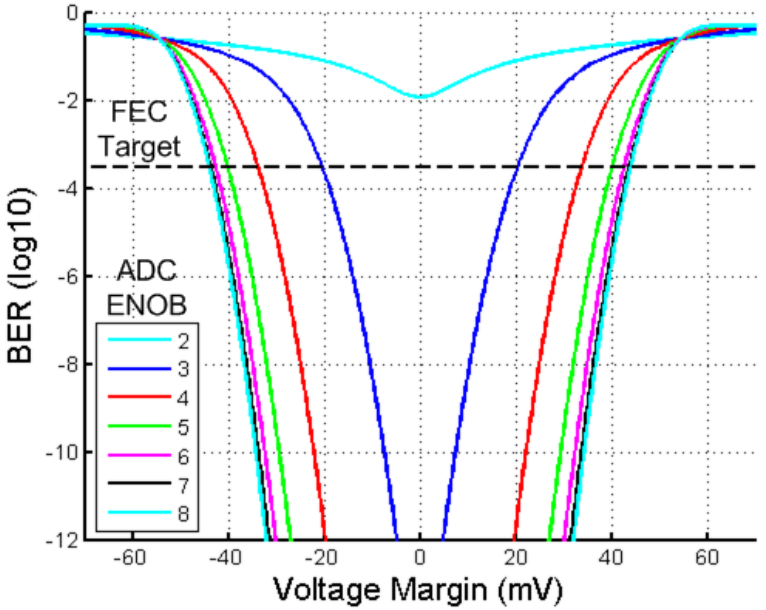
56Gb/s PAM4 Example



37.2dB Channel



9.4dB Channel



- High-loss channel requires 3-4b ENOB for FEC BER (3e-4) and >5b ENOB to achieve a 1e-12 raw BER
- Low-loss channel can achieve 1e-12 raw BER with only 3b ENOB
- Motivates configurable resolution ADCs

Key Simulator Settings

- 3-tap TX w/ 1Vpp swing
- CTLE/AGC FE w/ 7.4dB peaking and 16GHz BW
- 400mV ADC FSR
- Digital 14-tap FFE & 1-tap DFE
- $3mV_{rms}$ ADC input noise
- RJ=$300fs_{rms}$
- No TI effects (more later)

Recent ADC-Based XCVR/RX

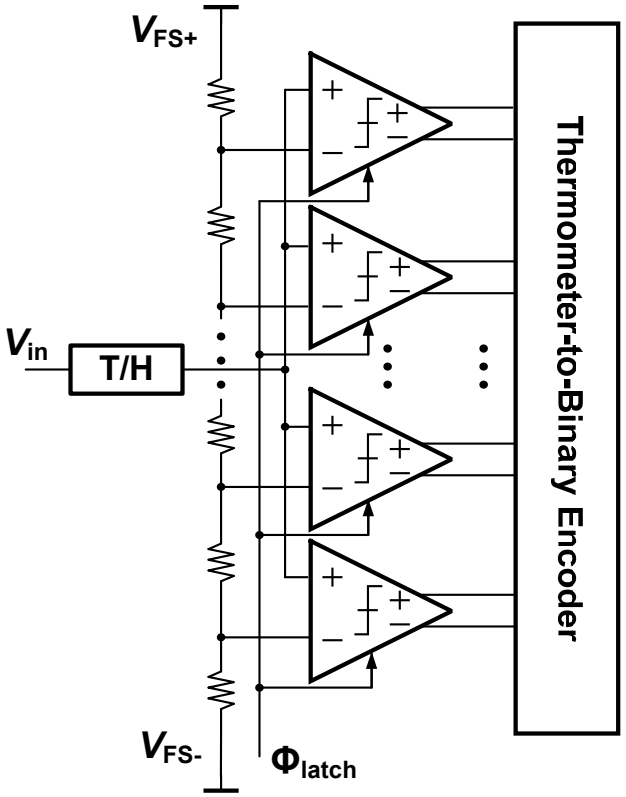
Specification	Frans JSSC'17	Gopalakrishnan ISSCC'16	Cui ISSCC'16	Rylov ISSCC'16	Shafik JSSC'16	Zhang JSSC'15
Data Rate (Gb/s)	56	56	32	25	10	11.5
Modulation	PAM4	PAM4	PAM4	PAM2	PAM2	PAM2
ADC Sample Rate (GS/s)	28	28	16	25	10	11.5
ADC Structure	Asynchronous SAR	Synchronous SAR w/ Redundancy	Asynchronous SAR w/ Redundancy	Flash	Asynchronous SAR	Rectifying Flash
ADC Resolution (bit)	8	7	8	5	6	6
ADC ENOB at Nyquist (bit)	4.9	4.9	5.85	3.8	3.9	4.6
ADC TI Factor	32	32	32	4	32	4
TX Swing (V_{ppd})	1.2	1.4	NA	NA	NA	NA
TX FFE Taps	3	3	NA	NA	NA	NA
RX FE Equalization	CTLE w/ 7dB Peaking	CTLE w/ 8dB Peaking	CTLE w/ 7dB Peaking	CTLE	Embedded 3-tap FFE in ADC	CTLE w/ 6dB Peaking
RX Digital FFE Taps	24	Multiple	NA	8	4	Multiple
RX Digital DFE Taps	1	1	NA	8	3	Multiple
Max Channel Loss (dB)	-31	-35	-32	-40	-36.4	-34
TX Power (mW)	140	NA	NA	NA	NA	NA
ADC/FE Power (mW)	370	NA	320	310	79	195
DSP Power (mW)	NA	NA	NA	143	10	NA
Clocking Power (mW)	40	NA	NA	NA	NA	NA
Area (mm^2)	2.8	30.87	0.89	0.39	0.81	0.82
Technology	16nm FinFET	28nm	28nm	32nm SOI	65nm	40nm

Some Observations

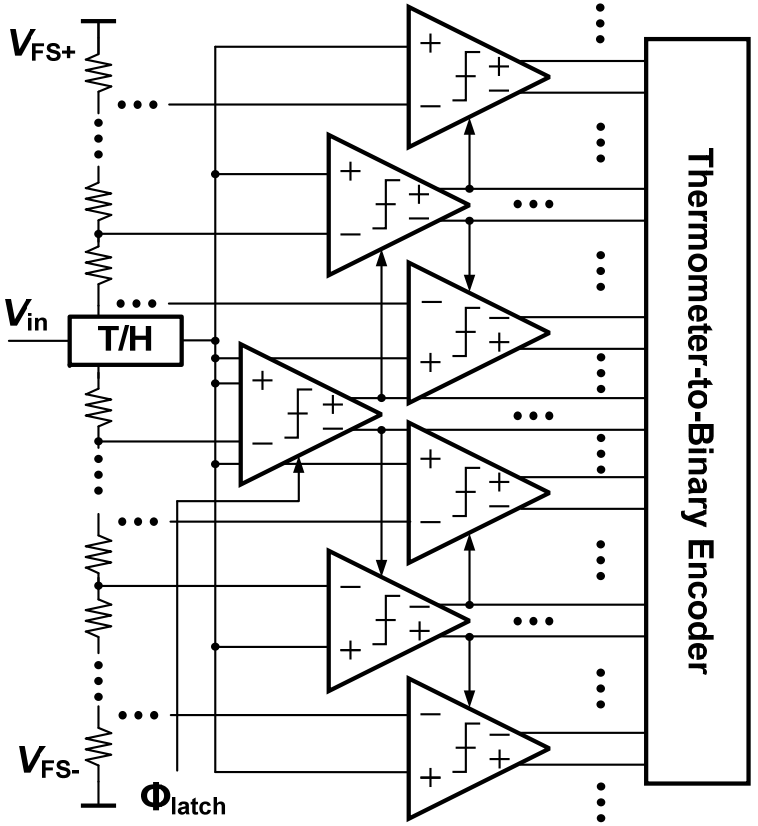
- PAM2 systems are generally implementing 5-6b ADCs and achieving close to 4-4.5b ENOB at Nyquist
  - A mixture of flash and SAR architectures are utilized
- PAM2 digital equalization enables robust implementation of RX-side FFE and multiple DFE taps
- PAM4 systems are generally implementing 7-8b ADCs and achieving close to 5-6b ENOB at Nyquist
  - SAR architectures are well suited for this resolution
- PAM4 digital equalization employs large tap count FFEs to effectively cancel residual ISI, but few DFE taps due to complexity

Common ADC Topologies

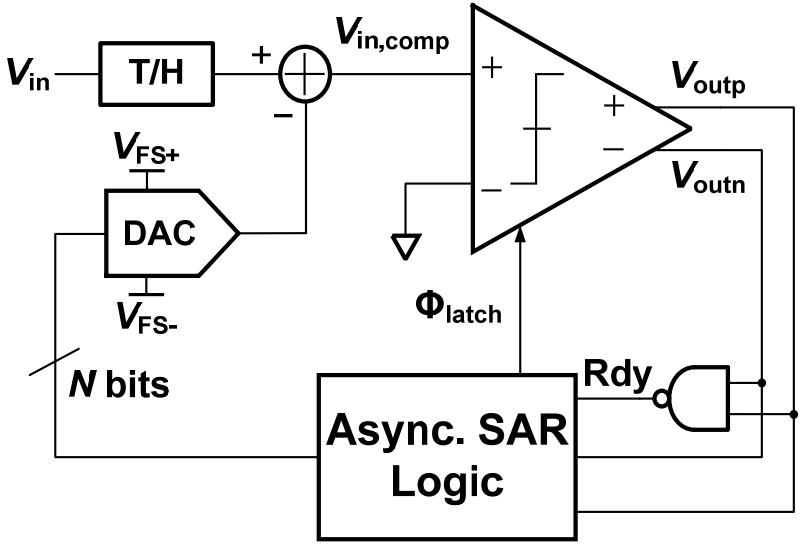
Flash



Binary (Multi-Bit) Search

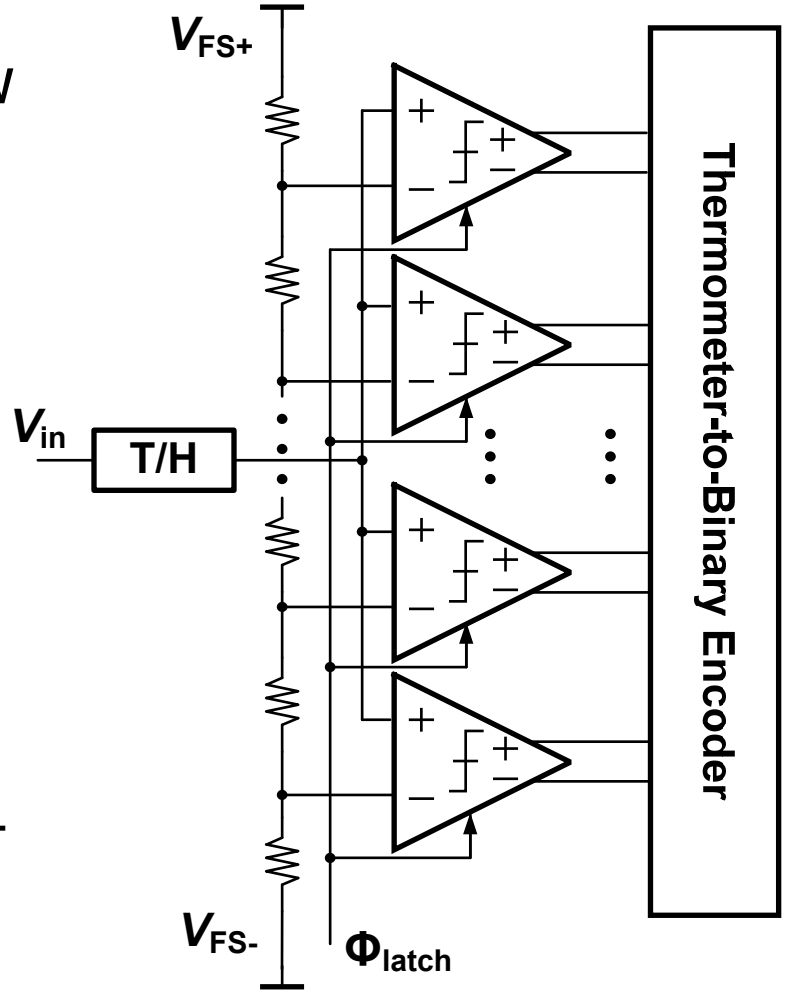


SAR



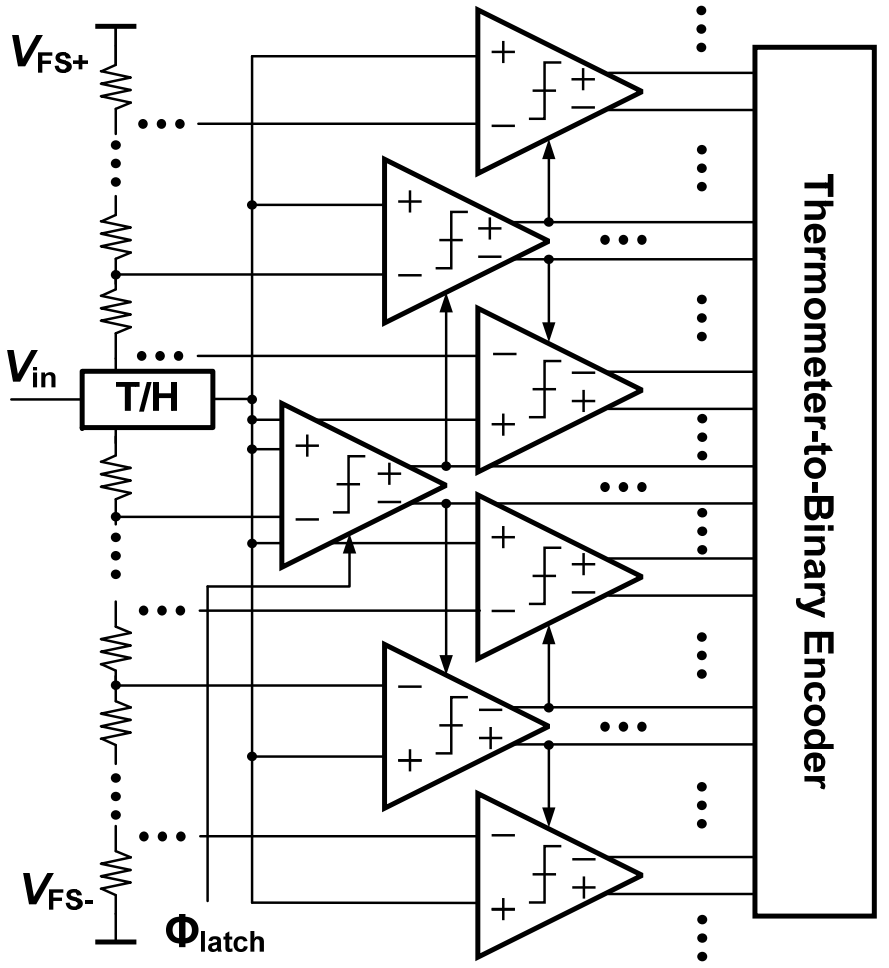
Flash ADC

- Comparators at each reference level allow for simultaneous parallel conversion
- Single cycle operation allows for high speeds
  - Typical interleave factors of 4-8
- Main downside is large comparator count
  - Rectifying flash architectures can reduce this
- Flash ADC is a reasonable choice for PAM2, but resolution is a bit low for PAM4



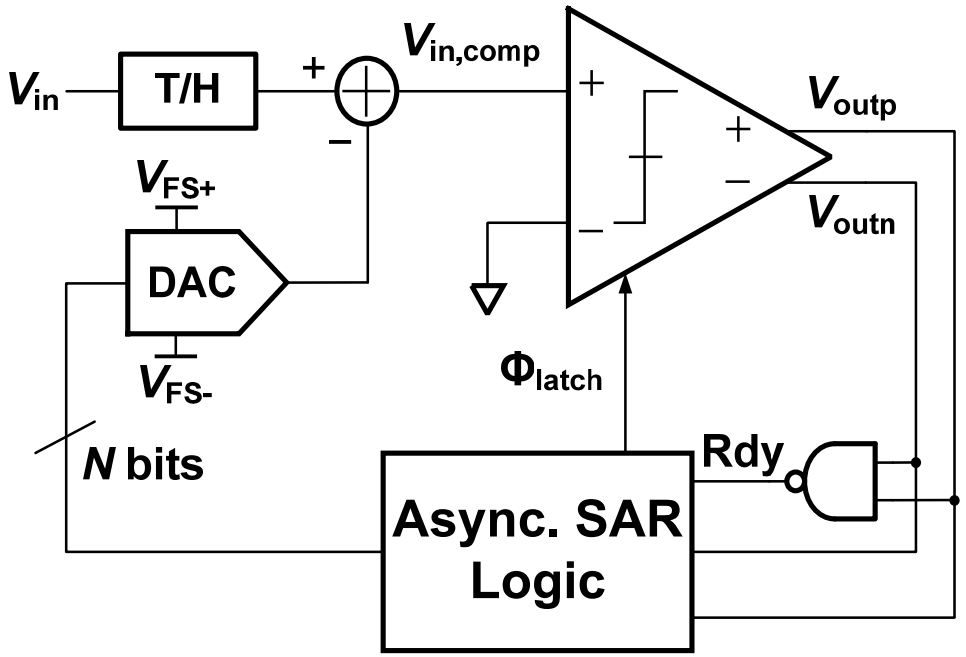
Binary (Multi-Bit) Search ADC

- Binary (multi-bit) search ADCs combine desirable properties of flash & SAR ADCs
- Efficient binary search algorithm allows only necessary comparator evaluation
- Avoids the DAC settling and logic delay present in SAR ADCs, but slower than flash due to serial comparator evaluation
- Good choice for PAM2 applications, area may be a bit high for PAM4 applications



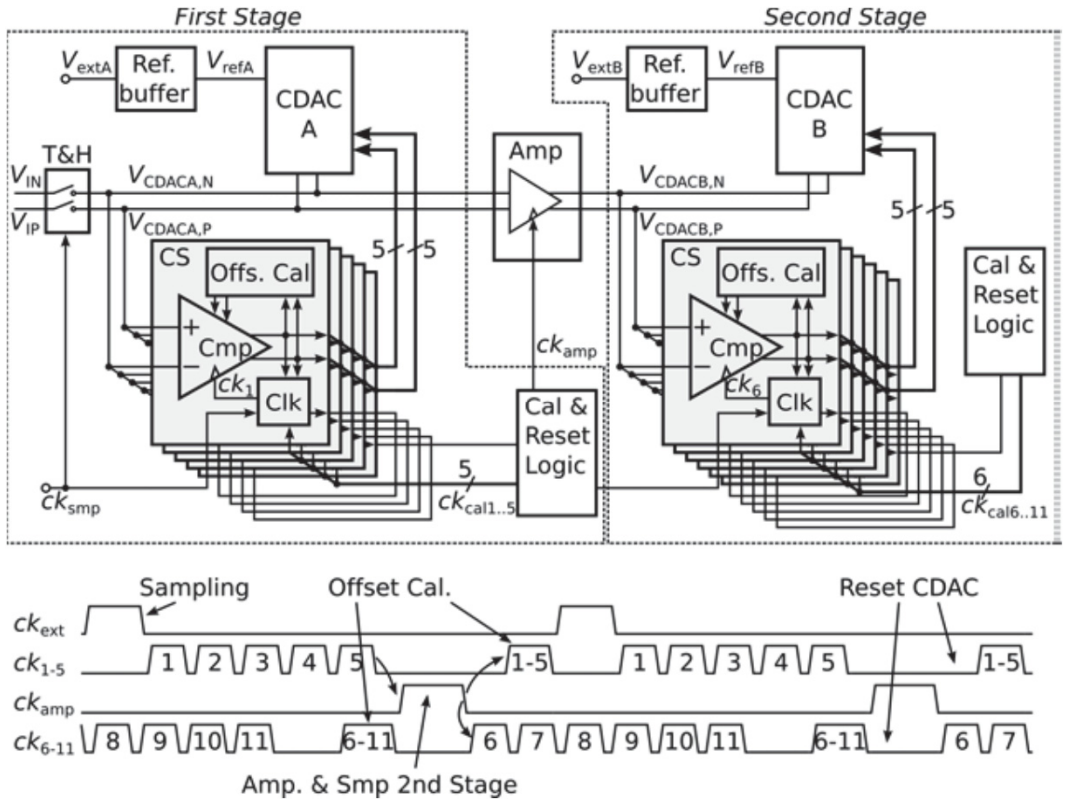
SAR ADC

- Performs a binary search conversion over multiple clock cycles
- Simplest implementations only require one comparator per unit ADC
- Slower unit ADC relative to flash/binary search
  - Typical interleave factors of 32-64
- Excellent choice for 6-8b resolution to support both PAM2 and PAM4
- The dominant architecture for PAM4 ADC-based receivers



Pipeline SAR ADC

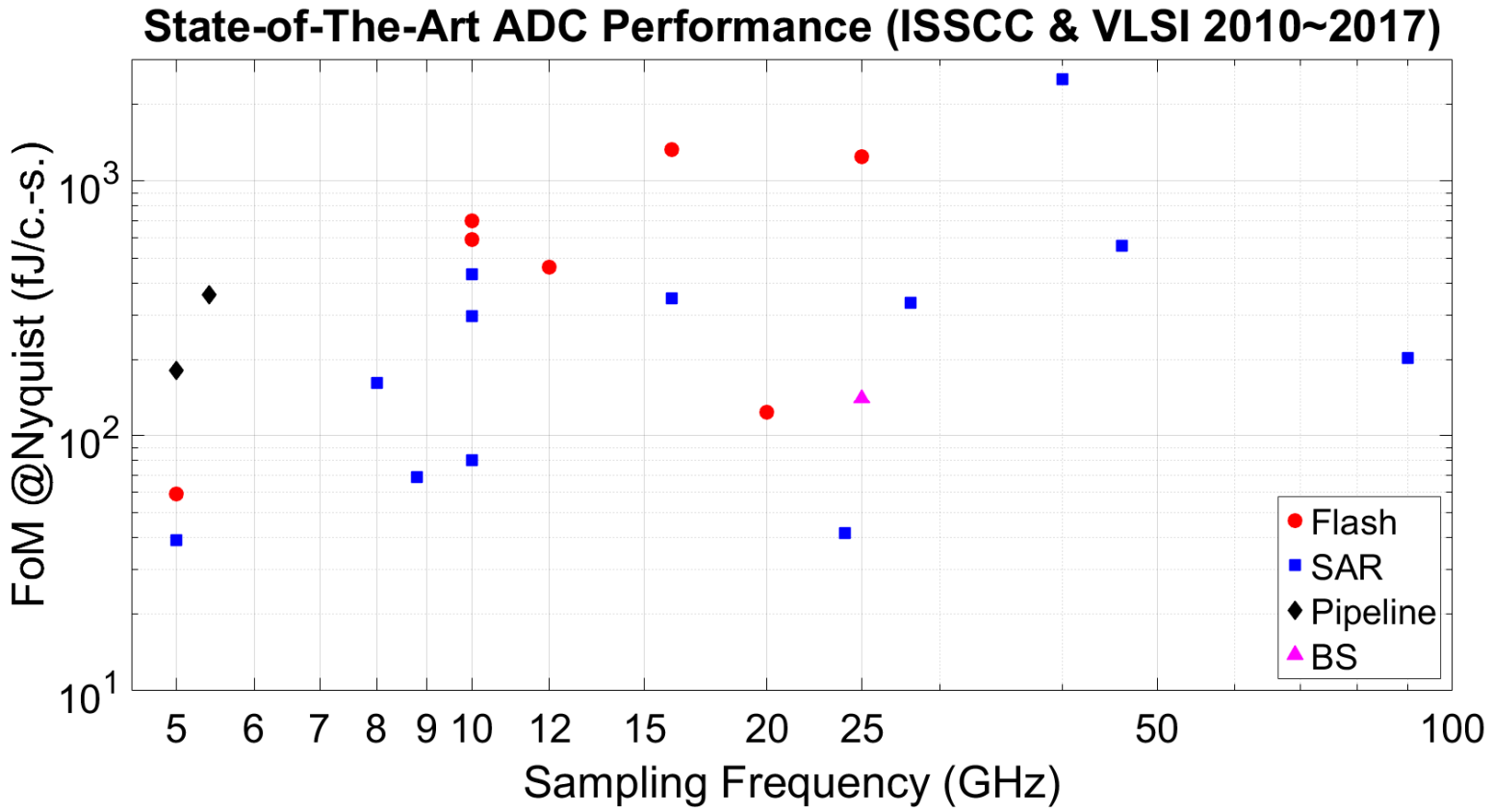
- Looking forward, pipeline SAR architectures are attractive in order to further push sample rates (100+Gb/s)
- Pipelining allows for higher sample rate and fewer unit ADCs
- Inter-stage gain block can reduce impact of comparator noise to allow for higher resolution



[Kull ISSCC 2017]

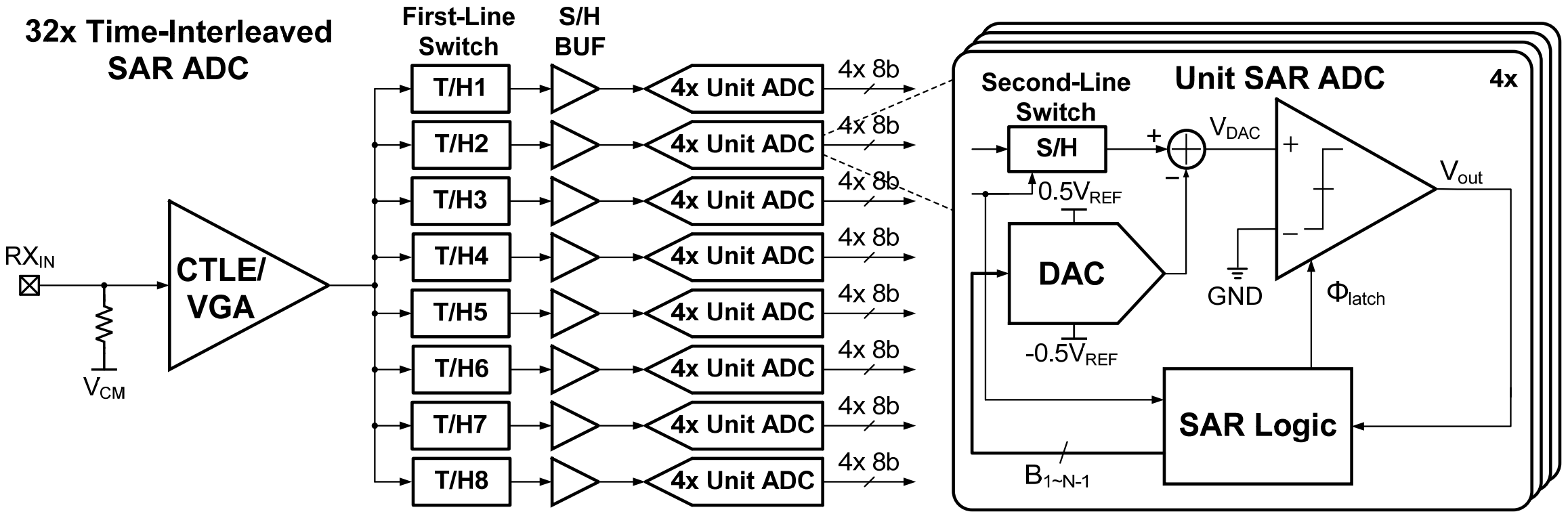
State-of-the-Art ADC Performance

$$FoM = \frac{Power}{2^{ENOB} \cdot f_s}$$



- SAR is the most popular architecture and provides best power efficiency for >10GS/s 6~8b ADC design

Time-Interleaved ADCs



- Wireline ADCs are time-interleaved to achieve high sample rates
- As the SAR ADC is the dominant wireline ADC architecture, we will walk through it's key circuits

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- Digital Equalization
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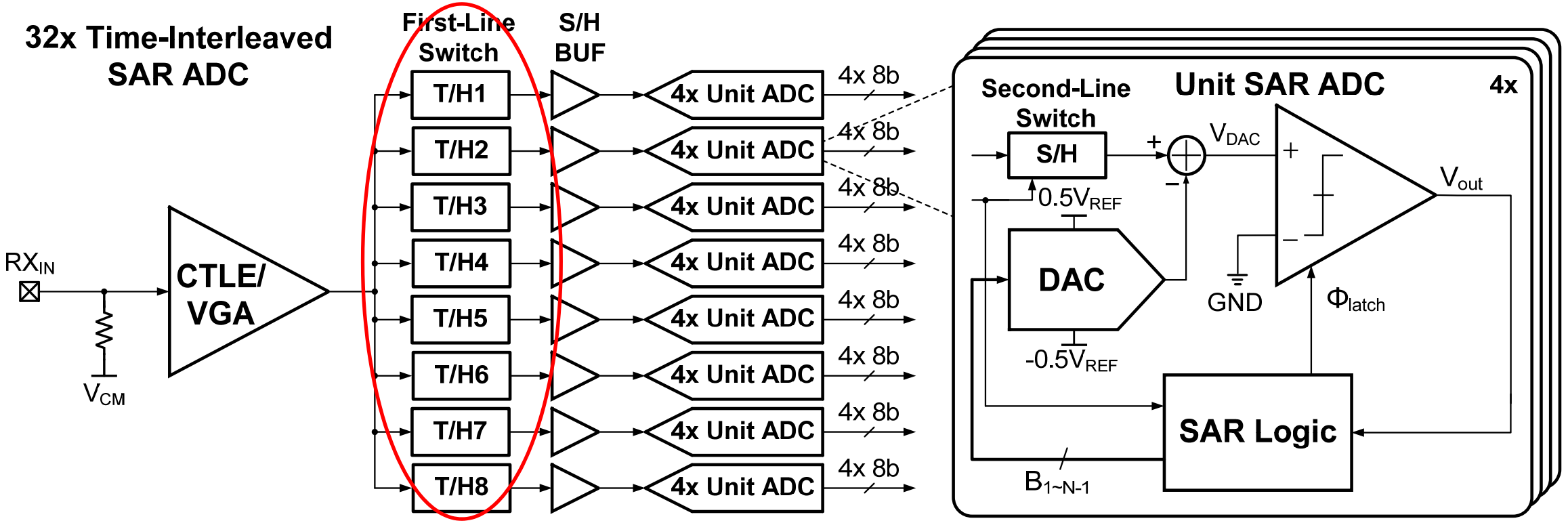
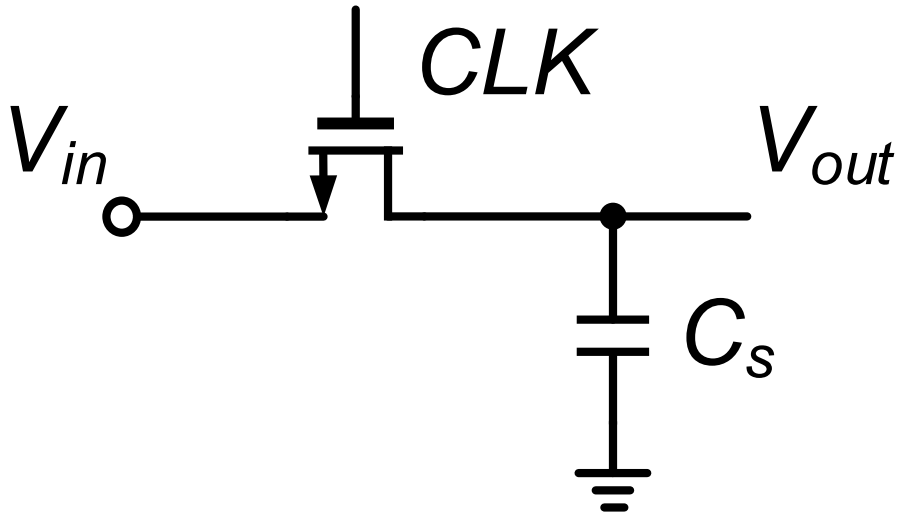
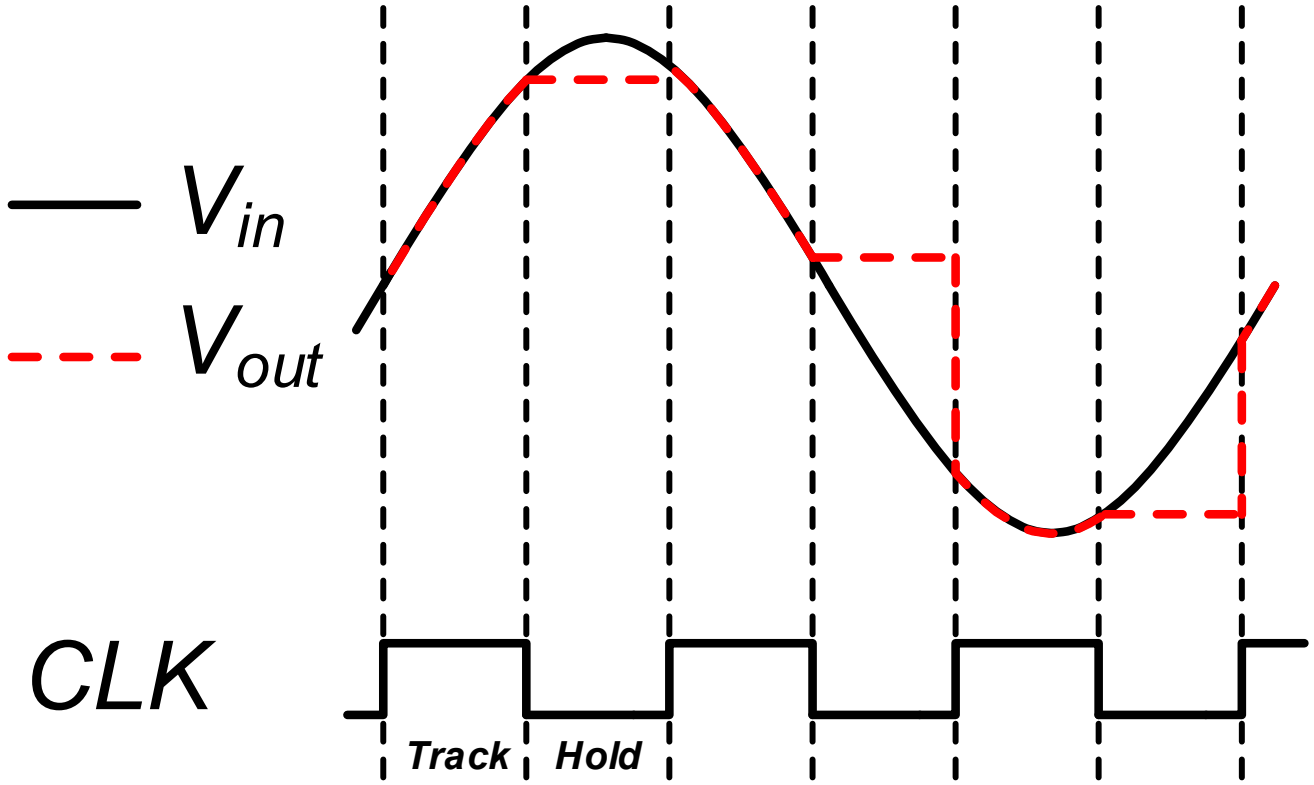
Time-Interleaved ADCs



- Because we can only generate a relatively small number of low-jitter, low-skew clock phases (4-16), input sampling is performed in 2 stages
- The input T/H must track and sample (hold) the full-bandwidth input signal for further sampling to the unit ADCs

Input T/H





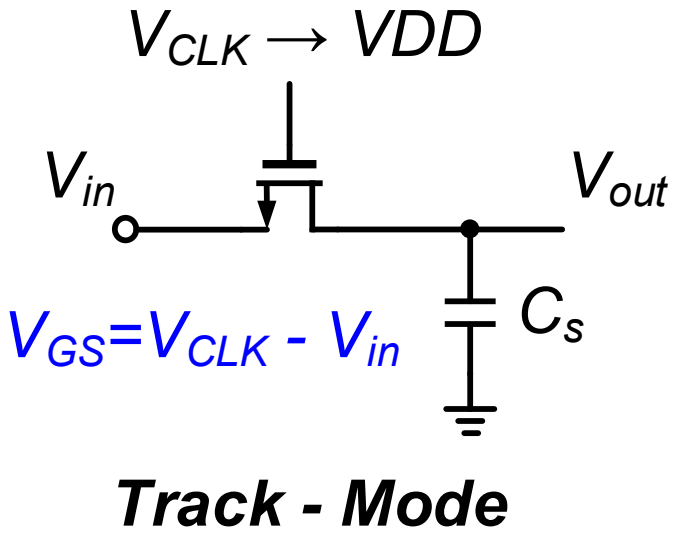
- Issues
  - On-resistance
  - Signal-dependent hold instant
  - Hold-mode input feedthrough

Signal-Dependent On-Resistance & Sample Point

During track-mode, the MOS operates in triode

$$I_D = \mu C_{OX} \frac{W}{L}\left(V_{GS} - V_{TH} - \frac{V_{DS}}{2}\right)V_{DS}$$

$$R_{ON} \cong \left[\left.\frac{dI_{D(triode)}}{dV_{DS}}\right|_{V_{DS}\to 0}\right]^{-1} = \frac{1}{\mu C_{OX}\frac{W}{L}(V_{CLK} - V_{IN} - V_{TH})}$$



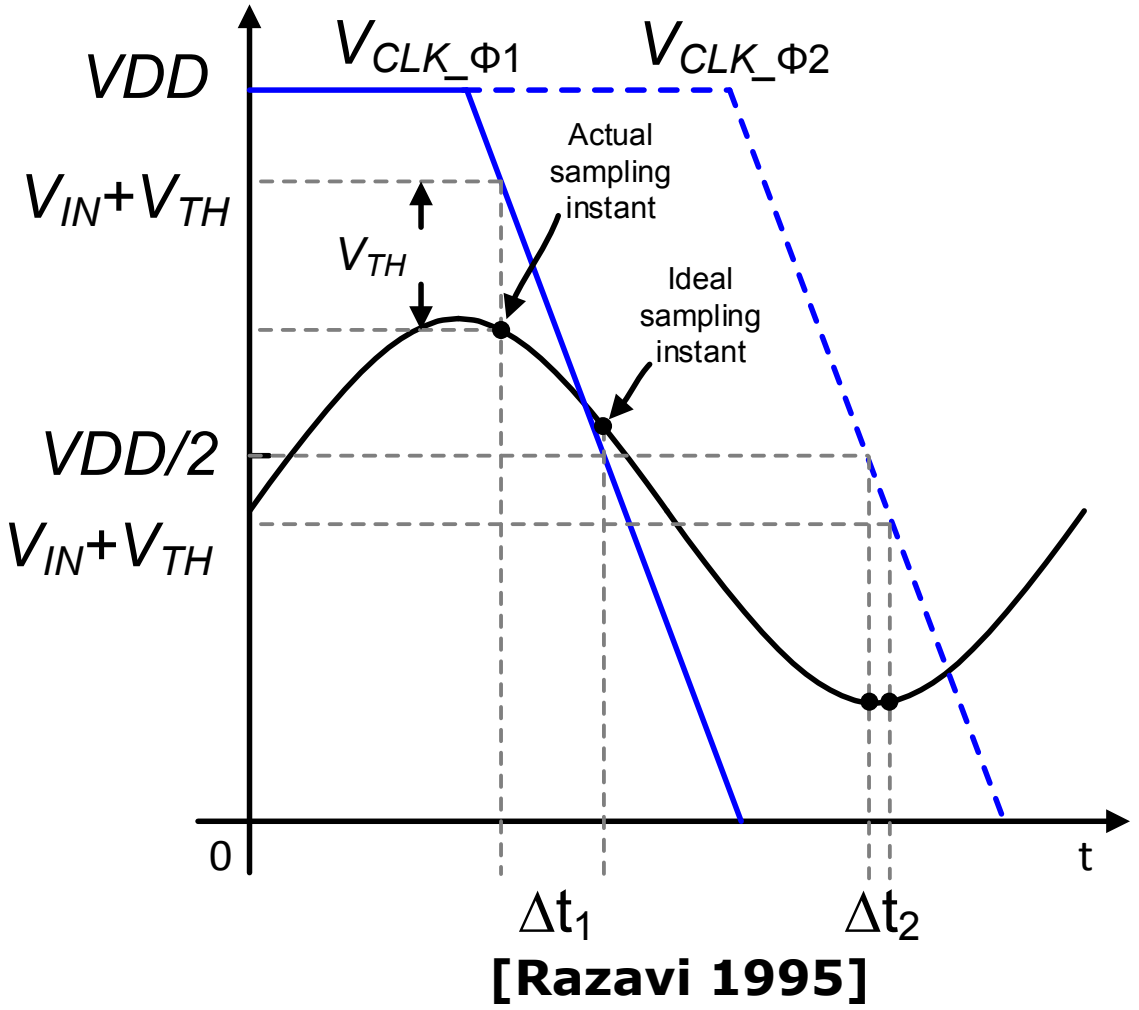
- Issues
  - R_{ON} is modulated by V_{IN} → Distortion
  - Signal dependent hold instant, occurs when $V_{CLK} = V_{IN} + V_{TH}$

Signal-Dependent On-Resistance & Sample Point

The signal is sampled when

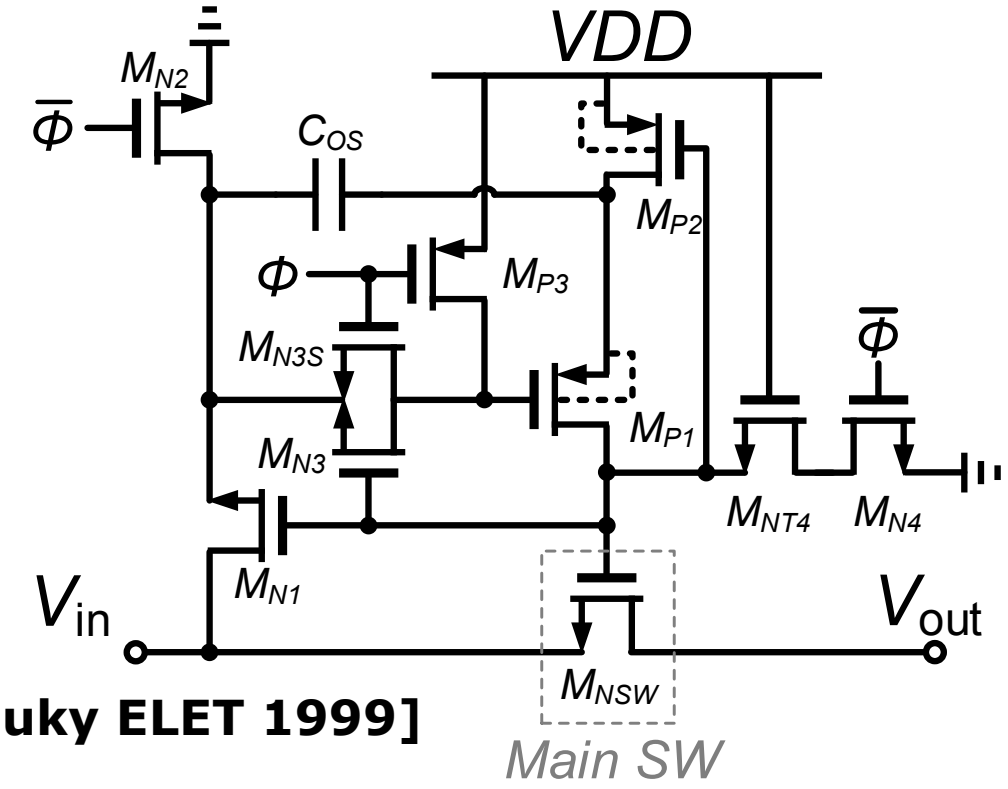
$$V_{CLK} = V_{IN} + V_{TH}$$

- The sampling clock fall time should be much faster than the maximum dV_{IN}/dt to minimize the sampling point mismatch

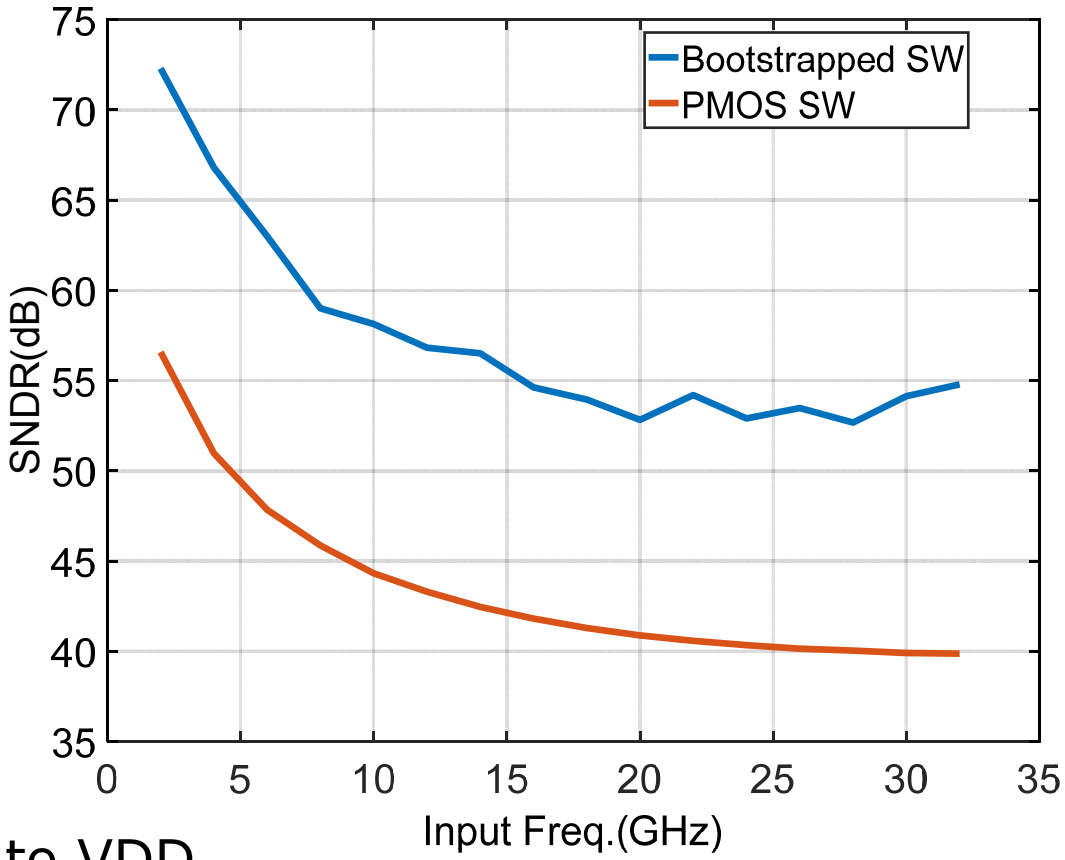


[Razavi 1995]

Bootstrapped Switch

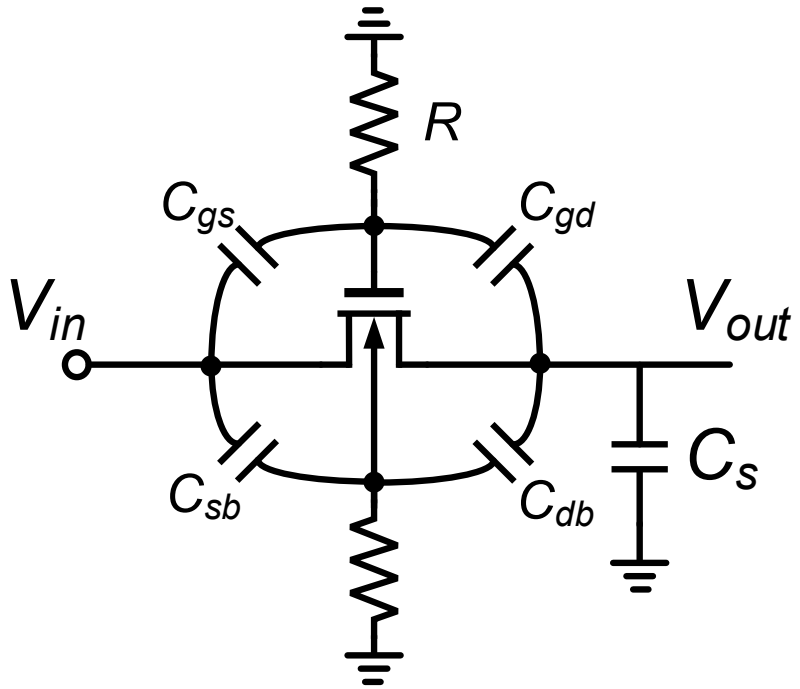


[Dessouky ELET 1999]



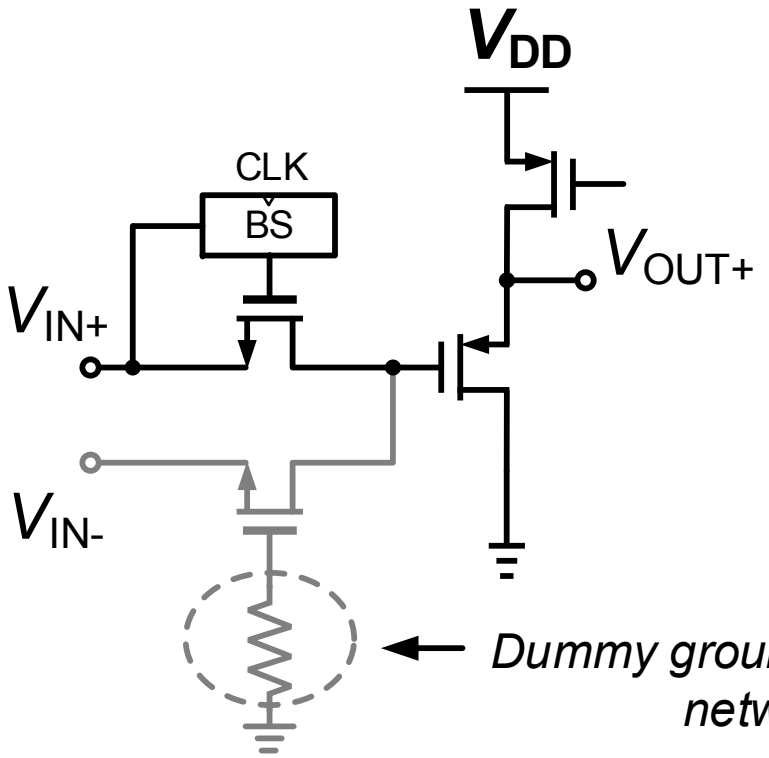
- $\Phi = 0$, switch off and C_{OS} is precharged to VDD
- $\Phi = 1$, main switch is on with constant V_{GS} = VDD and, to first order, both Ron and sampling instant are signal independent

Hold-Mode Feedthrough



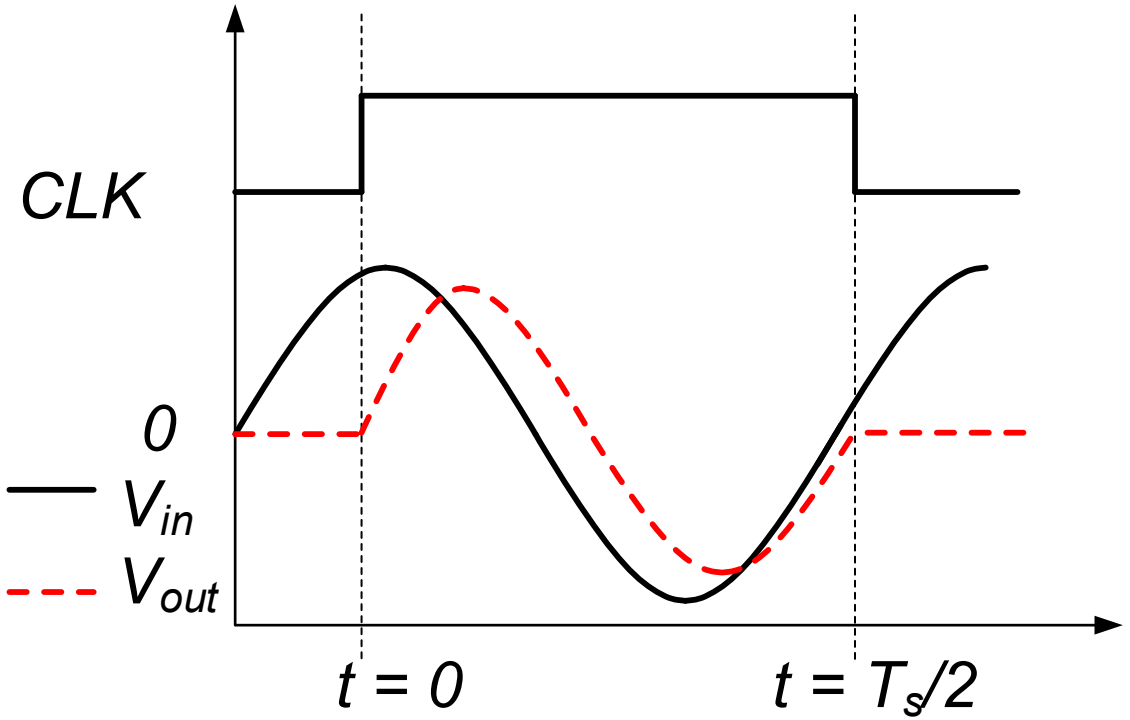
- High-pass feedthrough paths when switch ideally open

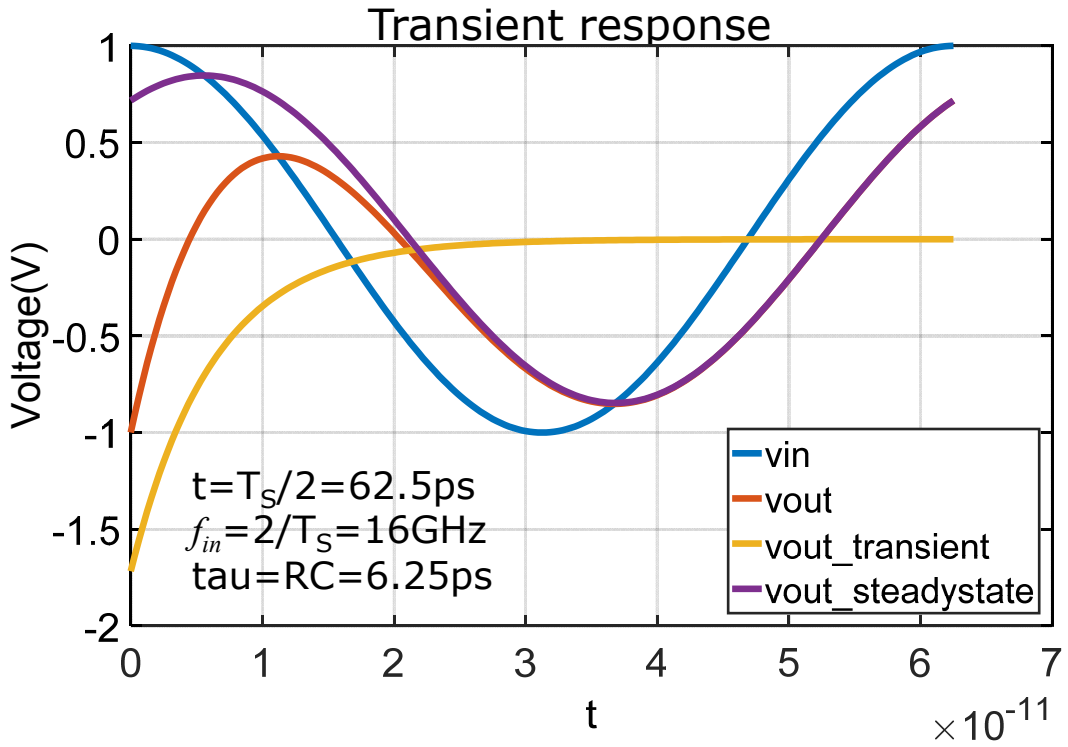
$$\left.\frac{V_{OUT}}{V_{IN}} = \frac{C_{gd}R \cdot s}{(C_{gs} + C_{gd})R \cdot s + 1}\right|_{C_s \gg C_{gs,gd}}$$



- Using a dummy path to generate an opposite feedthrough for cancellation
- Make sure to place a proper impedance on the dummy transistor gate

How Much Track Time?





$$v(t) = -\frac{A\cos(\phi-\theta)}{\sqrt{1+R^2C^2\omega^2}}\cdot e^{-\frac{t}{RC}} + \frac{Acos(\omega t+\phi-\theta)}{\sqrt{1+R^2C^2\omega^2}} - v_{in}(0)\cdot e^{-\frac{t}{RC}}$$

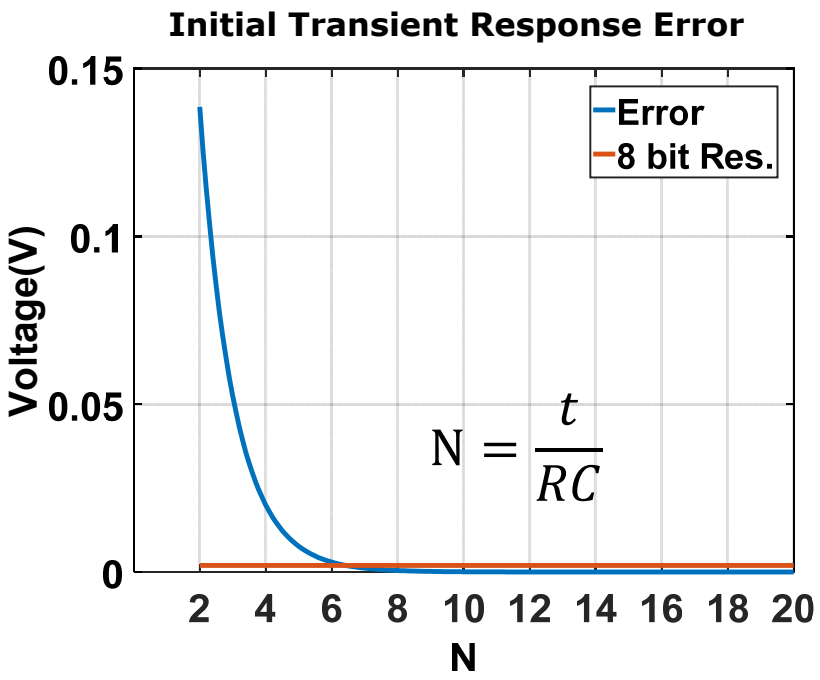
Initial Transient Response **Steady-State Response** **Worst-Case Natural Response**

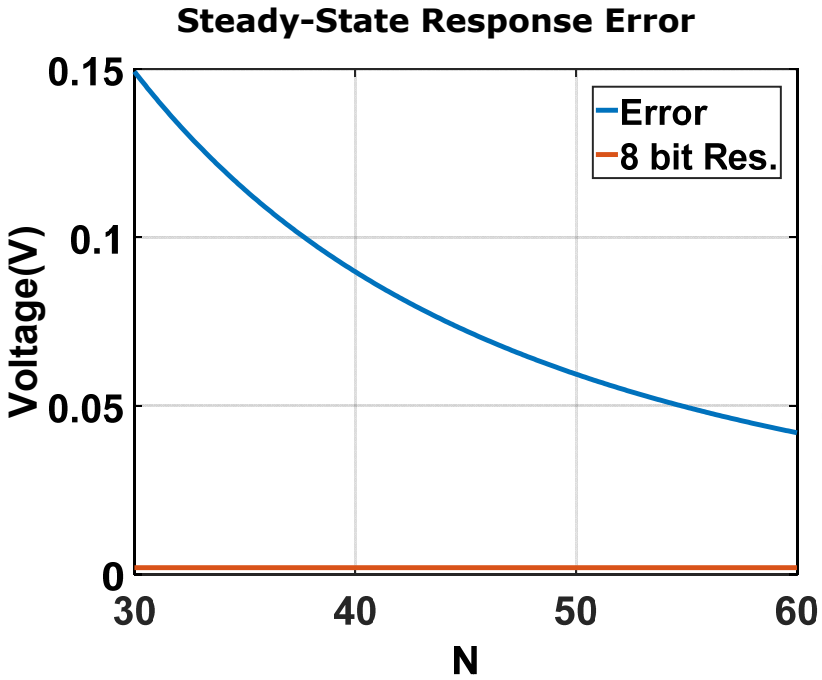
$$\tan\theta = RC\omega, v_{in}(0) = -A$$

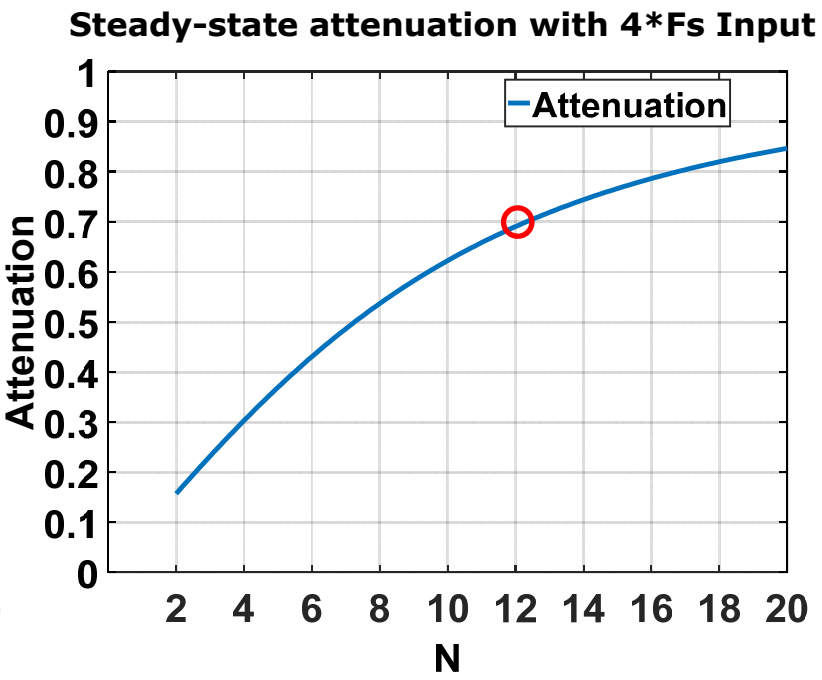
$$v_{in} = -Acos(\omega t+\phi)$$

- The initial transient response (yellow) goes to zero quickly with proper N=t/RC

How Much Track Time?

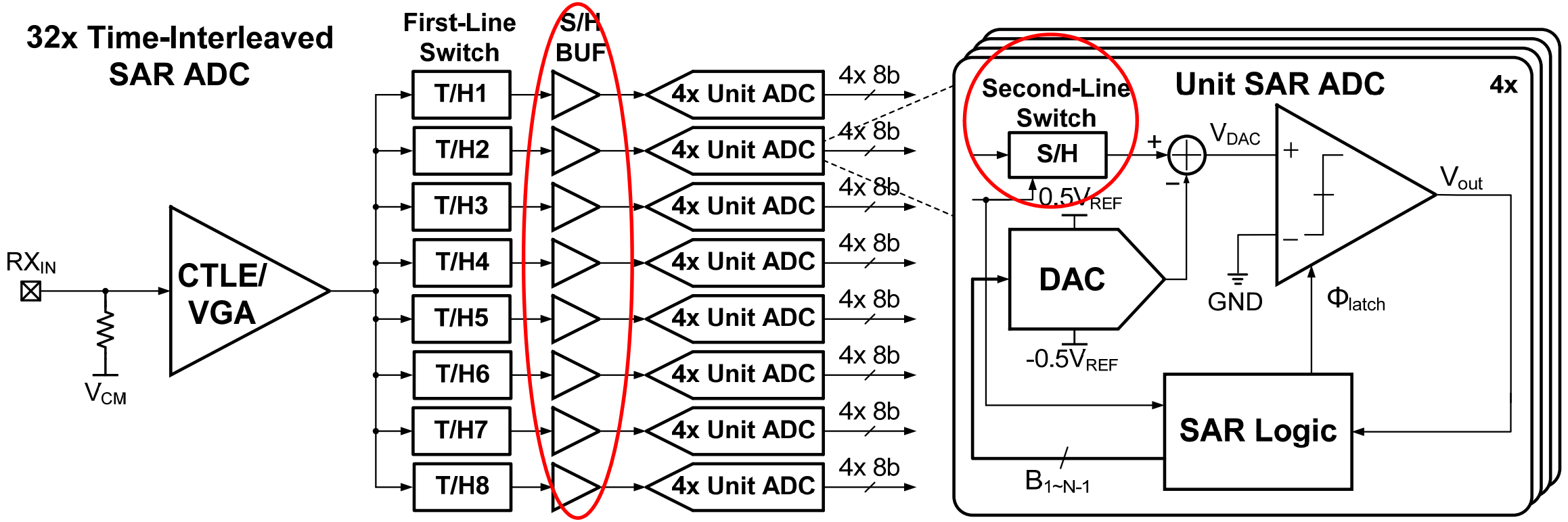






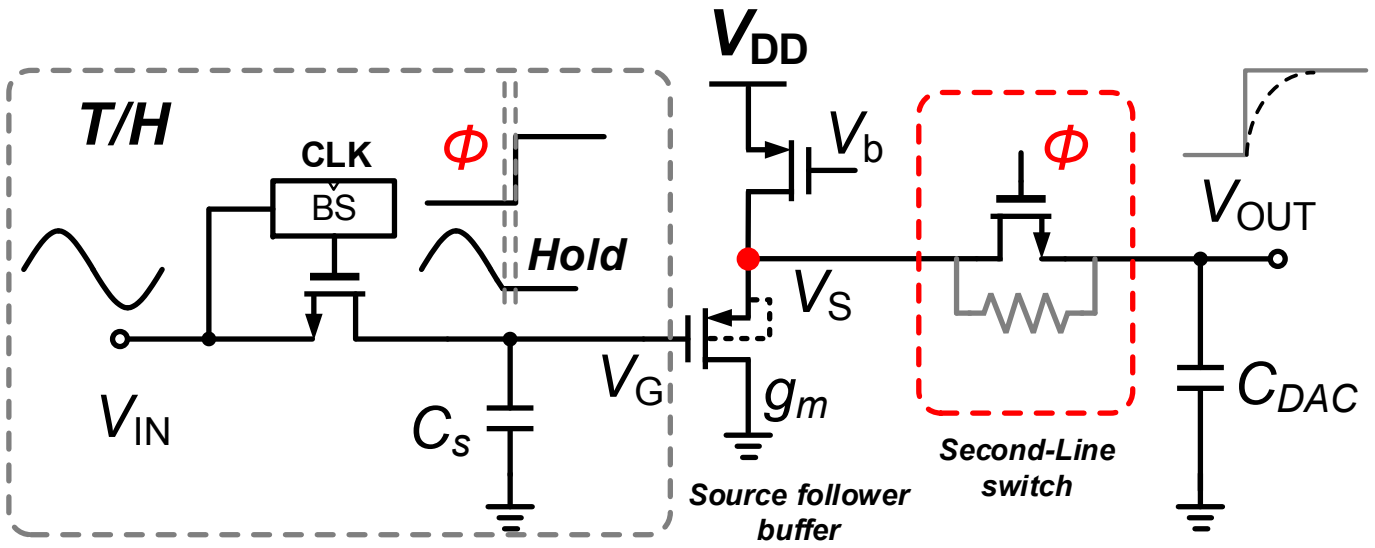
- The initial transient response error can be ignored by an 8 bit system when N>7
- It is unrealistic to lower the steady-state error by dramatically decreasing RC
  - Often compensated by digital equalizer
  - N=12 gives ~0.7x attenuation with a Nyquist input and a common 8-way first-line interleave factor

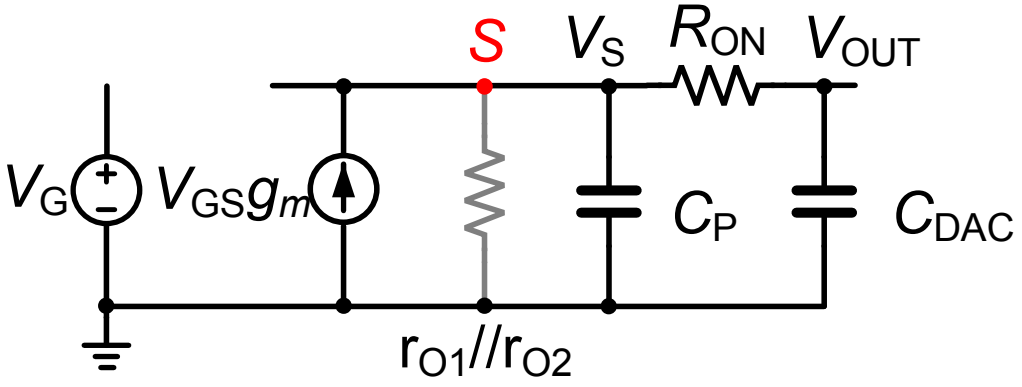
Time-Interleaved SAR ADC: S/H Buffer & Second-Line Switch



- Active buffer isolates ADC loading from the bootstrap switch
- Second-line switch (S/H) output should settle with ε<LSB/2
- As this settling is a function of both the buffer bandwidth and switch time constant, lets consider them together

S/H Buffer & Second-Line Switch





$$C_P \frac{dV_S}{dt} - g_m \cdot V_{GS} + \frac{V_S - V_{OUT}}{R_{ON}} = 0$$

$$V_S = R_{ON} \cdot C_{DAC} \cdot \frac{dV_{OUT}}{dt} + V_{OUT}$$

$$BW \cdot 2\pi = \frac{g_m}{C_P} \qquad k = \frac{C_P}{C_{DAC}} = 2$$

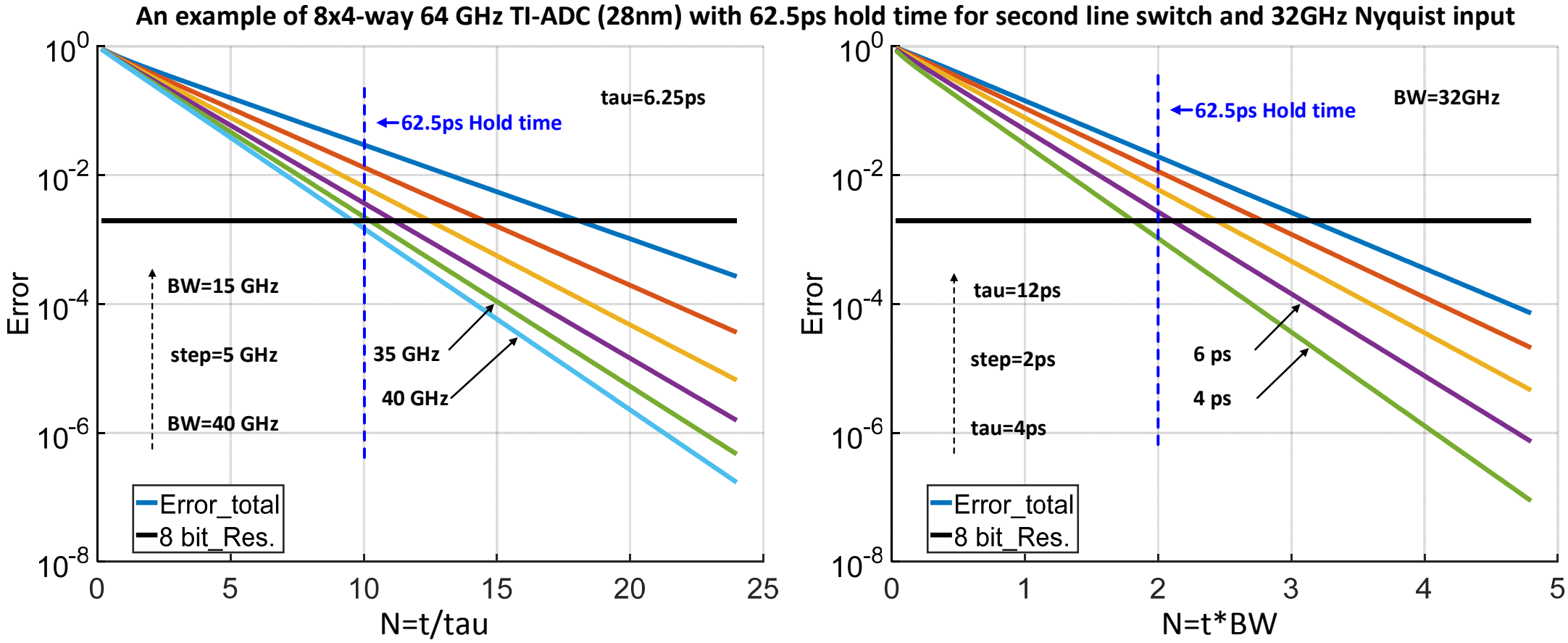
$$\tau = R_{ON} \cdot C_{DAC} \qquad V_{OUT}(0) = 0$$

$$V_S(0) = 1 - \max(|V_G(t) - V_S(t)|)$$

worst initial condition

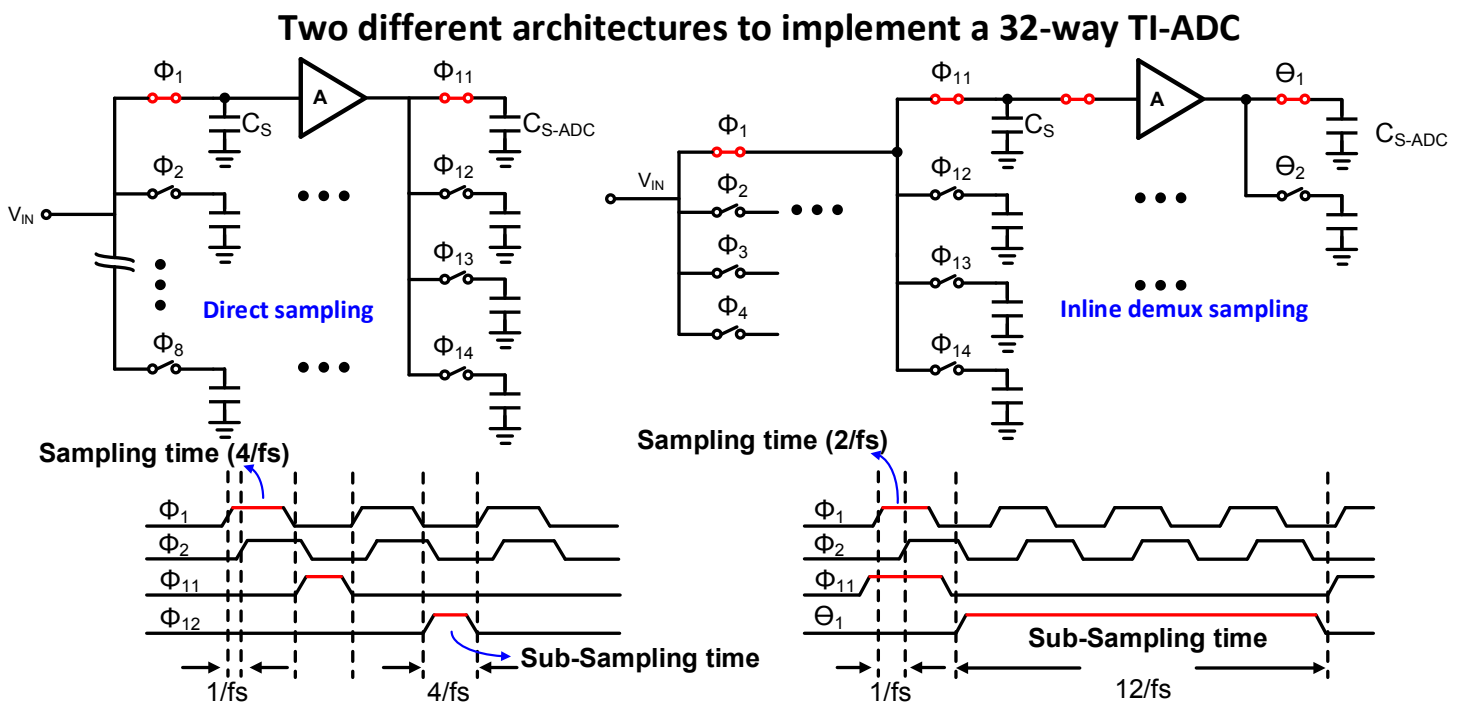
- The settling time of V_{OUT} is related both to the buffer BW and switch τ
- The worst case is when V_{OUT} settles from '0' to max amplitude with a Nyquist input
- Note that C_P can be larger than C_{DAC} due to long routing from buffer to unit-ADCs

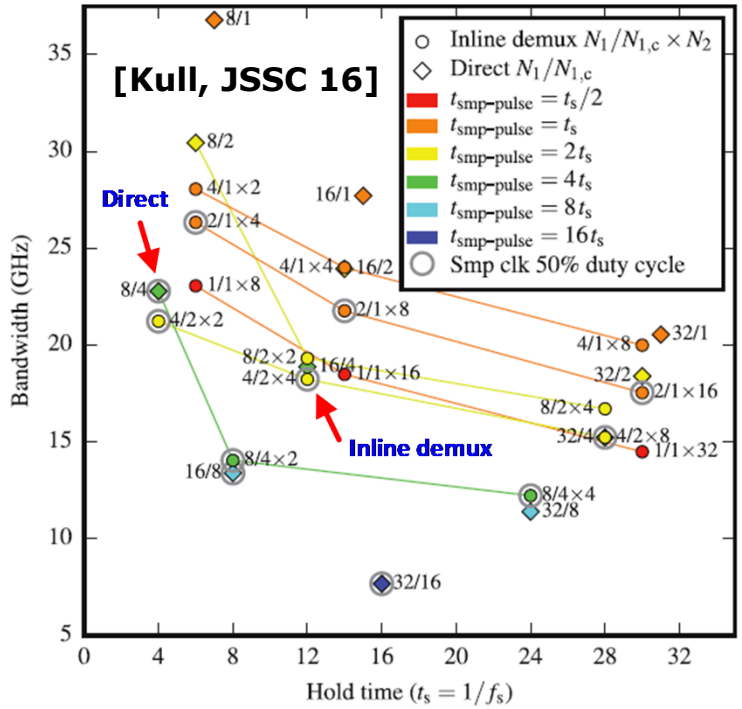
S/H Buffer & Second-Line Switch: 64GS/s Example



- For tau=6.25, the source follower BW should be larger than 35GHz for 8 bits
- A smaller BW=32GHz allows lower source follower power, but need smaller $\tau \approx 5$ ps

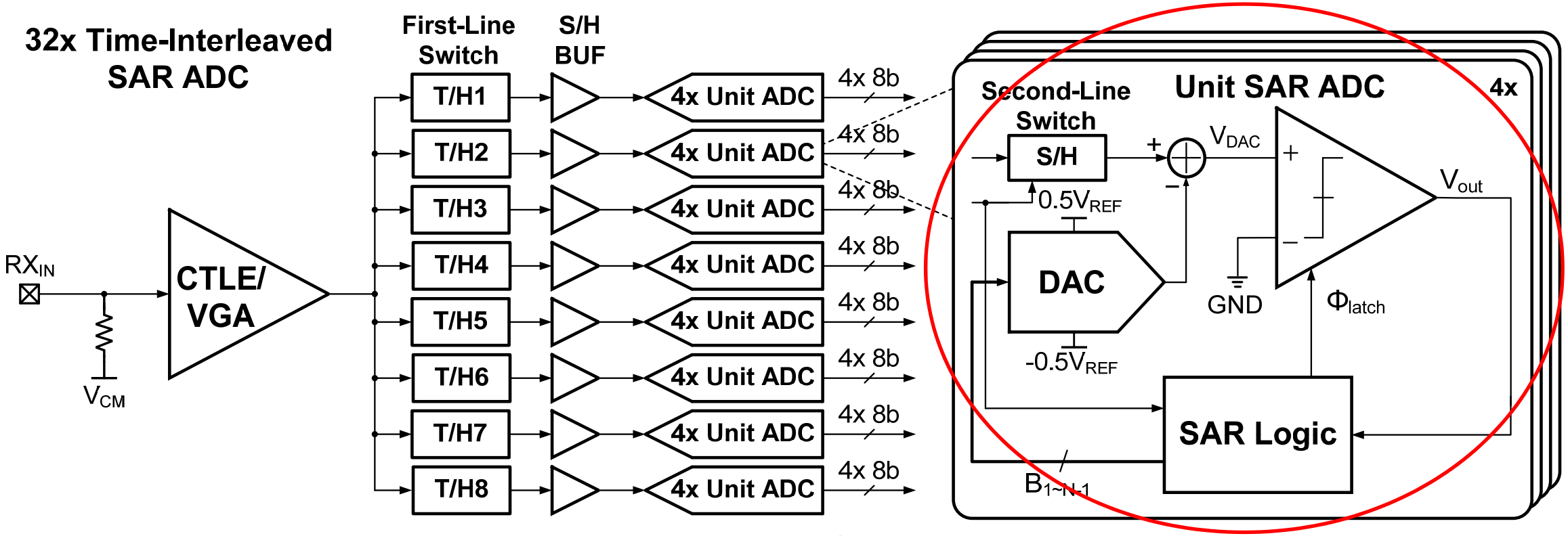
Time-Interleaving Sampling Architectures





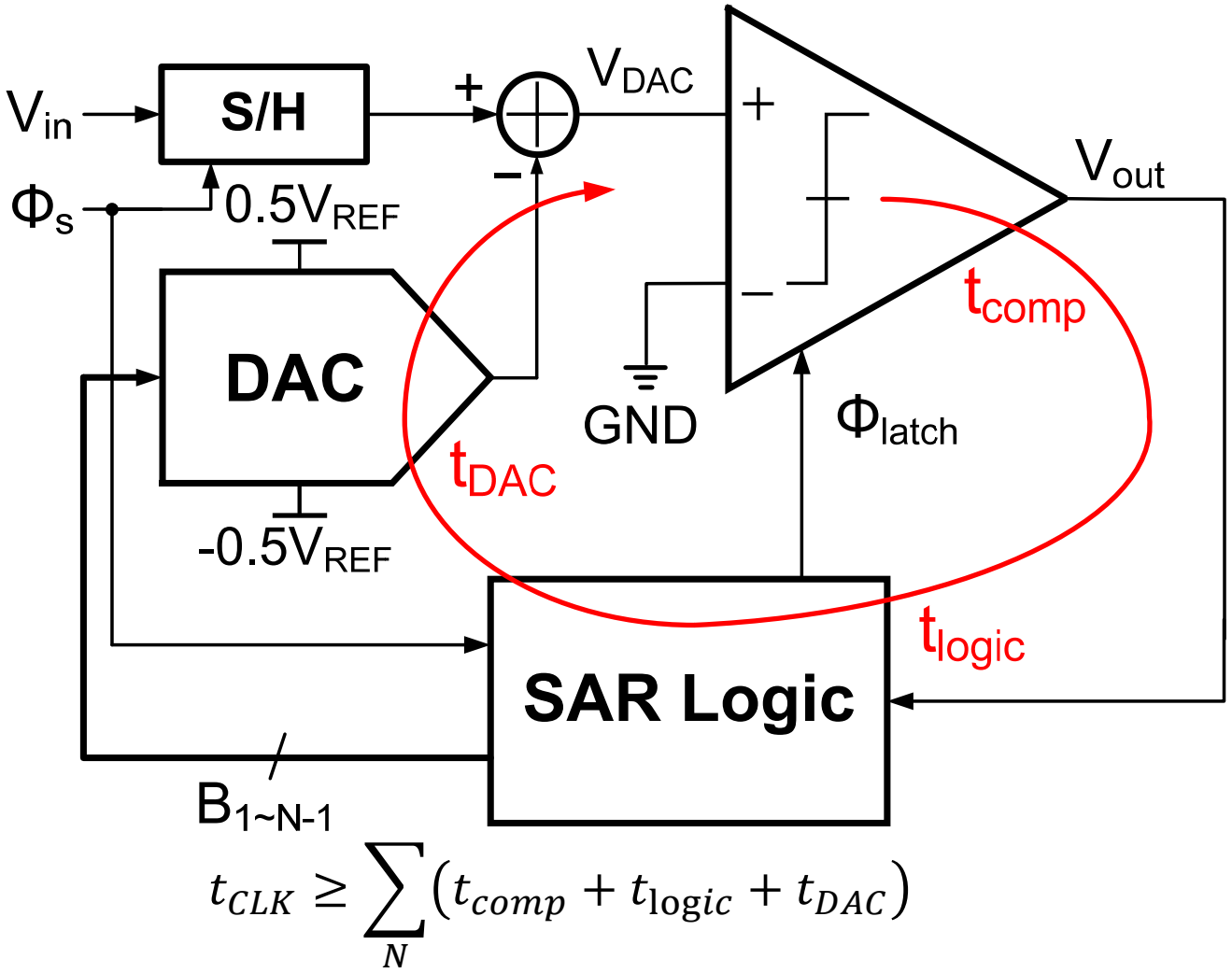
- Direct sampling has better BW due to the shortest path from V_{IN} to the C_{DAC}. But the sub-sampling time (second-line SW hold time) is just 4/fs (50% duty cycle).
- Serialized SW (ϕ_1, ϕ_{11}) lowers the BW of the inline demux arch, but allows for an increased hold time and a relaxed buffer design
  - Note, this often requires a higher sampling clock, which also decreases sampling time

Time-Interleaved SAR ADC: Unit ADC



- Unit SAR ADC speed sets the interleave factor
- It's noise and linearity limit the achievable ADC ENOB
- Mismatches between the unit ADCs (and the preceding individual T/Hs and S/H buffers) will need to be calibrated

Unit SAR ADC: Critical Timing Path

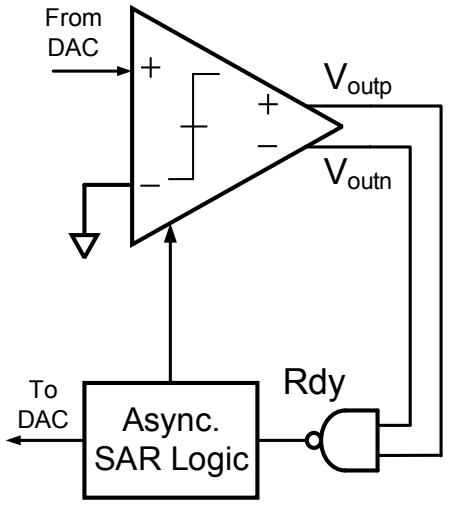


$$t_{CLK} \geq \sum_{N} \left(t_{comp} + t_{\log ic} + t_{DAC} \right)$$

- SAR ADC consists of S/H, DAC, comparator and SAR logic
- The conversion speed of SAR ADCs depends on the delay from comparator, logic and DAC in the critical timing path
- Various techniques to reduce the delay for faster SAR ADC speed

Unit SAR ADC: Advanced Techniques

- Asynchronous SAR operation

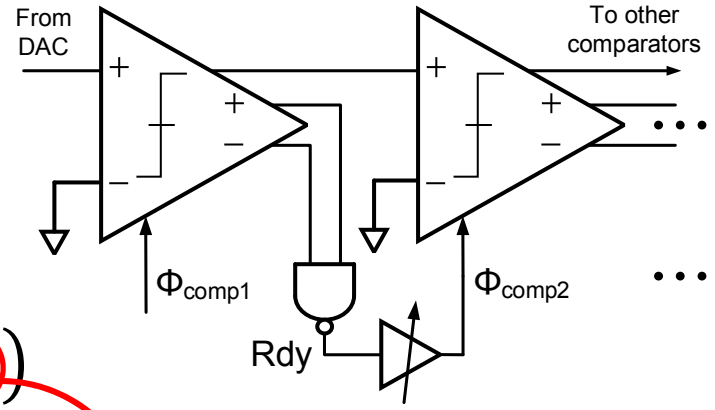


$$\sum_{i=0}^{N-1} \ln\left(\frac{V_{FS}}{V_{DAC}(i)}\right)$$

[Chen JSSC 2006]

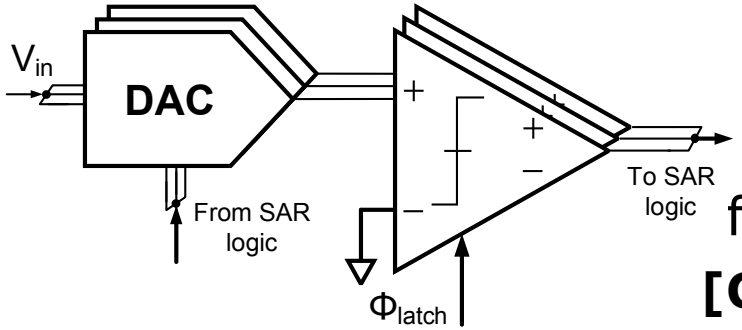
$$t_{CLK} \geq \sum_{N} \left(t_{comp} + t_{logic} + t_{DAC}\right)$$

- Loop-unrolled SAR



[Jiang JSSC 2012]

- Multi-bit/stage conversion

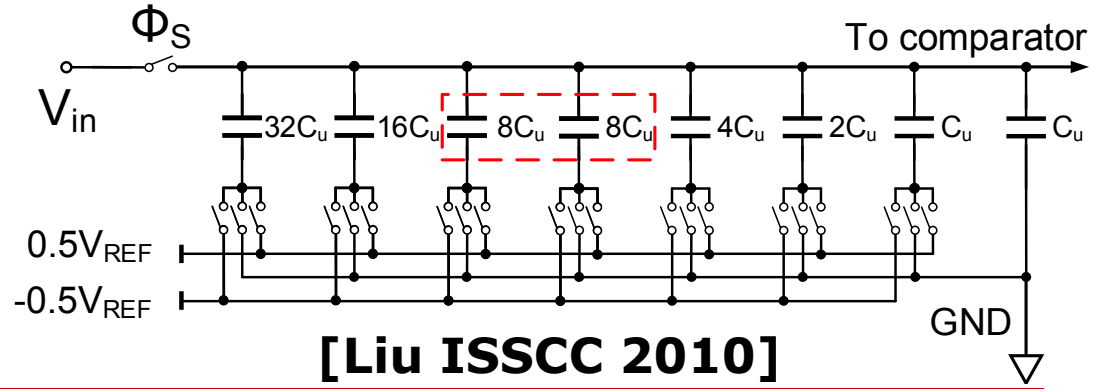


$$N' = \left\lceil \frac{N}{M} \right\rceil$$

for M-bit/stage

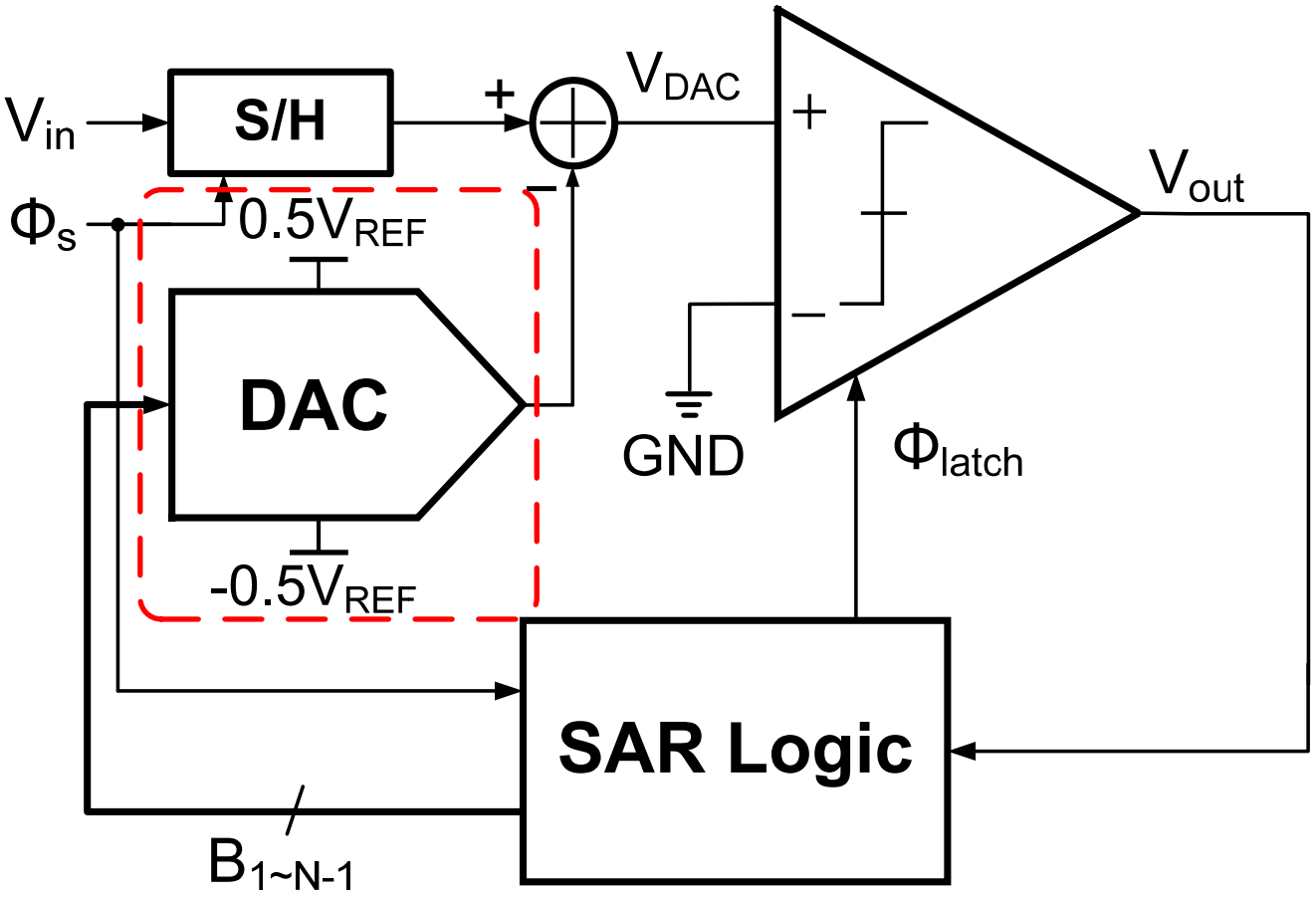
[Cao JSSC 2009]

- Redundant SAR algorithm (trade-off N)



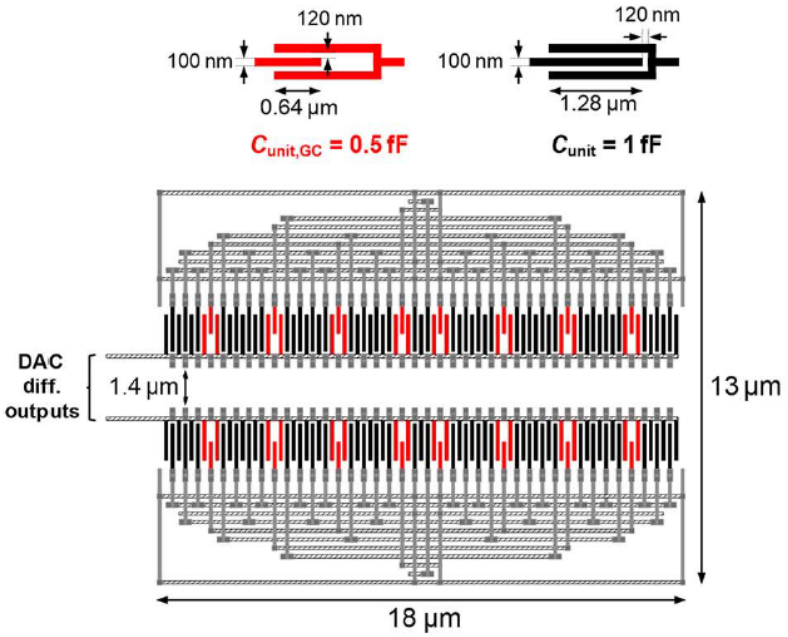
[Liu ISSCC 2010]

DAC

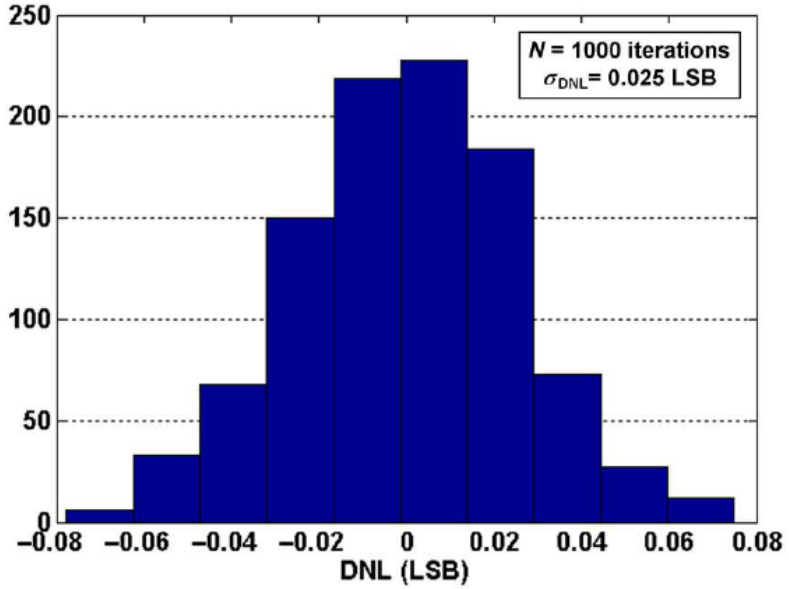


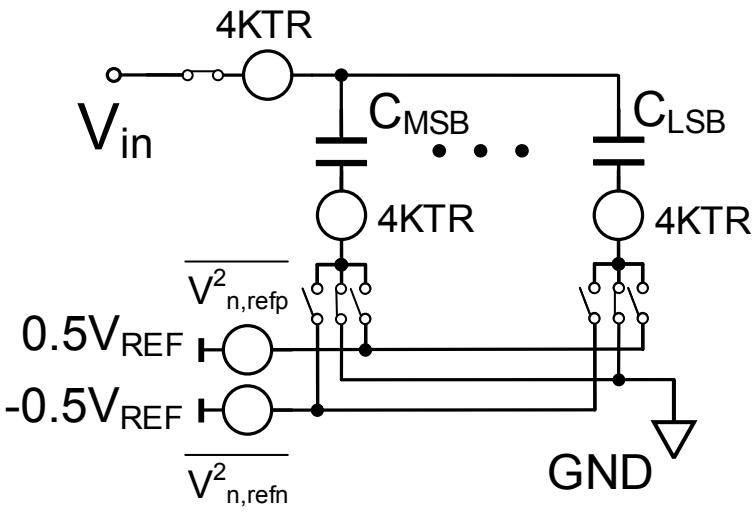
- DAC generates residue signals by subtracting binary weighted reference from input
- Capacitive DAC is the most popular DAC structure due to low power consumption

DAC Implementation



Worst case error w/ cap mismatch

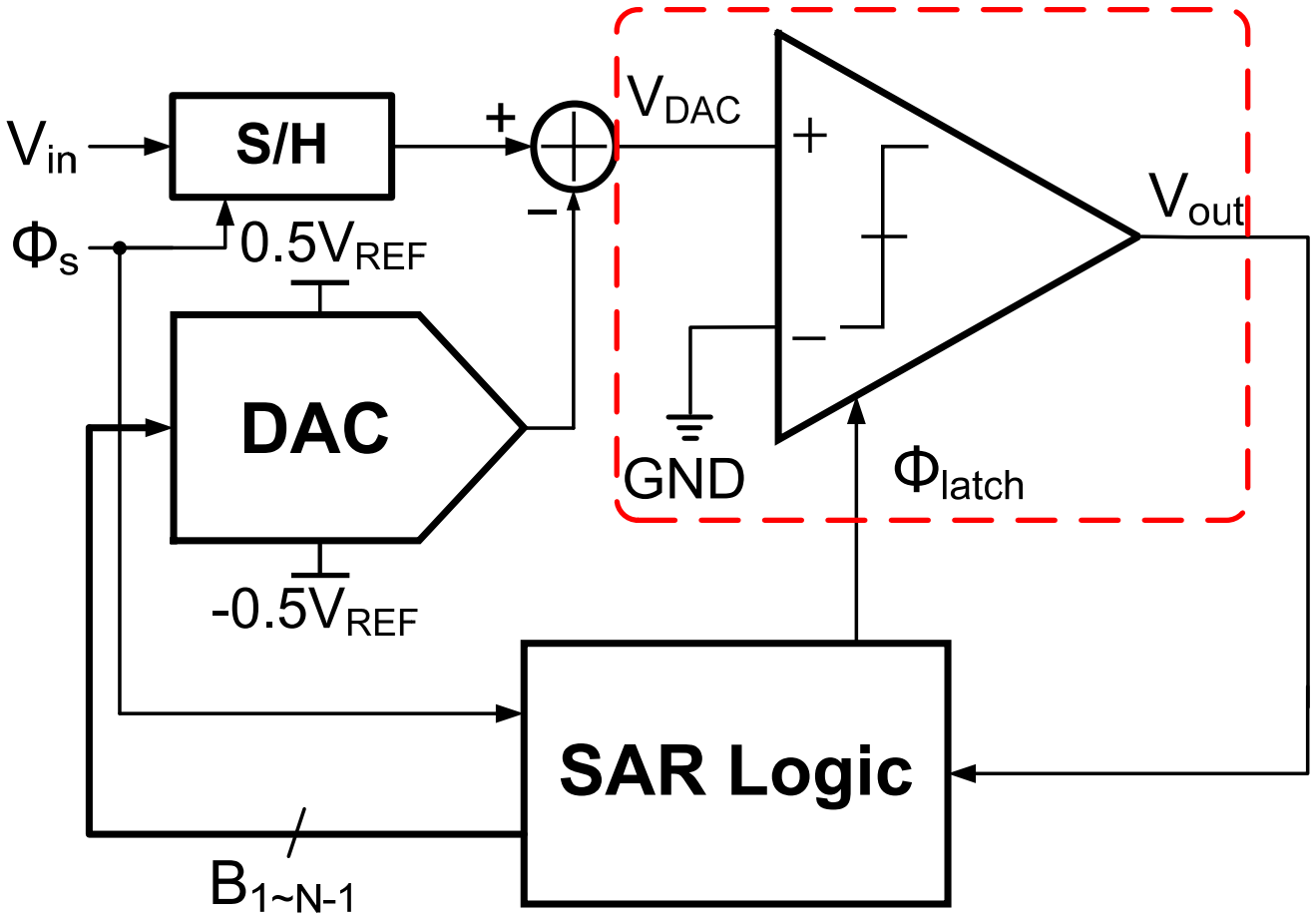




[Shafik JSSC 2016]

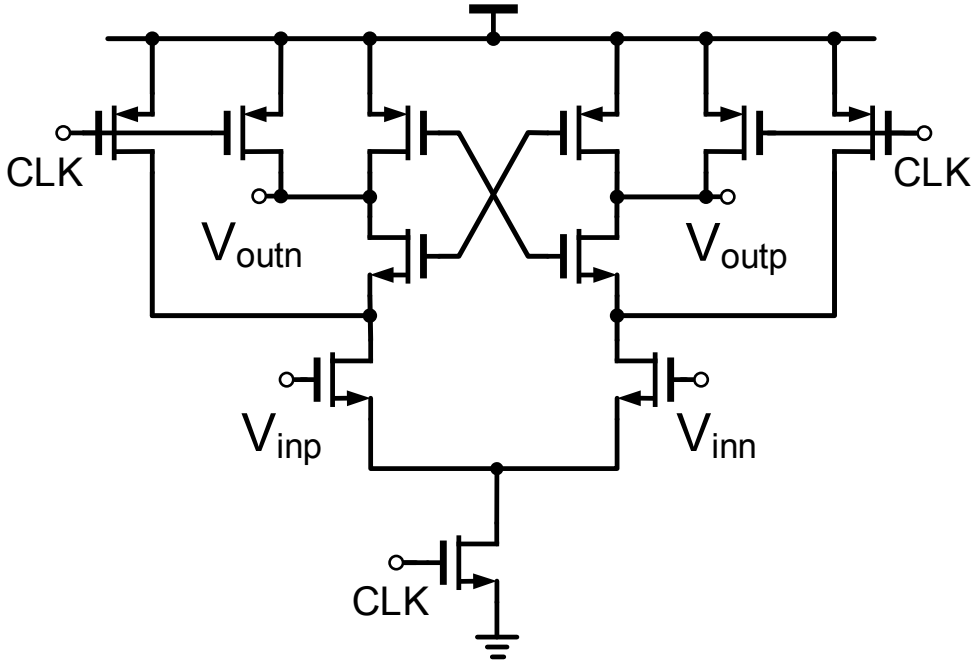
- Minimize cap size for medium resolution SAR (6~8bit)
- Minimum unit cap size limited by matching requirement and KT/C noise (noise usually dominated by front-end and comparator)

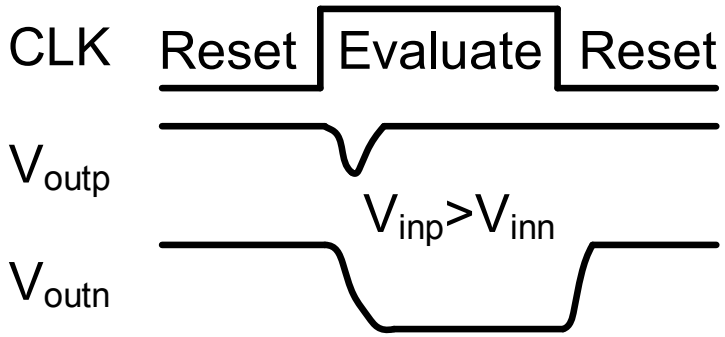
Comparator



- Comparator makes decision on the DAC signal and generates binary search codes for SAR logic and DAC

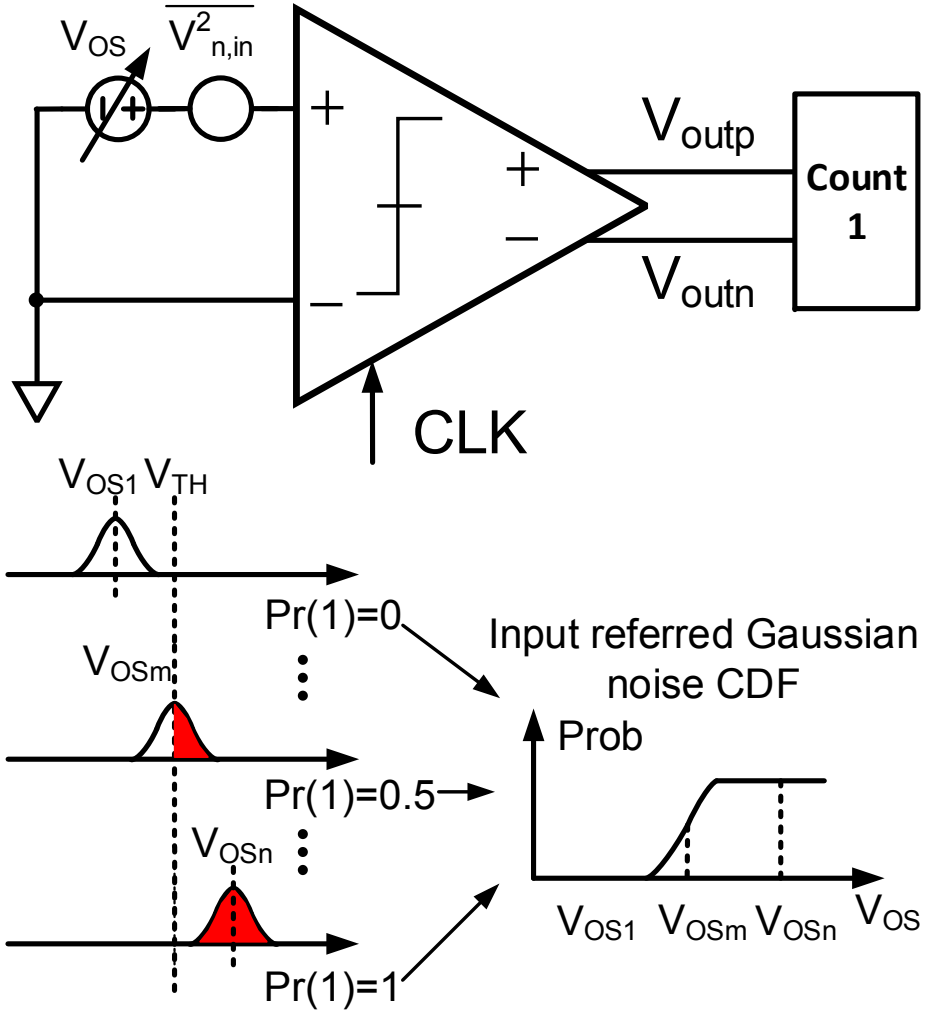
Dynamic Comparator





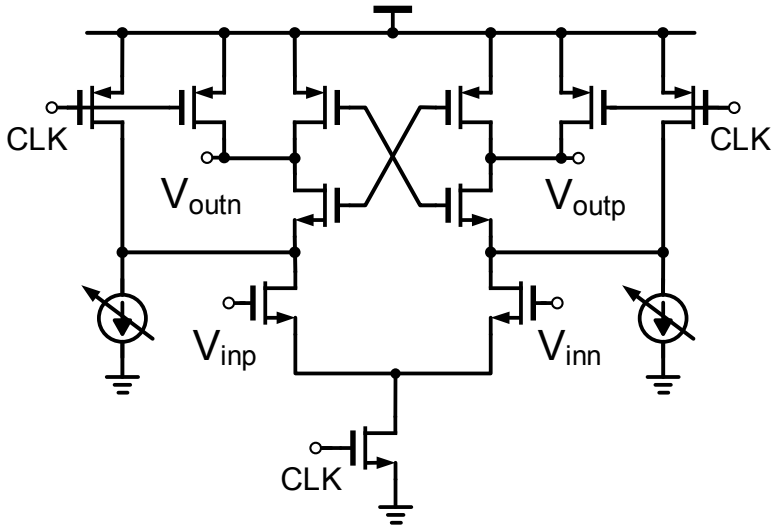
- Dynamic latch specs
  - Noise
  - Offset
  - Metastability

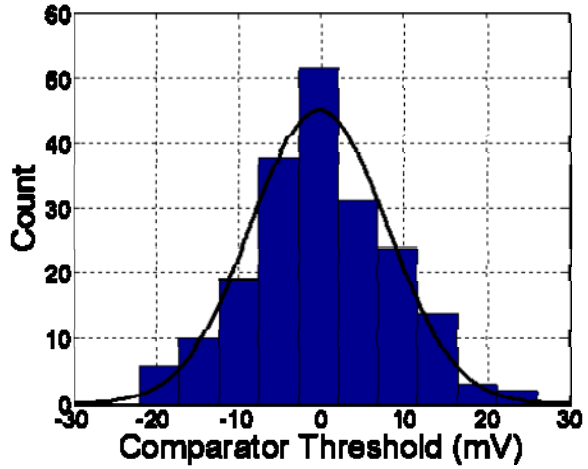
Comparator Noise



- Device noise causes random decisions even with zero input signal
- Noise variance can be found by fitting output to a Gaussian CDF as the input is swept and transient noise is enabled
- Noise can also be simulated with PSS+PAC+PNOISE, but requires post processing to find ISF from sideband transfer function [Kim TCAS-I 2009]

Comparator Offset



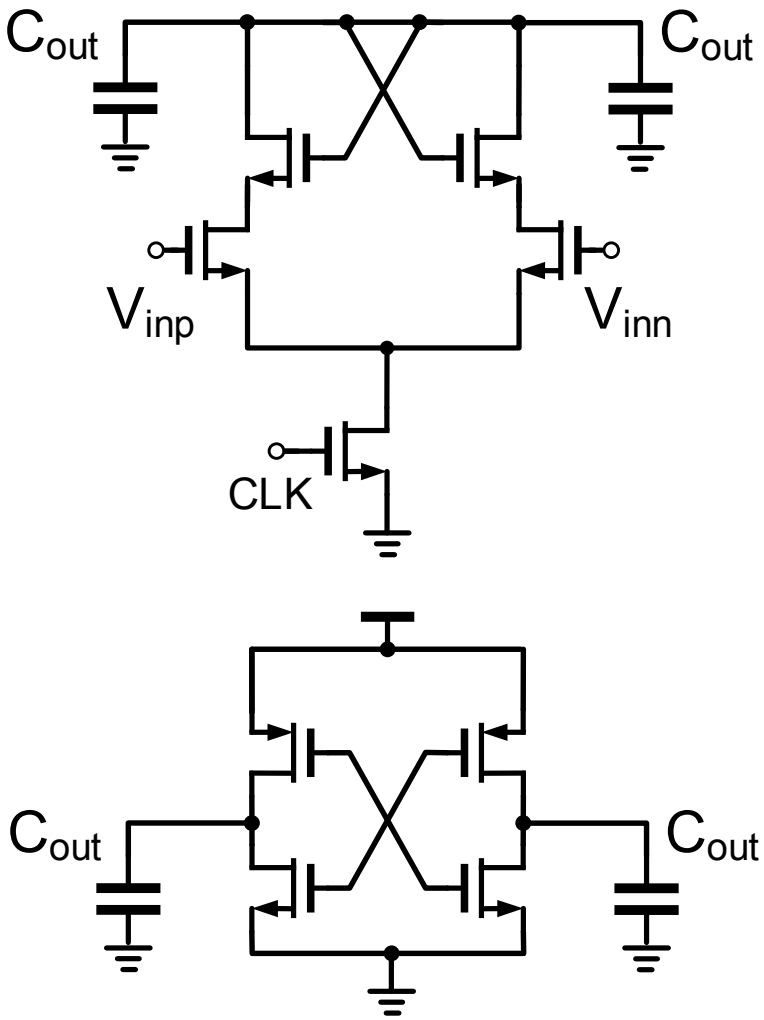


- The input referred offset is primarily a function of Vth mismatch and a weaker function of β (mobility) mismatch

$$\sigma_{V_t} = \frac{A_{V_t}}{\sqrt{WL}}, \quad \sigma_{\Delta\beta/\beta} = \frac{A_\beta}{\sqrt{WL}}$$

- To reduce input offset 2x, we need to increase area 4x
- Not practical due to excessive area and power consumption
- Offset correction necessary to efficiently achieve good sensitivity

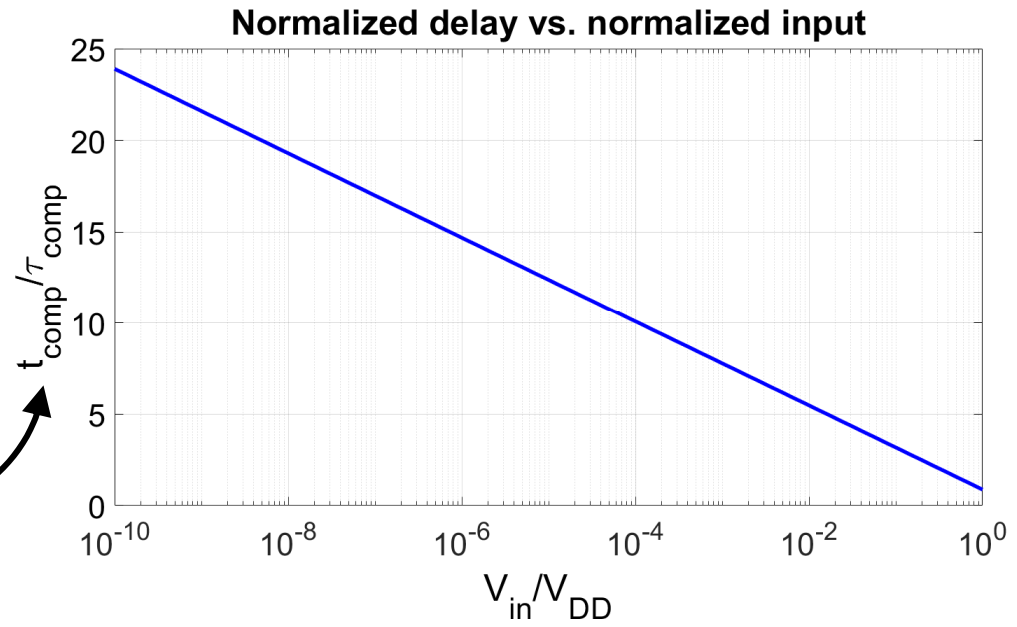
Comparator Metastability



$$t_{samp} \sim \frac{C_{out} V_{THP}}{I_D}$$

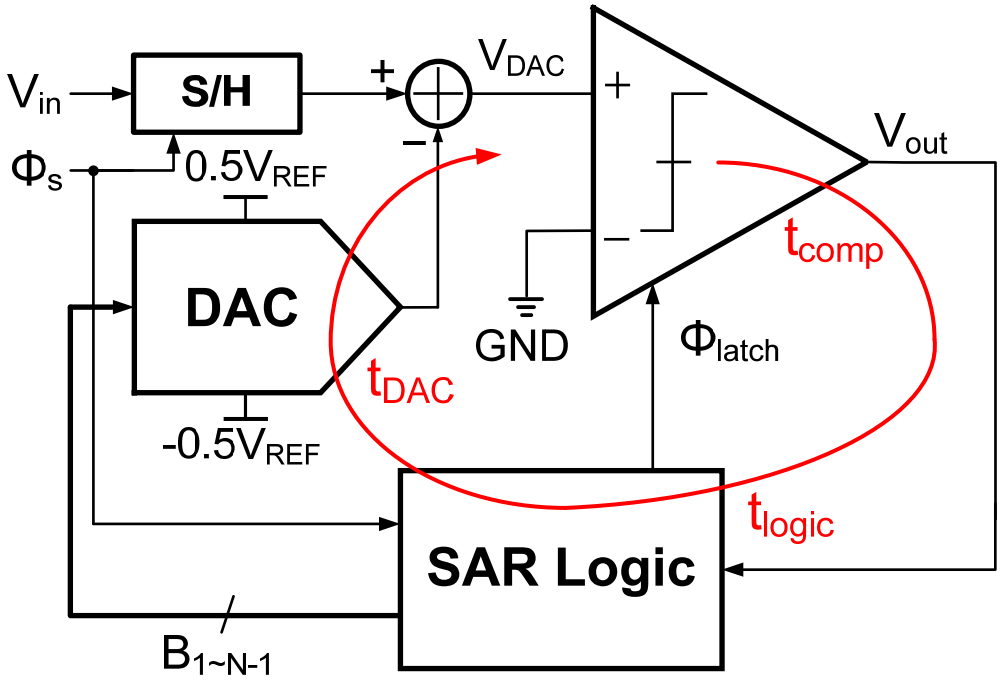
$$+$$

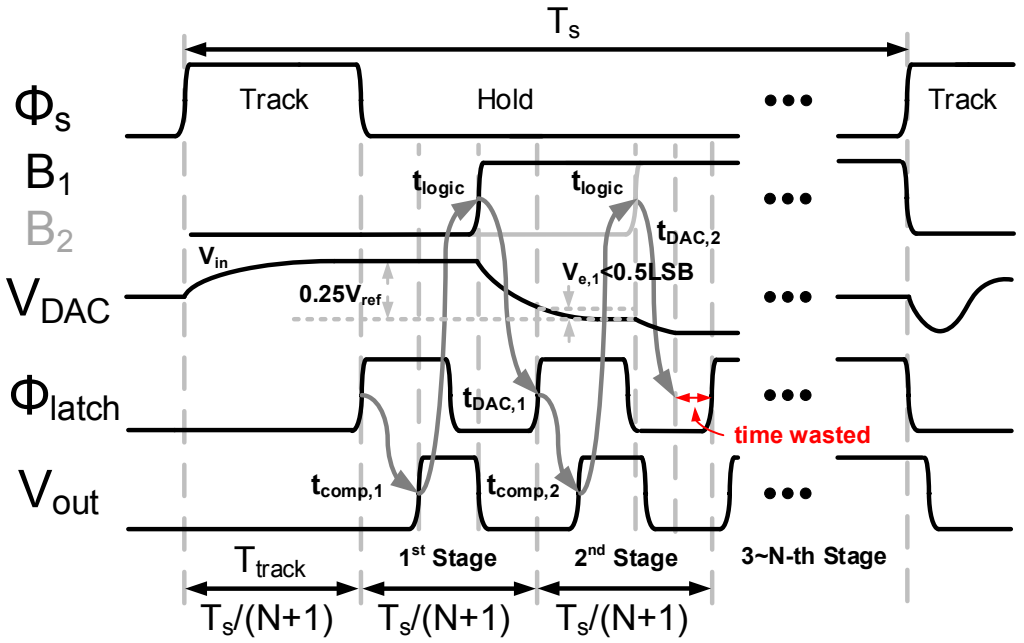
$$t_{reg} \sim \ln\left(\frac{V_{DD}}{V_{in}}\right)$$



- Comparator evaluation is exponentially proportional to input voltage
- Probability of metastability error depends on ADC architecture

Synchronous SAR Logic

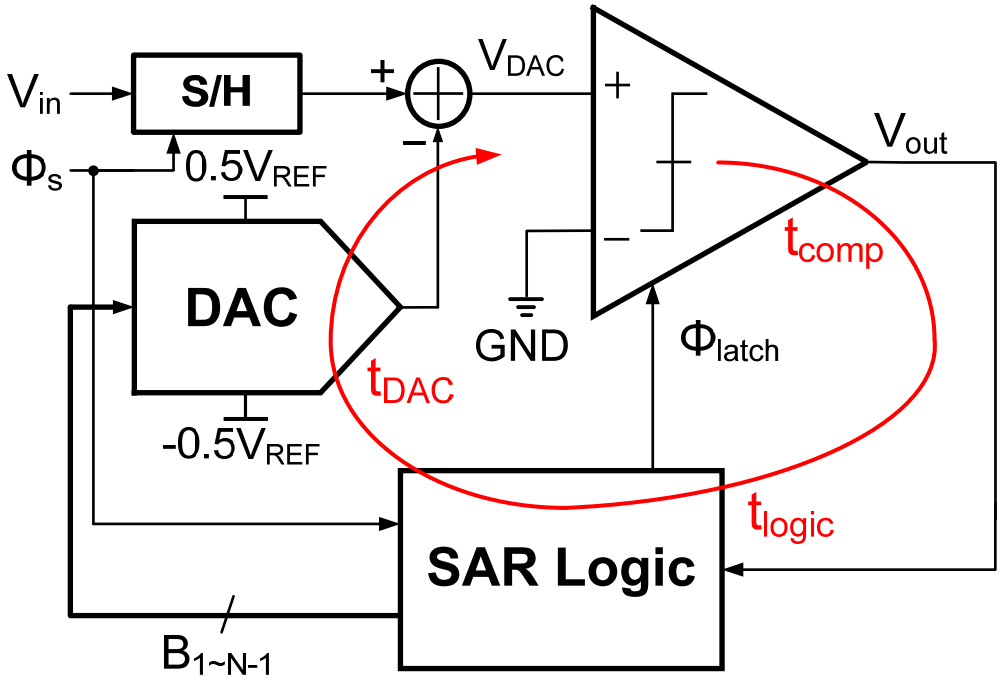


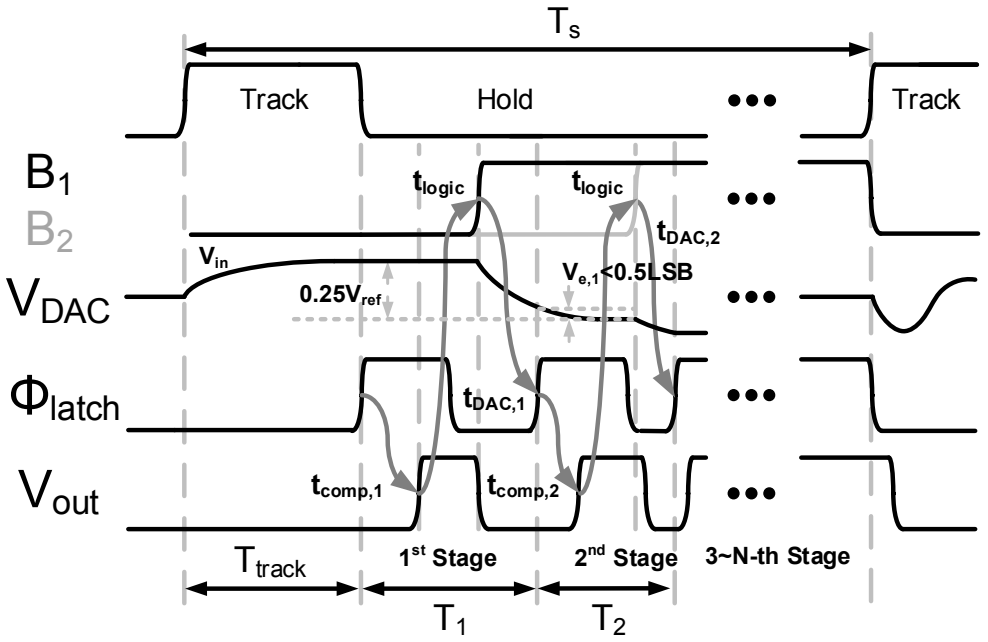


- Need an internal clk at N+1 times sampling frequency
- Maximum frequency limited by worst case stage delay

$$f_S = \frac{1}{(N+1)\max_i\left(t_{comp,i} + t_{\mathrm{logic},i} + t_{DAC,i}\right)}$$

Asynchronous SAR Logic

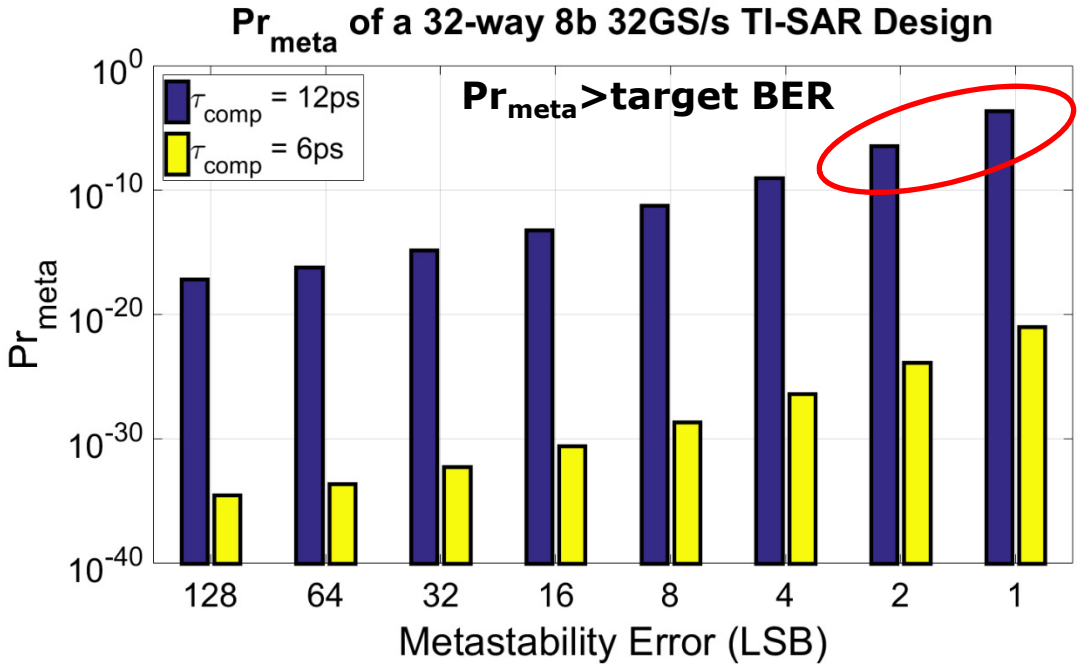


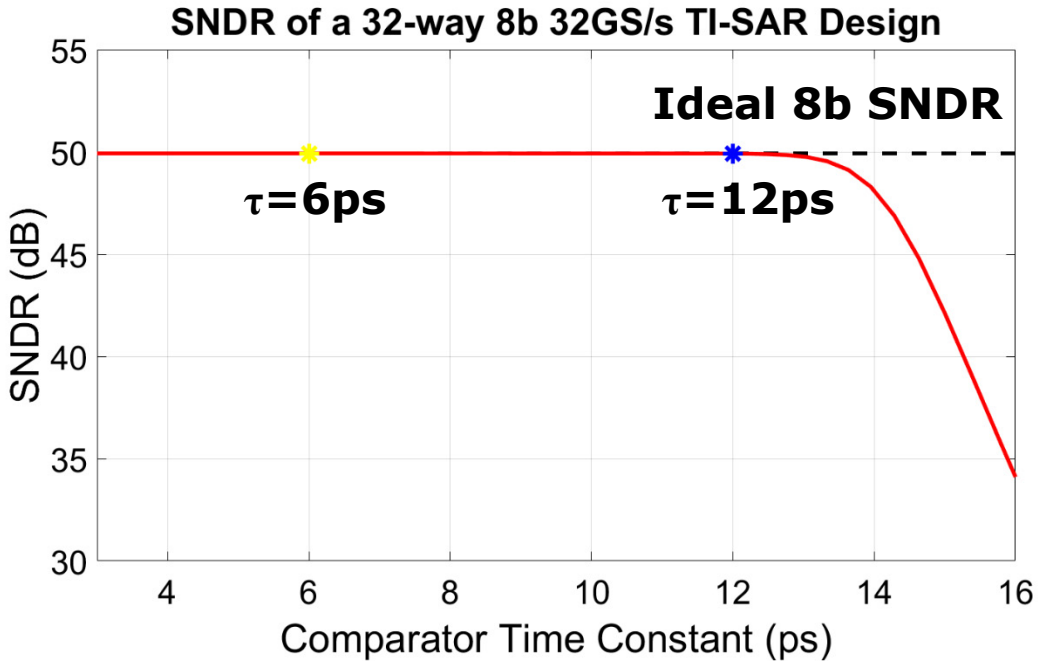


- Comparator triggered in a ripple fashion, no need for (N+1)fs
- Maximum frequency speeded up by reducing the non-worst-case stage delay

$$f_S = \frac{1}{T_{Track} + \sum_{i=1}^{N} \left(t_{comp,i} + t_{\mathrm{logic},i} + t_{DAC,i} \right)}$$

Metastability Error Rate



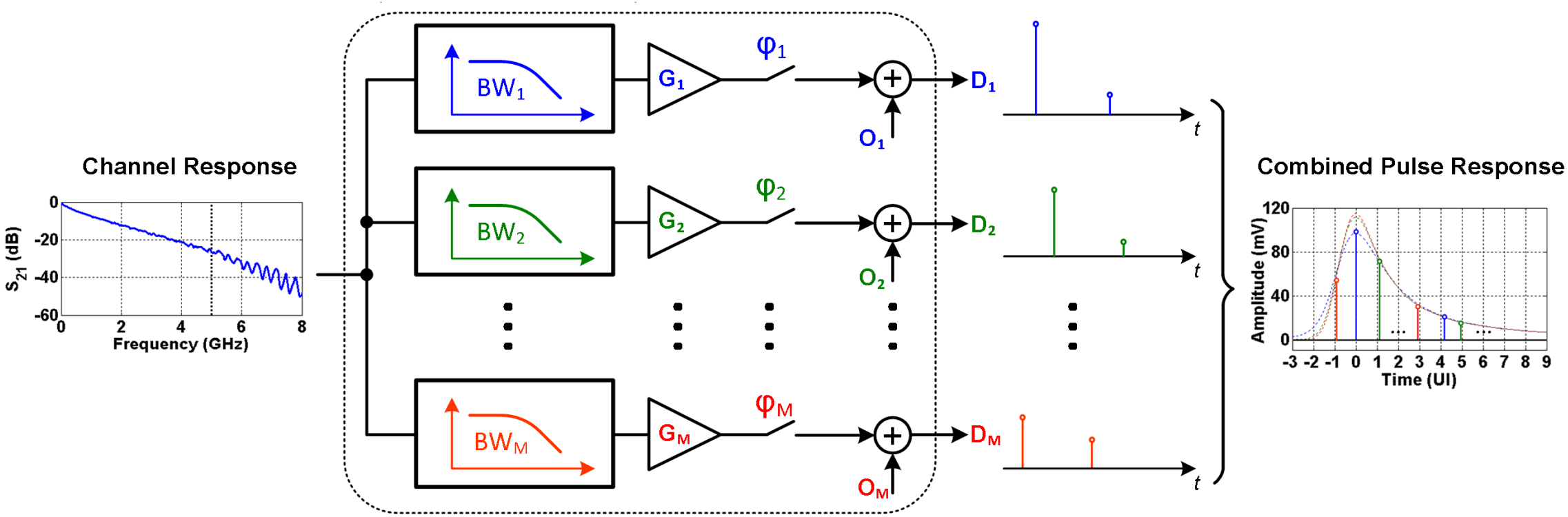


- Metastability error rate can be improved with a faster comparator
- Metastability error could be propagated through digital FFE and impact RX BER performance even if it meets the ADC SNDR specification

Outline

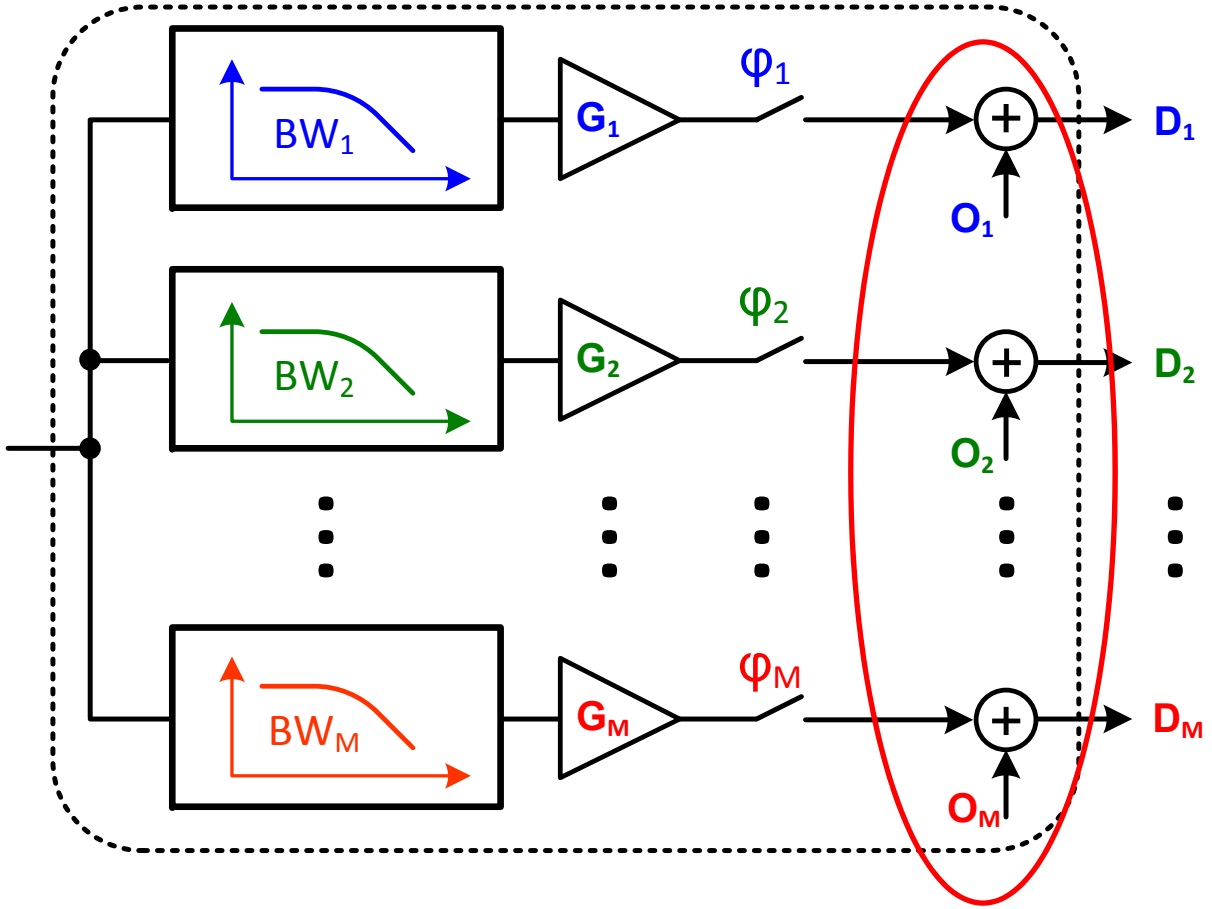
- ADC Resolution Requirements & Topologies
- Key ADC Circuits
- ADC Calibration Techniques
- Digital Equalization
- Analog Front-End
- Conclusion

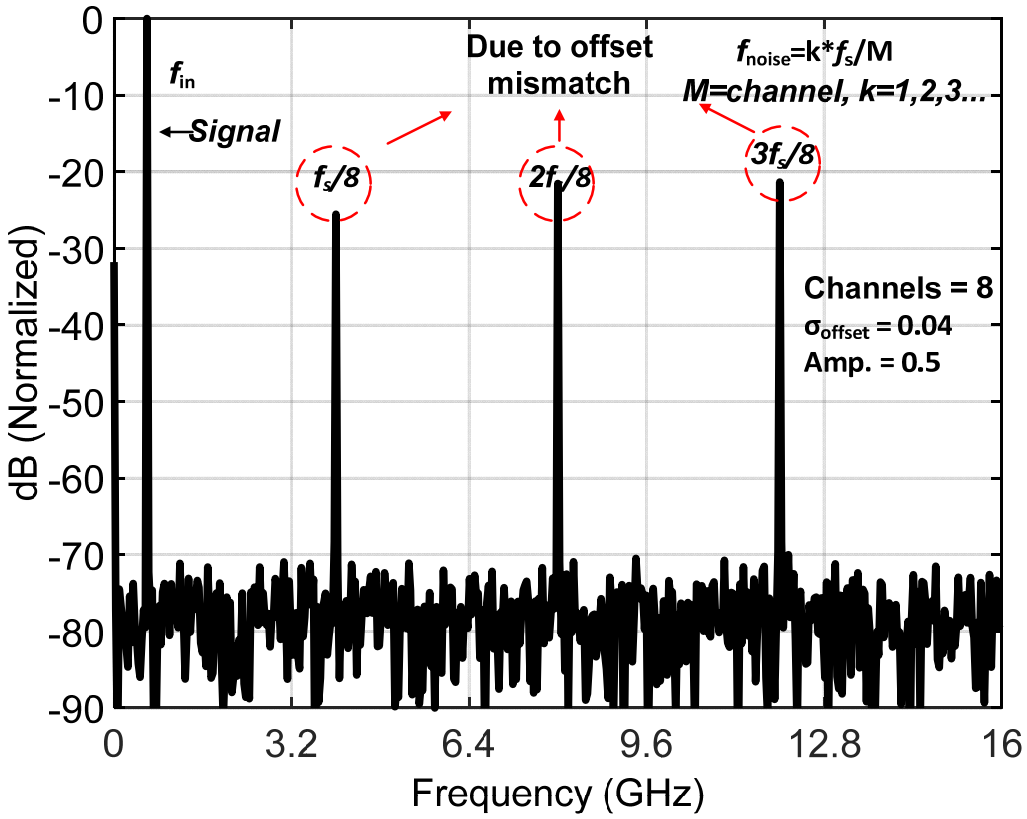
Time-Interleaving Errors



- Mismatches between time-interleaving channels degrade performance
- Modelled as an effective pulse response from each time-interleaved ADC channel, including offset, gain, bandwidth, and skew effects
- Both analog and digital calibration techniques are employed to correct these issues

Offset Errors

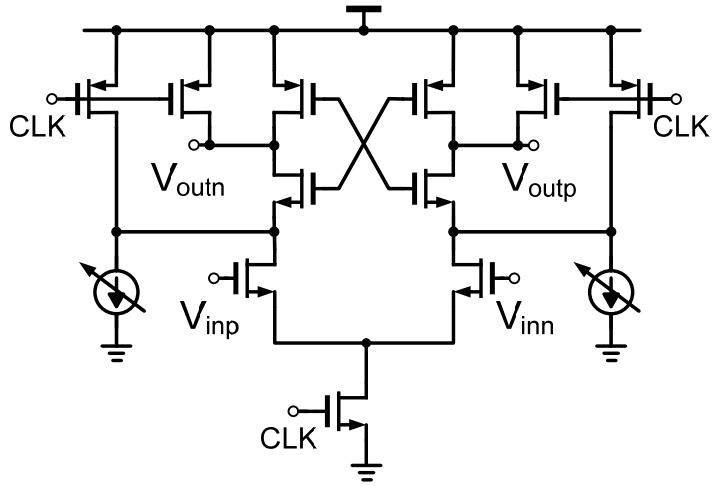




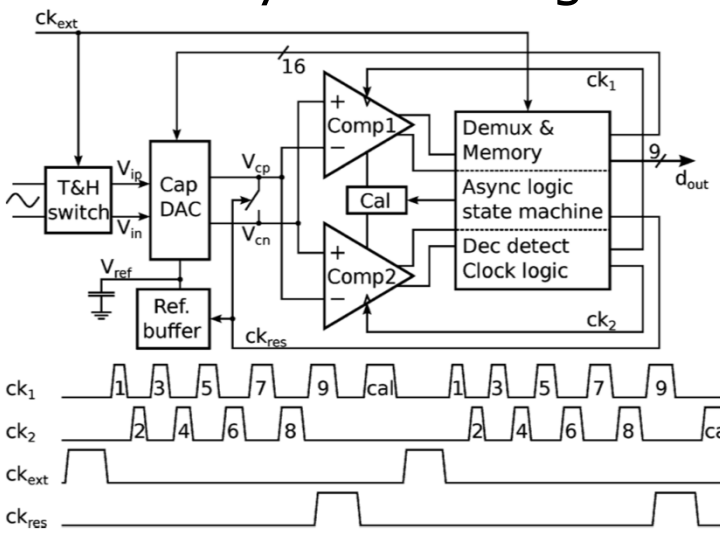
- Caused by device mismatches in T/Hs, DACs, and comparators

Offset Error Correction

- Most commonly corrected in the analog domain in the comparators
  - Current-mode/Capacitive DACs
  - Parallel diff pair driven by ref voltage
- Common foreground calibration scheme involves shorting inputs and adjusting offset DACs until 50% output 1/0



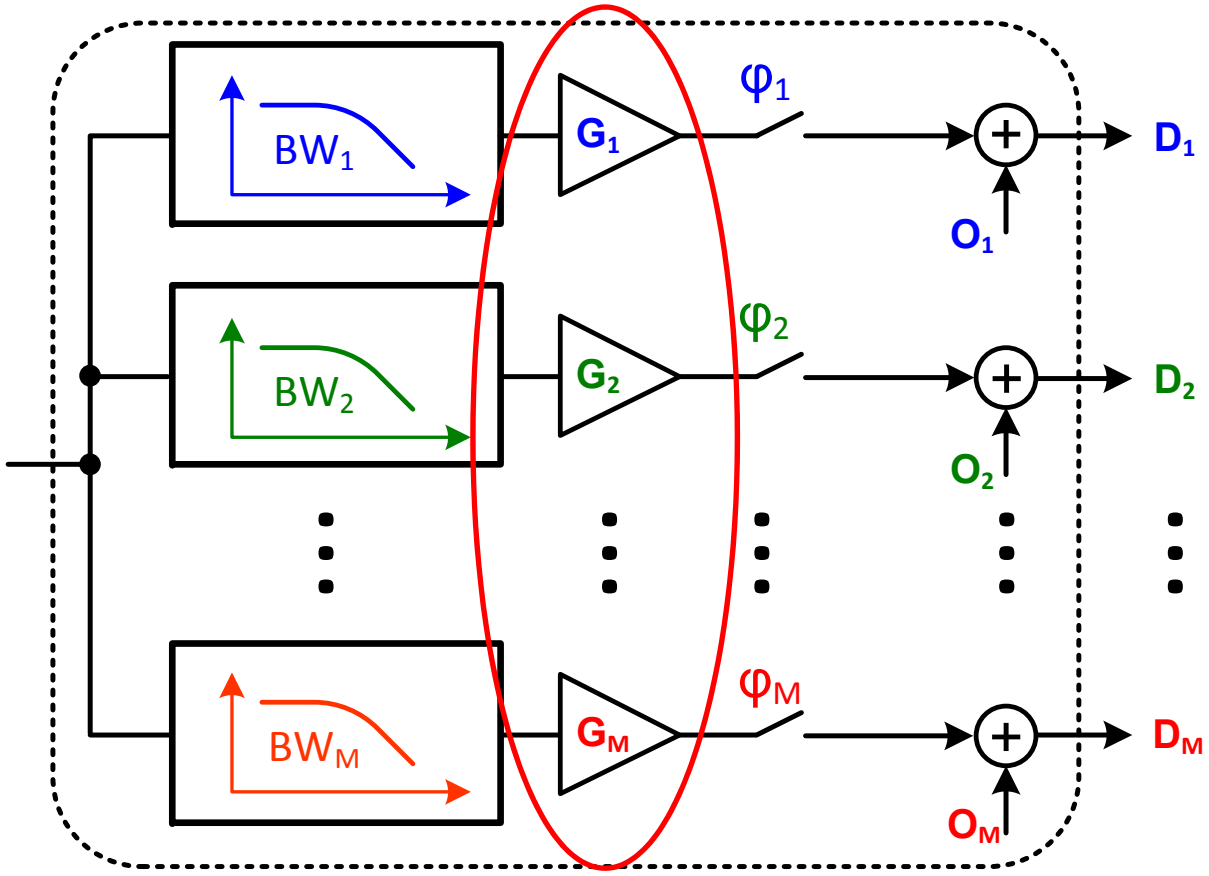
- Background calibration includes monitoring the average digital output or adding extra ADC correction cycles
- Can also be corrected in the digital domain with the loss of some dynamic range

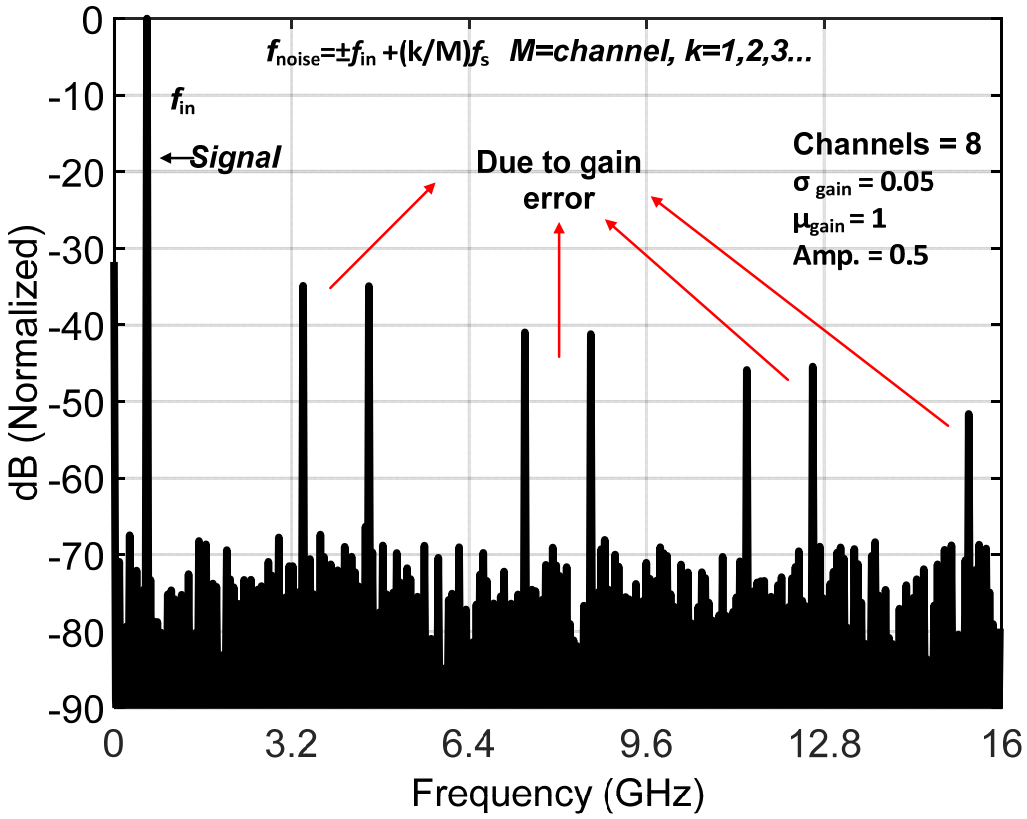


Background Offset Calibration w/ Extra SAR Cycle

[Kull JSSC 2013]

Gain Errors



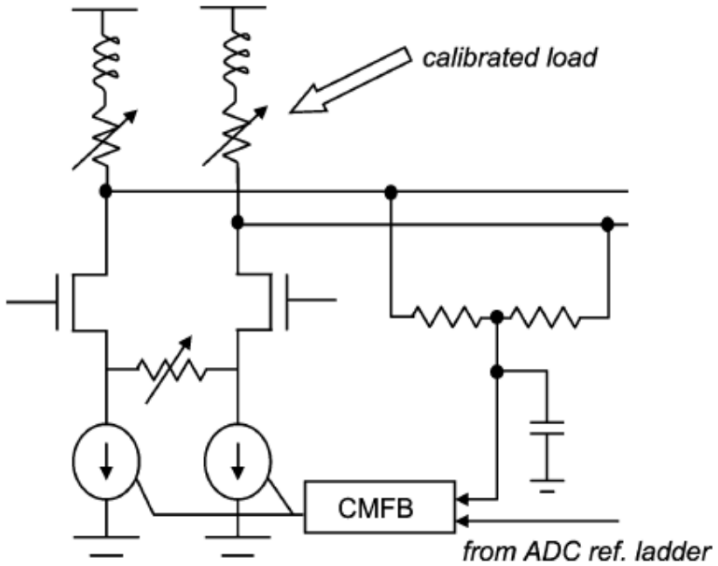


- Caused by device mismatches in T/Hs, DACs, and comparators

Gain Error Correction

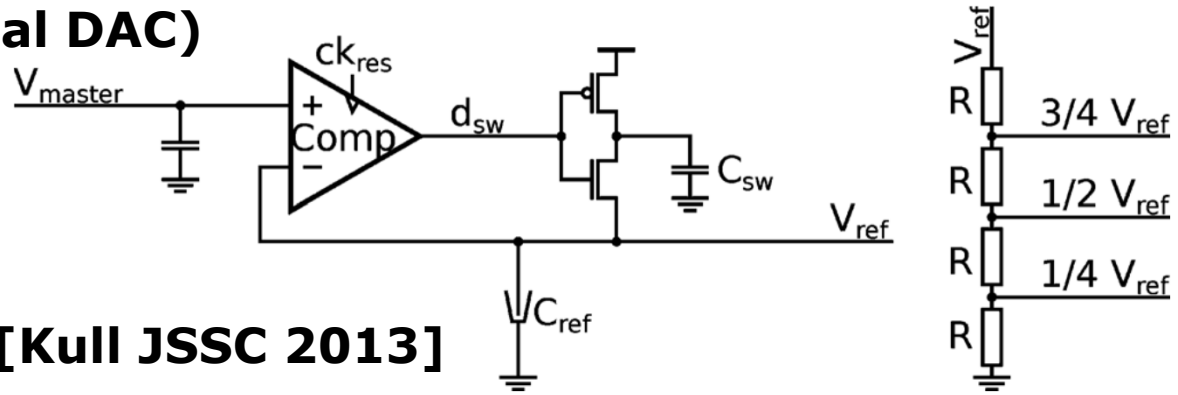
- Effective background calibration involves digitally monitoring the ADC peak output and correcting it to match the FSR
- Flash ADC
  - Adjustment of comparator thresholds
  - Programmable gain amplifier in sub-ADC
- SAR ADC
  - Adjusting capacitive DAC reference voltage
  - Introducing additional programmable capacitors
- Further fine gain calibration can also be implemented in the DSP

Programmable Gain Amplifier



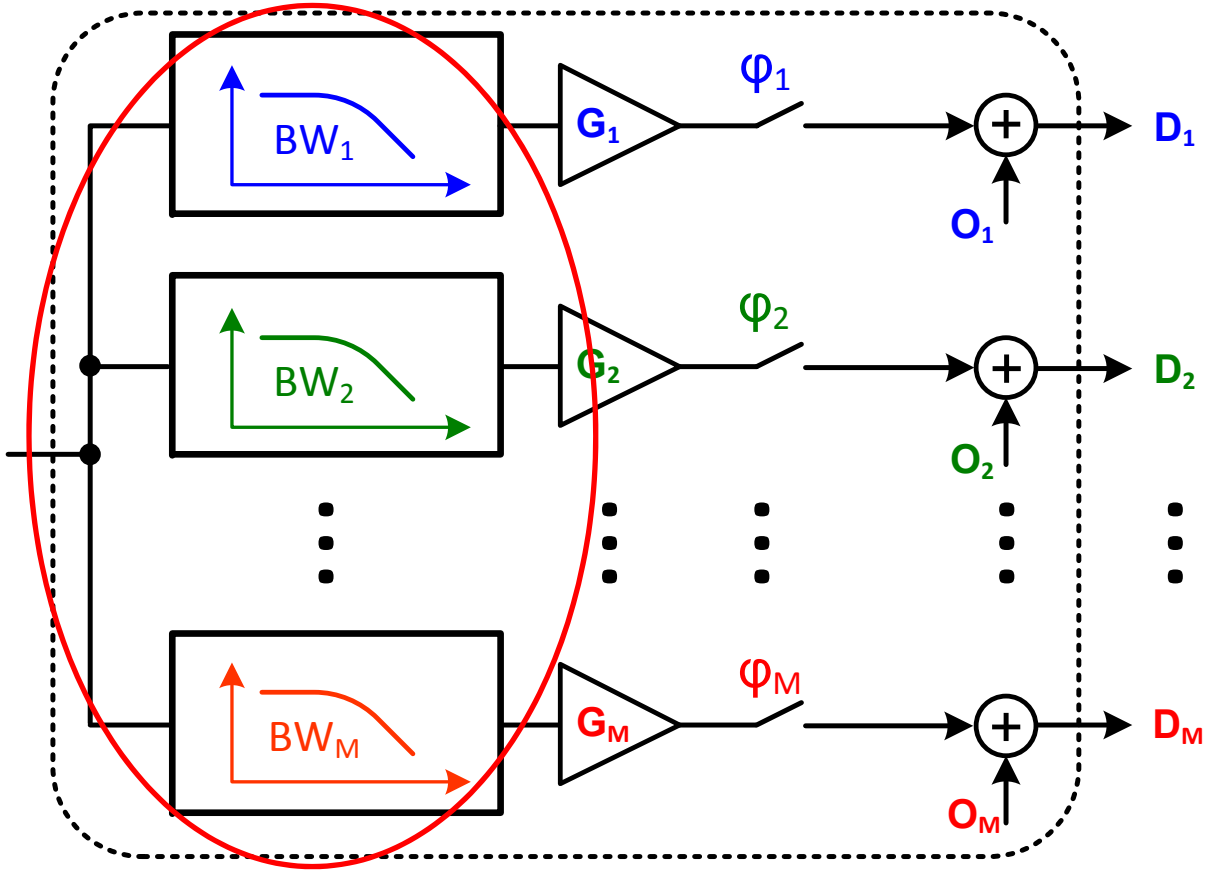
[Cao JSSC 2010]

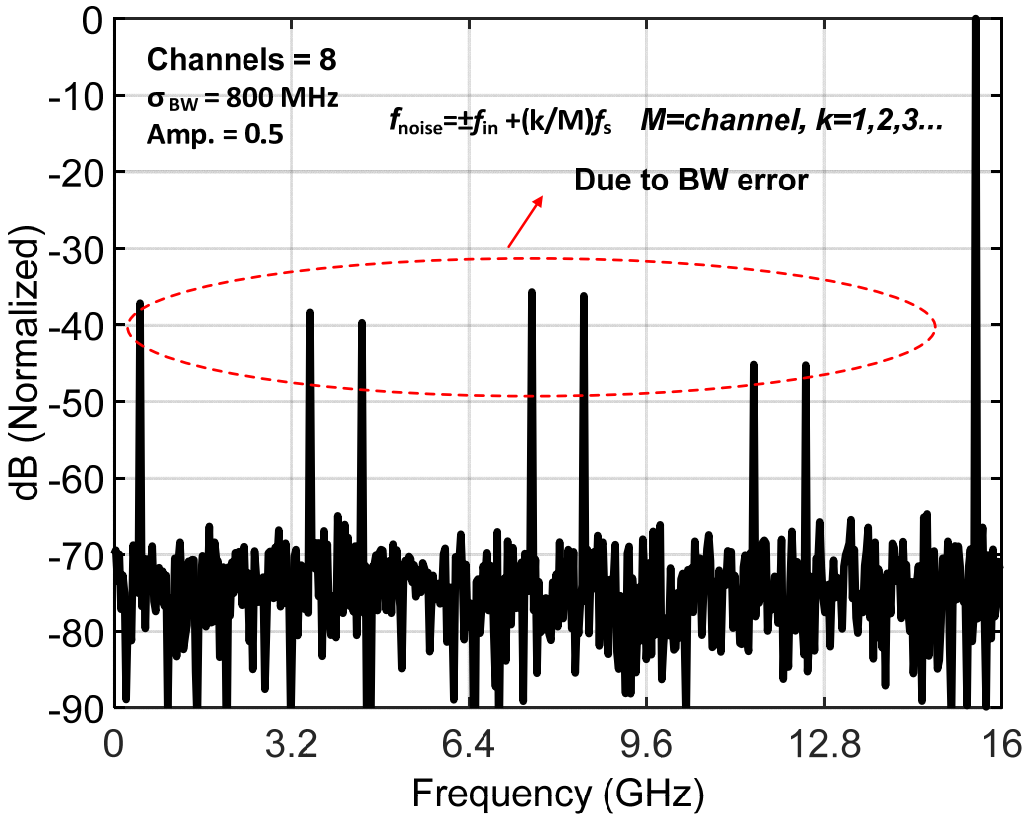
Unit SAR DAC Programmable Reference (From Gain Cal DAC)



[Kull JSSC 2013]

Bandwidth Errors

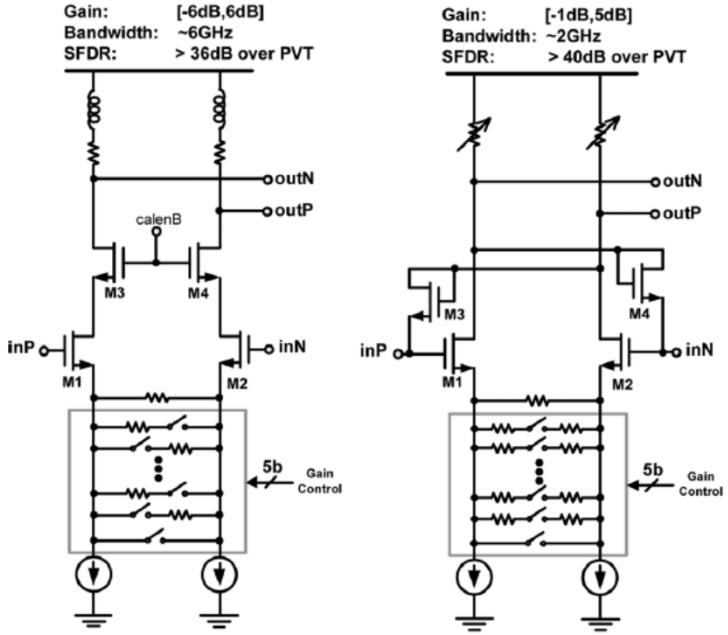




- Caused by layout asymmetries and device mismatches in T/Hs, DACs, and comparators

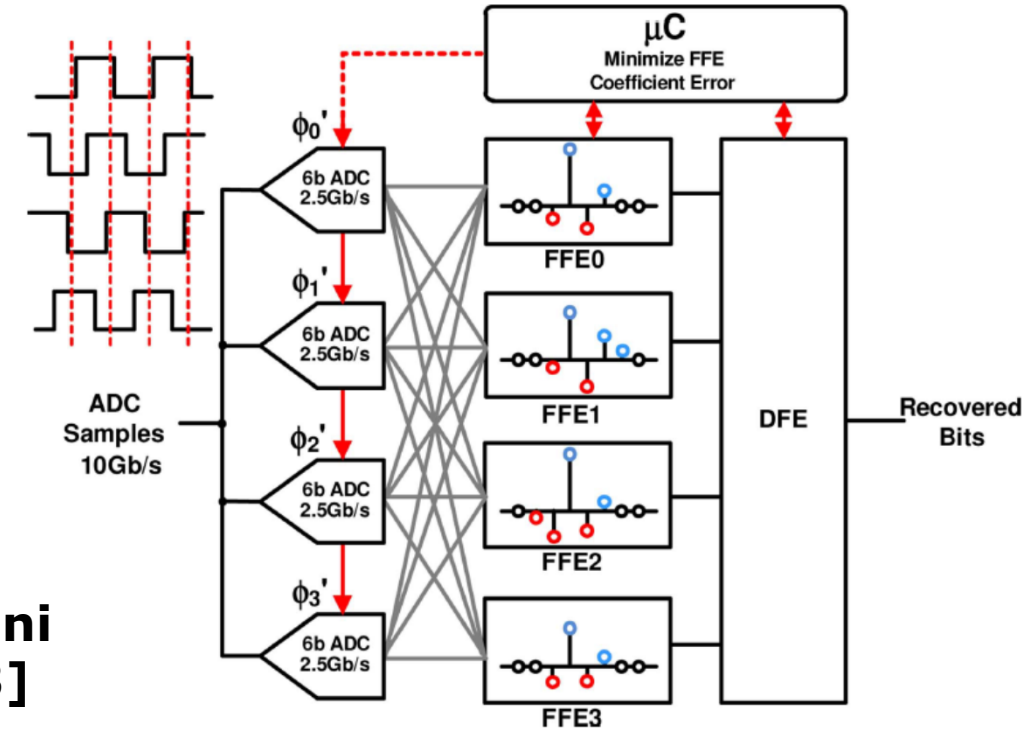
Bandwidth Error Correction

- Simply design the signal path with sufficient bandwidth such that any variations don't translate into major differences in the pulse response
  - Shunt peaking PGAs

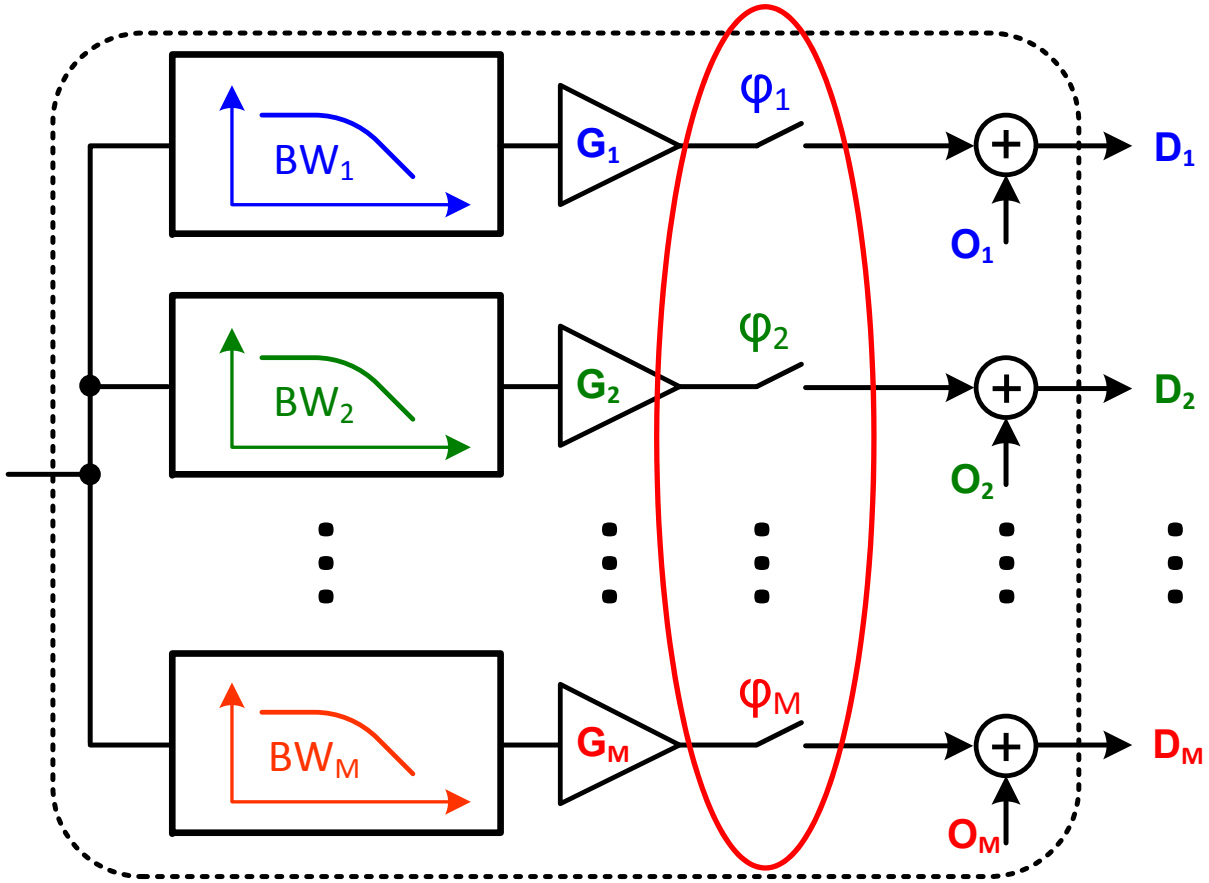


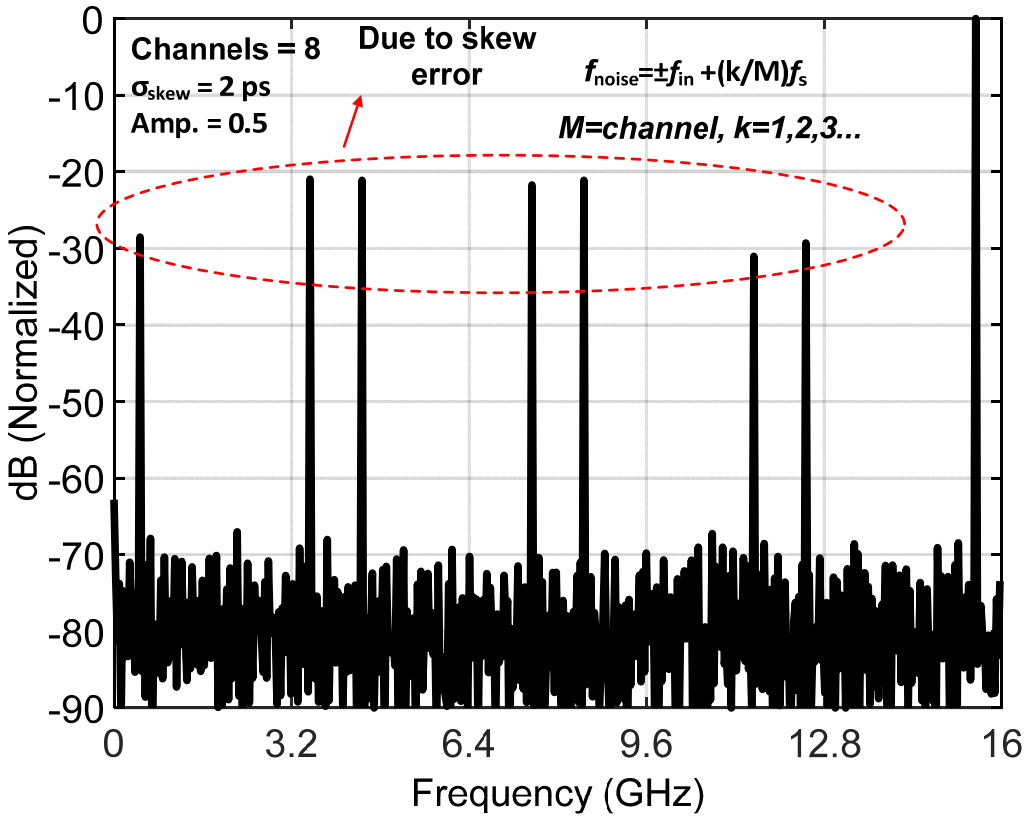
[Varzaghani JSSC 2013]

- Digital domain compensation treats each sub-ADC as a unique channel
  - Per-slice independent adaptation of FFE and DFE taps



Skew Errors

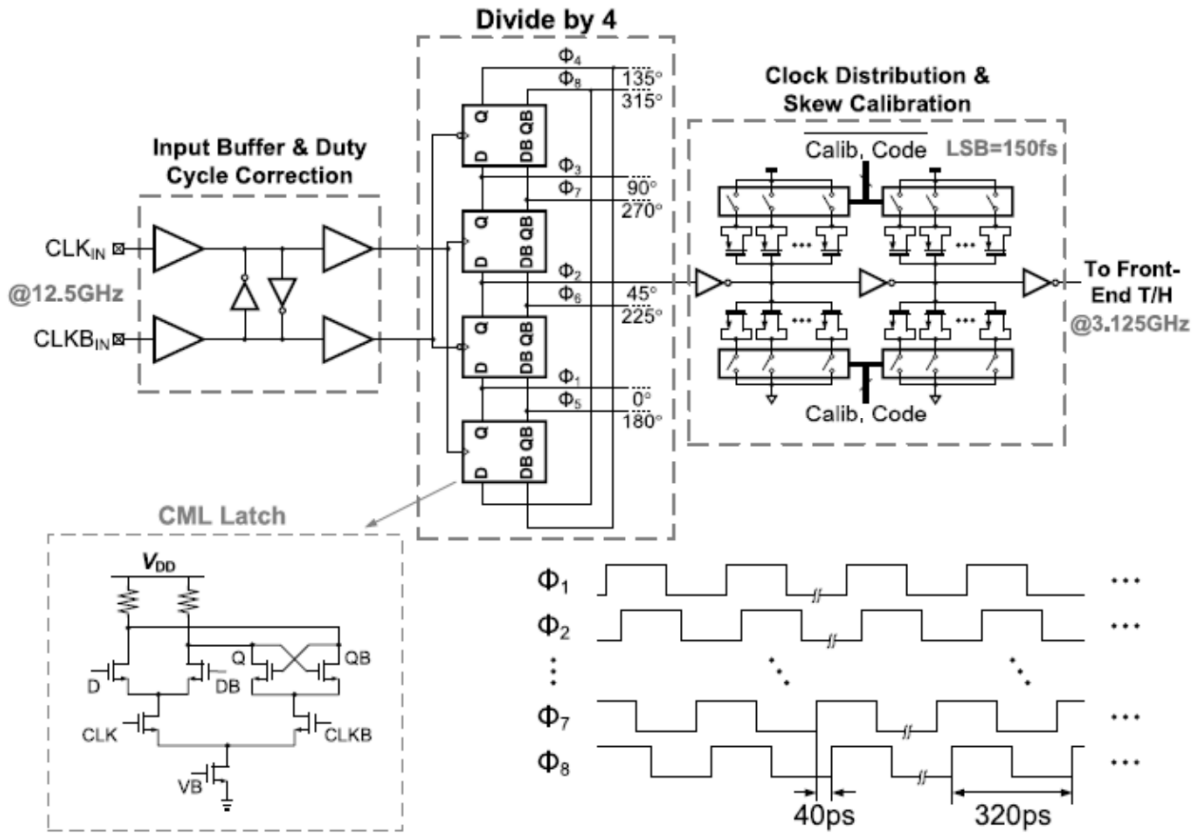




- Caused by device mismatches and layout asymmetries in the multi-phase clock generation and distribution to the input track-and-holds

Skew Error Correction

- Calibrated with per-phase digitally-adjustable delay cells in the clock distribution buffers or phase interpolators with independent phase offset codes
- Similar to bandwidth errors, skew errors will cause each sub-ADC to generate a pulse response with a slightly different ISI characteristic
- Efficient approach to detect skew errors is to monitor the differences in the converged tap coefficients of a per-slice adaptive equalizer



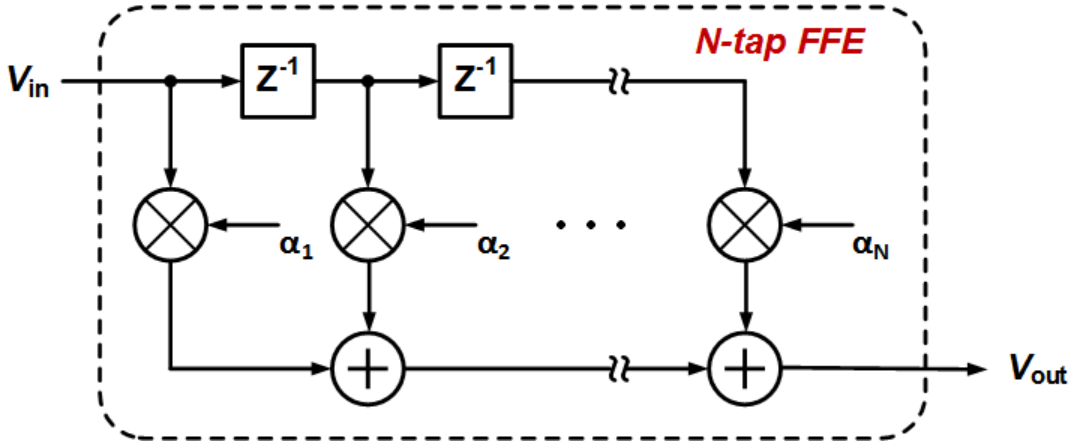
[Cai JSSC 2017]

Outline

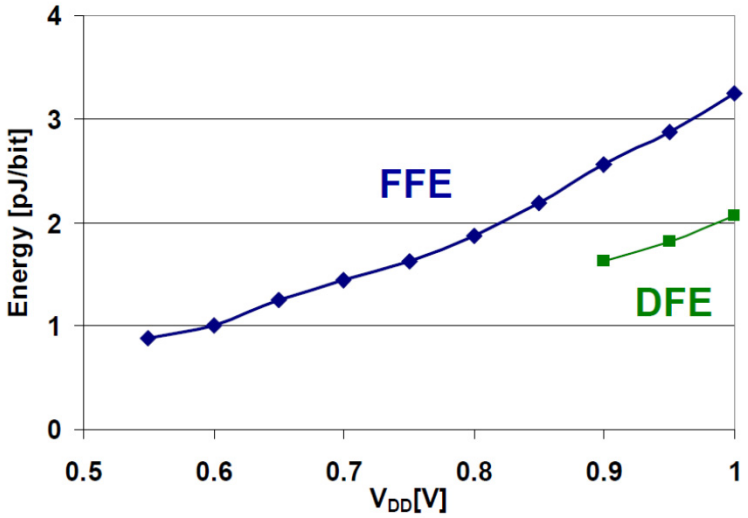
- ADC Resolution Requirements & Topologies
- Key ADC Circuits
- ADC Calibration Techniques
- Digital Equalization
- Analog Front-End
- Conclusion

Feed-Forward Equalizer

- Symbol by symbol linear equalizer
- Parallel implementation often matches or exceeds the ADC time-interleaving factor
- Timing constraints can be easily met through pipelining
- FFE power efficiency can be improved through several techniques such as
  - Power supply scaling
  - Employing CSD representation for taps
  - Tapering coefficient range for taps far from main tap
- FFE architecture is independent of modulation format

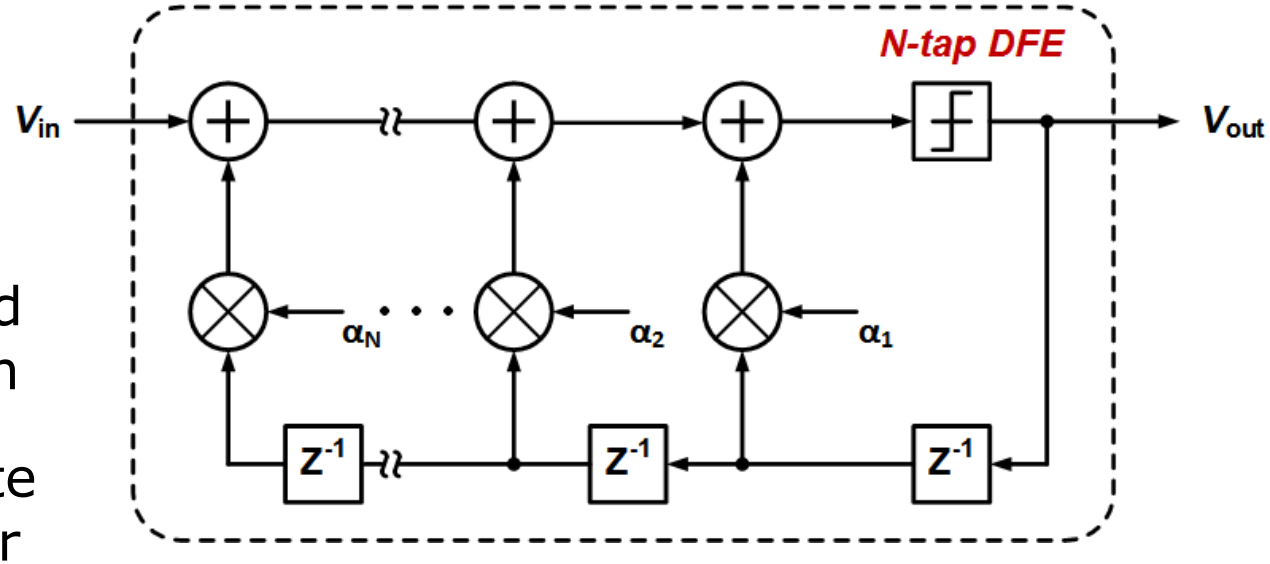


Energy efficiency of an 8-tap FFE vs supply level [Toifl ESSCIRC 2014]



Decision Feedback Equalizer

- Non-linear equalizer that cancels post-cursor ISI
- Conceptual full rate implementation has all the summers, 1 multiplier and 1 comparator in the 1-UI critical path
- Loop critical path delay in the full rate implementation is significantly longer than the iteration bound
  (1*(summer + multiplier + slicer) / 1UI)

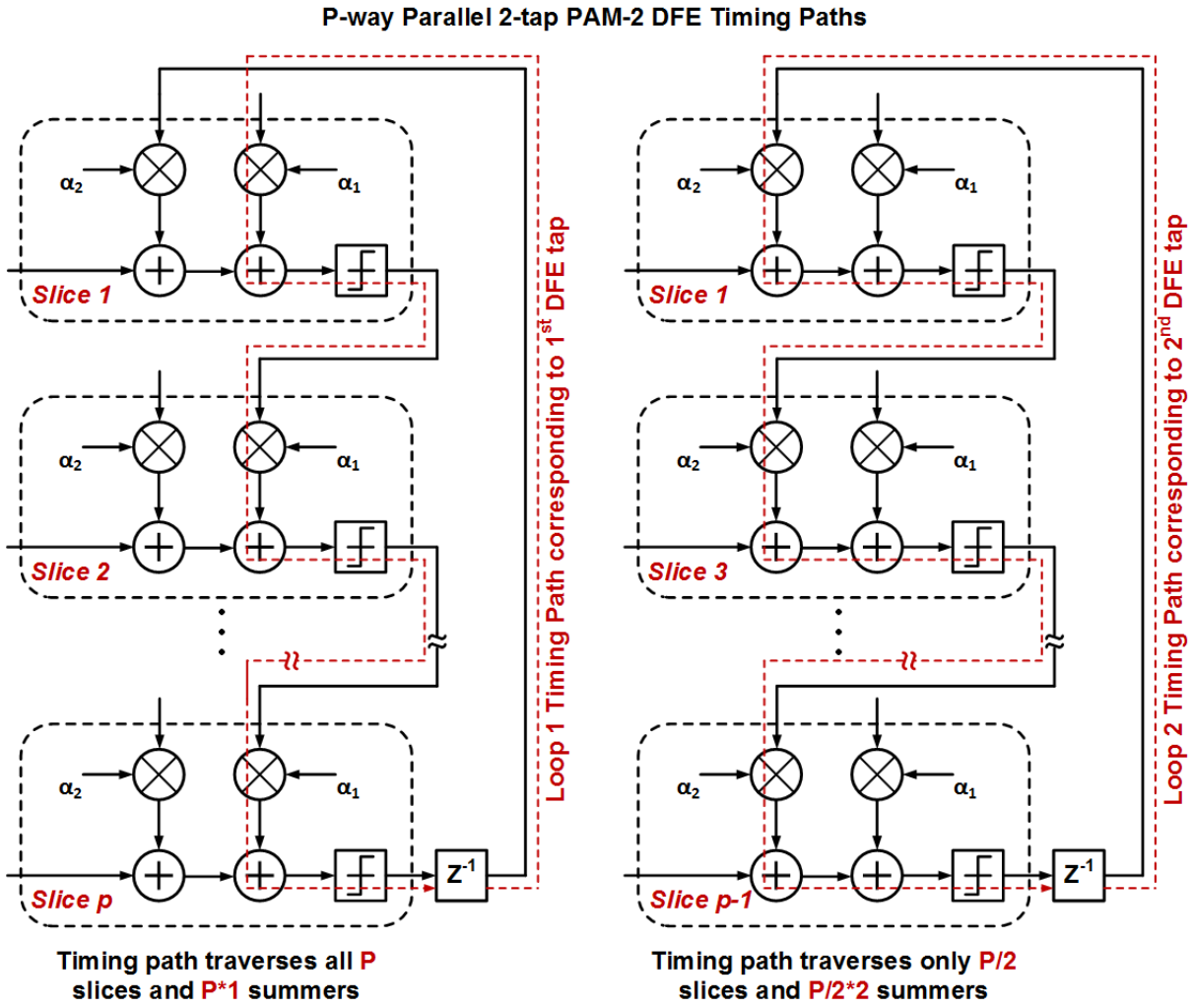


$$Iteration\ Bound = Max\left(\frac{Total\ Logic\ Delay}{Total\ Loop\ Time}\right)\ over\ all\ loops$$

- DFE often implemented to have the same number of parallel slices as the preceding FFE
  - Does this effectively solve the critical path issue?

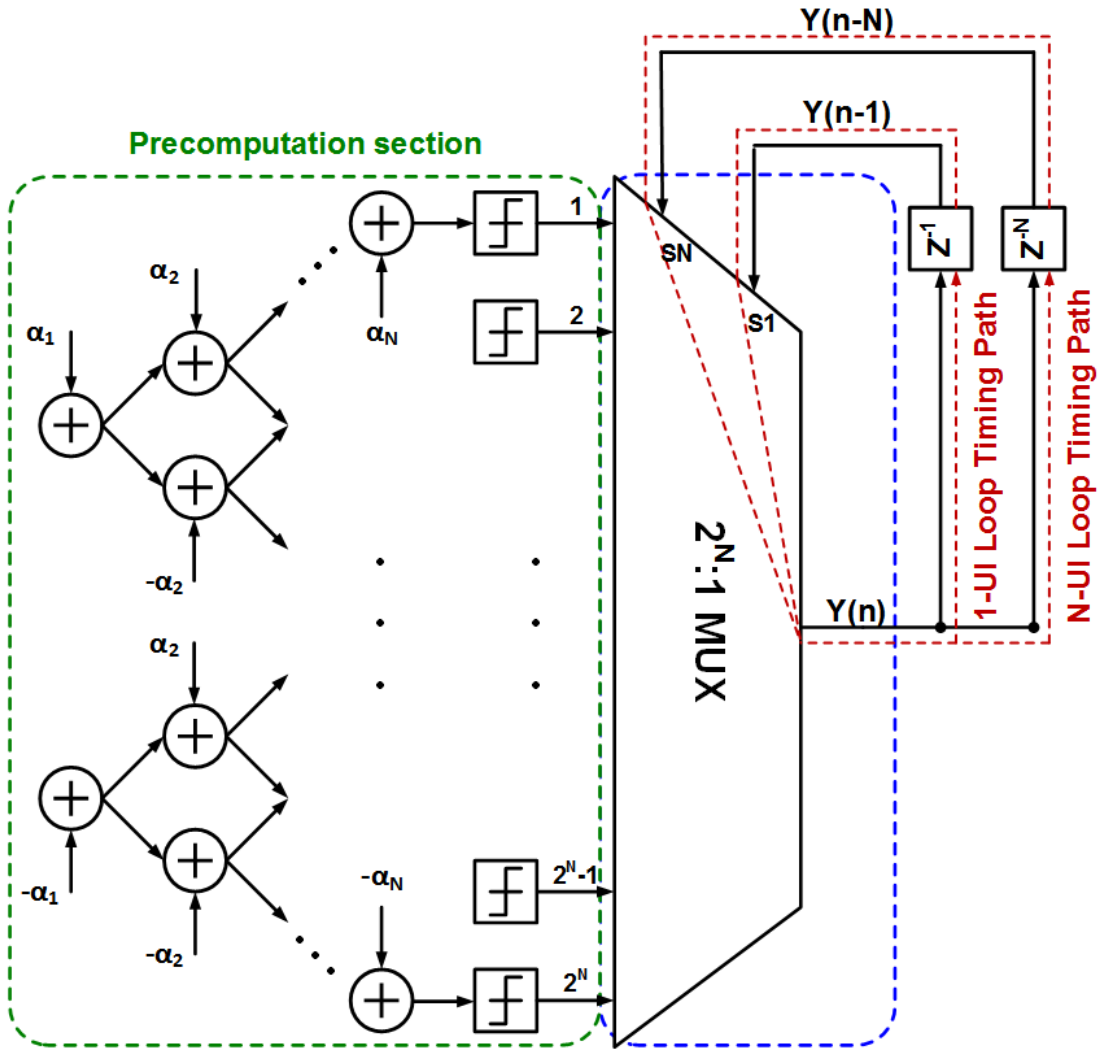
Parallel Slice Decision Feedback Equalizer

- DFEs are implemented with P parallel slices operating with a clock period of P UIs
- This still results in a maximum of P adders in the timing paths for the timing loops
- Even though the clock period increases by a factor of P, the logic delay also effectively increases by the same P factor
- While the parallel implementation brings the loop critical path period much closer to the iteration bound, advanced techniques are necessary to operate at high data rates

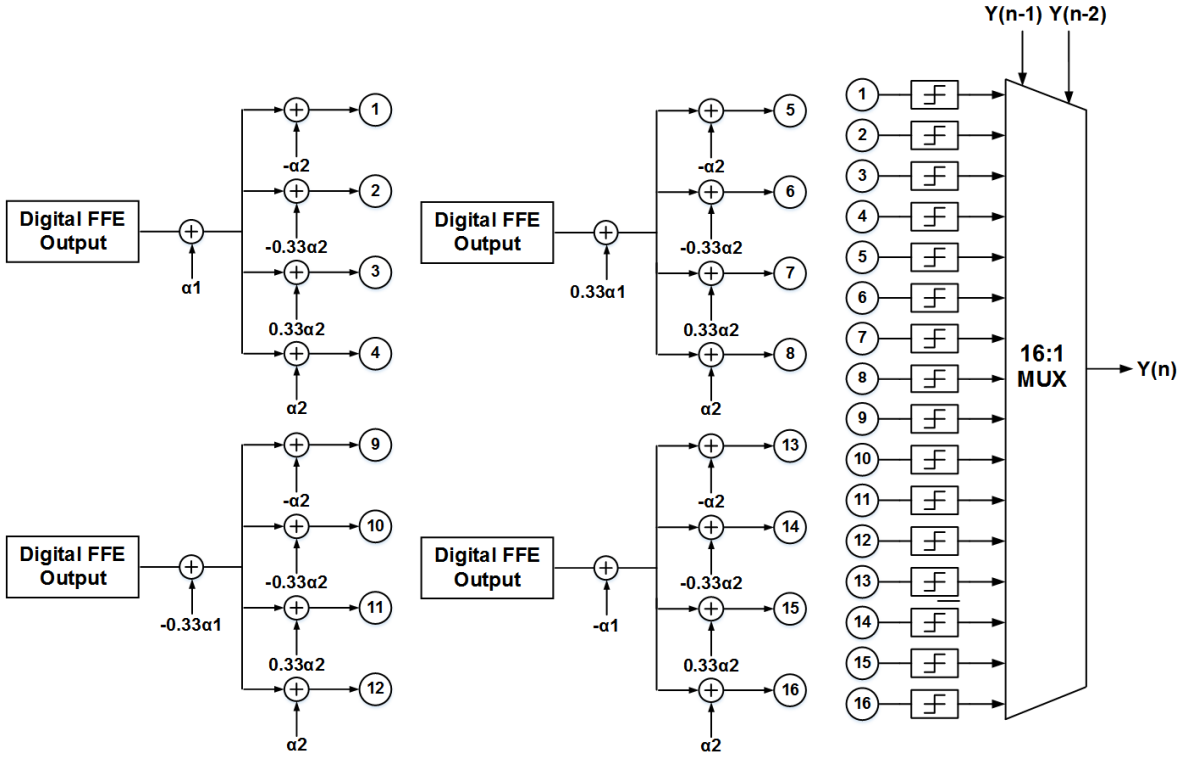


Loop-Unrolled DFE

- Loop-unrolling involves precomputing all the possible decision for the current symbol using all possible decisions for the preceding decisions that are part of the DFE
- Results in 2^N precomputed decisions for PAM-2 and 4^N precomputed decisions for PAM-4
- The adder is removed from the loop critical path as the precomputations can be pipelined
- The loop critical path primarily contains 2:1 muxes for PAM-2 and 4:1 muxes for PAM-4



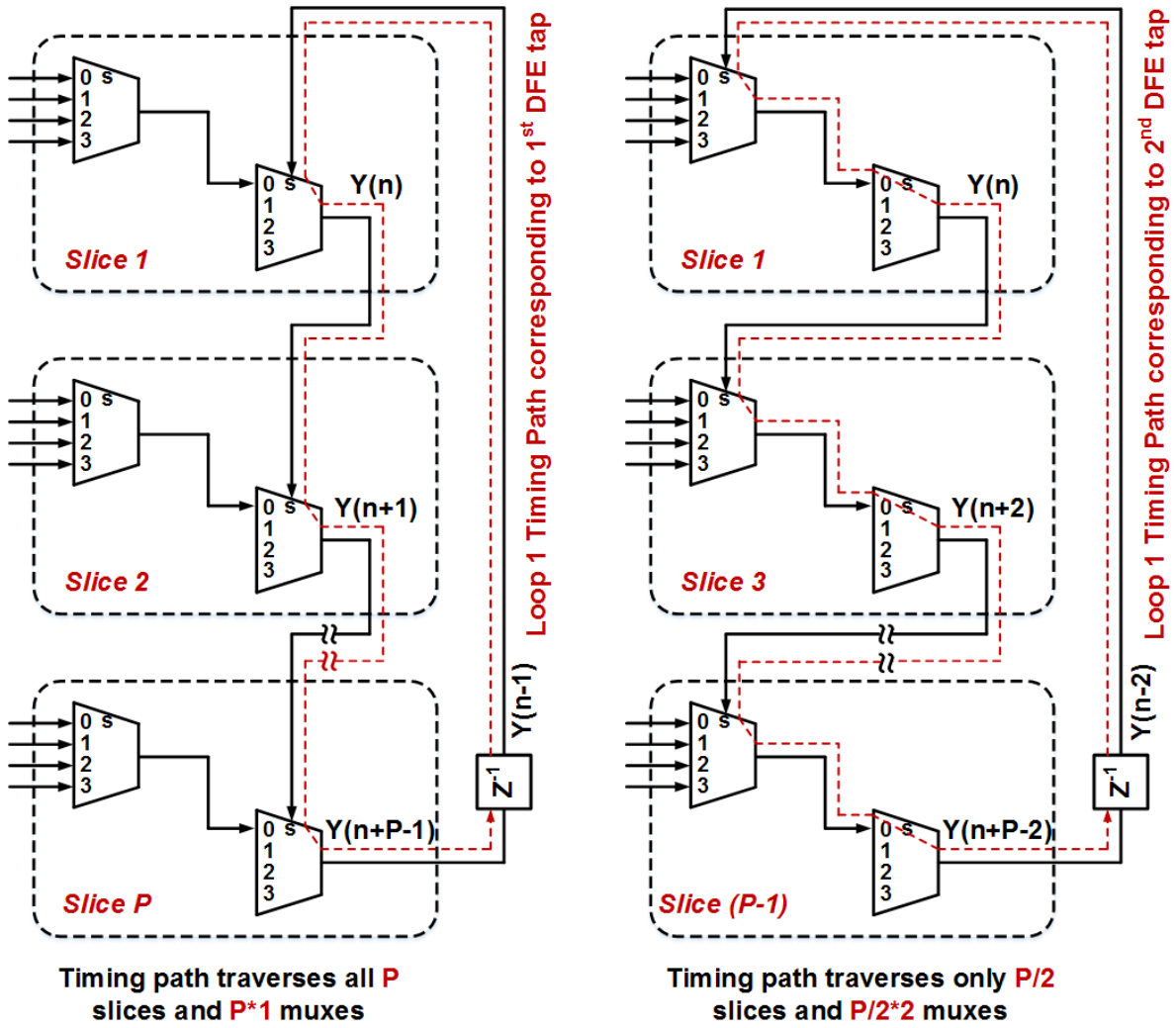
Example: PAM-4 2-tap Loop Unrolled DFE



- 4^2 = 16 decisions are precomputed with a 2-tap loop-unrolled DFE
- The output of the summers is sliced and fed into a 16:1 mux
- Select lines to the multiplexers come from the two immediately preceding decisions that have been made

Example: Timing Paths for PAM-4 2-tap Loop-Unrolled DFE

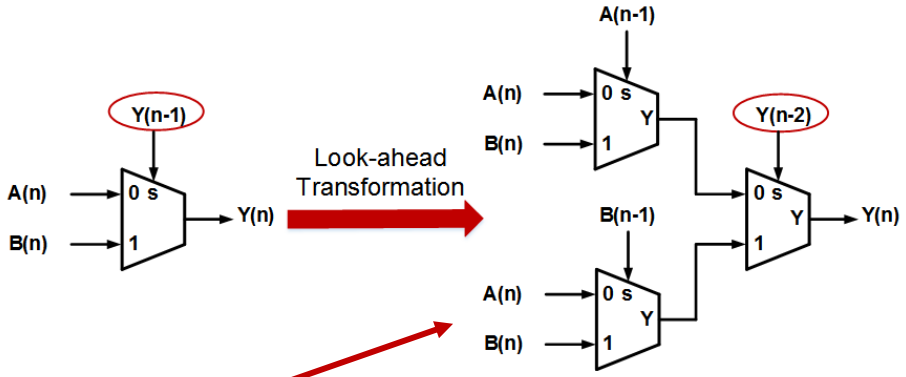
- Assuming P is even, each timing loop goes through P 4:1 muxes
- The total loop critical path is P 4:1 muxes, 1 Clk->Q delay, 1 setup time delay and routing delay
- For the Nth tap of the DFE, the timing loop contains $(1+\left\lfloor\frac{P-1}{N}\right\rfloor)*N$ 4:1 muxes
- For high data rates, further techniques to reduce the number of muxes in the loop critical path becomes necessary



Look-Ahead Multiplexer Loops

- Look-ahead architecture reduces the number of muxes in the loop critical path

- A mux loop is described by
  - $Y_n = A_n Y'_{n-1} + B_n Y_{n-1}$...(1) and
  - $Y_{n-1} = A_{n-1} Y'_{n-2} + B_{n-1} Y_{n-2}$...(2)



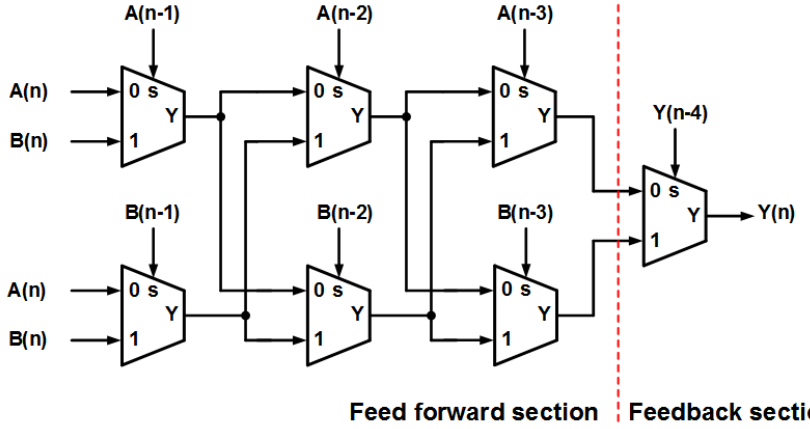
- Substituting (2) in (1)
  - $Y_n = (A_n A'_{n-1} + B_n A_{n-1}) Y'_{n-2} + (A_n B'_{n-1} + B_n B_{n-1}) Y_{n-2}$...(3) **[Parhi TVLSI 2005]**

- In (3) Y_n's dependency on Y_{n-1} has been removed! (Iteration bound halved)

Look-Ahead Multiplexer Loops

- The look-ahead multiplexor loop comes at the cost of extra muxes
- The feed forward section can be pipelined but the feedback section cannot be
- In case of PAM-2 N tap DFE, with LF way look-ahead the number of 2:1 muxes need is: $2^N(LF-1)+\sum_{i=1}^{N}2^{N-i}$

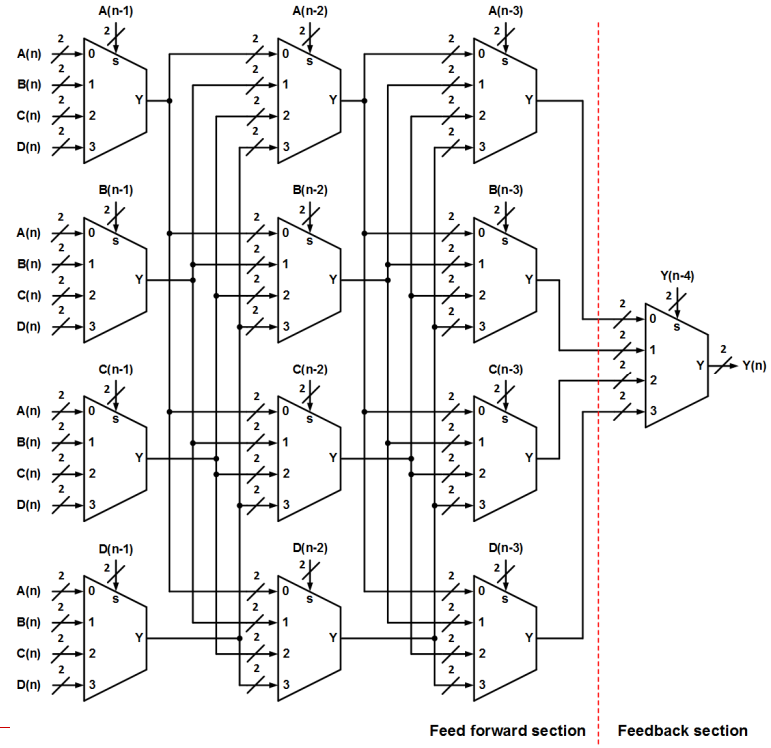
1-tap PAM-2 4-way look-ahead mux architecture



- In the case of PAM-4, the number of 2:1 muxes needed is:

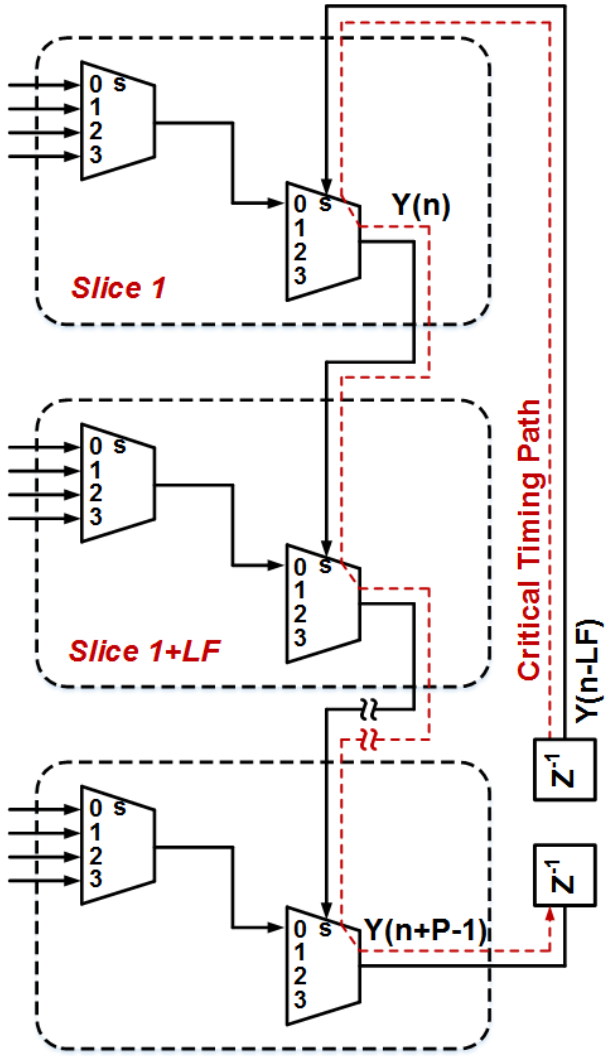
$$(4^N(LF-1)+\sum_{i=1}^{N}4^{N-i})*2*3$$

1-tap PAM-4 4-way look-ahead mux architecture



Example: PAM-4 Look-Ahead Loop Timing Path

- Select lines of the mux come from decisions made LF-UIs ago where LF is the look-ahead factor
- Input lines of the mux are fed from a bank of look-ahead muxes which can be pipelined
- Critical path for Nth DFE tap consists of 1 Clk->Q delay, $(1+\left\lfloor\frac{P-1}{LF+N-1}\right\rfloor)*N$ 4:1 muxes, 1 setup time and routing delay
  - Approximately divided by the look-ahead factor



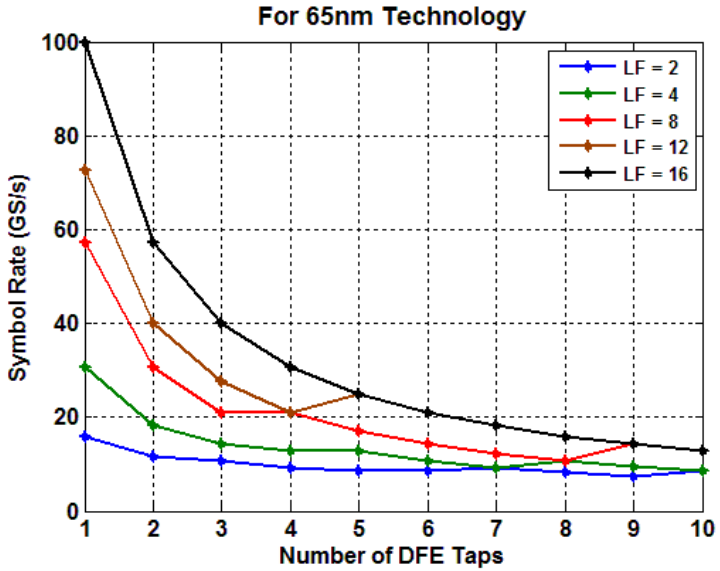
Maximum Achievable Data Rate

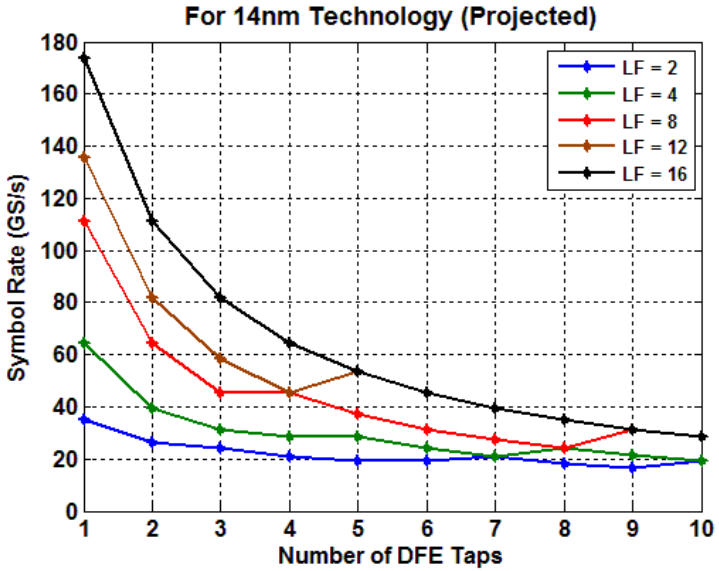
- For P-parallel path, N-tap DFE if Td is the 4:1 mux delay
- DFE timing constraint with no look-ahead must satisfy

$$P*UI = (1+\left\lfloor\frac{P-1}{N}\right\rfloor)*N*(Td) + \text{clock uncertainty} + 1\ \text{Clk->Q delay} + \text{setup time}$$

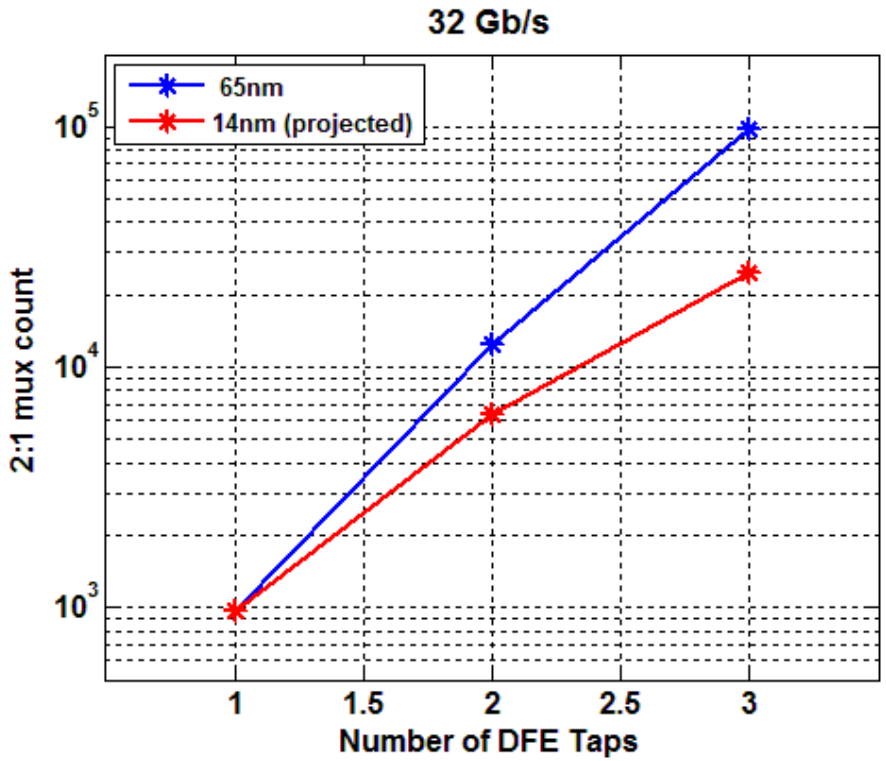
- With look-ahead factor LF the constraint is

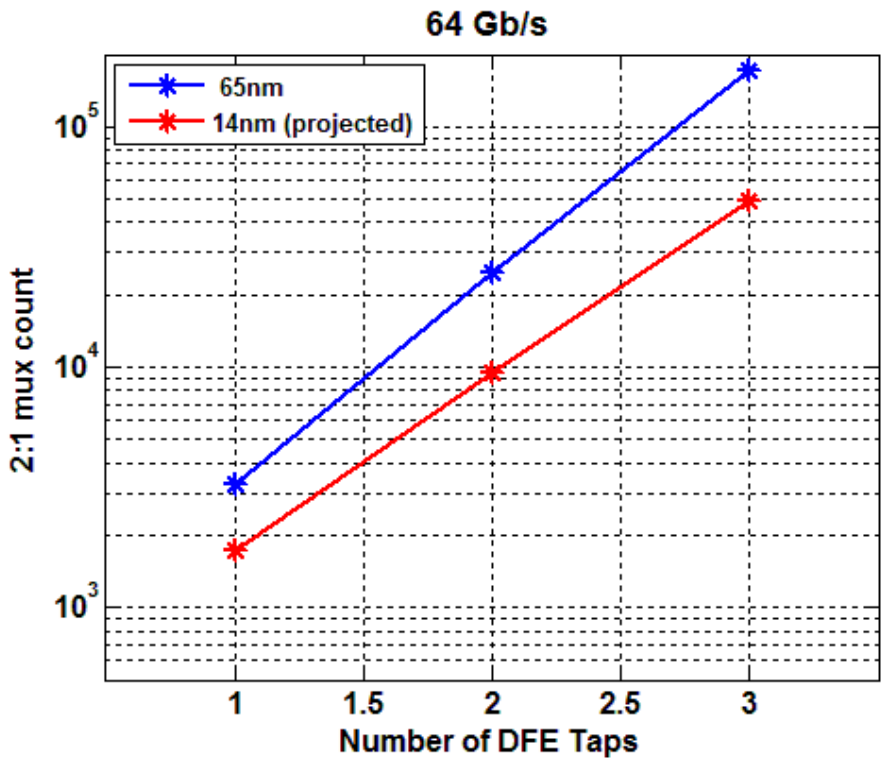
$$P*UI = (1+\left\lfloor\frac{P-1}{LF+N-1}\right\rfloor)*N*(Td) + \text{clock uncertainty} + 1\ \text{Clk->Q delay} + \text{setup time}$$





Complexity





- The 2:1 mux count for different number of DFE taps employing the minimum possible look-ahead factor necessary for that tap number shows the dramatic increase in going from 1 to 3 taps of DFE

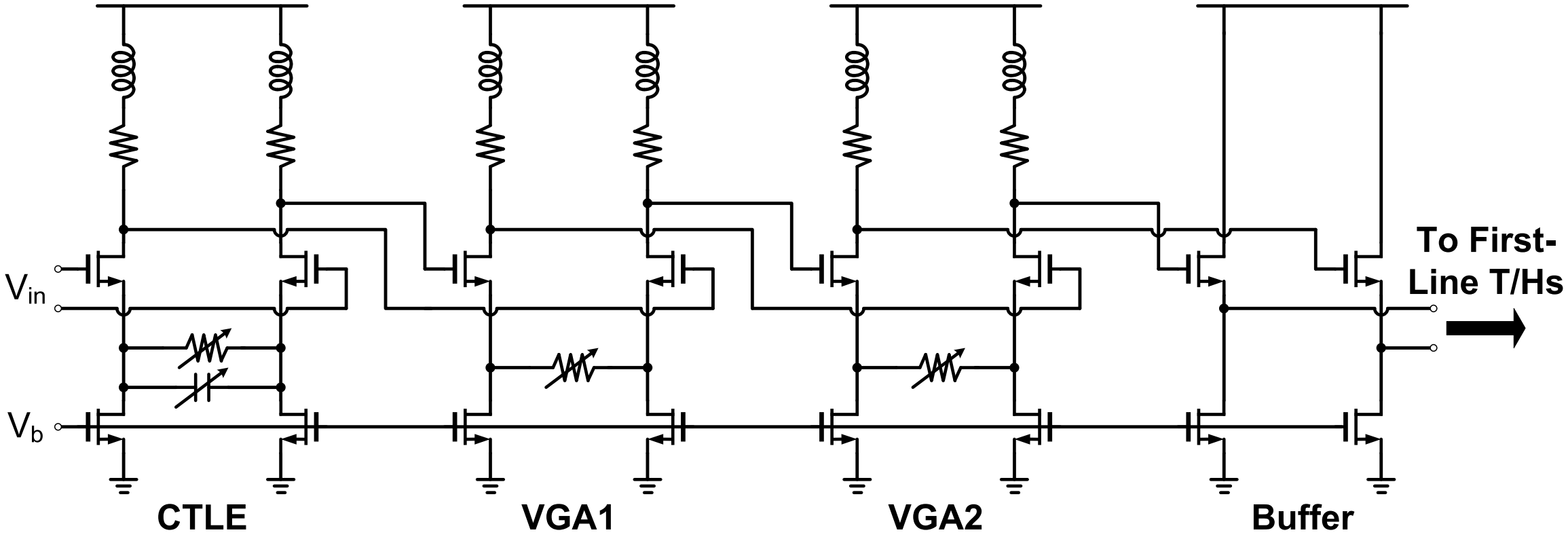
Digital DFE Take-Aways

- PAM-4 system unit delay element is a 4:1 mux, as opposed to 2:1 mux for NRZ
  - At the same baud rate makes timing closure much harder than NRZ
- Loop-unrolling and look-ahead techniques can significantly reduce the critical path delay and enable high data rates
- High data rates come at the cost of huge complexity
  - Grows as power of 4 for PAM-4 systems

Outline

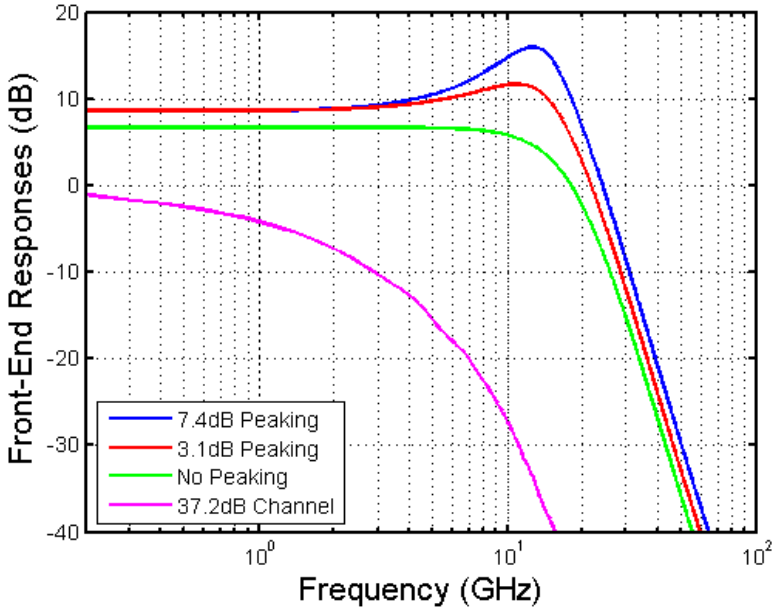
- ADC Resolution Requirements & Topologies
- Key ADC Circuits
- ADC Calibration Techniques
- Digital Equalization
- Analog Front-End
- Conclusion

Analog Front-End (AFE)

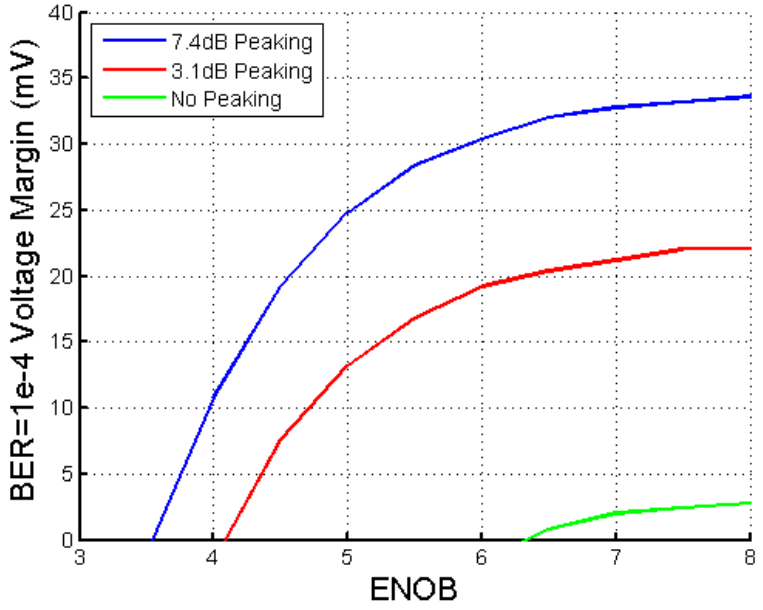


- Provides CTLE equalization to partially compensate for channel loss
- Variable gain amplifier (VGA) stages sets the ADC input to match the FSR for different channel and equalization configurations

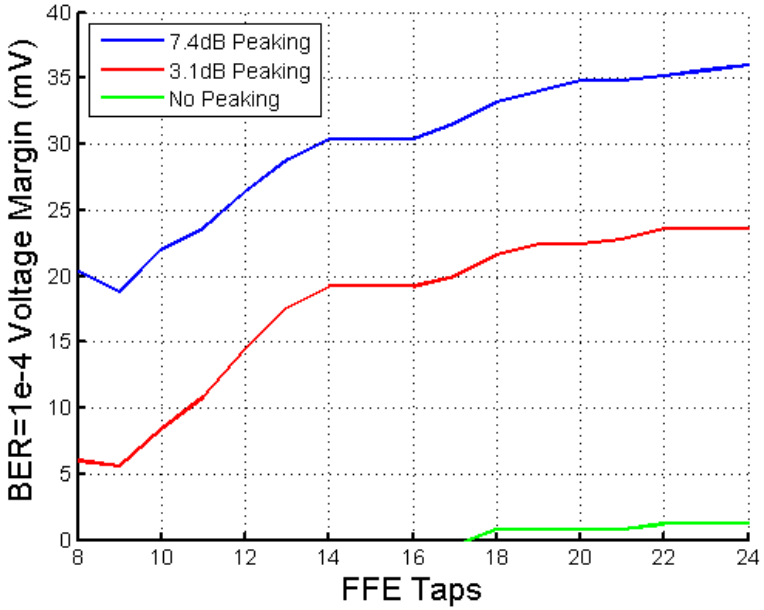
AFE Impact on ADC Resolution & Digital FFE Taps



TX=3-tap, RX=14-tap FFE & 1-tap DFE



6b ENOB

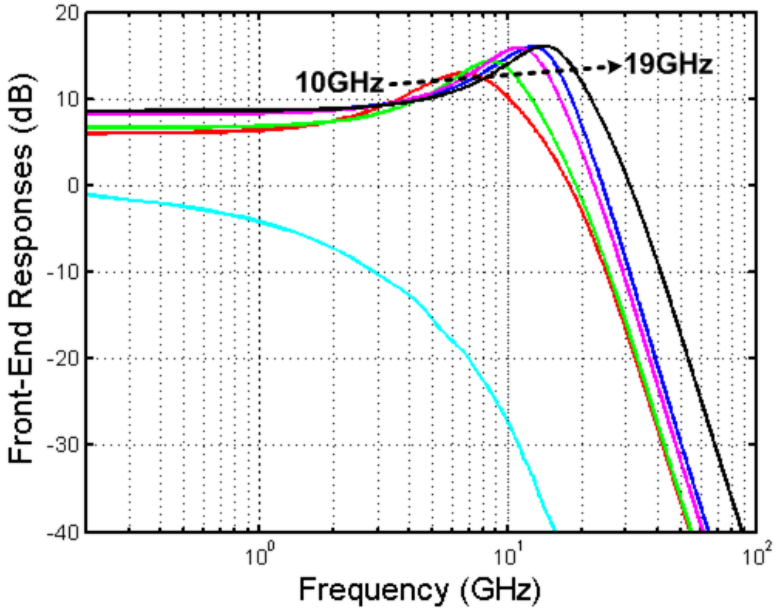


- CTLE peaking allows reduction in digital FFE tap count and strength
- This reduces quantization noise amplification and allows for a lower ENOB

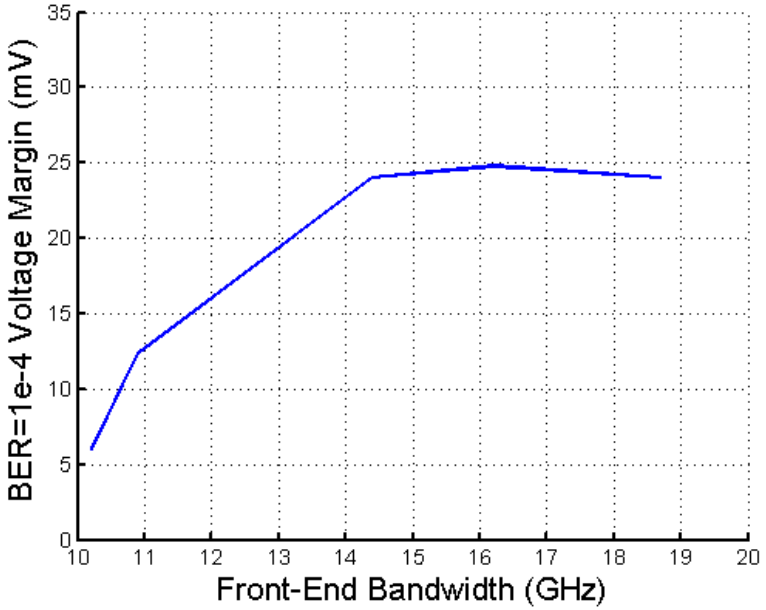
Key Simulator Settings

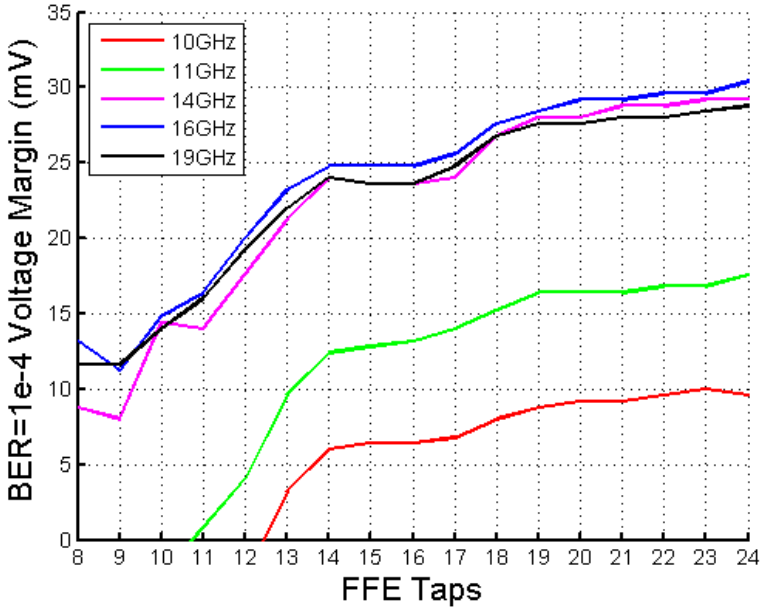
- 3-tap TX w/ 1Vpp swing
- 400mV ADC FSR
- $3mV_{rms}$ ADC input noise
- $RJ=300fs_{rms}$
- No TI effects

AFE Bandwidth



TX=3-tap, RX=14-tap FFE & 1-tap DFE





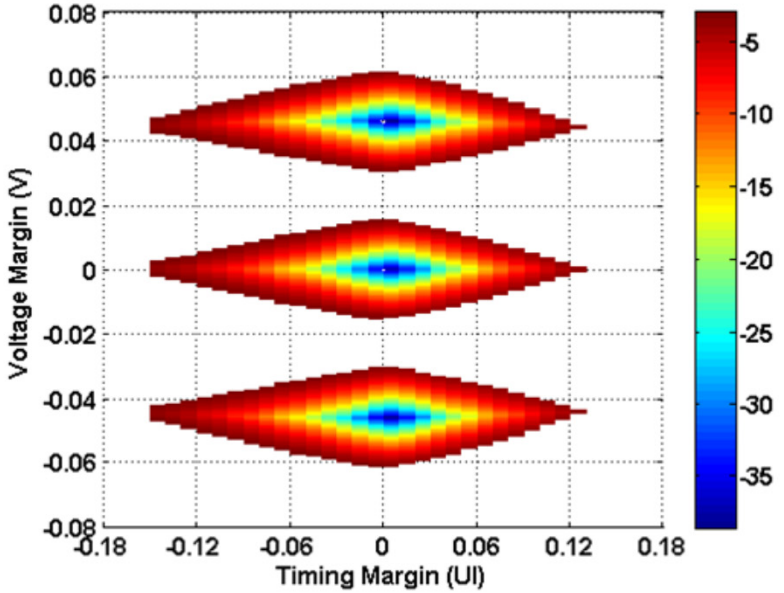
- Additional ISI is introduced if the AFE bandwidth drops below Nyquist
- This can be partially compensated with additional digital FFE taps

Key Simulator Settings

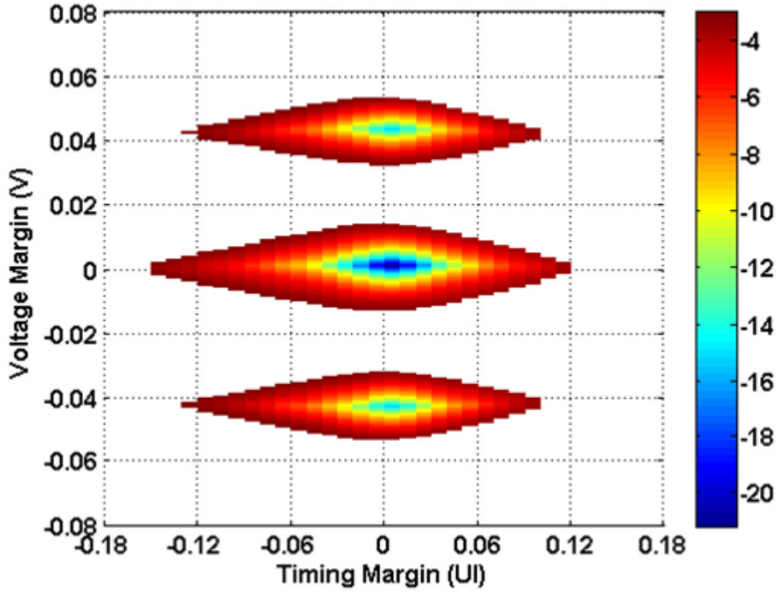
- 3-tap TX w/ 1Vpp swing
- 5b ENOB
- 400mV ADC FSR
- $3mV_{rms}$ ADC input noise
- $RJ=300fs_{rms}$
- No TI effects

AFE Linearity

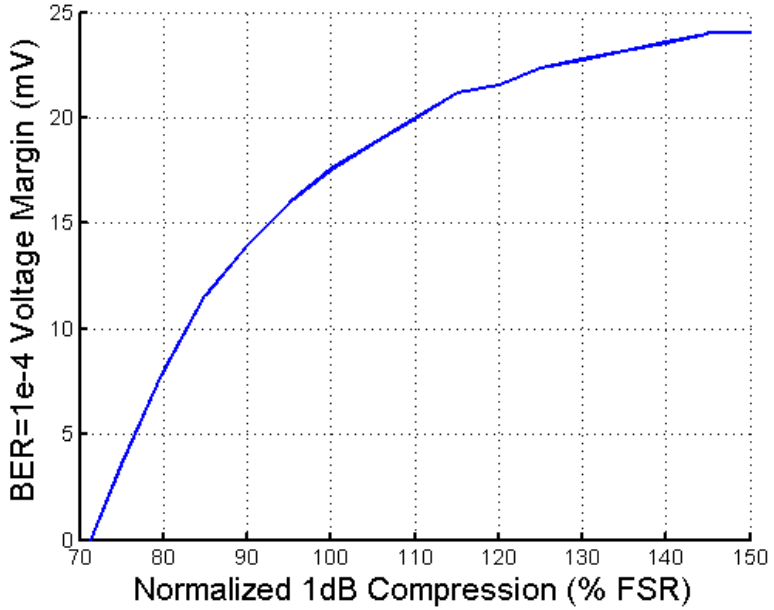
No Compression



Finite 1dB Compression



5b ENOB (w/o Compression)



- AFE compressive non-linearity degrades performance
- Setting the AFE 1dB compression voltage to >1.25X ADC FSR allows for minimal impact
- Severe degradation as the 1dB compression falls below the ADC FSR

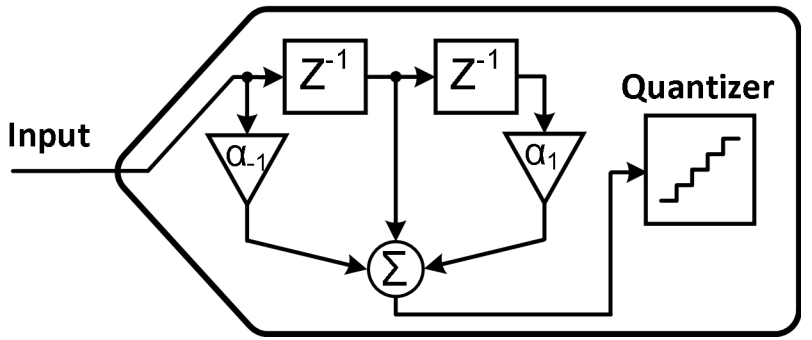
Key Simulator Settings

- 3-tap TX w/ 1Vpp swing
- CTLE/AGC FE w/ 7.4dB peaking and 16GHz BW
- 400mV ADC FSR
- Digital 14-tap FFE & 1-tap DFE
- $3mV_{rms}$ ADC input noise
- $RJ=300fs_{rms}$
- No TI effects

Embedded FFE in ADC

- Partial analog equalization in the form of an FFE filter can be efficiently embedded inside a SAR ADC
- Translates into reduced power and complexity in both the ADC and the digital equalizer

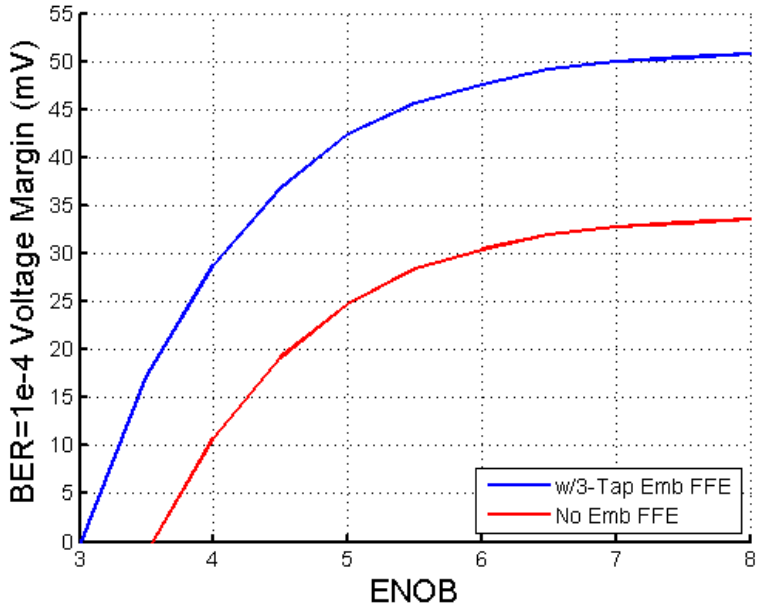
ADC with Embedded 3-Tap FFE



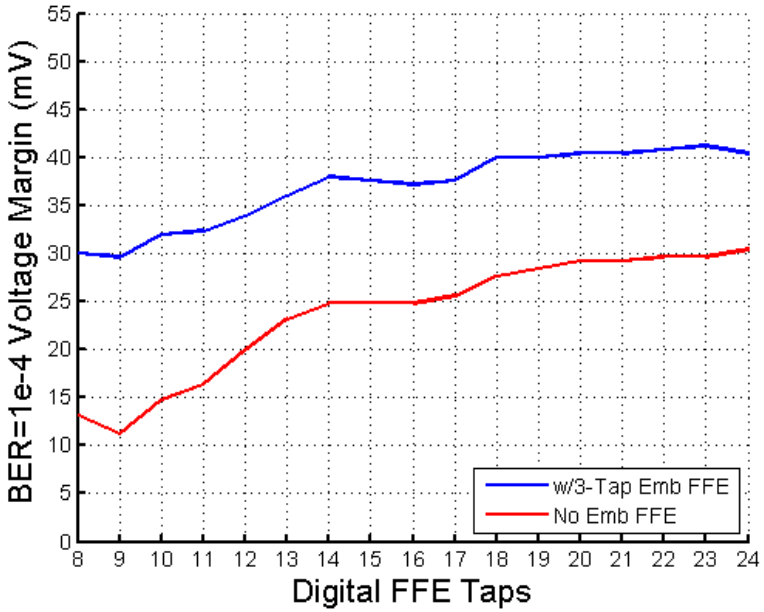
Key Simulator Settings

- Same 56Gb/s PAM4 over the 37dB channel
- 3-tap TX w/ 1Vpp swing
- CTLE/AGC FE w/ 7.4dB peaking and 16GHz BW
- 400mV ADC FSR
- Digital 1-tap DFE
- $3mV_{rms}$ ADC input noise
- $RJ=300fs_{rms}$
- No TI effects (more later)

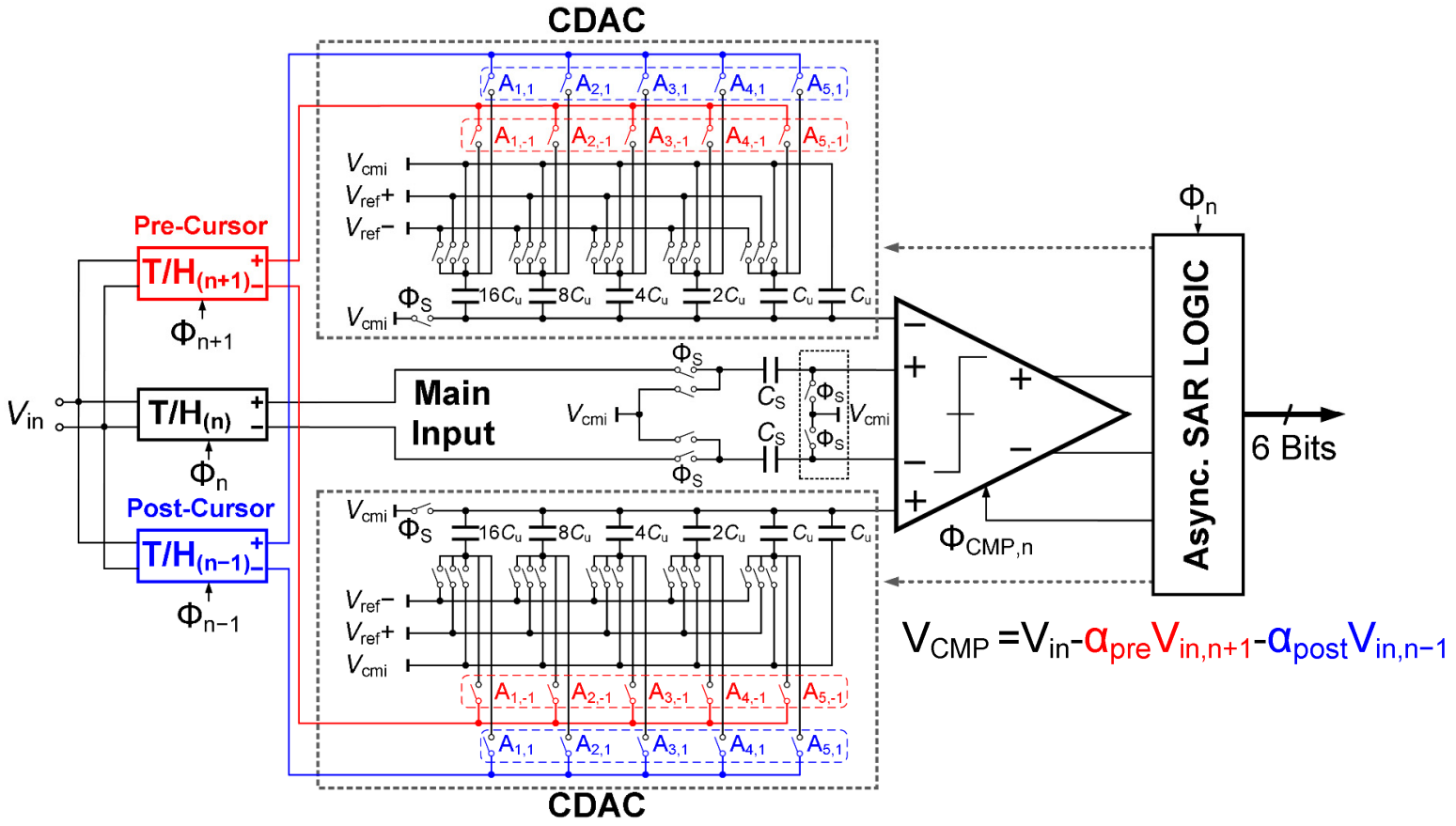
TX=3-tap, RX=14-tap FFE & 1-tap DFE



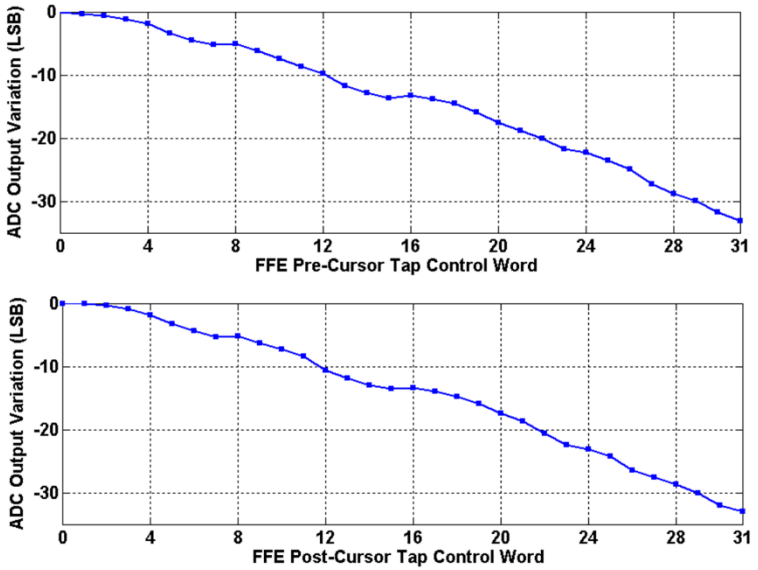
5b ENOB



Unit SAR ADC with Embedded FFE



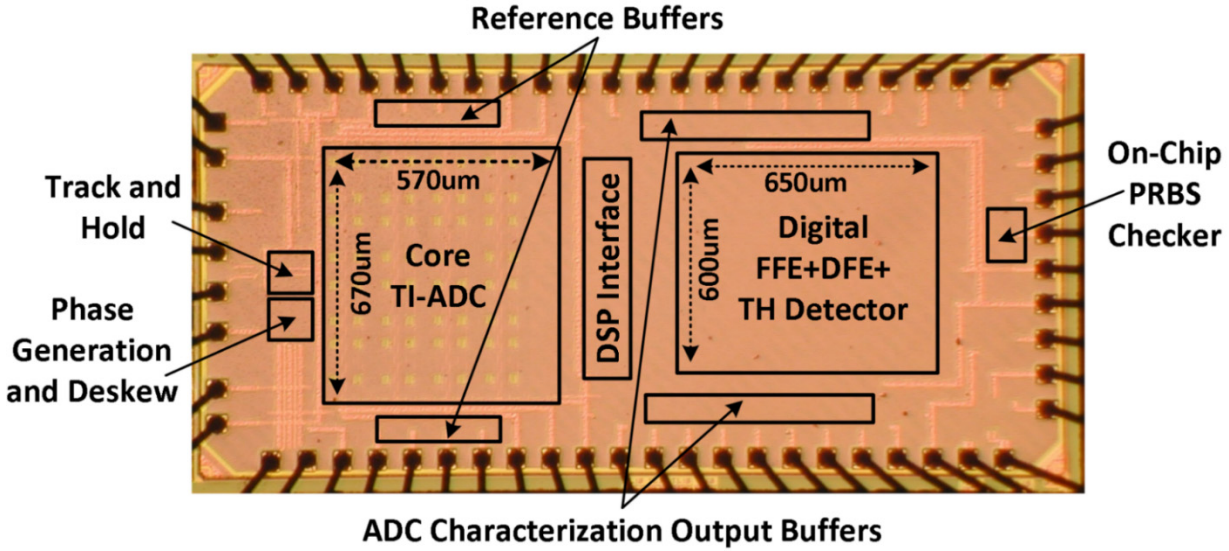
$$V_{CMP} = V_{in} - \alpha_{pre} V_{in,n+1} - \alpha_{post} V_{in,n-1}$$

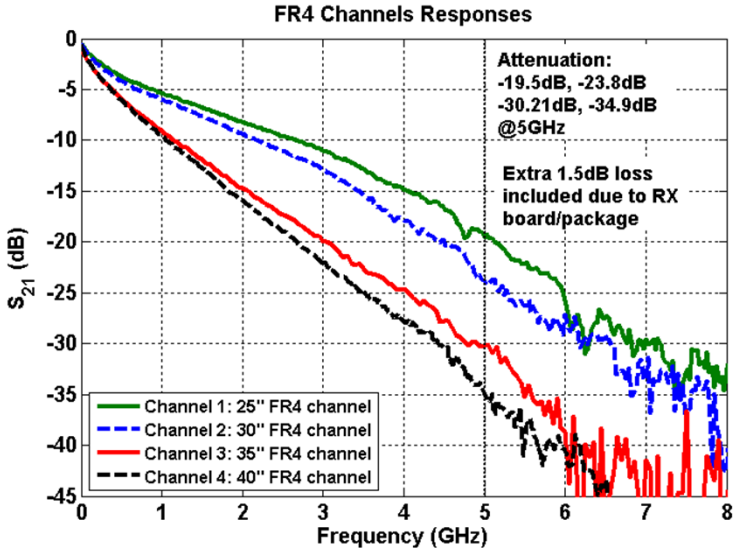


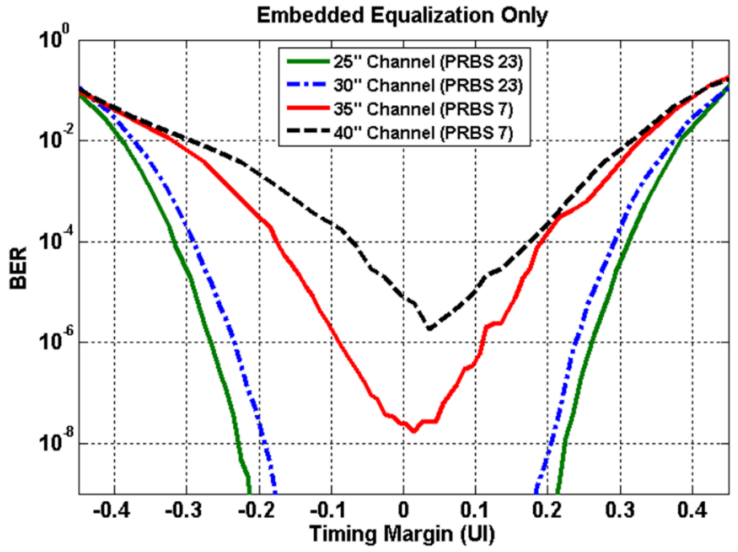
- 3-tap FFE efficiently embedded in the SAR CDAC
- Main trade-off is increased T/H loading (3X)

Both pre- and post-cursor taps have ~33 LSB range and ~1.1 LSB resolution

10Gb/s NRZ ADC-Based RX 65nm CMOS Prototype







- 10GS/s 32-way interleaved SAR ADC with embedded 3-tap FFE
- Digital 4-tap FFE and 3-tap loop-unrolled DFE
- Embedded equalization alone is sufficient for the two lowest-loss (21, 25dB) channels
- Additional digital equalization is necessary for the two highest-loss (32, 36dB) channels

Conclusion

- CMOS ADC-based receivers enable powerful digital equalization and symbol detection techniques for high data rate operation over electrical and optical wireline channels
- Time-interleaved ADCs are implemented to achieve the high effective sample rates
  - Calibration is necessary to compensate for channel mismatches
- Digital equalization allows for straight-forward implementation of large-tap digital FFEs, but PAM4 DFEs suffer from large complexity
- Analog front-end (CTLE & VGA) is critical to reduce ADC resolution requirements and match the input signal to ADC FSR
  - Must be designed with sufficient bandwidth and linearity

Acknowledgement

- My graduate students Shengchang Cai, Shiva Kiran, and Yuanming Zhu for assistance in slide preparation

- Intel, Semiconductor Research Corporation, and National Science Foundation for funding support

Suggested Papers at ISSCC 2018

- 6.4: A Fully Adaptive 19-to-56Gb/s PAM-4 Wireline Transceiver with a Configurable ADC in 16nm FinFET
- 6.5: A 64Gb/s PAM-4 Transceiver Utilizing an Adaptive Threshold ADC in 16nm FinFET
- 22.1: A 24-to-72GS/s 8b Time-Interleaved SAR ADC with 2.0-to-3.3pJ/conversion and >30dB SNDR at Nyquist in 14nm CMOS FinFET

References

Motivation

- [Cisco Global Cloud Index 2016] (2016). *Cisco Global Cloud Index: Forecast and Methodology*, 2015–2020. [Online]. Available: http://www.cisco.com.

Recent ADC-Based XCVR/RX

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