ISSCC 2013 Tutorial

Circuit Design using FinFETs

Bing Sheu, Ph.D. & IEEE Fellow
Director, at R&D
TSMC

email: bing_sheu@tsmc.com

February 17, 2013

© 2013 IEEE

Acknowledgment

Special thanks to the following people for contribution of content:
Chih-Sheng Chang, Clement Wann; Ken Wang; L.J. Tyan;
Kuo-Ji Chen, Ming-Hsiang Song; Tommy Chen, H.J. Liao;
Yung-Chow Peng; and Chris Huang;
from several groups inside TSMC R&D:
Advanced Technology Research;
Design Flow; Layout; Library & IPs, I/O & ESD;
Memory Design; High-Speed Circuits;
and especially to **CTO/VP Jack Sun** & **DTP VP Cliff Hou**.

SPICE BSIM-CMG Modeling slides are provided by **Chair-Professor Chenming Hu** at University of California, Berkeley.

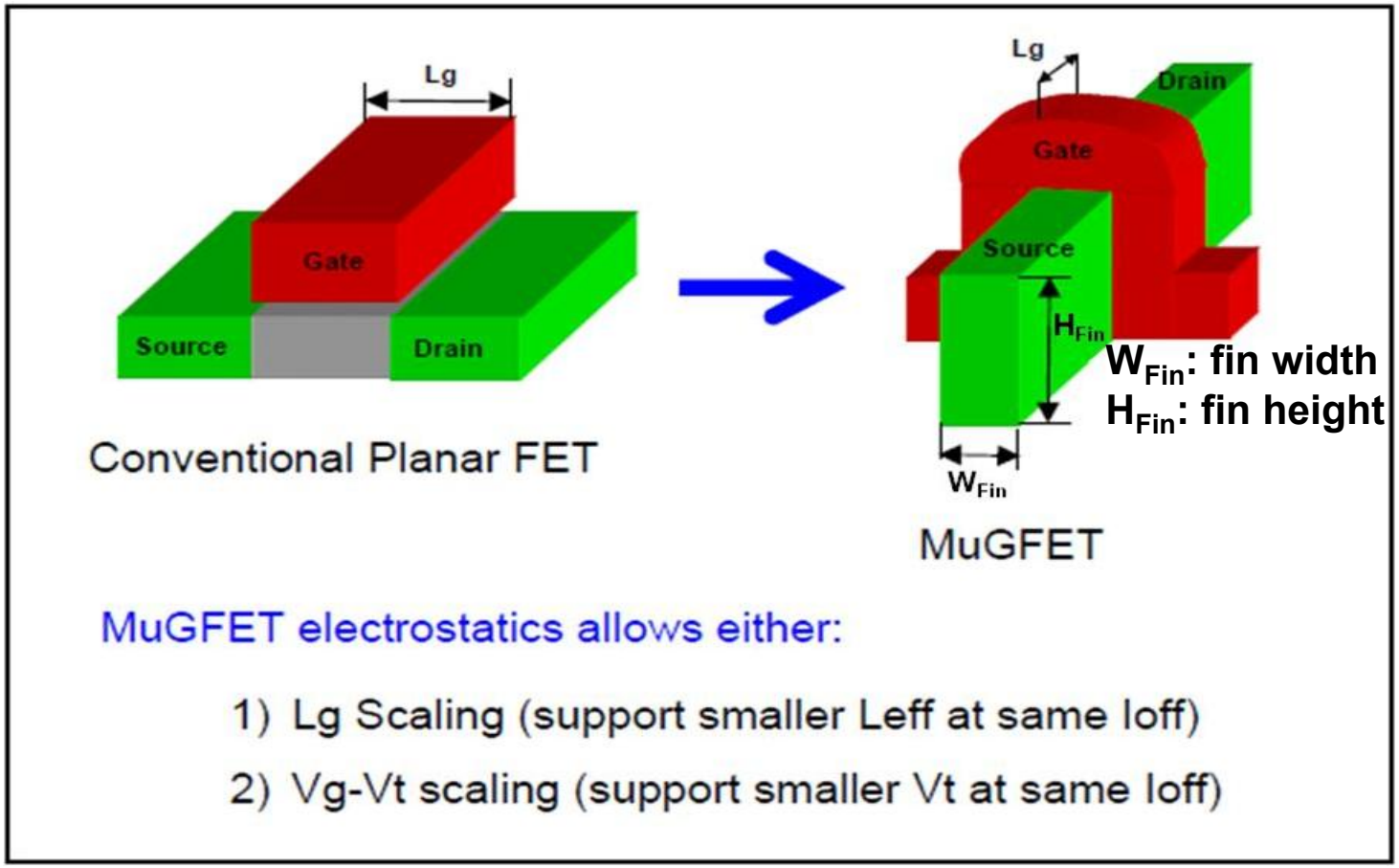
Assistance from **Ali** Sheikholeslami at University of Toronto for ISSCC Tutorial Program, and from **Stephen** Kosonocky of AMD and **Victor** Zyuban of IBM at Energy-Efficient Digital Track is highly appreciated.

© 2013 IEEE

Outline

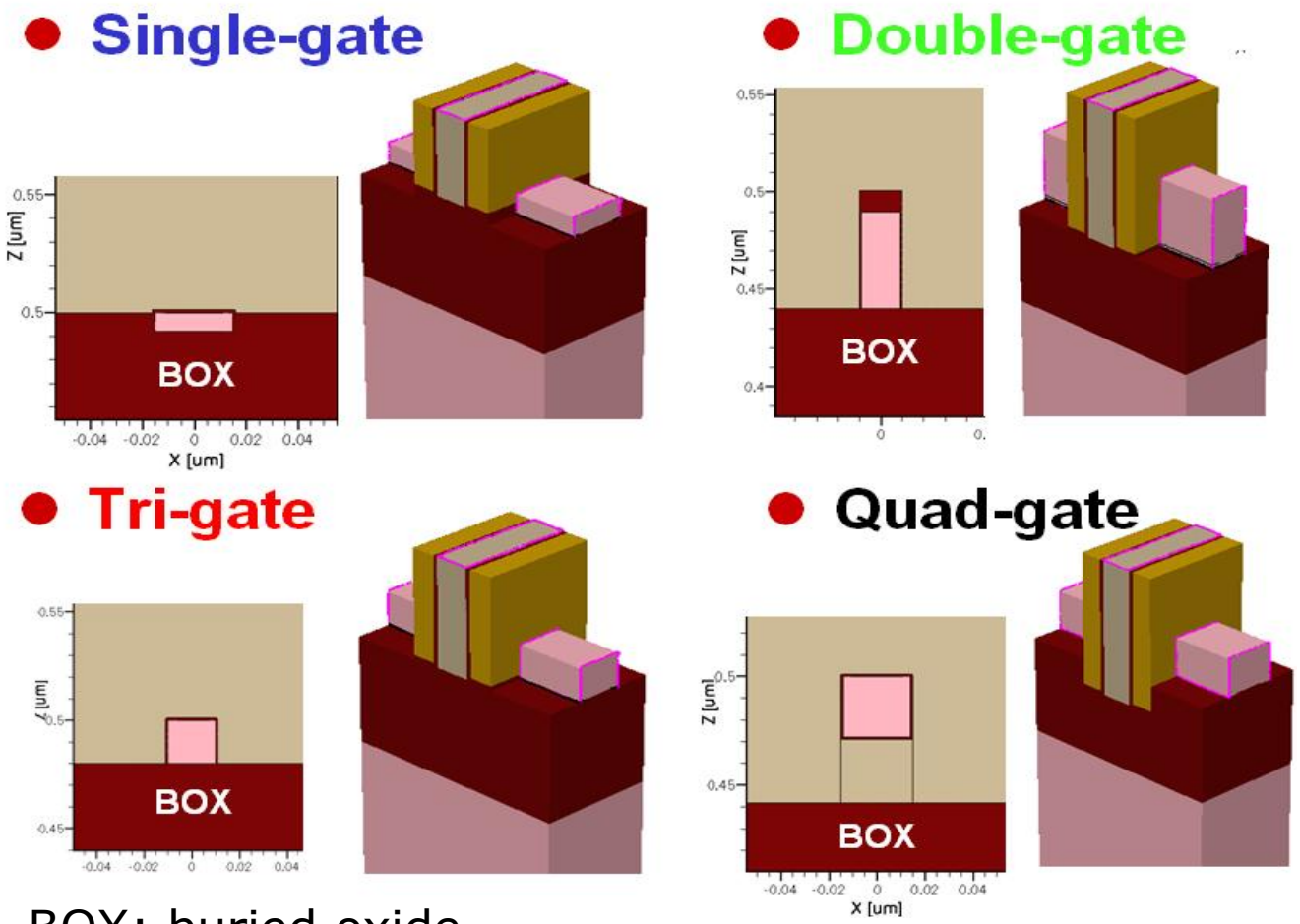
- 1. Technology Considerations
- 2. Spice Modeling
- 3. Design Methodology and CAD Tools
- 4. Digital Design
  - Standard Cells, Layout
  - IO and ESD
- 5. SRAM
- 6. Analog & Mixed-Signal, RF
- 7. Conclusion
- References

Key FinFET Benefits: Electrostatics



Modified (re-wording) from Ref: J. Kavalieros, Technology Short Course, VLSI Symposium, 2008

Multi-Gate Simulation Structures

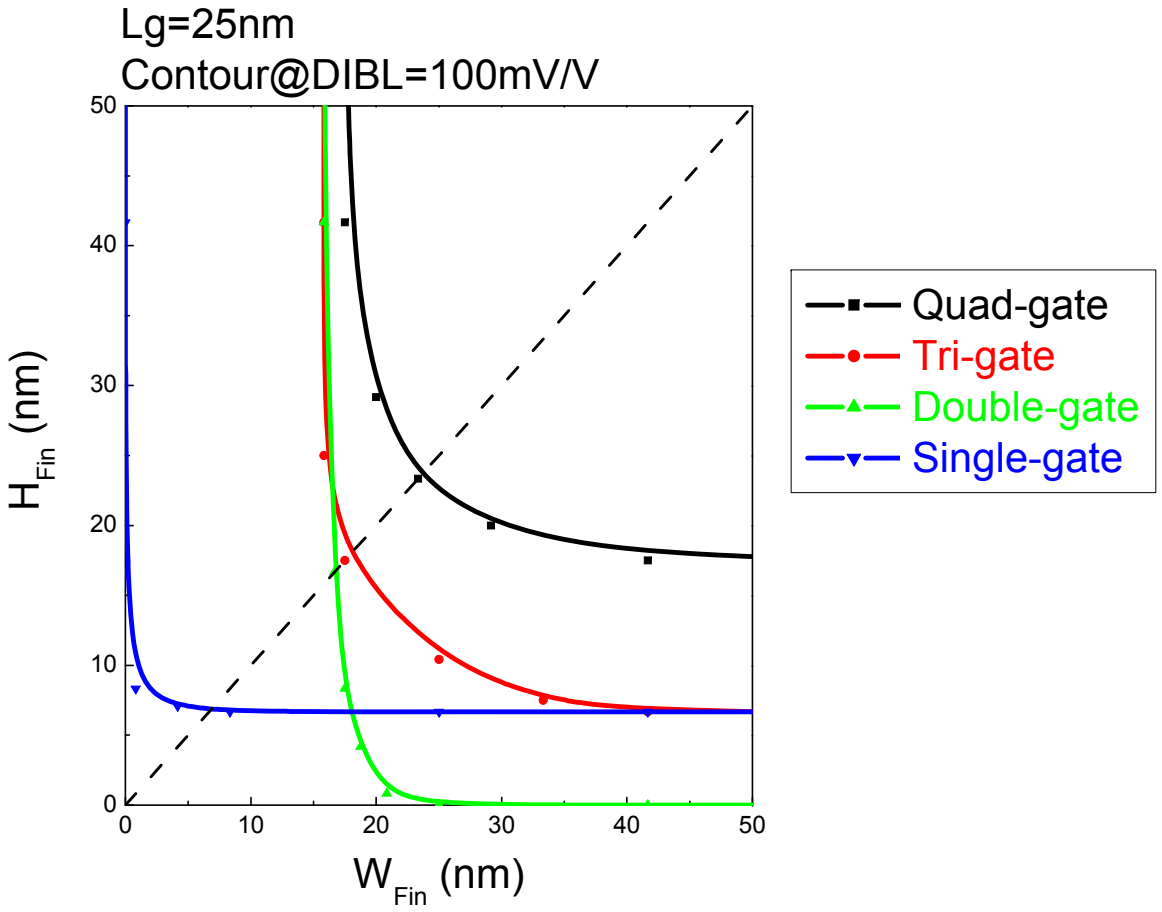


BOX: buried oxide

- SOI substrate was used for this simulation study

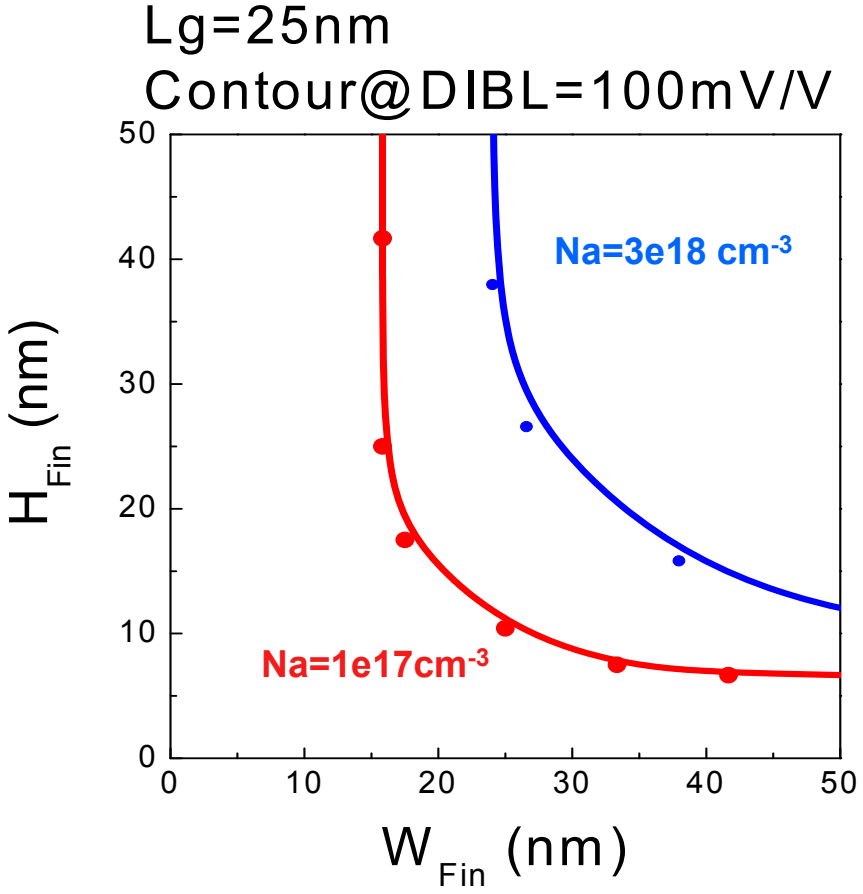
© 2013 IEEE

FinFET Electrostatics Simulation -1



- With more gate control, a wider fin width could be used to achieve same DIBL (drain-induced barrier lowering)

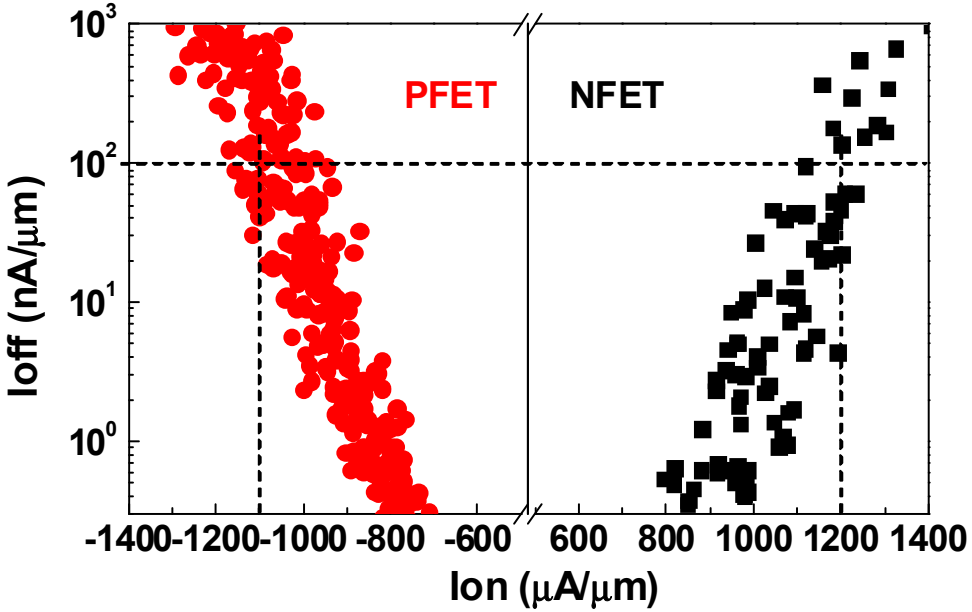
FinFET Electrostatics Simulation -2

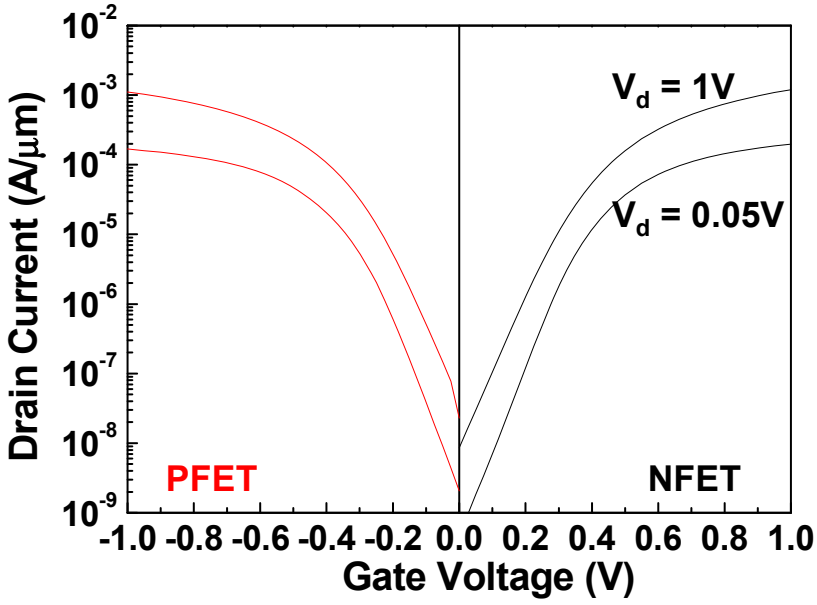


- Traditional channel doping could also be used to further improve DIBL

© 2013 IEEE

22/20nm FinFET Device



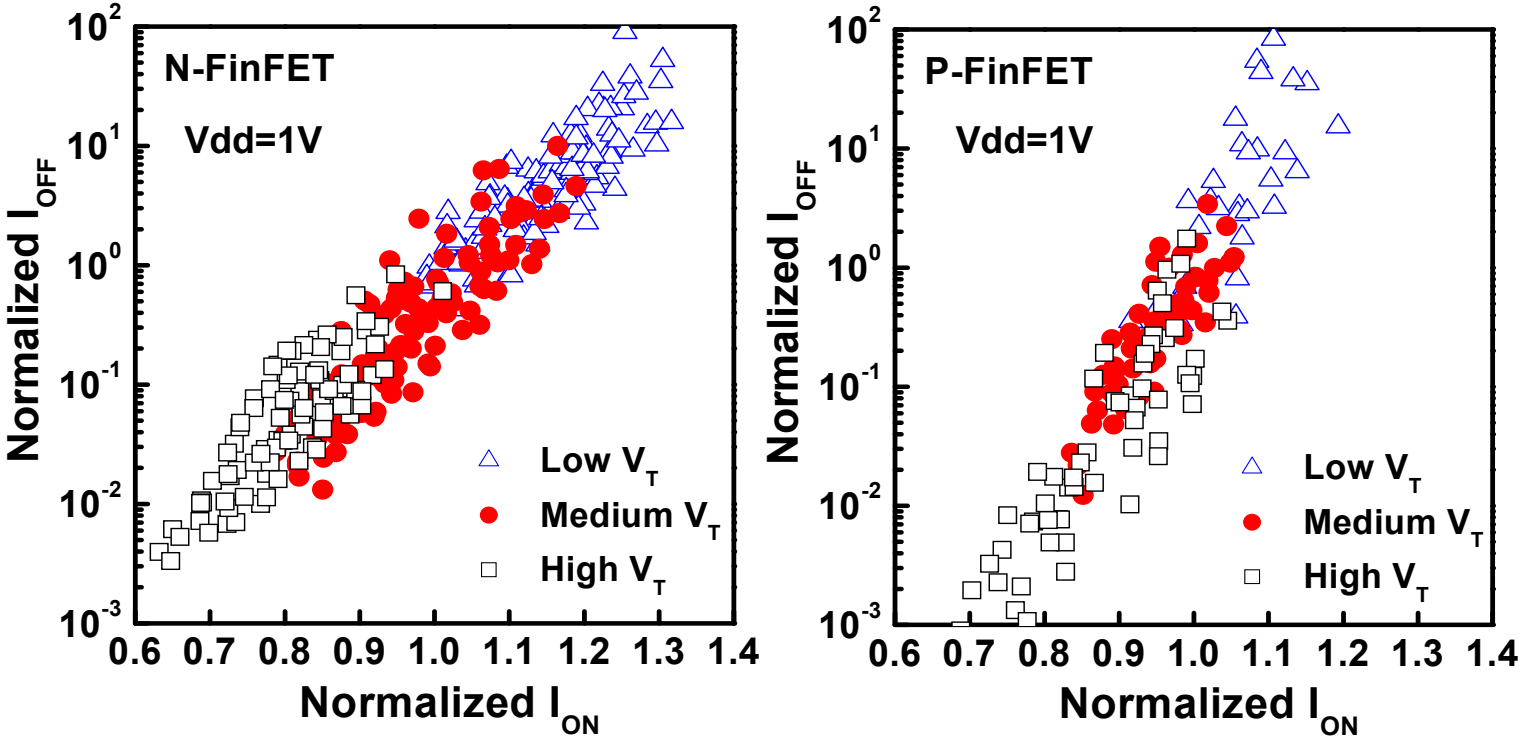


- High performance 22/20nm FinFET with
  - Ion (n/p)= 1200/1100 uA/um at Vdd=1V, Ioff=100nA/um
  - DIBL (n/p)=100/120 mV/V
  - Sub-threshold swing ~ 80mV/dec

Ref: C. C. Wu, paper 27.1, IEEE IEDM, 2010

© 2013 IEEE

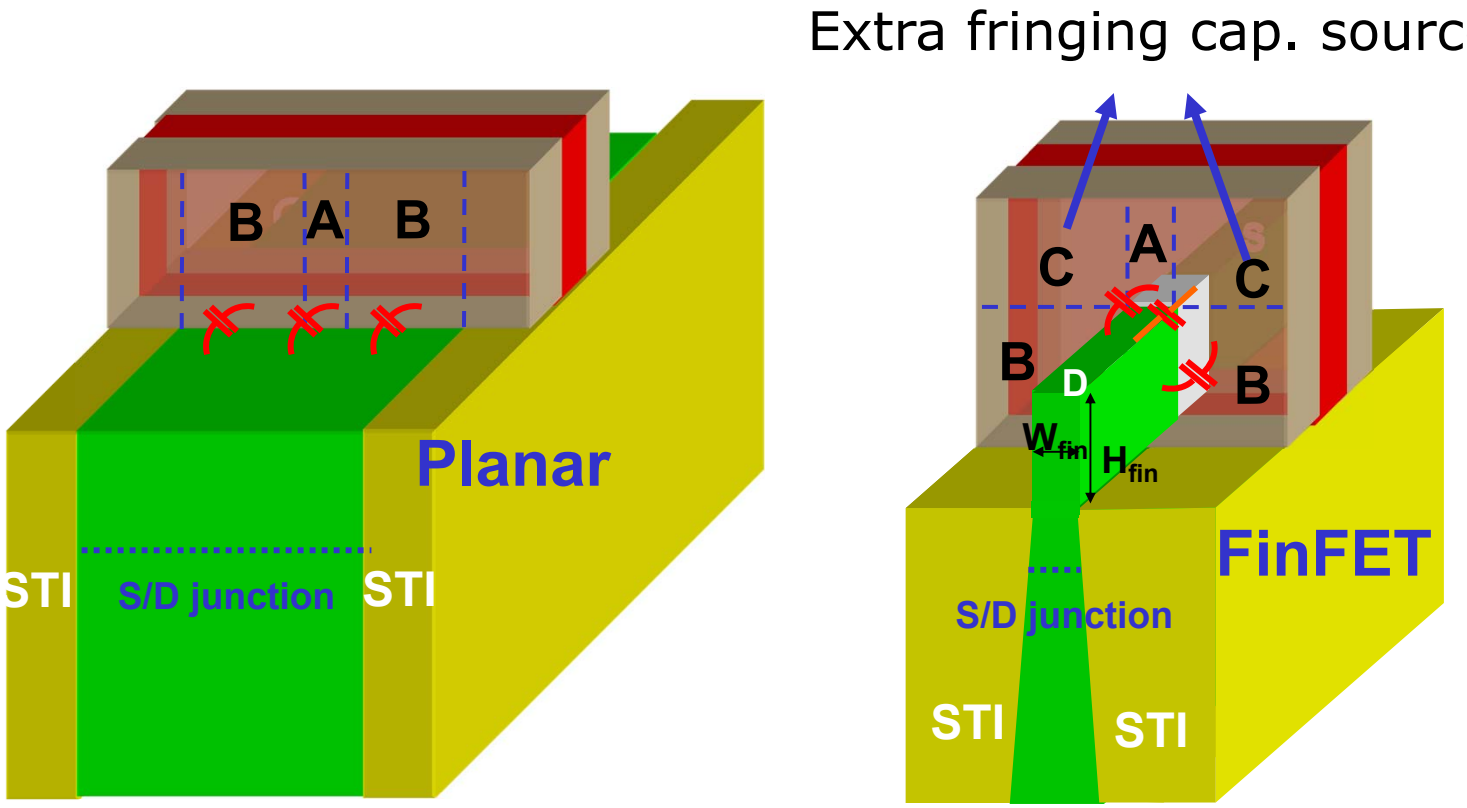
32/28nm SoC FinFET



- 32/28nm SoC FinFET technology with
  - Low, medium and high Vt transistors follow the same trend line
  - Multi-Vt techniques do not compromise FinFET performance

Ref: C.-C. Yeh, paper 34.1, IEEE IEDM, 2010

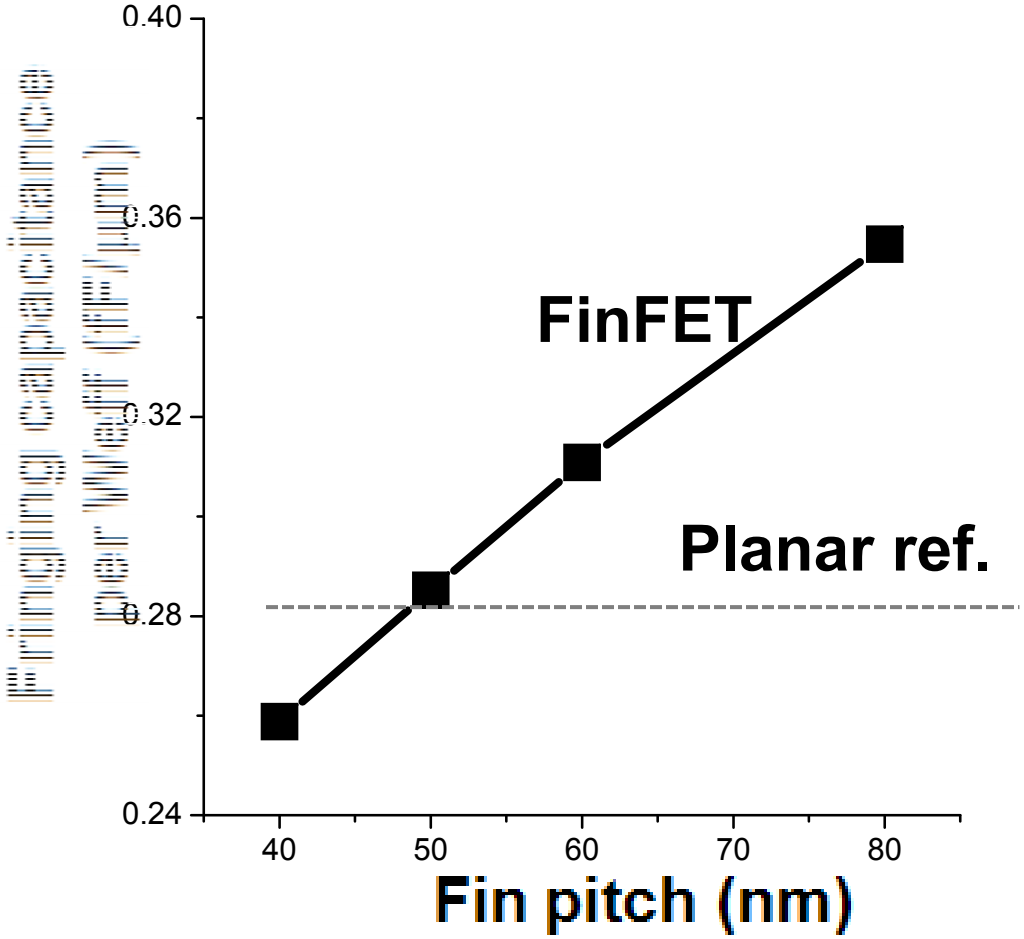
FinFET Parasitic Fringing Capacitance



- FinFET parasitic fringing capacitance could be higher than that of planar MOSFET due to extra gate-to-S/D coupling area (C regions)
- The extra coupling (area of C) could be greatly reduced with tight fin pitch

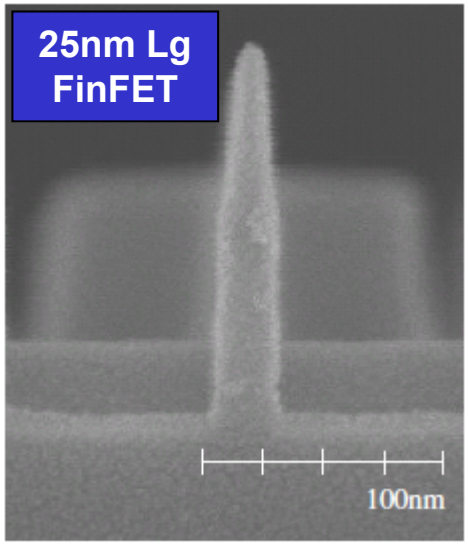
© 2013 IEEE

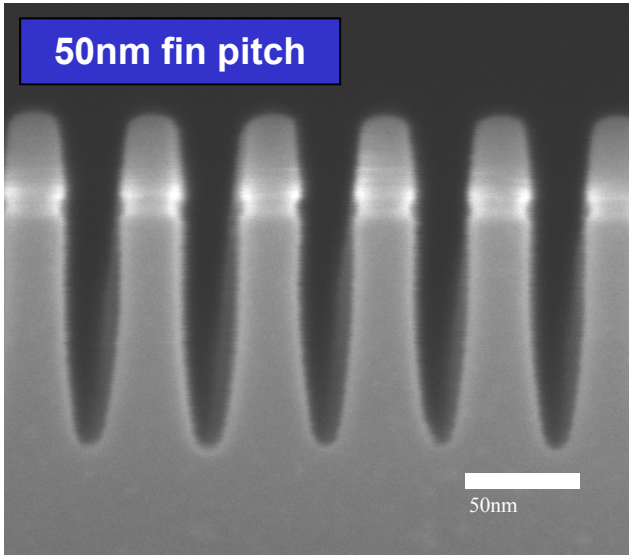
Effect of Pitch on Fringing Cap.

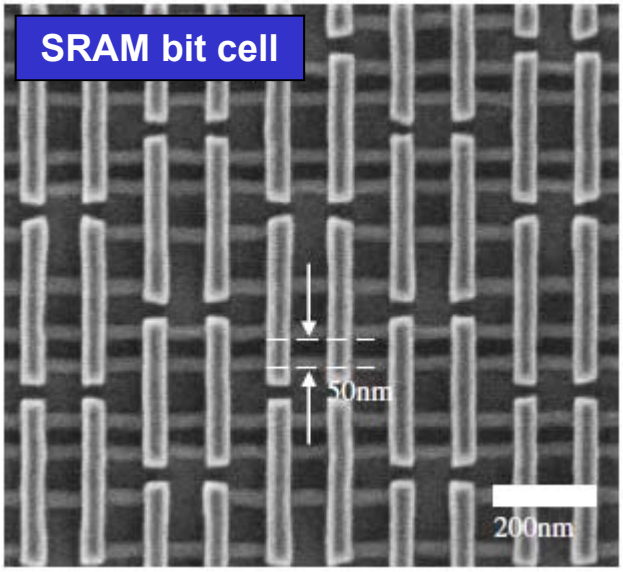


- TCAD simulation showed that with an aggressive fin pitch scaling, the 3D FinFET fringing capacitance penalty could be greatly reduced.

Pitch Scaling with Spacer Patterning



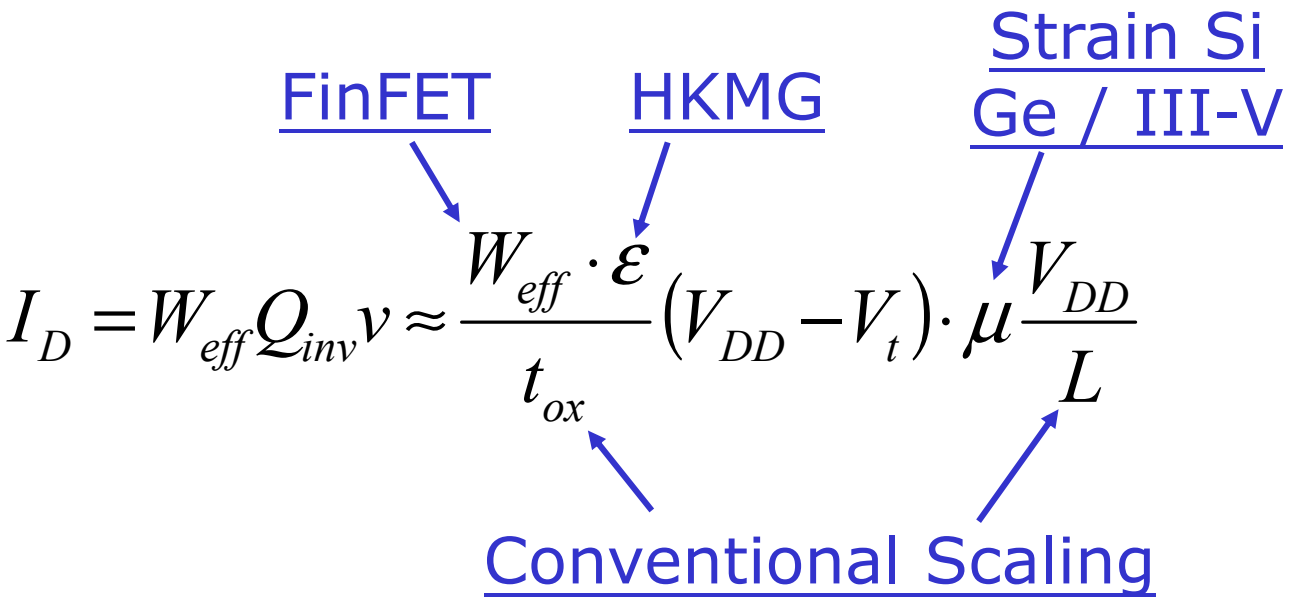




- 32/28nm tool used to demonstrated 50nm fin pitch by spacer pitch halving technique.

Ref: C.-Y. Chang, paper 12.2, IEEE IEDM, 2009

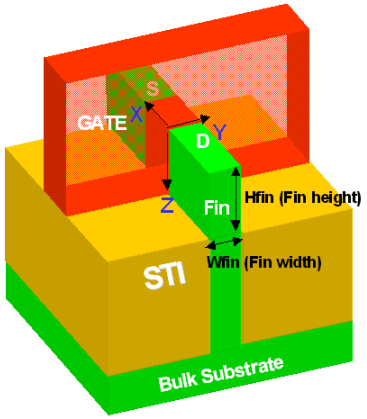
Equivalent Scaling



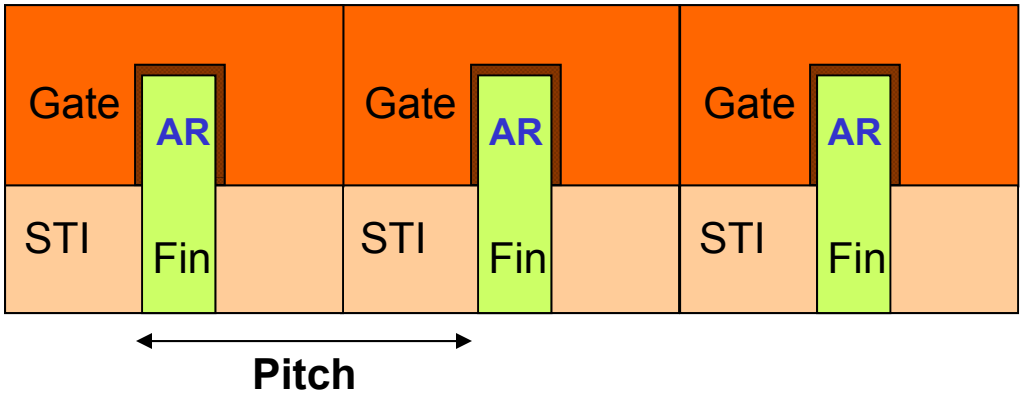
- More current in the same layout footprint
- Weff > fin_pitch

© 2013 IEEE

More Current per Footprint

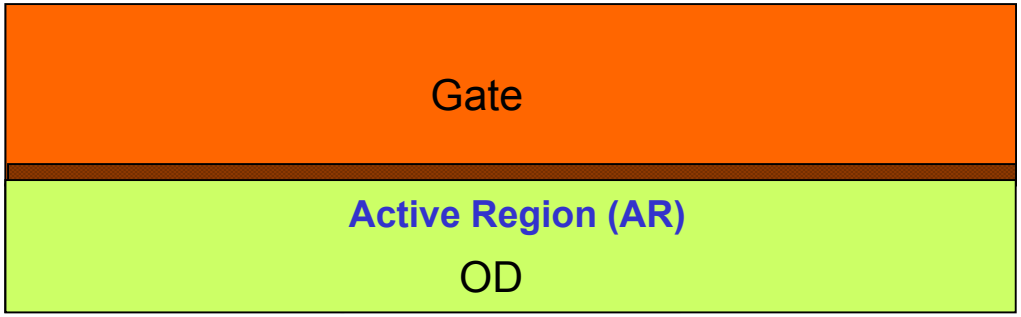


- FinFET: Cross-section view on Y-Z plane



	Effective width
FinFET	**3 * (2*H_{Fin}+W_{Fin})**
Planar	**W_{OD}**

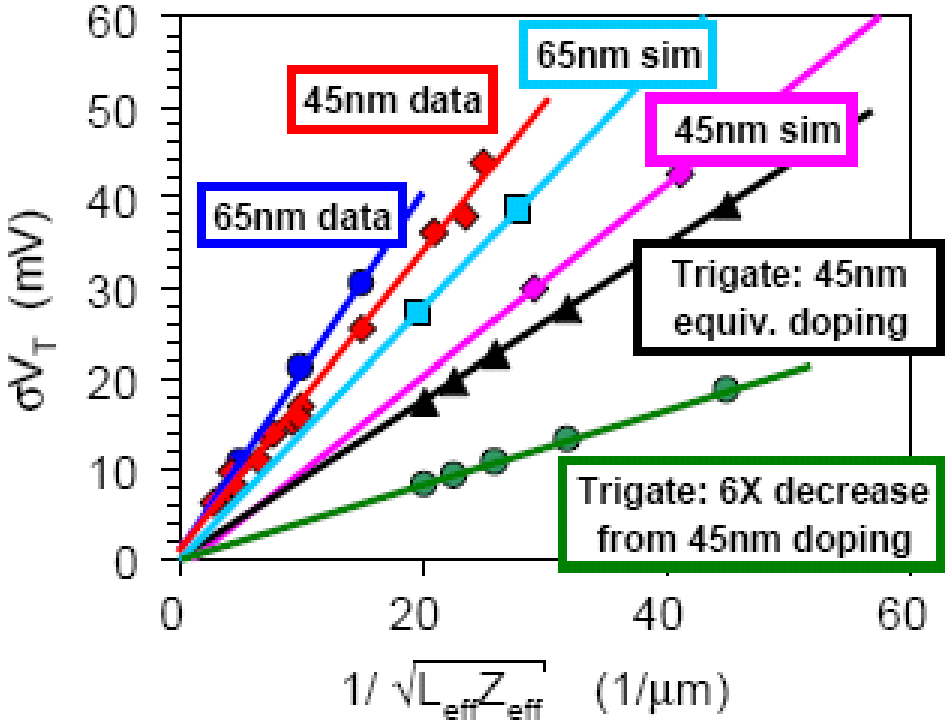
- Planar: Cross-section view on width direction



- Increase effective width for a given footprint: increase H_{Fin} and/or reduce fin pitch

© 2013 IEEE

FinFET Random Doping Fluctuation



Ref: K. J. Kuhn, paper 18.2, IEEE IEDM, 2007

- With the same doping, simulation showed that FinFET structure can reduce RDF by ~10%
- With a lower doping, the RDF can be further reduced

© 2013 IEEE

Outline

- 1. Technology Considerations
- **2. Spice Modeling**
- 3. Design Methodology and CAD Tools
- 4. Digital Design
  - Standard Cells, Layout
  - IO and ESD
- 5. SRAM
- 6. Analog & Mixed-Signal, RF
- 7. Conclusion
- References

BSIM SPICE Models

558 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-22, NO. 4, AUGUST 1987

BSIM: Berkeley Short-Channel IGFET Model for MOS Transistors

BING J. SHEU, MEMBER, IEEE, DONALD L. SCHARFETTER, FELLOW, IEEE, PING-KEUNG KO, MEMBER, IEEE, AND MIN-CHIE JENG

Berkeley **S**hort-channel **I**GFET **M**odel

- 1997: BSIM3 became first industry standard MOSFET model for IC simulation
- BSIM3, BSIM4, BSIM-SOI used by hundreds of companies for design of ICs worth half-trillion U.S. dollars
- BSIM models of FinFET and UTBSOI are available & free

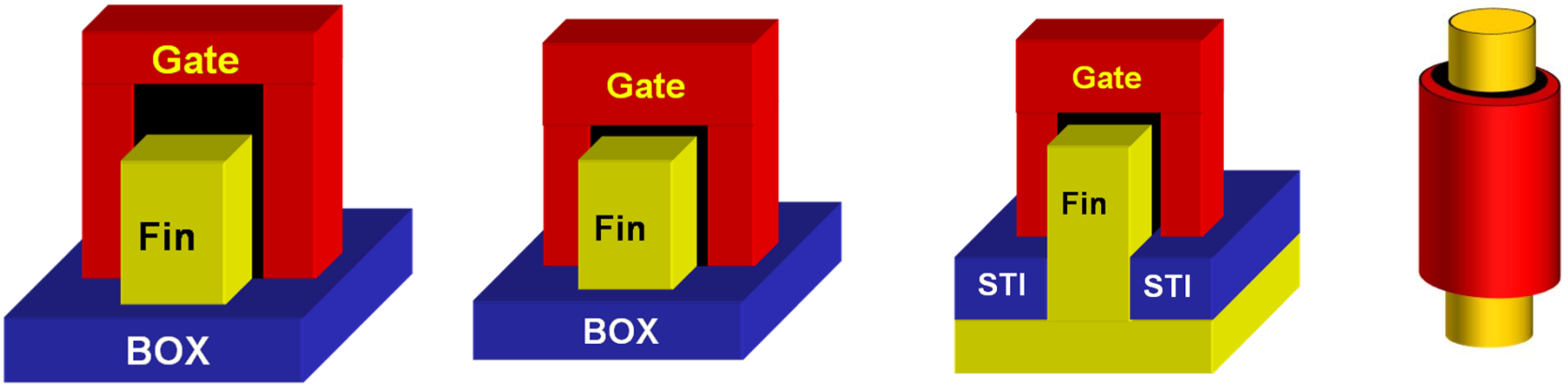
BSIM-CMG

- Core Model
  - Surface Potential Equation
  - Drain Current
  - Capacitance Model
- Real Device Effects
- Symmetry / Continuity Tests
- Model Availability: A versatile model for double-gate, triple-gate, even cylindrical gate FET. Passed Industry FinFET Standard balloting in Jan. 2012. Available now.
  - BSIM-IMG is a related model for Ultra-Thin-Body SOI technology (used by ST Microelectronics). Available now.

This slide is provided by UC Berkeley Prof. Chenming Hu

© 2013 IEEE

Common-Multi-Gate Modeling

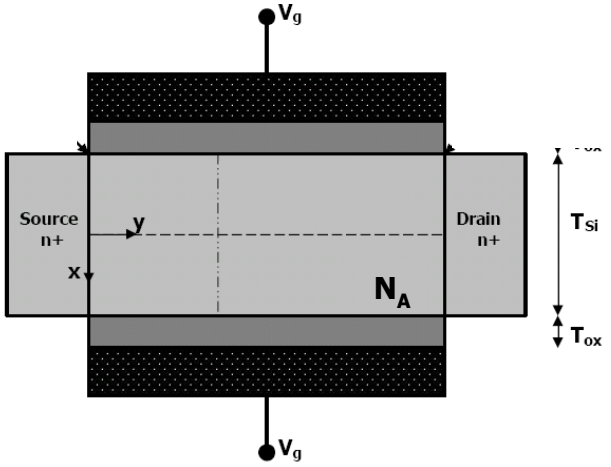


- Common Multi-gate (BSIM-CMG):
  - All gates tied together
  - Surface-potential-based core I-V and C-V model
  - Supports double-gate, triple-gate, quadruple-gate, cylindrical-gate; Bulk and SOI substrates

This slide is provided by UC Berkeley Prof. Chenming Hu

Surface Potential Core

- Surface potential is obtained from solution of Poisson's equation & Gauss' Law.
- Poisson's equation inside the body can be written as (V_{ch} is channel potential)



$$\frac{d^2\psi}{dx^2} = \frac{qn_i}{\epsilon_{Si}} \cdot \left(\underbrace{e^{\frac{q\psi}{kT}} \cdot e^{\frac{-q\phi_B}{kT}} \cdot e^{-\frac{qV_{ch}}{kT}}}_{\text{Inversion Carriers}} + \underbrace{e^{\frac{q\phi_B}{kT}}}_{\text{Body Doping}} \right)$$

where $\phi_B = \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right)$

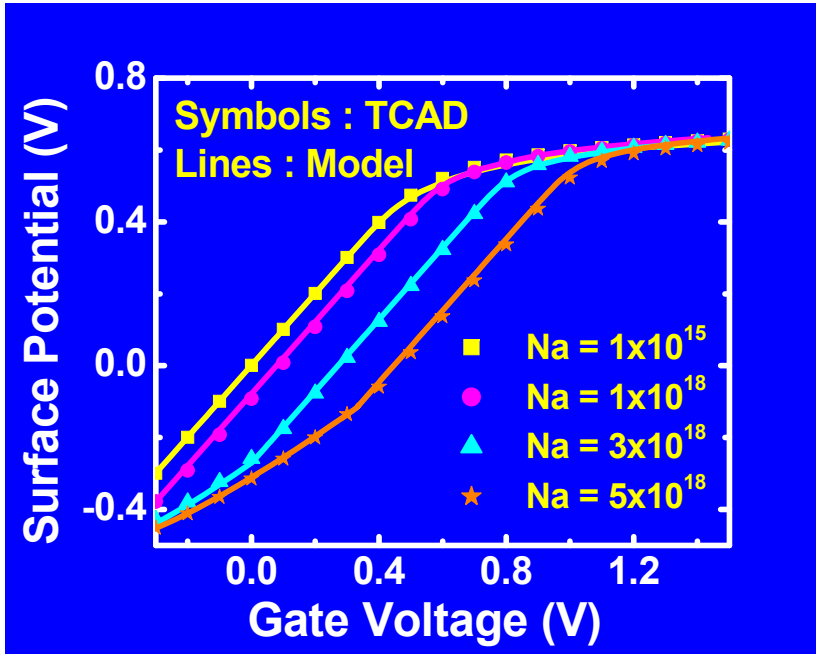
$$\underbrace{\psi}_{\text{Net Surface Potential}} = \underbrace{\psi_{inv}}_{\text{Inversion Carriers only}} + \underbrace{\psi_{pert}}_{\text{Perturbation due to finite doping}}$$

- Body doping complicates the solution of the Poisson's equation.
- Perturbation approach is used to solve this problem.

Ref. M. Dunga et al., IEEE TED, No. 9, 2006; M. Dunga, et al., VLSI 2007; Mohan Dunga, PhD Dissertation, UC Berkeley. Slide provided by Prof. C. Hu

© 2013 IEEE

Surface Potential Calculation



- Model matches 2D TCAD very well without fitting parameters for different body doping concentrations

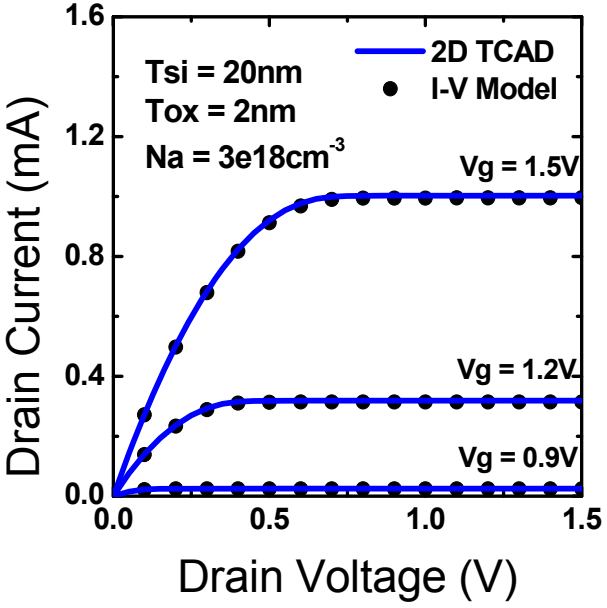
This slide is provided by UC Berkeley Prof. Chenming Hu

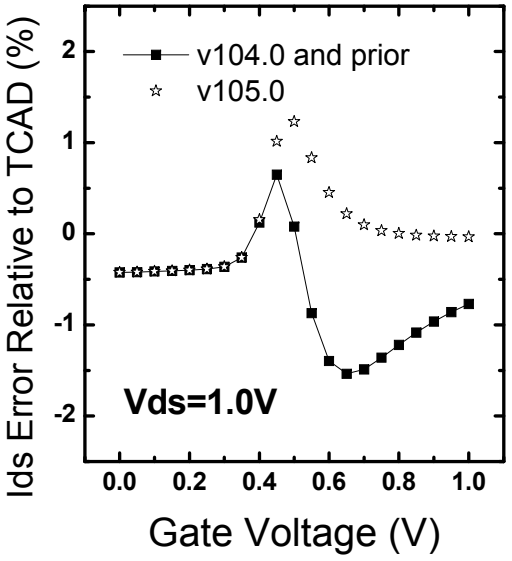
Core Drain Current Model

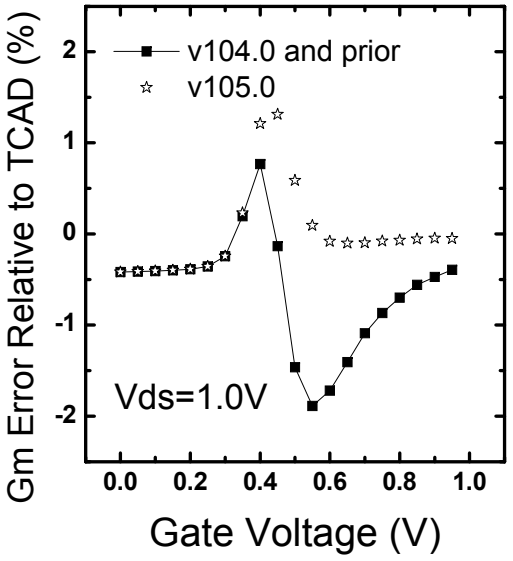
- Drain Current (Pao-Sah, No charge sheet approximation)

$$Id = \mu \cdot \frac{W_{eff}}{L_{eff}} \cdot \left[\frac{Q_{is}^2 - Q_{id}^2}{2\,C_{ox}} + V_t \cdot \left(2 - \frac{2\,Q_0}{2\,Q_0 + Q_{is} + Q_{id}} \right) (Q_{is} - Q_{id}) \right]$$

$$Q_0 = 2Q_B + 5V_tC_{si}$$

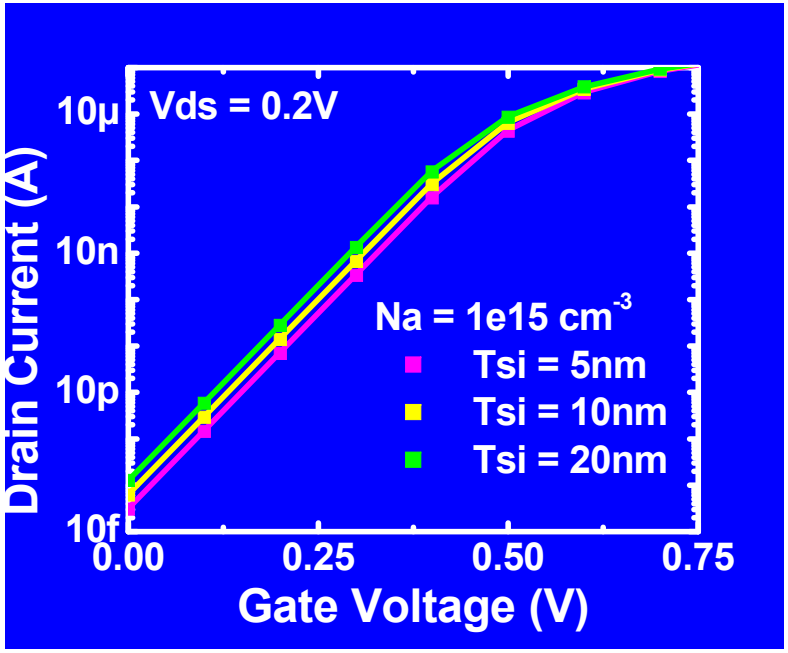






This slide is provided by UC Berkeley Prof. Chenming Hu

Drain Current in Volume Inversion



Lines: Model
Symbols: TCAD

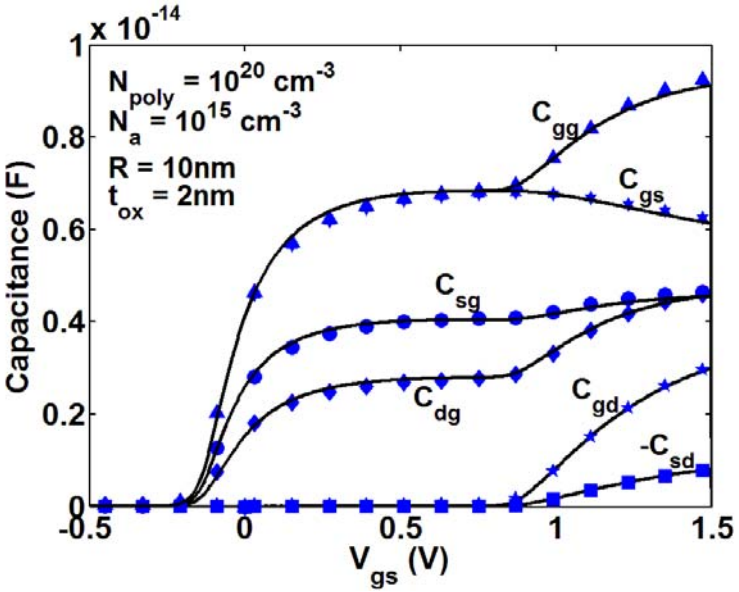
Ref. M. Dunga, VLSI Symposium, 2007

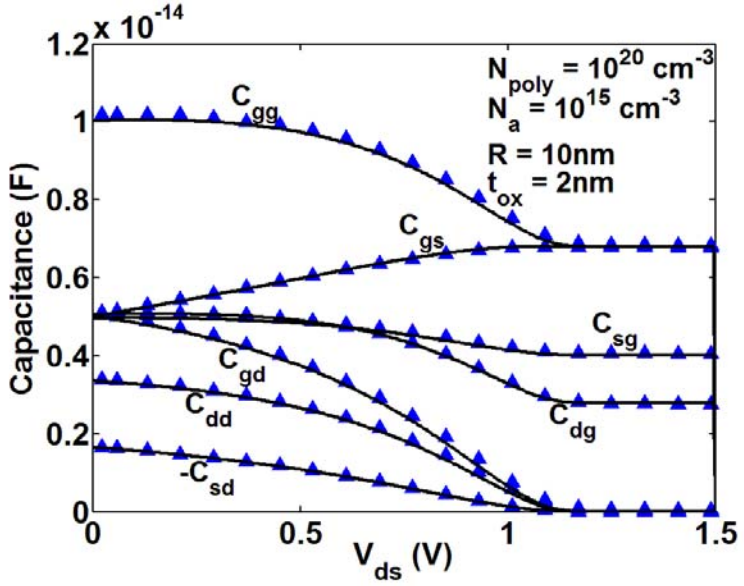
- The proportionality of inversion carrier density and hence current to the body thickness in sub-threshold region for un-doped/lightly-doped channel is captured.

This slide is provided by UC Berkeley Prof. Chenming Hu

Core Capacitance Model

- Model inherently exhibits symmetry
  - $C_{ij} = C_{ji}$ @ V_{ds}= 0 V
- Model overlies TCAD results
  - No tuning parameters used
- Accurate short channel behavior – RF Design



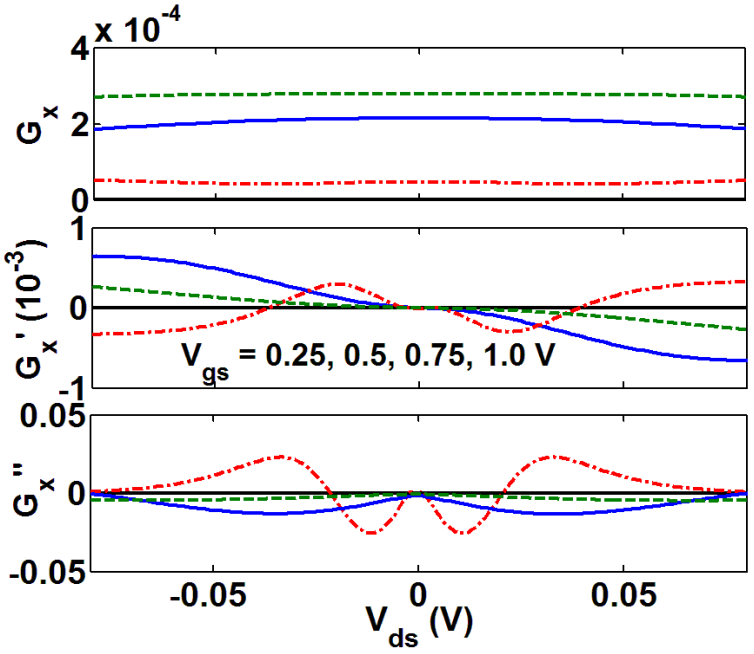


Symbols: TCAD Results; Lines: Model

Slide provided by UCB Prof. C. Hu

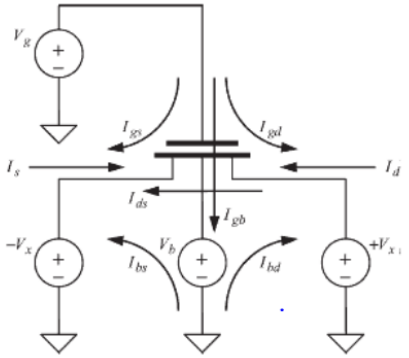
Symmetry / Continuity Tests

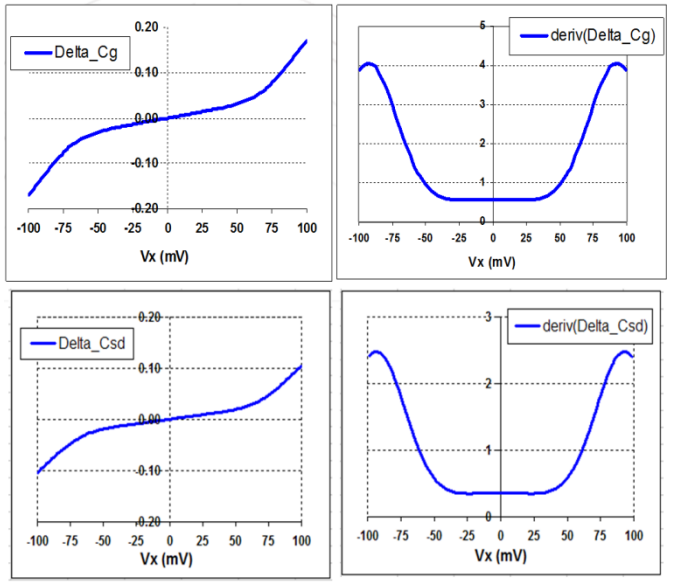
- Model passes both DC and AC Symmetry Tests



Drain Current

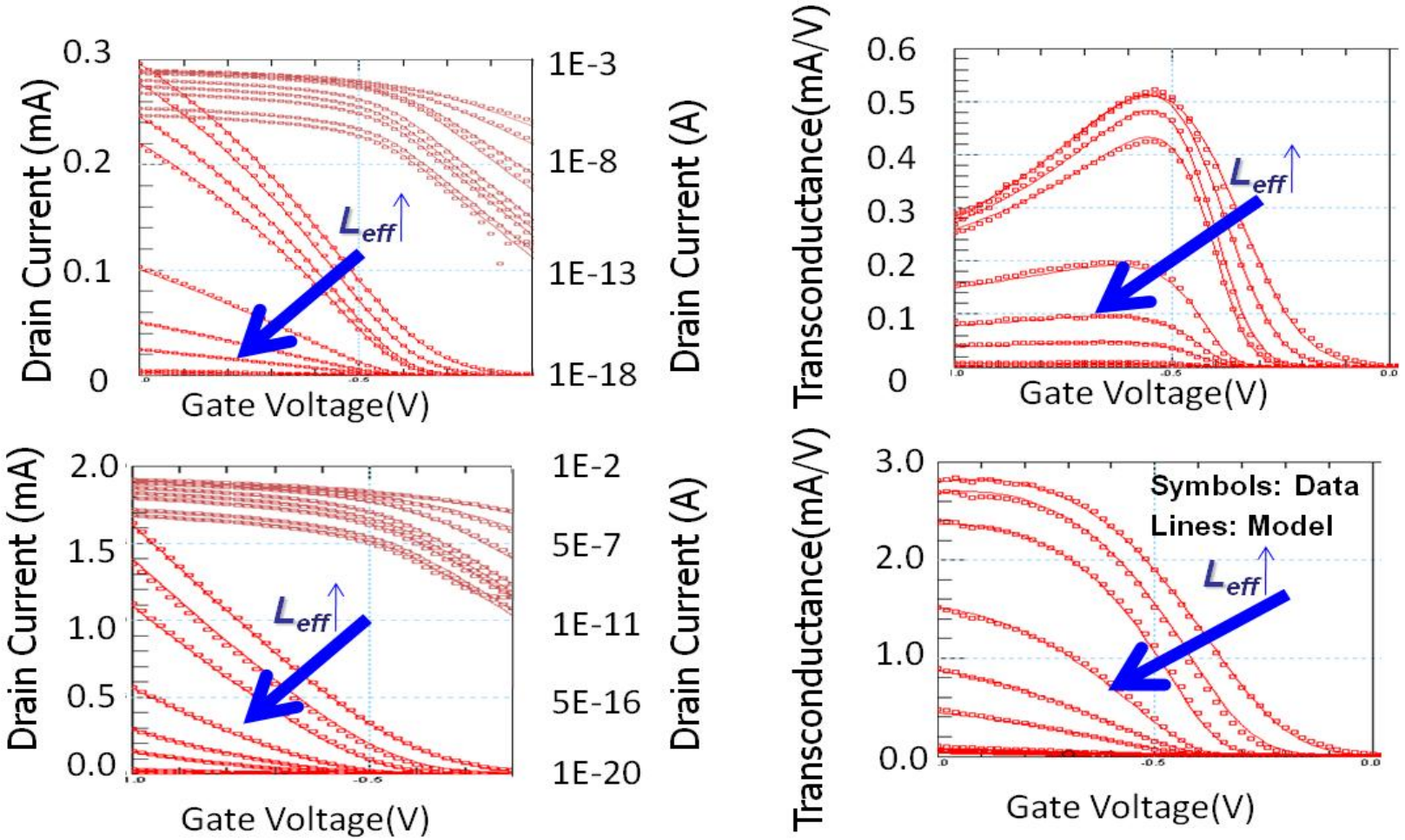
Slide is provided by UCB Prof. C. Hu





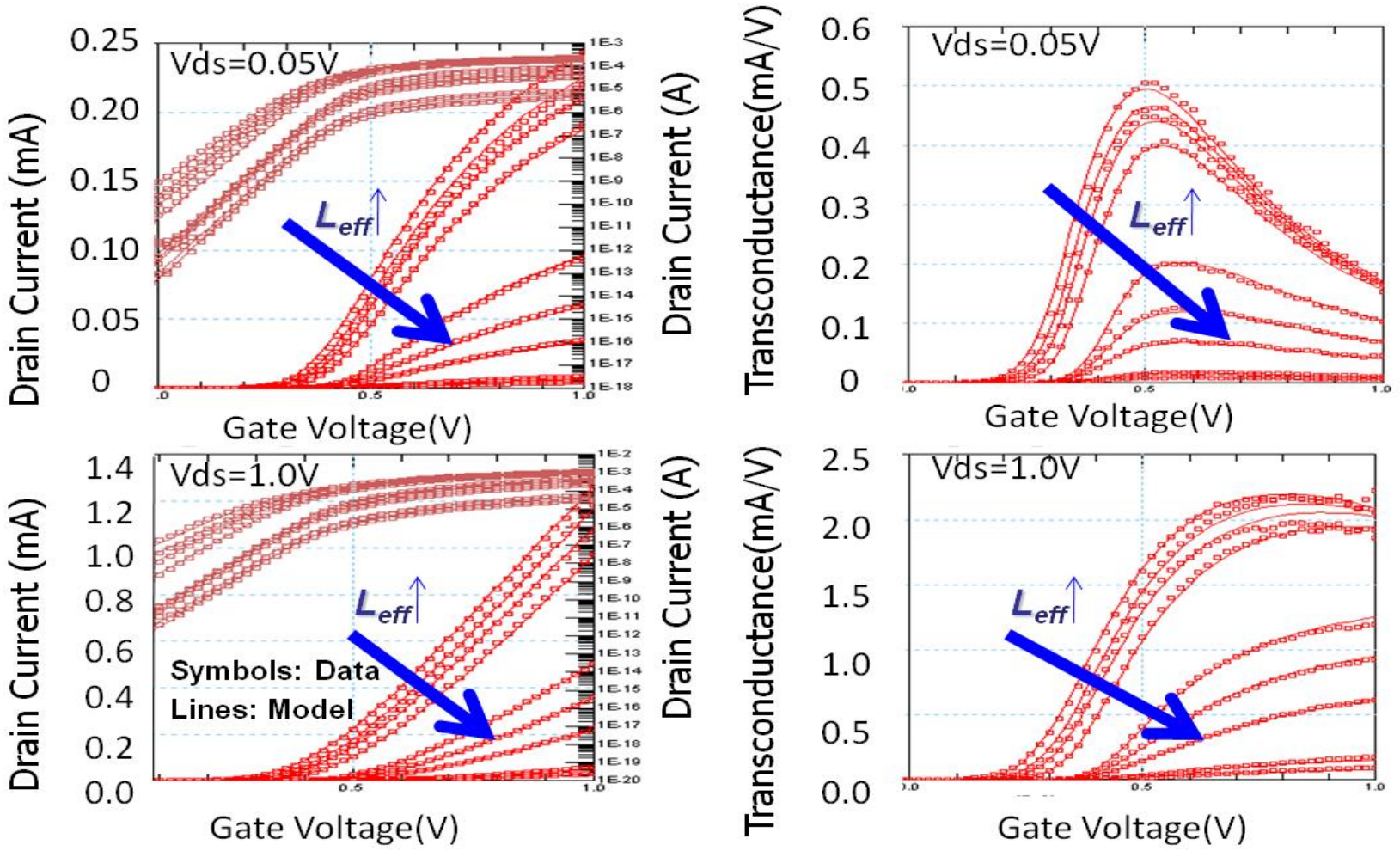
Capacitances (C_{gg} and C_{sd})

PMOS FinFET 35nm to 10um



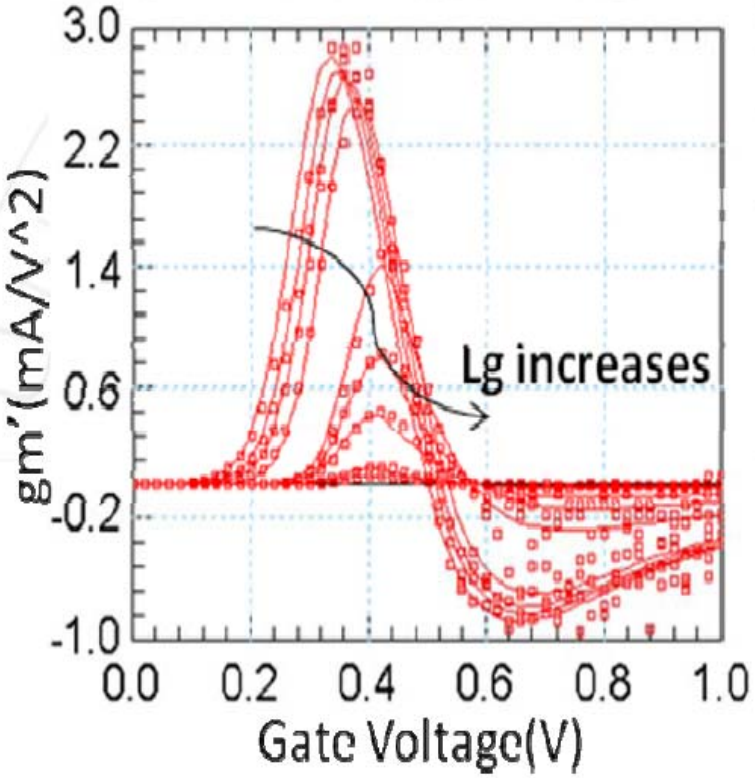
This slide is provided by UC Berkeley Prof. Chenming Hu

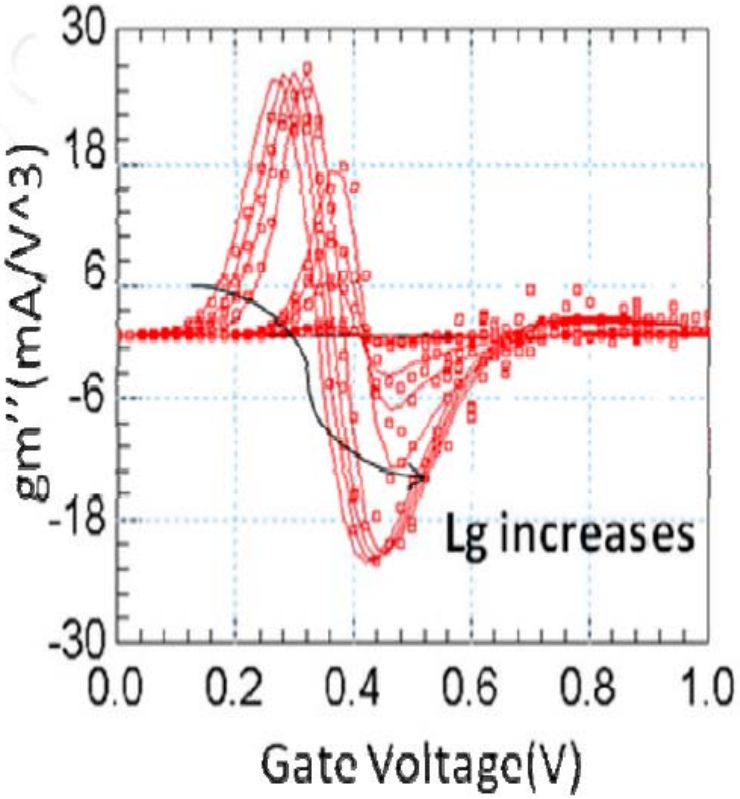
NMOS FinFET 30nm to 10um



This slide is provided by UC Berkeley Prof. Chenming Hu

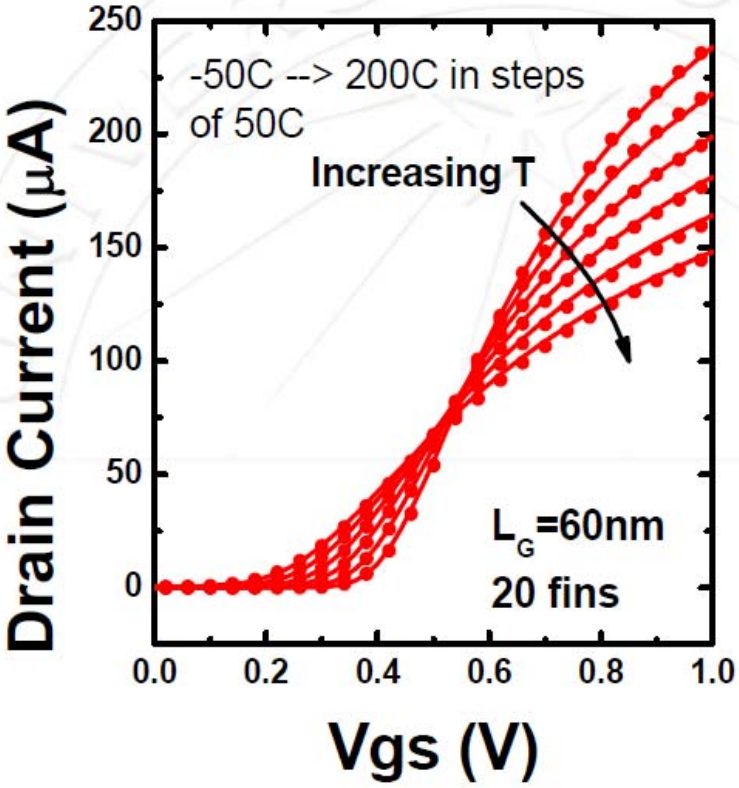
Global fitting with 30nm-10um FinFETs

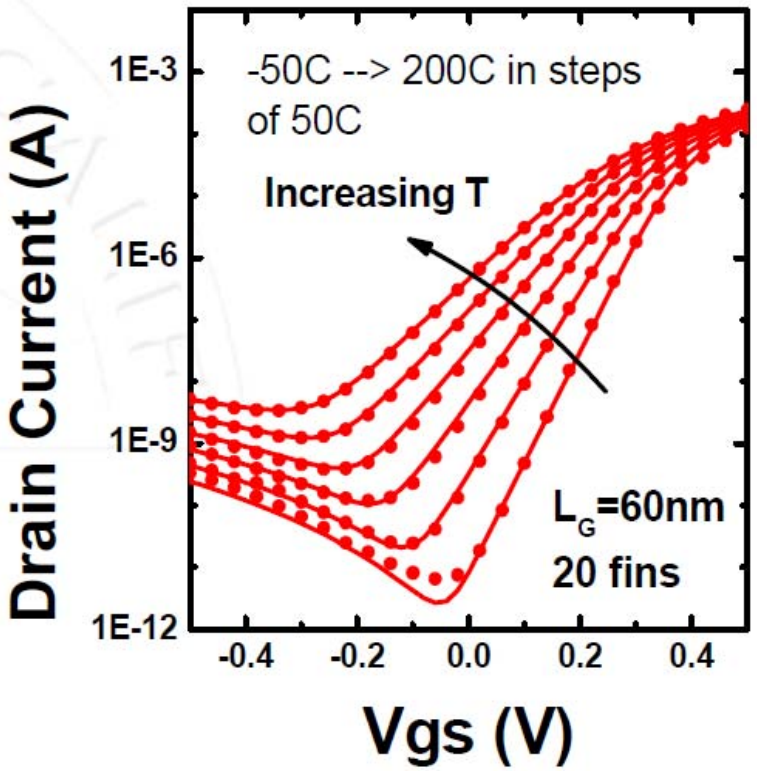




This slide is provided by UC Berkeley Prof. Chenming Hu

Temperature Model Verified for FinFET





This slide is provided by UC Berkeley Prof. Chenming Hu

Outline

- 1. Technology Considerations
- 2. Spice Modeling
- **3. Design Methodology and CAD Tools**
- 4. Digital Design
  - Standard Cells, Layout
  - IO and ESD
- 5. SRAM
- 6. Analog & Mixed-Signal, RF
- 7. Conclusion
- References

© 2013 IEEE

FinFET Design Issues

- Width Quantization
  - Significantly better layout density for high fin height process [1]
  - High driving strength cell has larger area reduction [1]
  - Four QOR indexes to evaluate quantization [2]
- L_g and V_{th} biasing replacement
  - Adjust V_{th} through Gate work function engineering [3]
  - Adjust L_{eff} through gate-drain/source overlap engineering [4]
- Implementing weak feedback devices in latches and keepers
  - Need to use S/D underlap to weaken feedback devices [4]
- Quantization effect on Leak estimation
  - Worse leaking fin dominant leakage distribution [5]
- Reduced variation by larger W_{eff} in the same footprint [6]

FinFET Parasitic Modeling

- Parasitic Capacitance
  - Raised S/D reduce Rpara but increase Cpara [7]
  - Outer fringe cap in FinFET is larger compared to planar counterparts [7]
  - Parasitic capacitance modeling [8]
- Parasitic Resistance
  - Larger gate resistance [9]
  - S/D parasitic resistance modeling [10]
  - Rpara reduces Ion by ~5% [11]

Challenges in Parasitic Extraction

- Complex 3D transistor structure
- More R and C components

- 3D RC extraction for critical circuits but needs run-time improvement
- 2.5D RC extraction enhancement for accuracy is required

Source of Variations in FinFETs

- Variation in threshold voltage
  - Fin Thickness and Fin Height [12, 16]
  - LER and WER [12–14]
  - LER is major variation source in lightly doped channel [13,14]
  - Higher trap density for HKMG (10^{19}/eVcm^3 for HfO_2) [15]
- Variation in mobility & Work function variation (WFV)
  - Surface roughness scattering [16]
  - Found WFV of 16meV in FinFET with Lg = 23nm [17]
  - WFV dominant TiN metal gate FinFET V_{th} variation [18–20]
  - WFV due to Grain-Orientation-induced Quantum Confinement [21]
- Variation on I_D
  - Rpara variation correlates closely with Tfin variation [22]

© 2013 IEEE

EDA Ecosystem Assessment -1

Note: Content To be filled by Attendees.

		EDA Tool	Tech File/model/PDK	Comment
Spice Simulation		☆☆☆☆☆	☆☆☆☆☆	* Need accurate BSIM-CMG model * To drive SPICE simulators to support the model in Q2
MEOL Model + RC Extraction	2.5D	☆☆☆☆☆	☆☆☆☆☆	* To define MEOL targets and corners * Need accurate FinFET MEOL handing
	3D	☆☆☆☆☆	☆☆☆☆☆	* Need to clarify device cap partition * Tools need to handle R in addition to C
DRC		☆☆☆☆☆	☆☆☆☆☆	* DRC commands to handle fin quantization and FinFET related rules
LVS/LPE		☆☆☆☆☆	☆☆☆☆☆	* Need to consider FinFET specific parameters and LDE spec

★★★ means quite good.

© 2013 IEEE

EDA Ecosystem Assessment -2

Note: Content To be filled by Attendees

	EDA Tool	Tech File/model/PDK	Comment
RTL Synthesis	☆☆☆☆☆	--	* No change perceived
Floorplan/Placement	☆☆☆☆☆	--	* Need to drive CAD tool to honor FinFET region or FinFET pitch rule
Routing	☆☆☆☆☆	☆☆☆☆☆	* FinFET std cell pin access *16 /14 nm DPT rules
Static Timing Analysis	☆☆☆☆☆	--	* Need to validate CAD tool accuracy of timing model and pin cap model
Custom Design Tool/PDK	☆☆☆☆☆	☆☆☆☆☆	* Custom tools need to consider FinFET quantized rule and connectivity * PDK needs correct-by-construction Pcells and FinFET specific MOS analyzer and LDE utility

★★★ means quite good.

Design Methodology Assessment

Note: Content To be filled by Attendees.

	Readiness	Challenges
General	☆☆☆☆☆	* Quantization optimization for PPA (IP sizing, clock tree balancing, etc)
DFM	☆☆☆☆☆	* Modeling for random yield(CAA in 3D structure), dummies, LPC (fin width/space, OD/PO rounding, etc), CMP (3D structure)
Low Power	☆☆☆☆☆	Effective low-power design approaches: * Optimal operating voltages for best power/area * Power gating by header/footer design * Multi-Vt and gate bias approach (?)
Reliability	☆☆☆☆☆	* Electro-migration (EM), self heating
Variation	☆☆☆☆☆	* Geometry variation vs random doping

★★★ means quite good.

© 2013 IEEE

FinFET vs. Planar: Pros & Cons -1

	Pros	Cons	Potential Solutions
Std. Cells	a. High drive current b. Low subthreshold leakage current c. Better performance on low-V operation	1. Quantized OD has less flexibility on rise/fall balance and sizing optimization 2. On grid fin constraints layout routing capability 3. Fin structure causes worse heat dispatch	1. Enlarge cell size to improve cell balance
I/O & ESD	a. High drive current per footprint, enhancing I/O area density	1. Uni-gate direction causes 2-set IO (V & H) effort 2. Difficult for ≧2.5V IO 3. Degraded diode ESD 4. Low ESD self-protection	2. Cascade P/NFET or use VMOS 3. Large size or novel circuit

FinFET vs. Planar: Pros & Cons -2

	Pros	Cons	Potential Solutions
SRAM	a. Higher effective cell current for speed b. Less Vt mismatch c. Better Ion/Ioff ratio for longer BL length	1. Quantized device width limits the Vccmin optimization window	1. Enlarge bit cell, or use design assist
Analog	a. Better gain and matching b. Better headroom	1. Metal/Via EM-tolerance degradation 2. More sensitive to density control	1. With constrained layout style, or time interleaving design to reduce Metal conductance 2. Density control

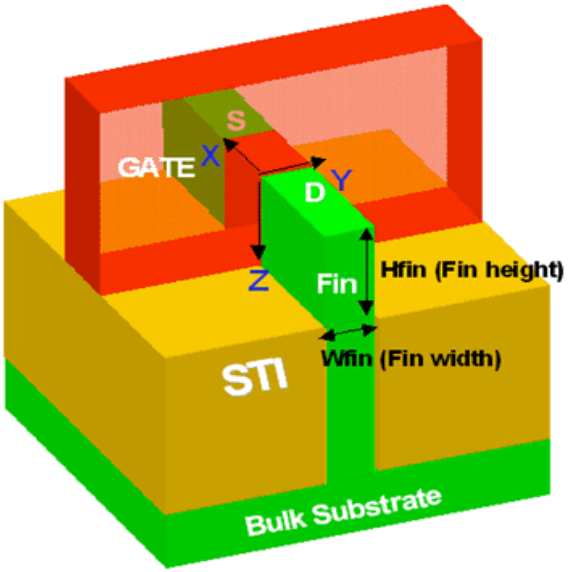
© 2013 IEEE

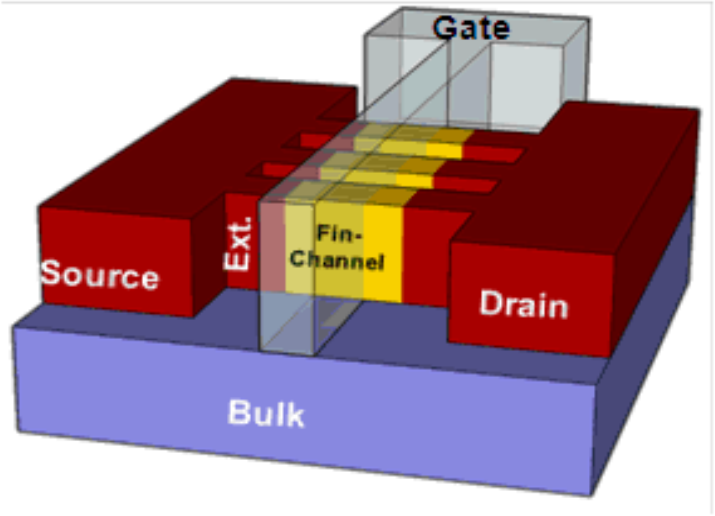
Outline

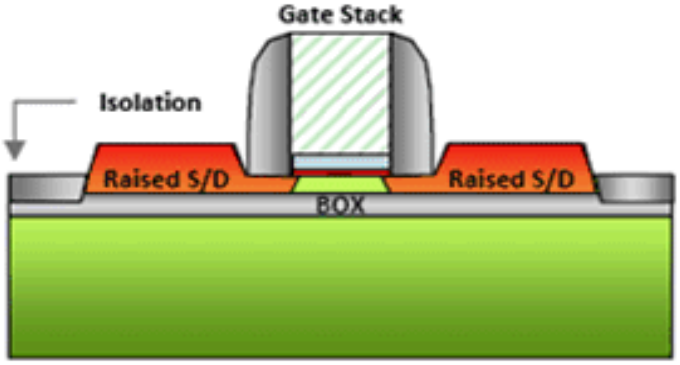
- 1. Technology Considerations
- 2. Spice Modeling
- 3. Design Methodology and CAD Tools
- **4. Digital Design**
  - Standard Cells, Layout
  - IO and ESD
- 5. SRAM
- 6. Analog & Mixed-Signal, RF
- 7. Conclusion
- References

© 2013 IEEE

FinFET Cross-Section

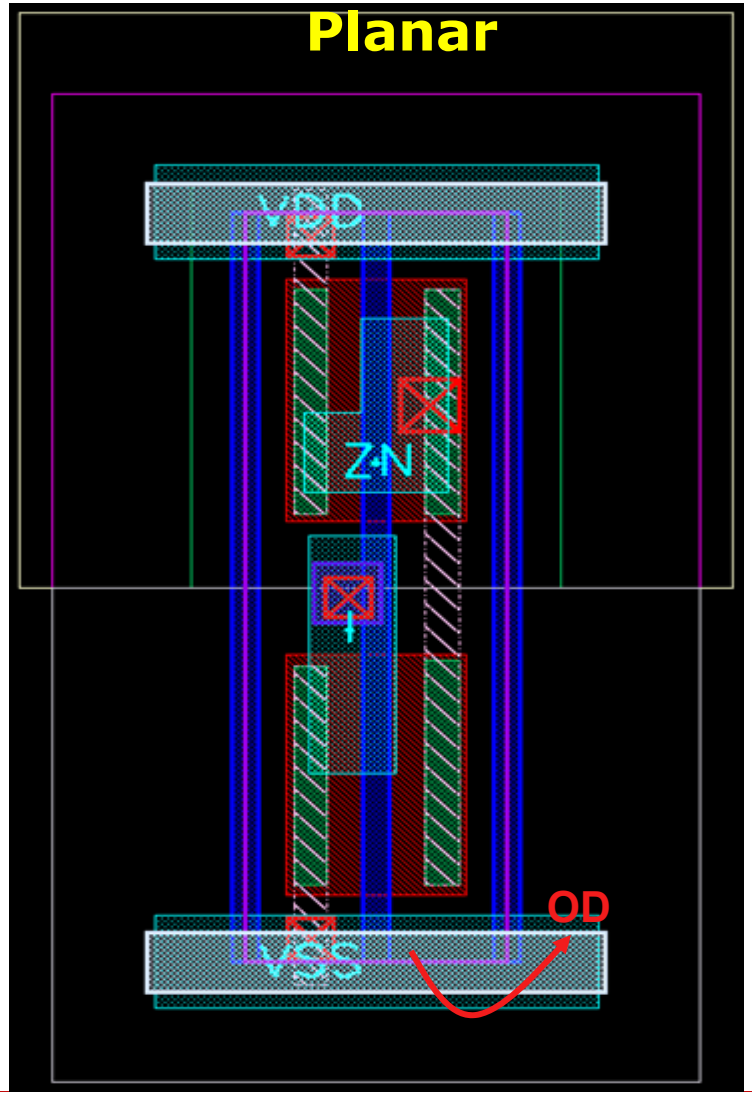


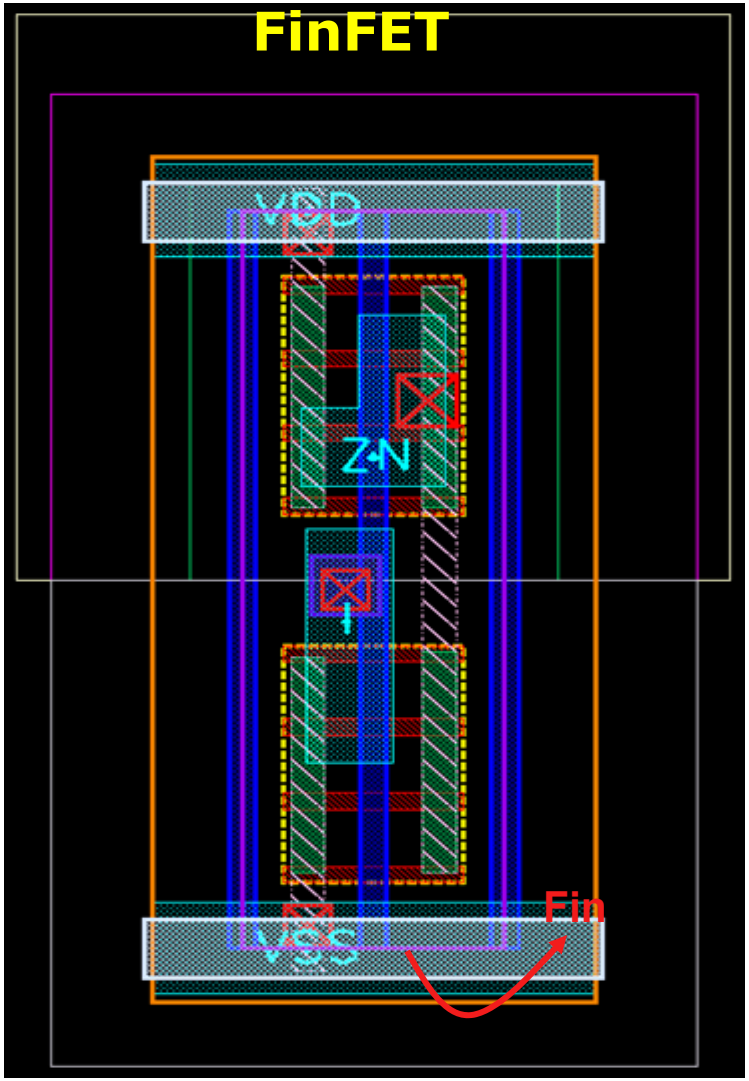




FD-SOI Device

Layout Examples



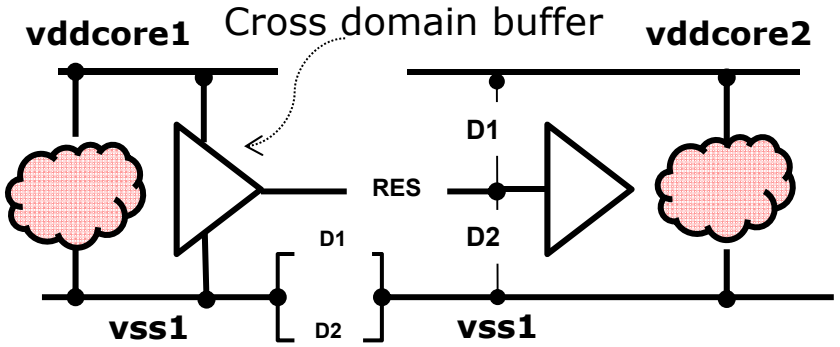


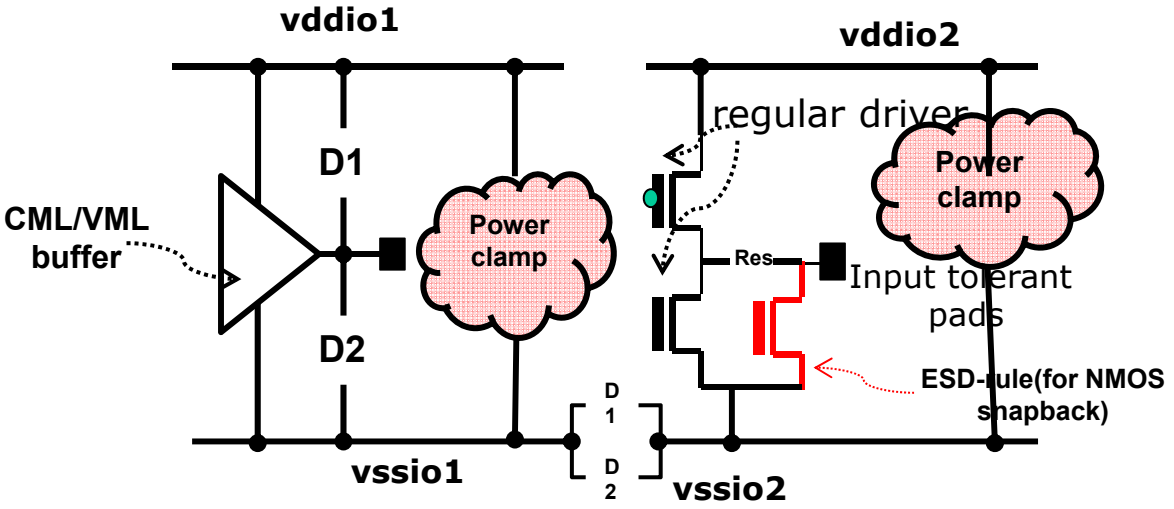
Quantization Impact on Std Cells

- Fin quantization performance impact is 0.7% in average for 200 standard cells
- Worst cell speed degradation is 5.9%, due to lack of single Fin device
- With single Fin, degradation can be reduced to 2.6%

I/O & ESD for Planar CMOS -1

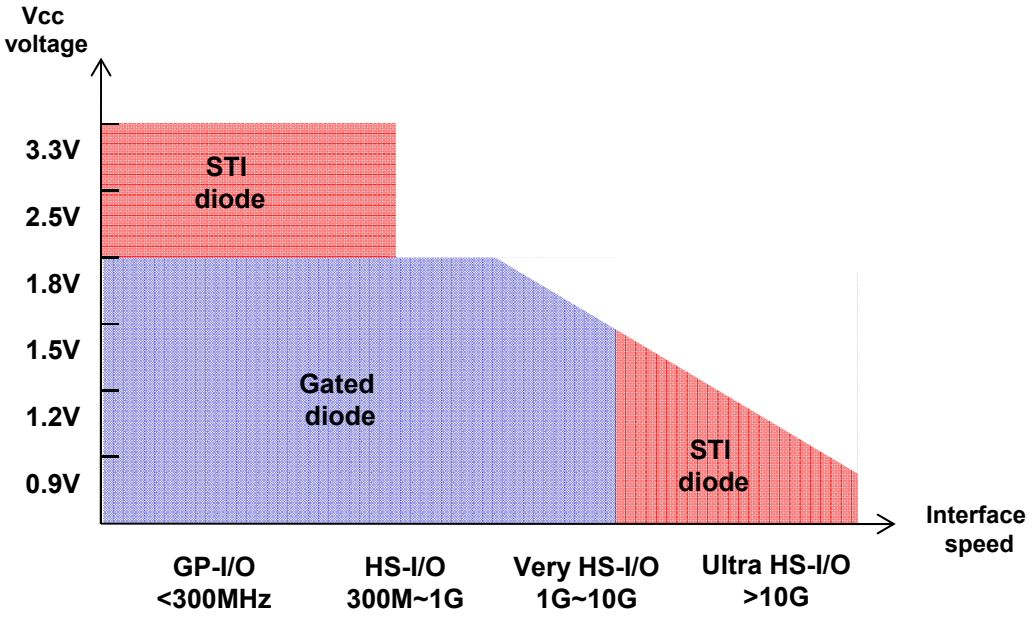
- Diode protect and self-protect ESD network scheme available
- Gated diodes for general purpose ESD protection to achieve
  - High ESD/um^2 & high cross domain CDM level





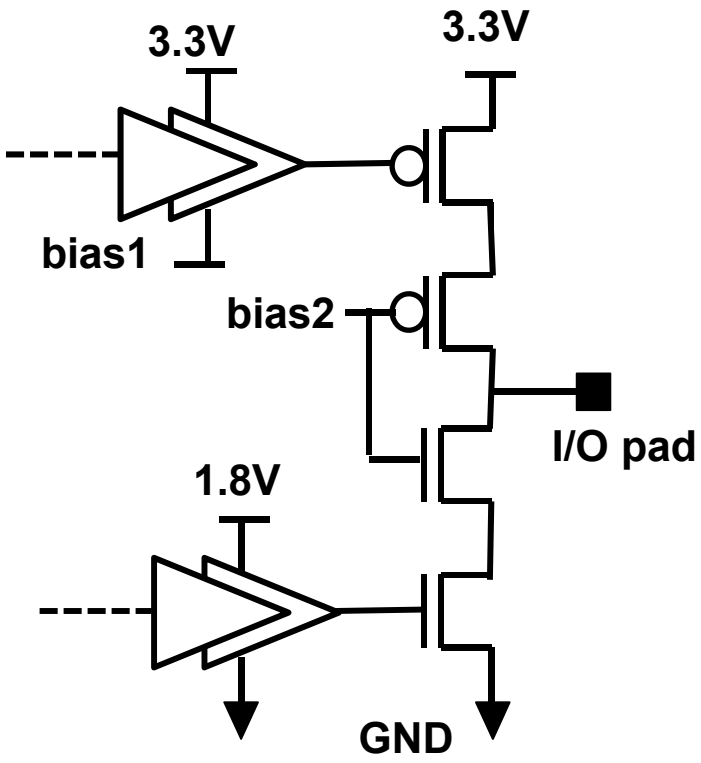
I/O & ESD for Planar CMOS -2

- STI diodes for specific ESD protection including
  - High ESD/fF (for low-cap/ ultra high speed) & high Vbd (for >1.8V interface protection)
- Power clamps (RC-trigger ESD to cover 0.85/1.8/2.5/3.3)
- Snapback NMOS available for input tolerant ESD protection



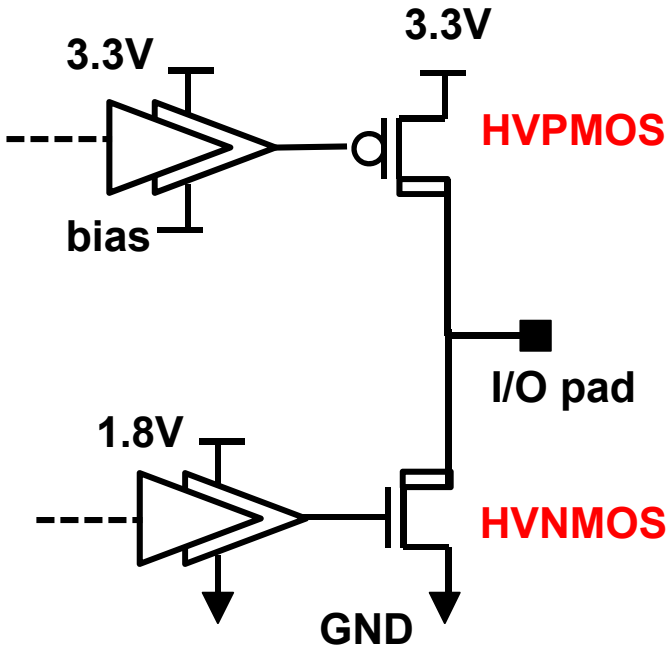
High Voltage I/O in Planar CMOS -1

- Thick oxide devices optimized for low voltage interface circuit (1.8V and below)
- For >2.5V I/O, design with 1.8V transistor cascode approach or HVMOS approach



3.3V interface circuit using 1.8V transistor cascode approach

High Voltage I/O in Planar CMOS -2



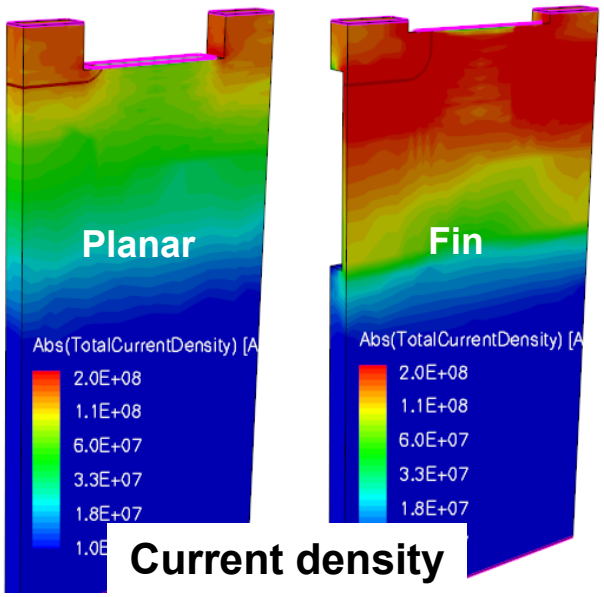
3.3V interface circuit using drain-extend HVMOS approach

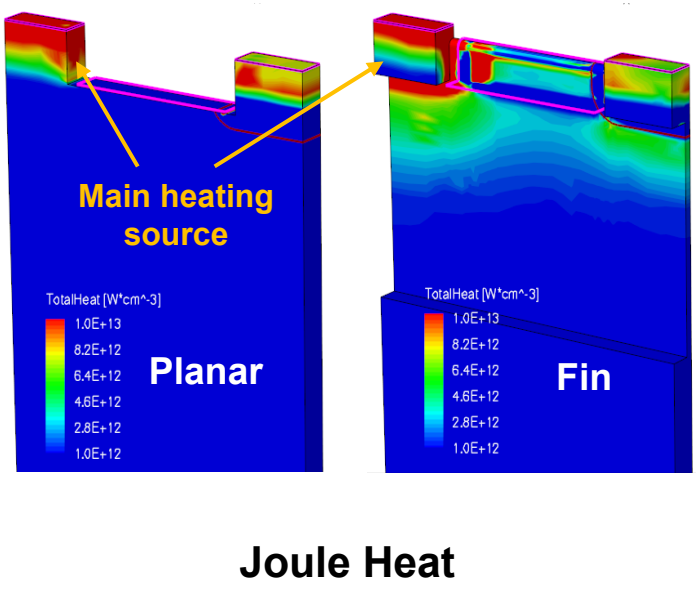
FinFET I/O & ESD Design Challenge

- I/O design and implementation
  - Cascode approach only for high voltage I/O design, no drain extend HVMOS available in FinFET
  - No native/low-Vt IO device for low-Vccmin I/O level shifter and low Vt-drop pass gate for input high voltage tolerant circuit
  - For uni-IO gate direction required for FinFET process, will need 2 sets of I/O for ring type placement
- ESD protection
  - Snapback-type ESD protection not available
  - Diode efficiency degradation due to high ESD current density

Gated Diode TCAD ESD Simulation

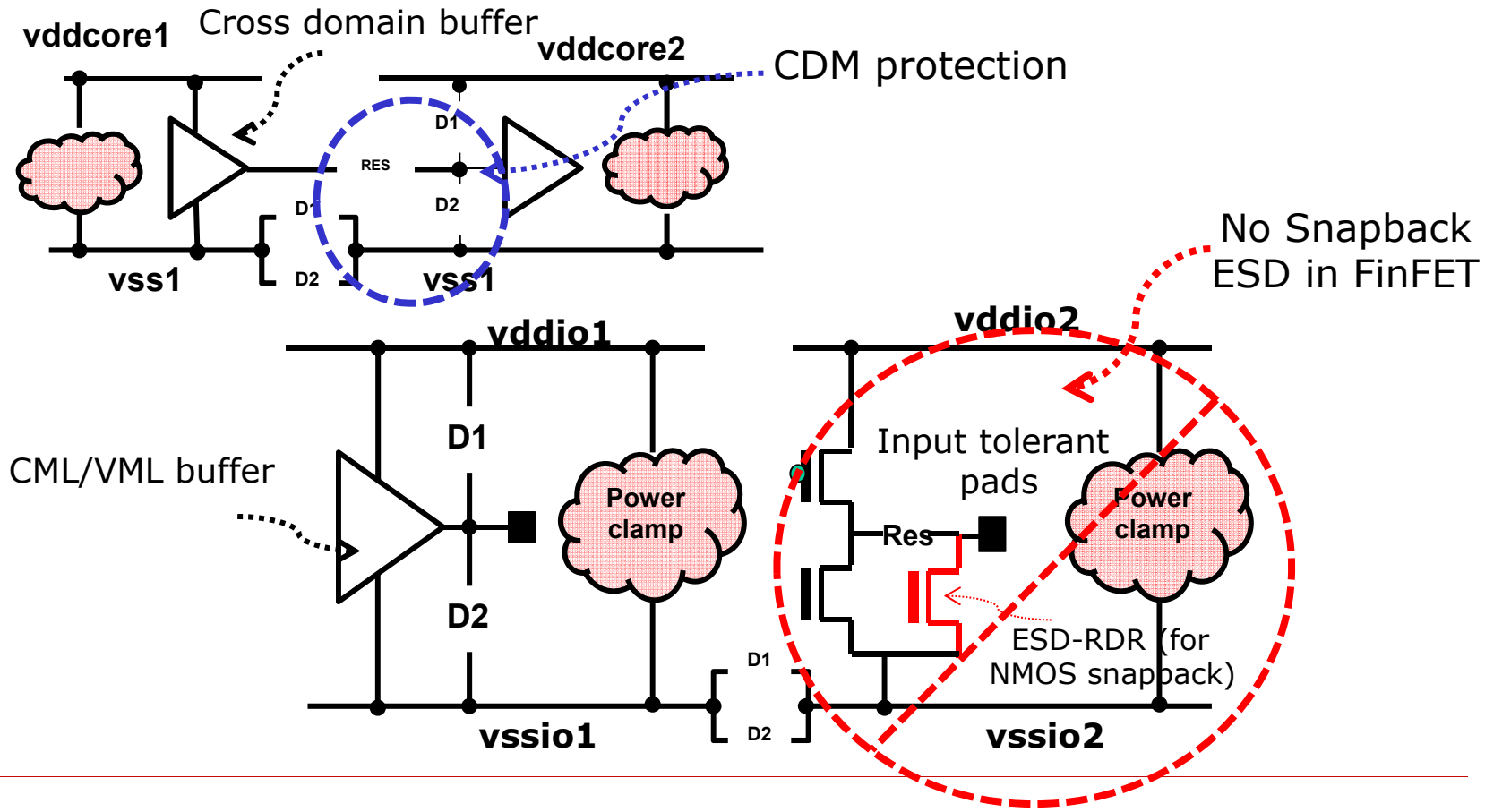
- Expect ESD level for FinFET to degrade by 20~40% due to increased current density & joule heating
- Need to implement ESD devices with bigger size to meet ESD spec.





ESD Network for FinFET I/O

- All FinFET devices protect by diodes and active clamp
- No snapback ESD in FinFET I/O



FinFET ESD Devices

Clamp type	Potential FinFET solution	Applications
Diode	Gated diode	CMOS push-pull GPIO Core/IO CML diver Cross domain CDM
	STI diode	Low-C for Gbps serdes/RF High voltage (>2.5V)
none-snapback MOS-driver	Resistor protected P/NMOS	GPIO CML driver
Power clamp (core voltage)	RC trigger with Fin-core large transistor	General purpose core voltage clamp
Power clamp (IO voltage)	RC trigger with Fin-IO large transistor	General purpose IO voltage clamp
Power clamp (High voltage, >2.5V)	RC trigger with Fin-cascode large transistor	High voltage interface PMU

Outline

- 1. Technology Considerations
- 2. Spice Modeling
- 3. Design Methodology and CAD Tools
- 4. Digital Design
  - Standard Cells, Layout
  - IO and ESD
- **5. SRAM**
- 6. Analog & Mixed-Signal, RF
- 7. Conclusion
- References

Challenges in Scaling CMOS SRAM

- The most challenge is SCE (Short Channel Effect) control
  - Requires heavy channel doping (>10^{18} cm^{-3}) and heavy super-halo implants to control surface leakage
  - Side effects of the heavy doping
    - Carrier mobility is severely degraded due to impurities scattering
    - High transverse electric field in the device "ON" state
    - The increased depletion charge density results in a larger depletion capacitance hence a larger sub-threshold slope.
    - Off-state leakage current increase due to band-to-band tunneling between the body and drain.
- Vt variation caused by Random Dopant Fluctuation (RDF) is another concern for planar CMOS

© 2013 IEEE

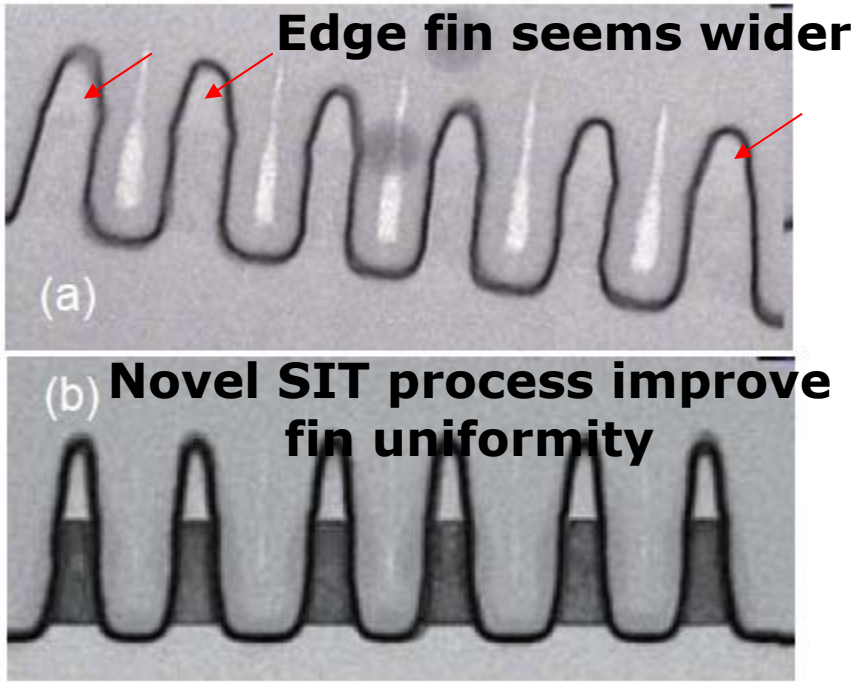
FinFET Benefits for SRAM Design

- SCE can be effectively suppressed by using thin-body transistor structure like FinFET: less gate length variability
- The Lg can scale down to 10nm region without using heavy channel/body doping
- Lightly-doped channel gives rise to
  - Lower transverse electrical field in the "ON" state
  - Reduced impurity scattering
  - Higher carrier mobility (2X higher)
  - Reduced depletion charge & capacitance lead to a steep sub-threshold slope
  - Both depletion and junction capacitances are effectively eliminated, which reduce the BL capacitive load.
  - Reduce random dopant fluctuation effects
- Strain benefit will be greater (Ref: ITRS, 2007)

Variation point of View on SRAM

- Less RDF (Random Dopant Fluctuation)
- More Sensitive to geometry variation
  - Fin height, width, edge roughness
  - PO patterning variation since topology is rough
  - Implies more RDR rules for CD control

Fin Edge Effect on Variation -1



Fin width =10nm
Fin pitch = 40nm
Fin height = 30nm

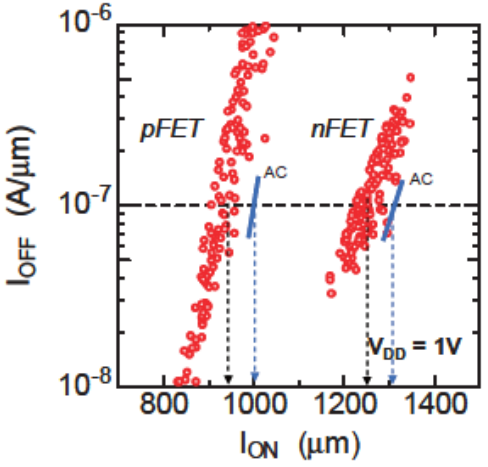
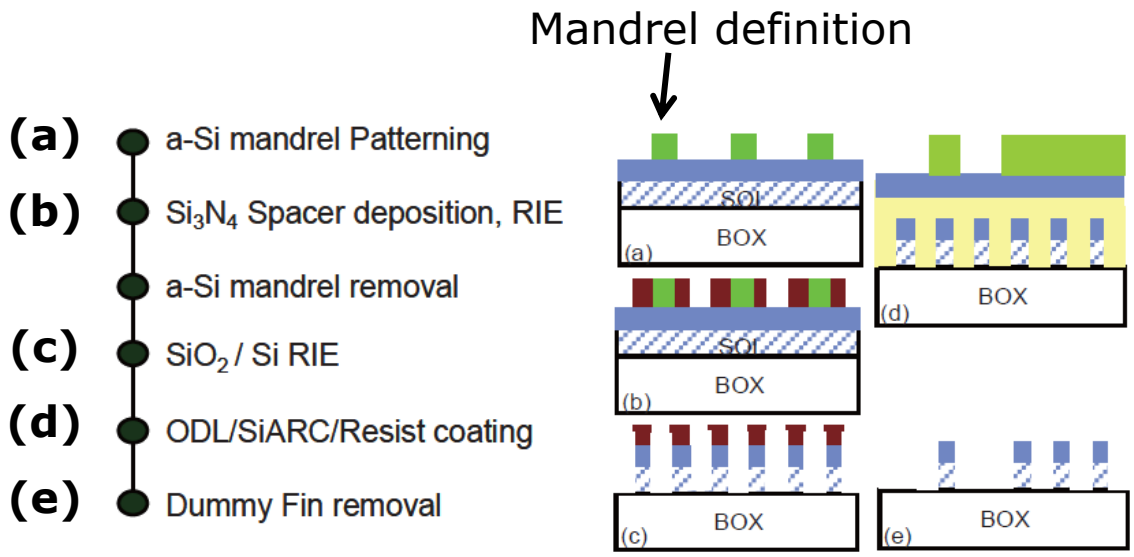


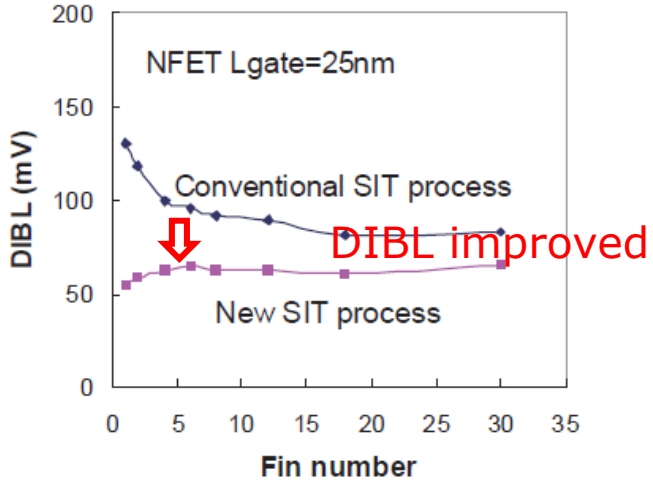
Fig. 12 Ion-Ioff of NFET/PFET at Vdd = 1 V. NFET Ion = 1300 uA/um and PFET Ion = 1000 uA/um at Ioff = 100 nA/um with self-heating correction.

Ref: T. Yamashita, et. al , (IBM) "Sub-25nm FinFET with Advanced Fin Formation and Short Channel Effect Engineering", VLSI Symp., 2011

© 2013 IEEE

Fin Edge Effect on Variation -2

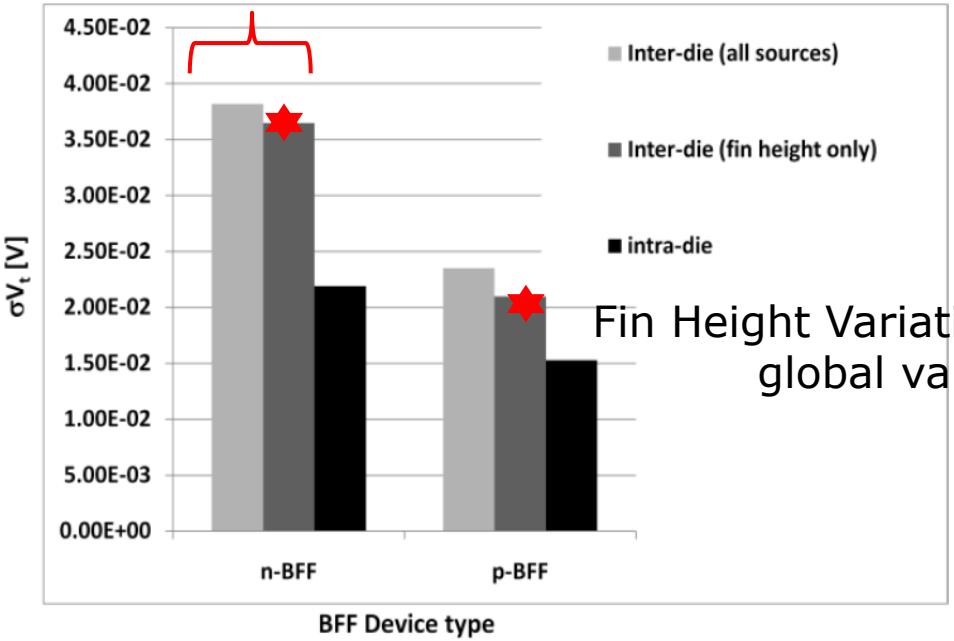




Fin Height Variation -1

- Global variation > local variation for FinFET (Seems good news for SRAM designer)
- Fin Height Variation (FHV) contribute a major portion of global variation

global variation > local variation



Fin Height Variation dominates global variation

Fin Height Variation -2

BFF: Bulk FinFET **SOIFF: SOI FinFET**

σ (ΔVt)	BFF [mV]		SOI [mV]		DIFF [mV]	
	N-fet	P-fet	N-fet	P-fet	N-fet	P-fet
Intra-die (local)	21.9	15.3	10.6	10.8	Not Appl.	Not Appl.
Inter-die (non-l.)	38.2	23.5	11.3	11.0	36.5	21.0

Inter-die: common part to all devices (other sources)

$(38.2^2 - 11.3^2)^{1/2} = 36.5$

Inter-die: specific to doping variations (Fin Height)

$\sigma^2 (\Delta Vt_{diff}) = \sigma^2 (\Delta Vt_{BFF}) - \sigma^2 (\Delta Vt_{SOI})$

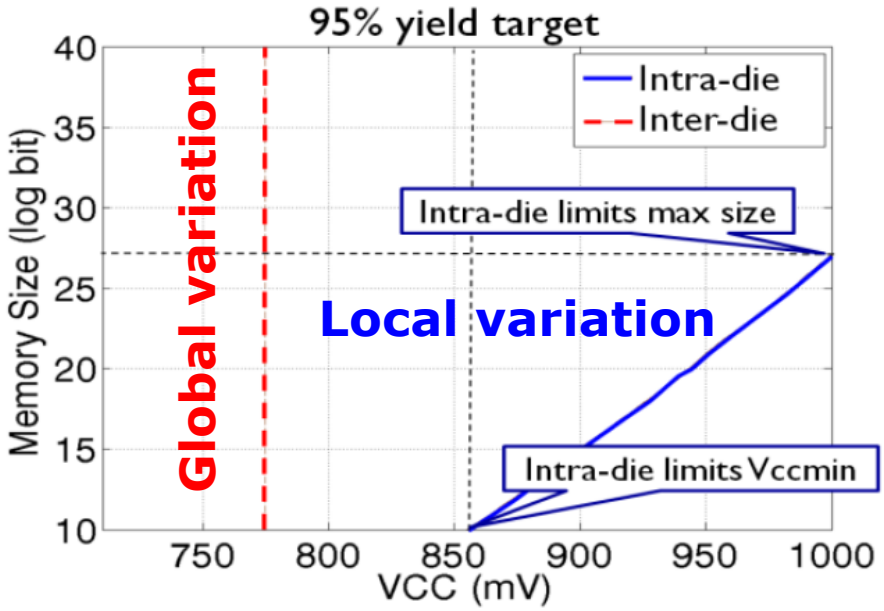
Assumptions:

- SOI: height variations do not affect Vt (no doping)
- Gaussian approximation
- Independence of random variables

Ref: P. Dobrovollny, et al., "Impact of fin height variations on SRAM yield", IMEC

SNM and WTP(WM) for FHV -1

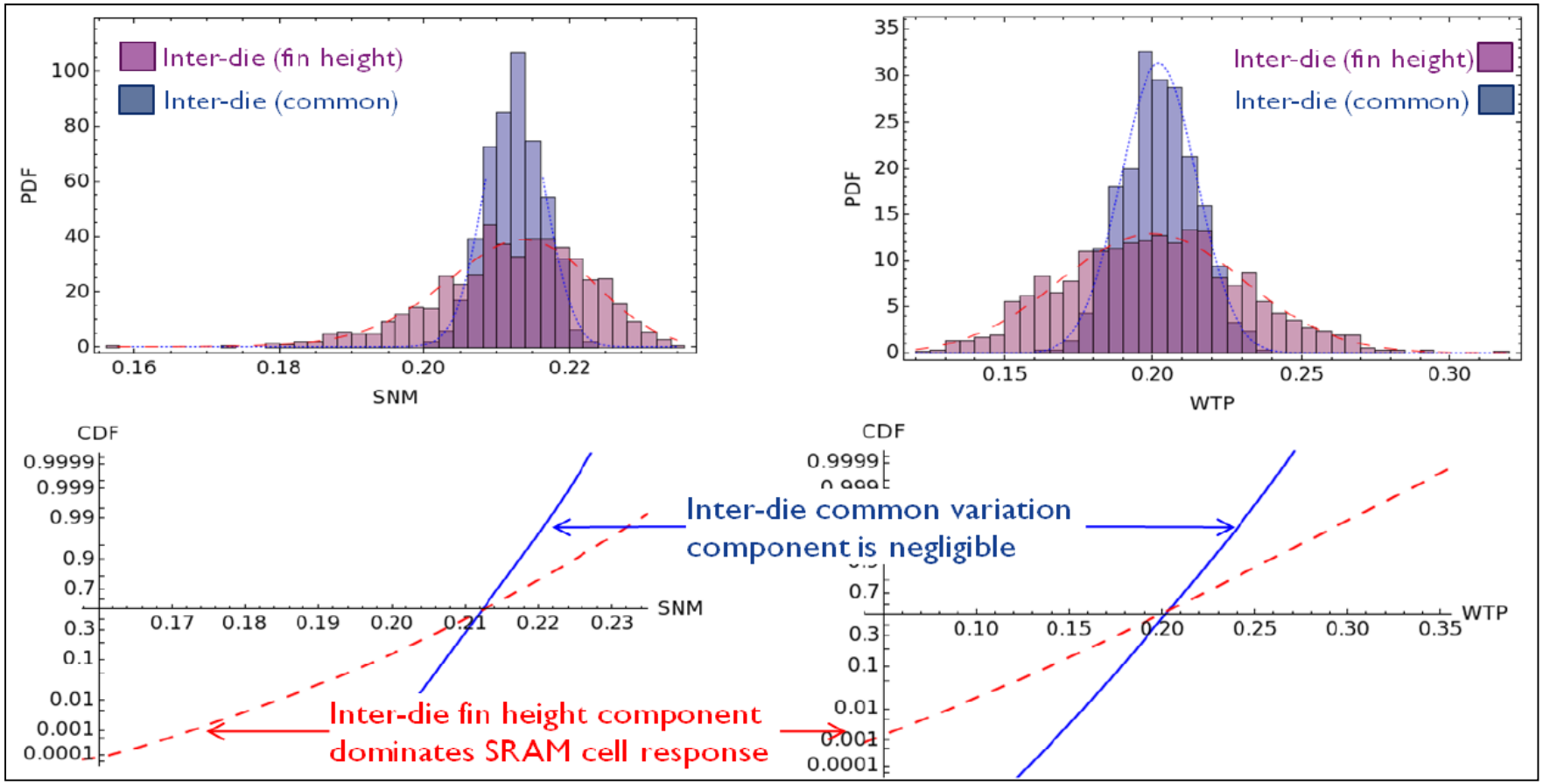
- FHV dominates the overall inter-die (global) variation
- At the product level intra-die (local) variation limits the max. size of SRAM capacity, due to the VCCmin target.



Ref: P. Dobrovollny, et al., "Impact of fin height variations on SRAM yield", IMEC

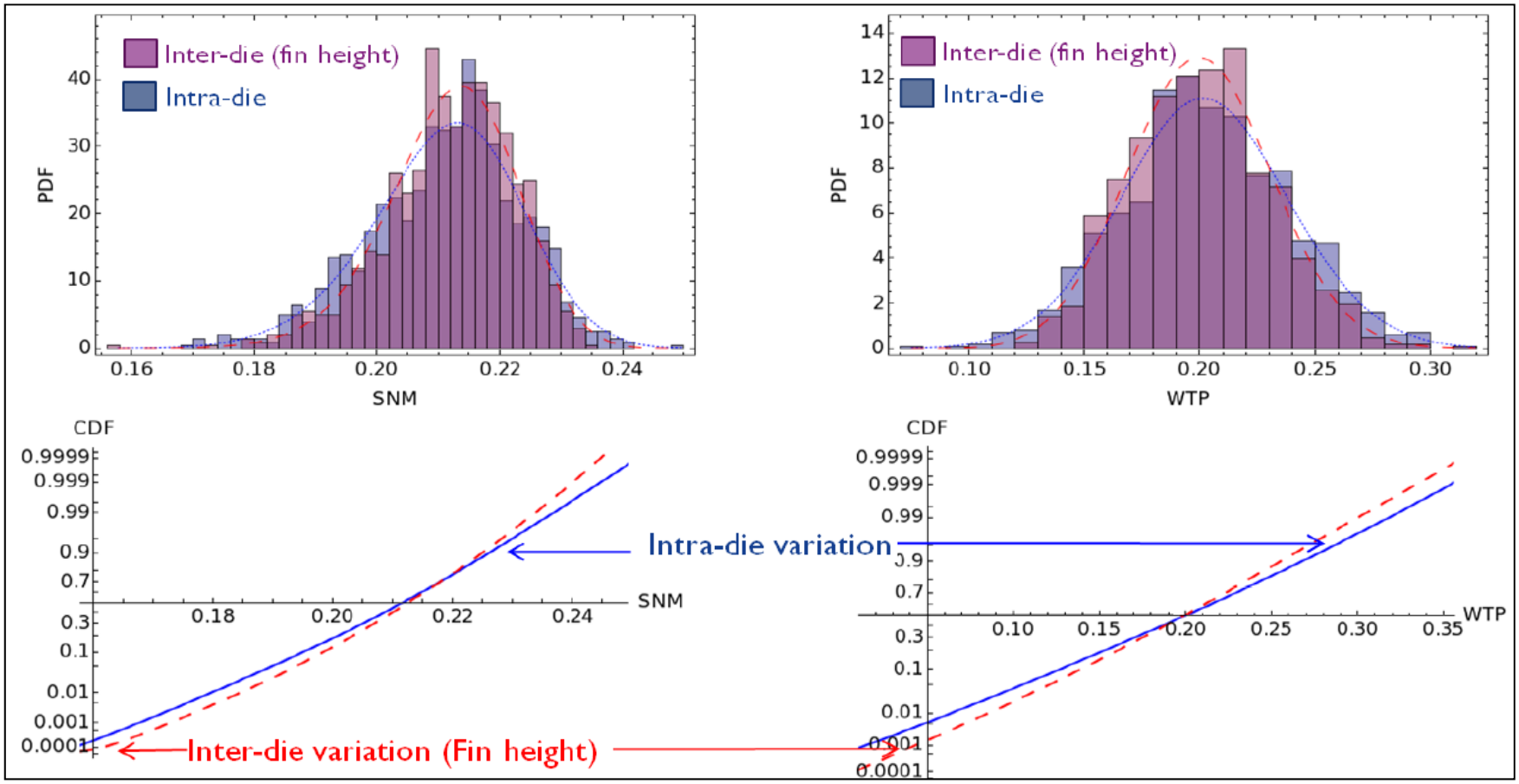
SNM and WTP(WM) for FHV -2

FHV dominates the global variation



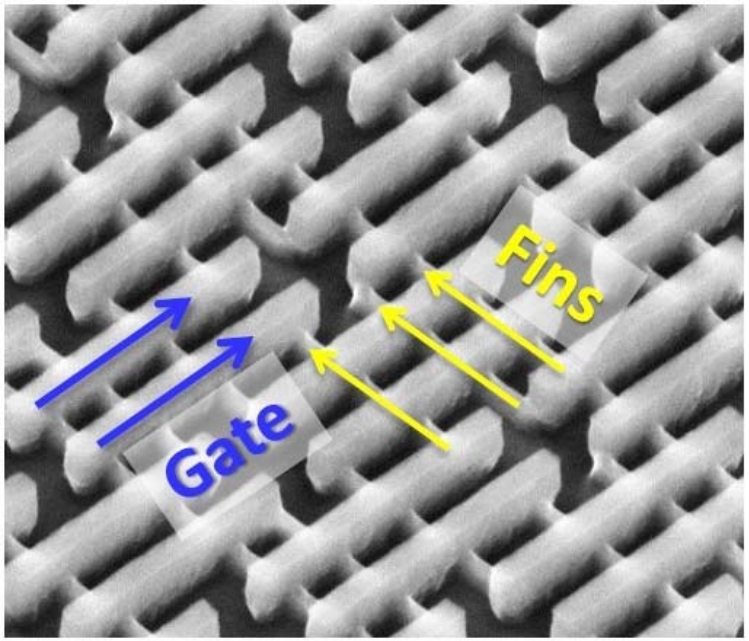
SNM and WTP(WM) for FHV -3

FHV contributes the same weighting as local variation

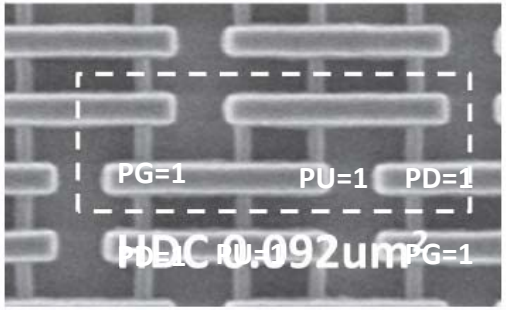


Challenges on SRAM Cell Design

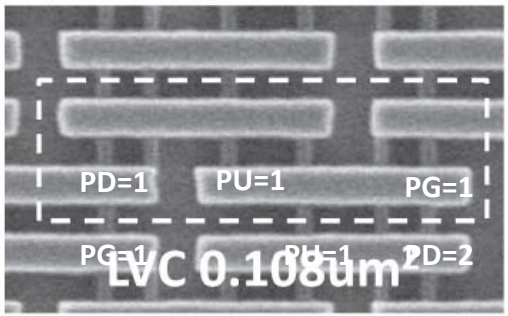
- Quantization fin
- For minimum area: α- and β-ratio = 1, a naturally read-preferred bit cell cause VCCmin issue
- For low VCCmin cell: enlarge β-ratio = 2, cost area penalty



Ref: paper 13.1 (Intel), ISSCC, 2012



High Density (HDC):
0.092 um2
1:1:1 PU:PG:PD

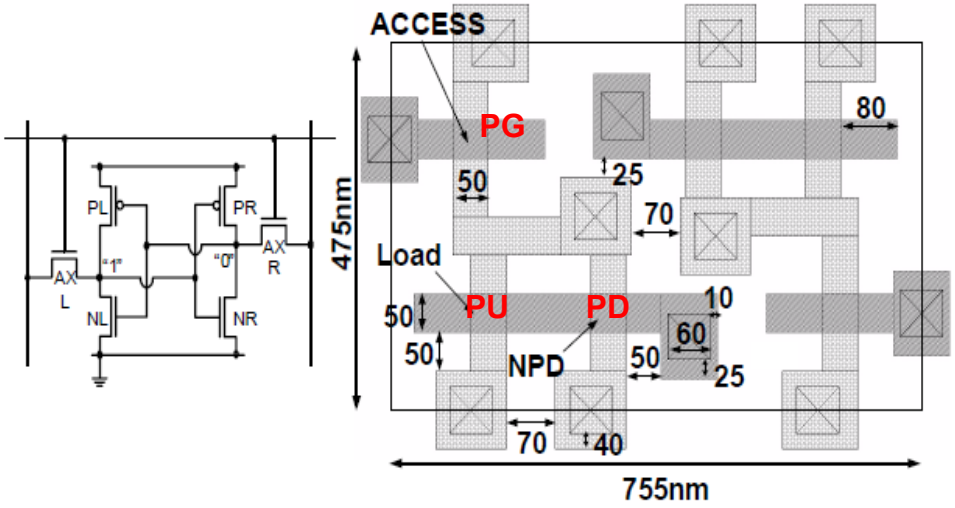


Low Voltage (LVC):
0.108 um2
1:1:2 PU:PG:PD

Surface Orientation for Vccmin -1

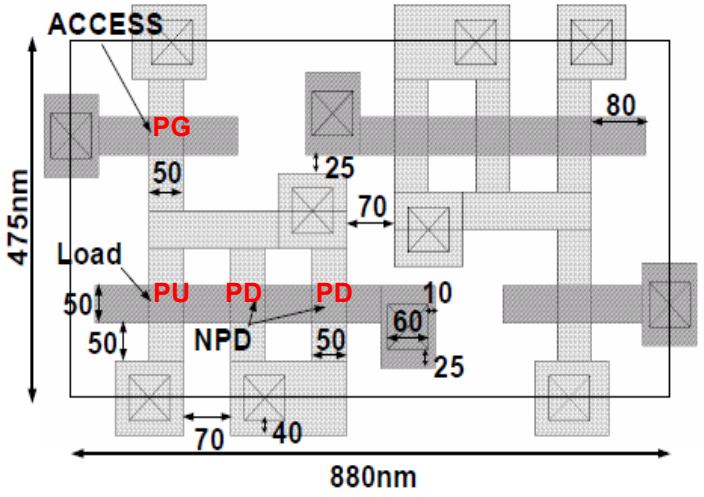
- Electron mobility along (100) plane is higher than along (110)
- PD device rotate to (100) to increase PD strength and also beta ratio
- Side effect is lithography challenge and may result in increased process variation

beta ratio = 1



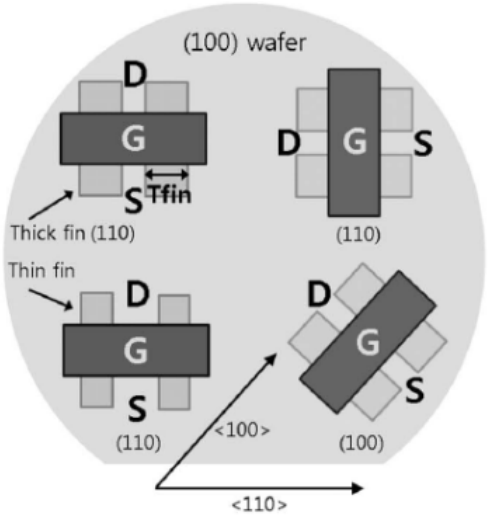
beta ratio = 2

Up sizing PD can greater improve read SNM

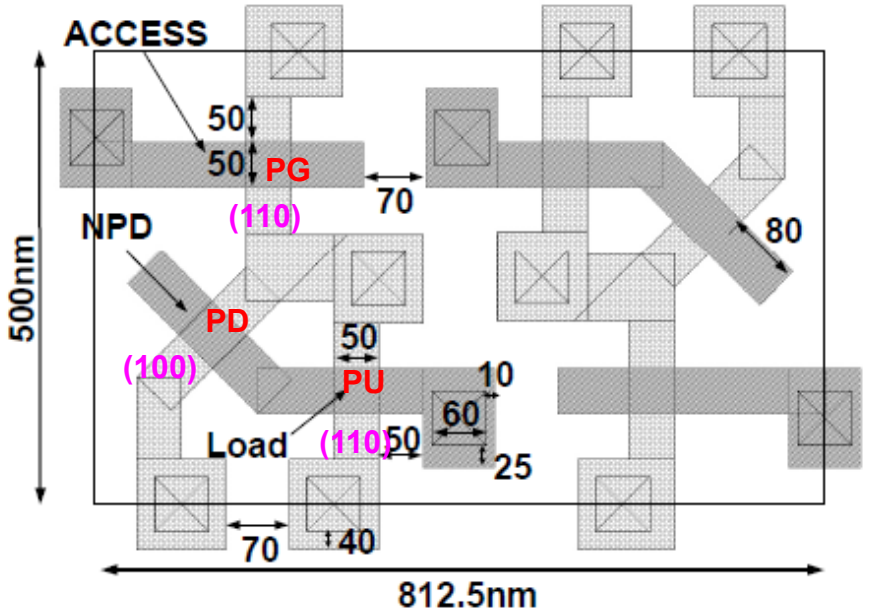


Surface Orientation for Vccmin -2

Wafer orientation



Beta ratio >1
Strength PD > PG

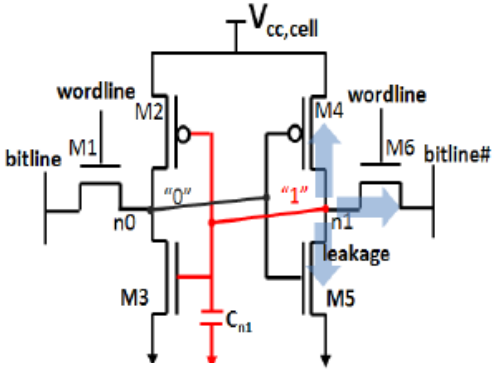


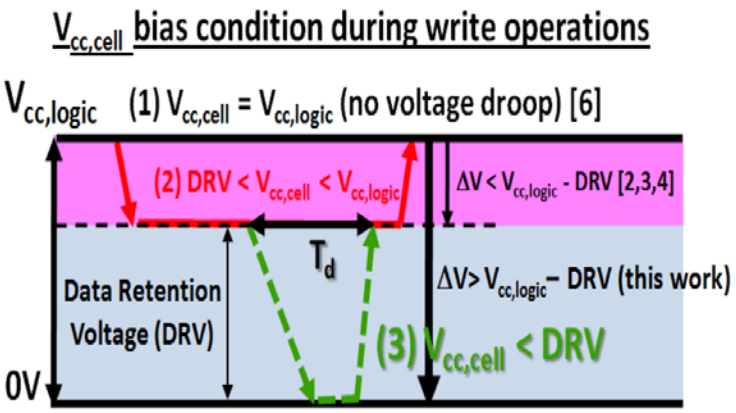
Ref: Zheng Guo, et al., "FinFET-based SRAM design", ISPED, 2005

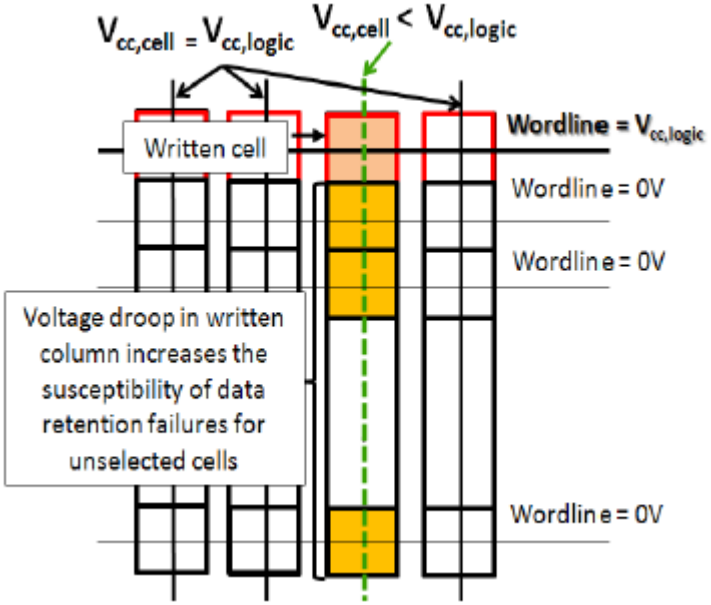
Write-Assist : VDD Collapse

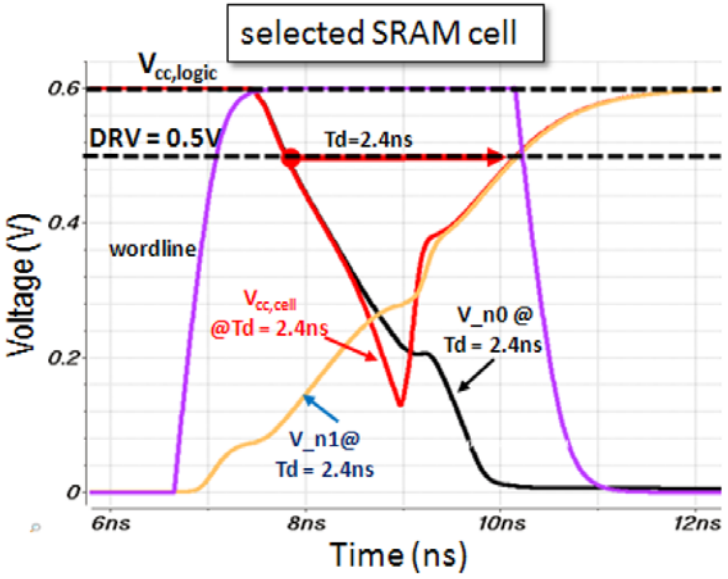
- Column-based Vcc,cell bias technique

Ref: VDD collapse, (Intel) IEDM, 2011



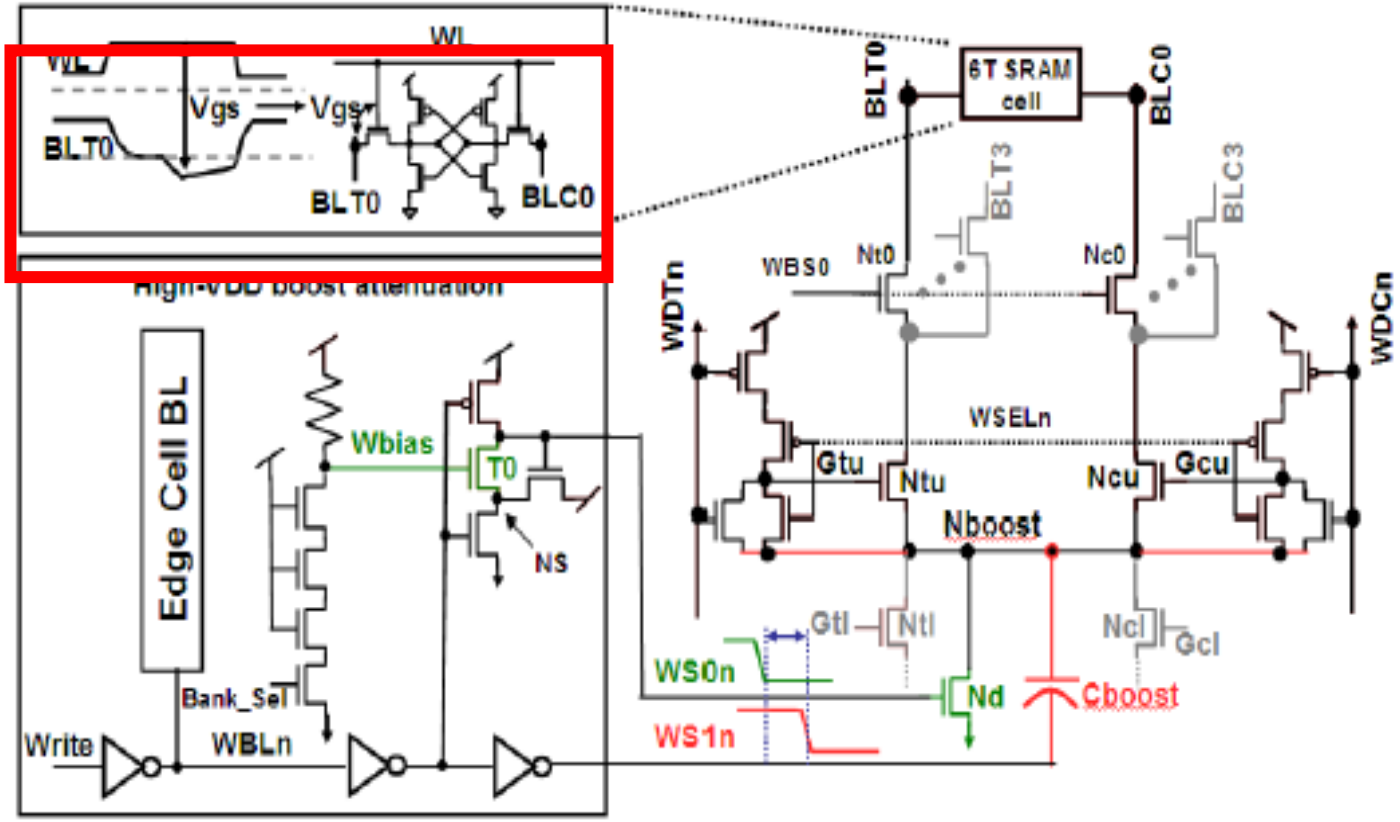






Write-Assist : Negative BL

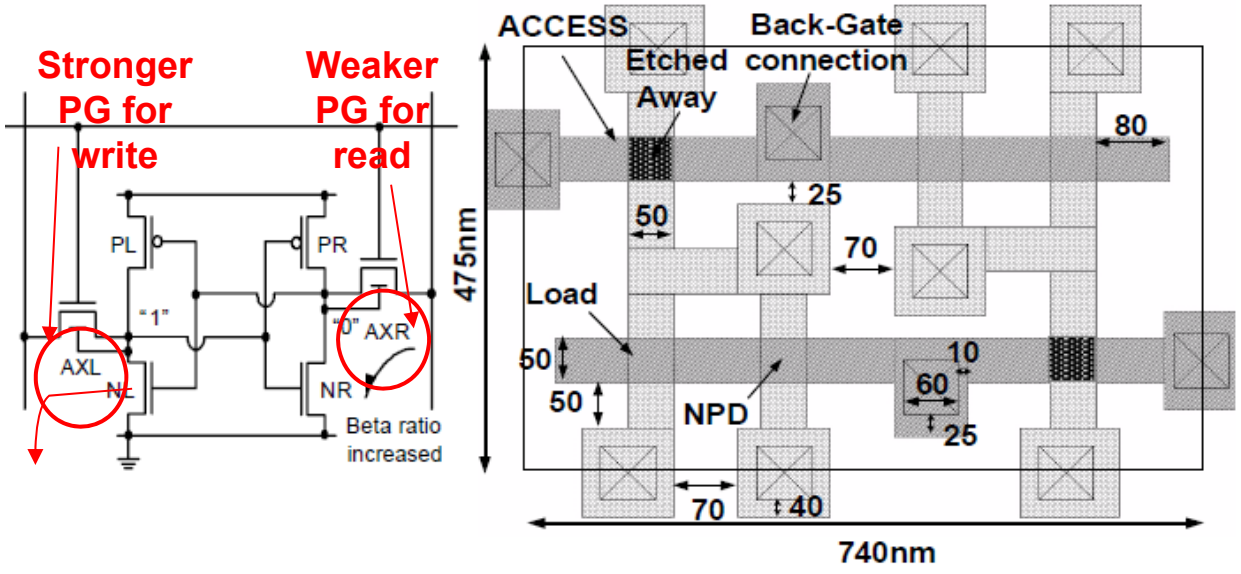
- Write driver with boosted control and attenuation



Ref: "Negative bit-line", (IBM), ISSCC, 2011

Example of Back-Gate SRAM Design

- Use back-gate control to improve the read-SNM



Ref: Zheng Guo, et al. (UC Berkeley), "FinFET-based SRAM design", ISPED, 2005.

Outline

- 1. Technology Considerations
- 2. Spice Modeling
- 3. Design Methodology and CAD Tools
- 4. Digital Design
  - Standard Cells, Layout
  - IO and ESD
- 5. SRAM
- **6. Analog & Mixed-Signal, RF**
- 7. Conclusion
- References

© 2013 IEEE

Key Device Requirements

- Headroom to support cascode structure
  - Vt < 0.2* Vdd
- Core device Ft to support 60GHz RF applications
  - Ft > 250Ghz
- Low gate resistance to minimize flicker noise
  - Sheet resistance < 50 Ohm
- Mismatch of IO device
  - IAVtgm < 5mv-um
  - Gain > 200 (or 46dB)
- Noise @ Core Lmin
  - < 30 $uV^{\wedge 2}$ $um^{\wedge 2}/Hz$ @ 1Hz
- Metal/Via EM handling capability close to device driving capability for driver applications

© 2013 IEEE

Pros & Cons on Analog/RF Circuits

- Pros:
  - Better matching
  - Higher current driving capability
  - Lower gds → higher gain
  - Smaller Vt → larger headroom
  - Effectively no body-effect
  - Lower leakage

- Cons:
  - Impact high frequency application (Ft)
    - Higher S/D resistance degrade gm
    - Higher Cco
  - Device EM handling capability
  - Passive components (diode, resistor) availability
    - Loop shape layout not allowed
    - Behavior not as usual
  - Self-Heating causes higher local temperature and degrades EM performance

© 2013 IEEE

Assessed EM Limitation on FinFET

- Via EM limits the maximum allowable power delivery from single FinFET transistor
  - Degradation for each new generation:
    - Via EM capability drop ~0.7X
    - Device driving capability increase ~ 1.25X
- Possible solutions
  - Shorter wire length
  - Lower local self-heating

© 2013 IEEE

Fin/PO/OD Local Density Impact

- With HKMG, device uniformity shows higher variation in traditional layout style
  - MG (metal gate) Hi-Resistor array with center effect
    - Affected by STI dishing due to low OD density
  - MOS array with edge effect
    - Edge devices of MOS array with higher variation due to poly gradient between array and surrounding patterns
  - Interference among analog blocks due to each with different and wide spreading density on poly and OD
- Fin density is likely new factor to impact device uniformity
- New layout style and flow needed to minimize this effect
  - Gradient control on density from array to surrounding patterns

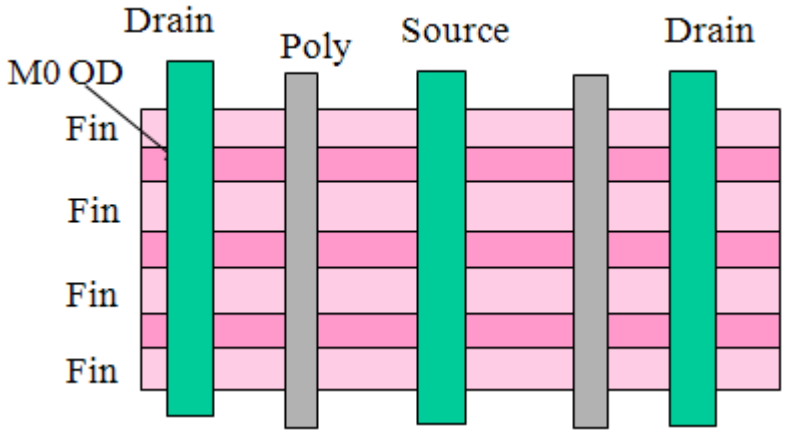
© 2013 IEEE

Design Flow Impact -1

- Quantized Fin
  - Limit the flexibility of IP porting
    - Due to discrete width
    - Fin on track limits the flexibility on analog block floor plan
  - Need CAD tool to optimize the quantized width and off-grid issue
  - Minimum 2-Fin transistor will limit the flexibility of low power design
    - Single-Fin transistor is desirable to have.

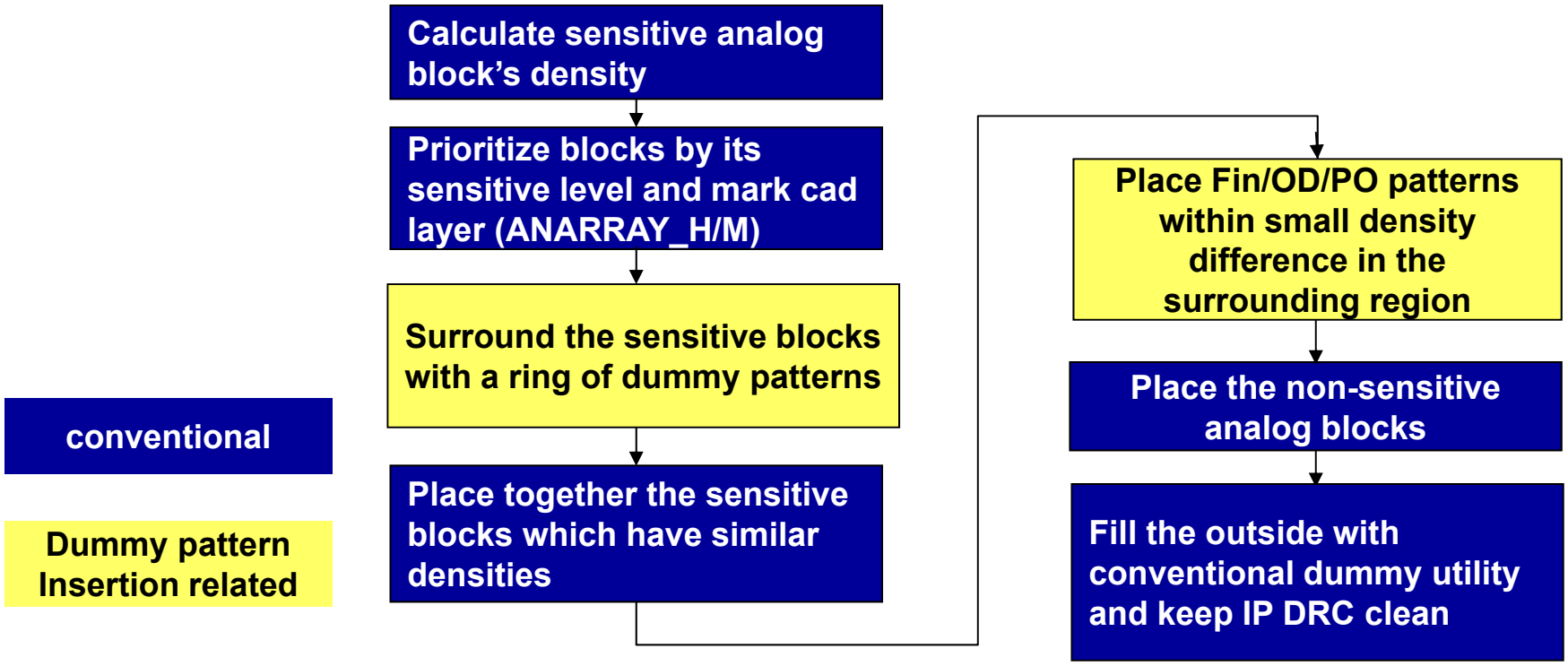
* If Fin Width=Fw (nm), Fin space Fs (nm), Fin Must be in OD edge.

→ OD Width=Fw+ (Fw+Fs)*n



Design Flow Impact -2

- Fin/PO/OD density control flow to minimize the device variation



Challenges & Opportunities

- FinFET vs. Planar CMOS on key analog parameters

Items	Opportunities	Challenges
Headroom	Vt 50~100mv lower	Device breakdown voltage
Mismatch	~ ½	Edge Fin variation Variation due to smaller OD
Idsat	20~30% higher	Via and Metal EM limitation Self heating
Ft	Higher gm	Higher Cco S/D serial resistance Gate serial resistance
Gain	~ 10dB higher	Smaller max. Lg

Outline

- 1. Technology Considerations
- 2. Spice Modeling
- 3. Design Methodology and CAD Tools
- 4. Digital Design
  - Standard Cells, Layout
  - IO and ESD
- 5. SRAM
- 6. Analog & Mixed-Signal, RF
- **7. Conclusion**
- References

Conclusion

- **FinFET design has been proven at 22 nm node**
  - See publications from Intel Corporation at 2012 ISSCC Conference and 2012 VLSI Technology/Circuits Symposia
  - Many Intel product announcements in 2012, at 22 nm node
- **FinFET design is gaining popularity**
  - FinFET design will be the norm at 16 / 14 nm node, and 10 nm node
- **For IC foundry, FinFET**
  - Problem study is identified
  - Solution is identified, too
  - The differences between FinFET and planar CMOS need to be taken care
  - Good progress by ecosystem: EDA tools and IP vendors

References -1

1. Alioto, M., "Comparative Evaluation of Layout Density in 3T, 4T, and MT FinFET Standard Cells," *IEEE T-VLSI*, vol.19, May 2011
2. Rao, R., et al., "Evaluation and Optimization of FinFET Quantization Error in Porting a Design from Planar Silicon Technology," *SOI Conference,* pp.49-50, Oct. 2007
3. Roy, K.; et al., "Device/circuit interactions at 22nm technology node," *DAC*, pp.97-102, July 2009
4.. Tawfik, S.A.; et al., "Manufacturable low-power latches for standard tied-double-gate FinFET technologies," *MWSCAS .* pp.471-474, Aug. 2009
5. Jie Gu; et al., "Statistical Leakage Estimation of Double Gate FinFET Devices Considering the Width Quantization Property," *IEEE T-VLSI*, vol.16, pp.206-209, Feb. 2008
6. Itoh, K., "Device-conscious circuit designs for low-voltage nanoscale CMOS LSIs," *Mixed Design of ICs and Systems (MIXDES),* pp.21-26, June 2010
7. Manoj, C.R., et al., "Impact of Fringe Capacitance on the Performance of Nanoscale FinFETs," *IEEE EDL*, vol.31, pp.83-85, Jan. 2010
8. Agrawal, S., et al.,"A Physical Model for Fringe Capacitance in Double-Gate MOSFETs," *IEEE T-ED*, vol.57, pp.1069-1075, May 2010

References -2

9. Wen Wu; et al.,"Gate resistance modeling of multifin MOS devices," *IEEE EDL*, vol.27, pp. 68- 70, Jan. 2006

10. Dixit, A., et al., "Analysis of the parasitic S/D resistance in multiple-gate FETs," *IEEE T-ED*, vol.52, pp. 1132- 1140, June 2005

11.Agrawal, S., et al.,"A Physical Model for Fringe Capacitance in Double-Gate MOSFETs With Non-Abrupt Source/Drain Junctions and Gate Underlap," *IEEE T-ED*, vol.57, pp.1069-1075, May 2010

12. Xin Sun, et al., "Variation Study of the Planar Ground-Plane Bulk MOSFET, SOI FinFET, and Trigate Bulk MOSFET Designs," *IEEE T-ED*, vol.58, pp.3294-3299, Oct. 2011

13. E. Baravelli, et al.,"Impact of line-edge roughness on FinFET matching performance," *IEEE Electron Devices, vol. 54, pp. 2466–2474,* Sep. 2007

14. E. Baravelli, et al.,"Impact of LER and random dopant fluctuations on FinFET matching performance," *IEEE Nanotechnol., pp. 291–298,* May 2008.

15. Bennamane, K., et al., "Static and low frequency noise characterization of FinFET devices," *ULIS Conference*, pp.39-42, March 2009

References -3

16. Jae Woo Lee, et al., "Experimental analysis of surface roughness scattering in FinFET devices," *IEEE ESSDERC,* pp.305-308, Sept. 2010

17. O'uchi, S., et al., "Characterization of metal-gate FinFET variability based on measurements and compact model analyses," *IEDM*, pp.1-4, Dec. 2008

18. Matsukawa, T., et al. , "Comprehensive analysis of variability sources of FinFET characteristics," *VLSI Tech Symposium*, pp.118-119, June 2009

19. Endo, K.; et al., "Variability Analysis of TiN Metal-Gate FinFETs," *Electron Device Letters, IEEE*, vol.31, pp.546-548, June 2010

20. H. Cheng, et al., "Random work function variation induced threshold voltage fluctuation in 16-nm bulk FinFET devices with high-k-metal-gate material," *Computational Electronics (IWCE)Workshop*, pp.1-4, Oct. 2010

21. Rasouli, S.H., et al., "Grain-Orientation Induced Quantum Confinement Variation in FinFETs and Multi-Gate Ultra-Thin Body CMOS Devices and Implications for Digital Design," *IEEE T-ED*, vol.58, pp.2282-2292, Aug. 2011

22. Matsukawa, et al., "Fluctuation Analysis of Parasitic Resistance in FinFETs With Scaled Fin Thickness," *IEEE EDL*, vol.30, pp.407-409, April 2009