Managing offset and flicker noise

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Outline

- Motivation and history
- Offset and flicker noise background
- Techniques to manage offset and flicker noise
  - Chopper Stabilization
    - Basic idea
    - Switched capacitor and continuous time implementations
    - Chop artifacts and their removal
    - Second order effects
  - Autozero
    - Basic idea
    - Implementation examples
    - Second order effects
  - Correlated double sampling
    - An extension of Autozero into switched capacitor circuits
- Conclusion

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Motivation: High Gain Example

- 1mV signal, 2μV of noise
- Would like an amplifier with a gain of 1000x
- 1V signal, 2mV noise,
- use a 10 bit ADC

BUT –

- 9mV of opamp offset
- limits the gain to 100x
- 900mV of amplified offset, 100mV of amplified signal, 0.2mV of amplified noise
- Use a 13 bit ADC

The year 1956:HP 150-1800

From www.hparchives.com

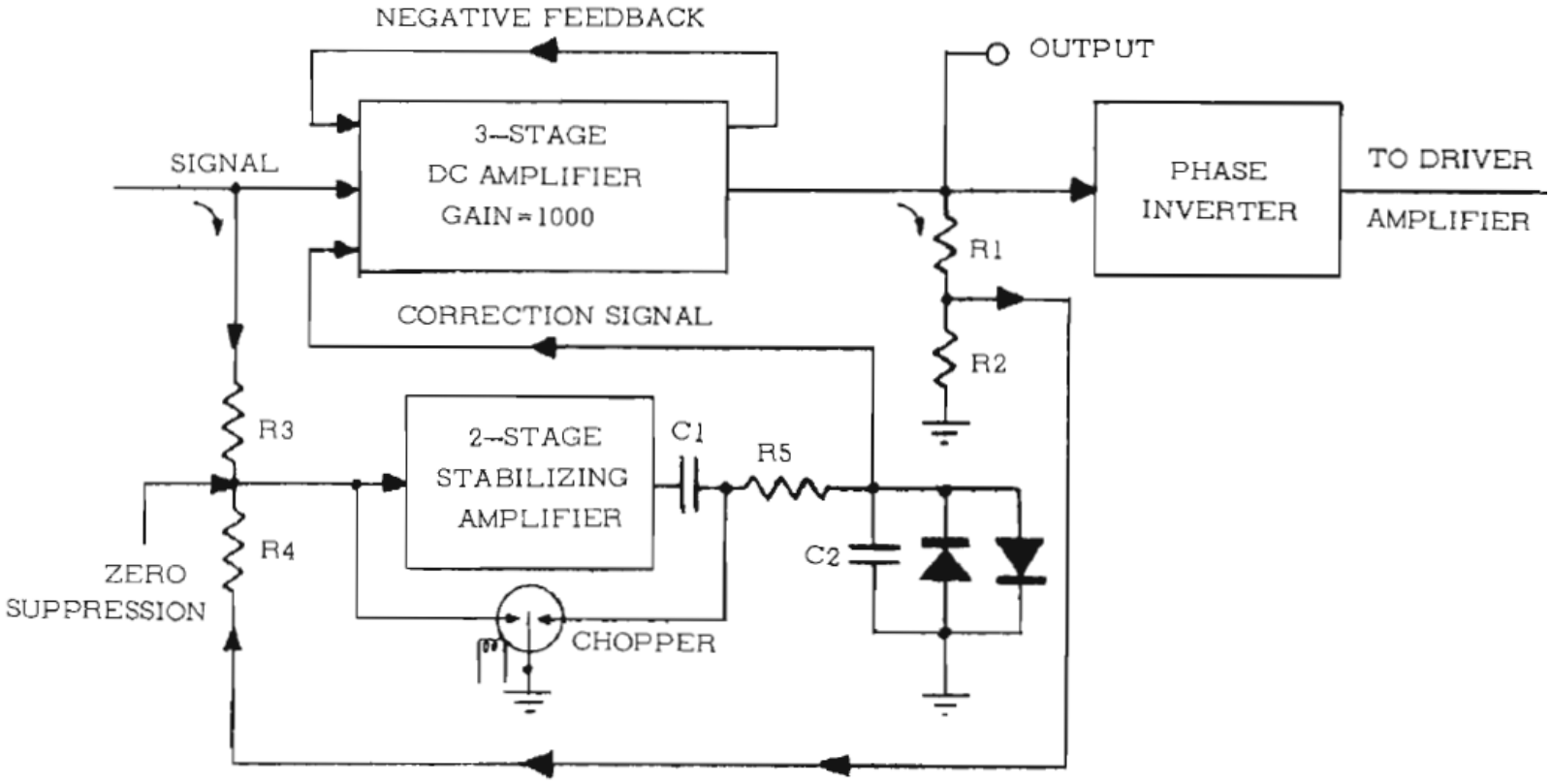
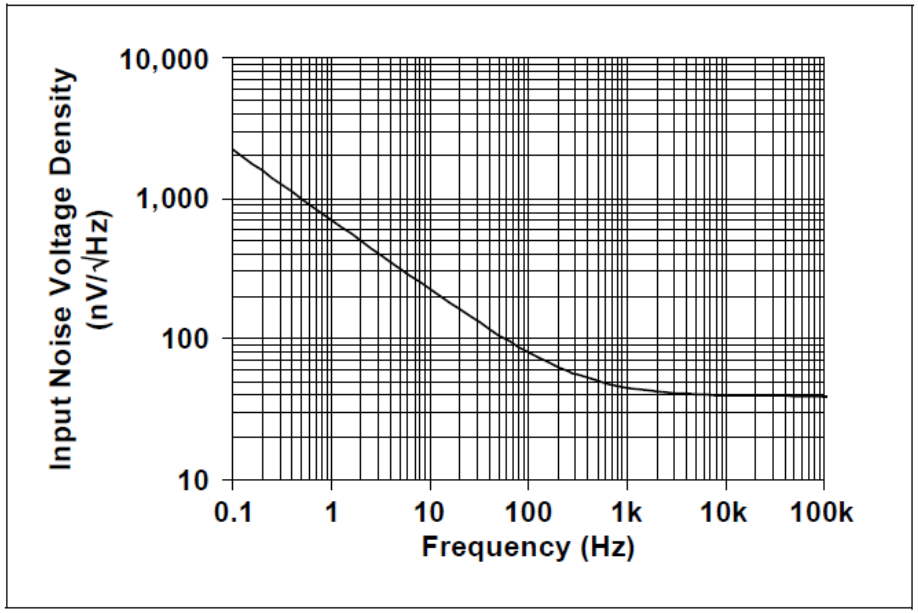


Figure 3. Basic Circuits of the Stabilized DC Preamplifier.

Motivation: Small Signals, Low Noise

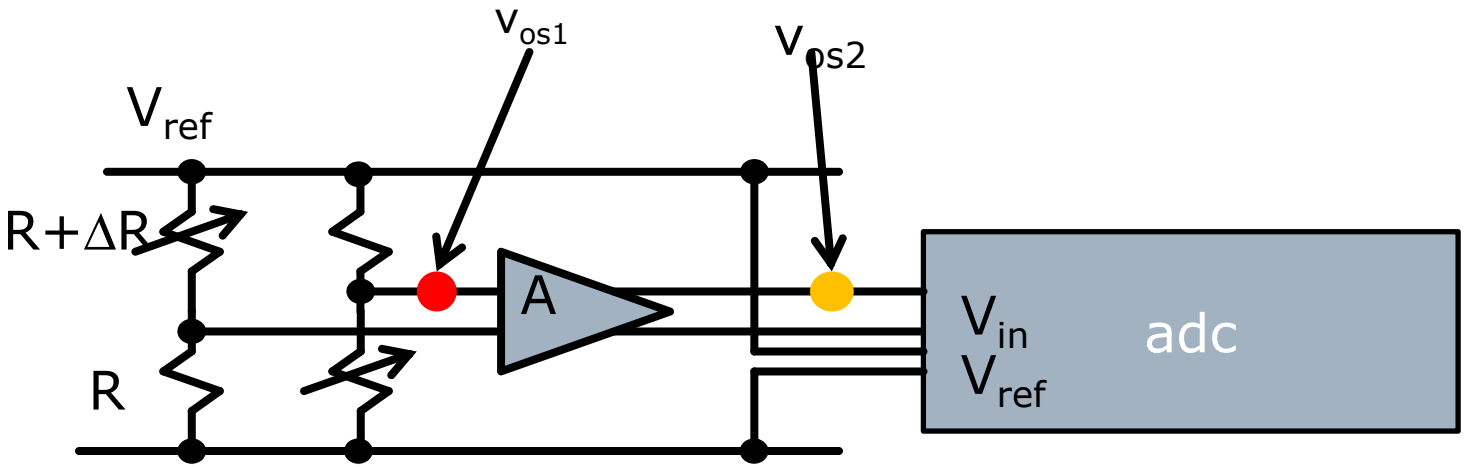
- Hall Sensor produces μV level signals
- Flicker noise in a FET based opamp can have $100\mu V_{pp}$ in 0.1 to 10Hz bandwidth
- Thermal noise in 10Hz can be around 1μVpp in the same band
- Flicker noise buries the signal – can be more than an order of magnitude above the thermal noise level



Typical noise spectrum of a MOSFET

Motivation: Ratiometric Example

- Bridge transducers – we want to measure $\Delta R/R$



$\Delta V_1 = V_{ref} * \Delta R/R$

$\Delta V_2 = A * \Delta V_1 + v_{os1}$

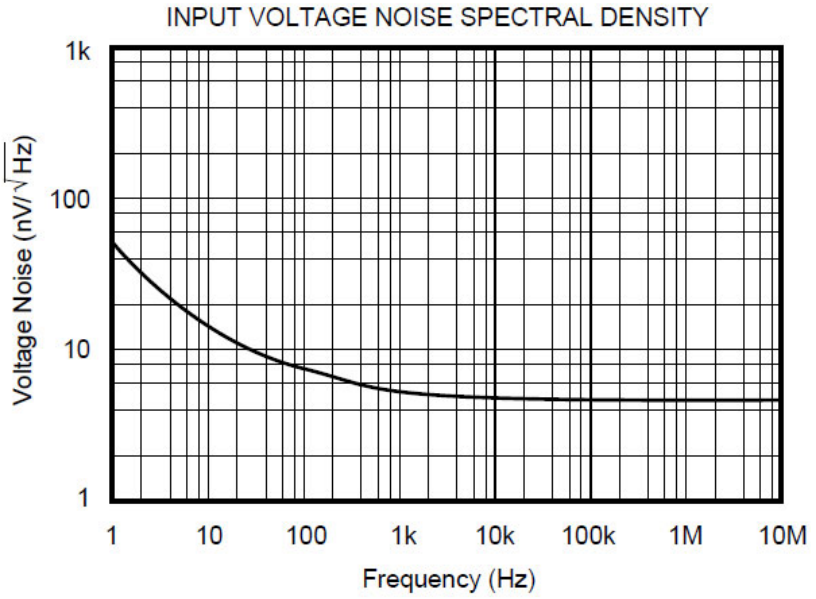
$D = (\Delta V_2 + v_{os2})/V_{ref}$

$D = A * \Delta R/R + (A * v_{os1} + v_{os2})/V_{ref}$

If $v_{os1}=0$ and $v_{os2}=0$, $D=A\Delta R/R$
Offset ruins this ratiometric measurement

The bipolar and JFET days

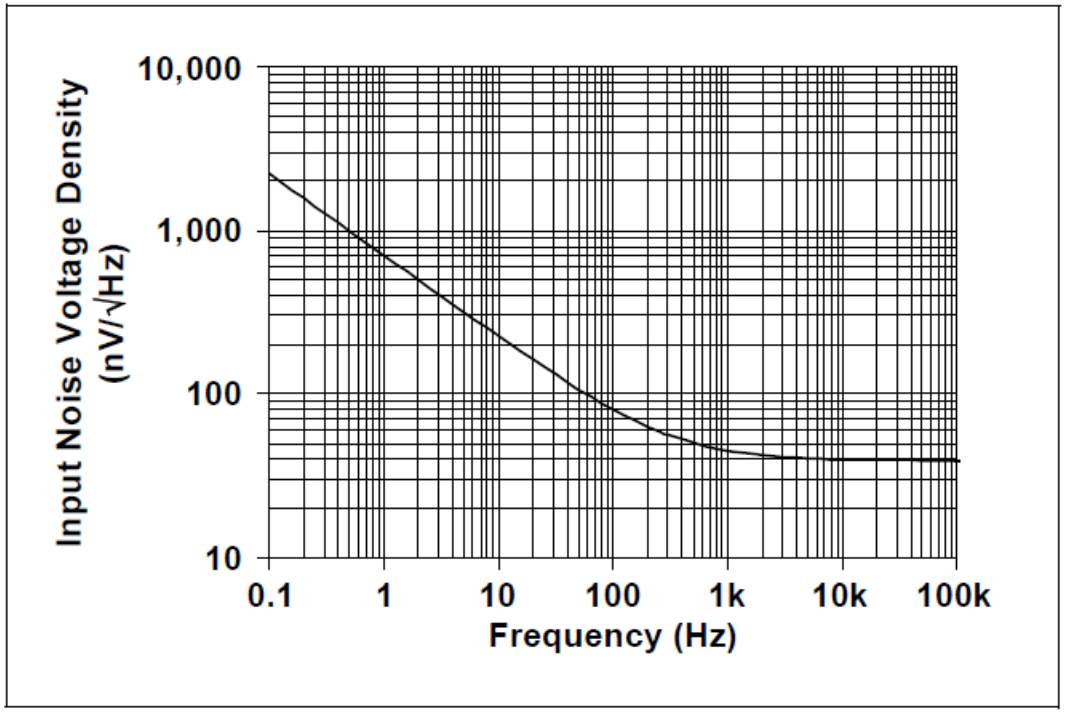
- Good devices from a matching and flicker noise perspective, especially JFETs
- Devices like the OP627 provided excellent DC measurement capability – JFET input
- Offset <100μV,
- offset drift <0.8μV/C
- 15nV/sqrtHz noise density at 10Hz
- Offset and flicker noise are minor problems.



Noise spectrum OP627

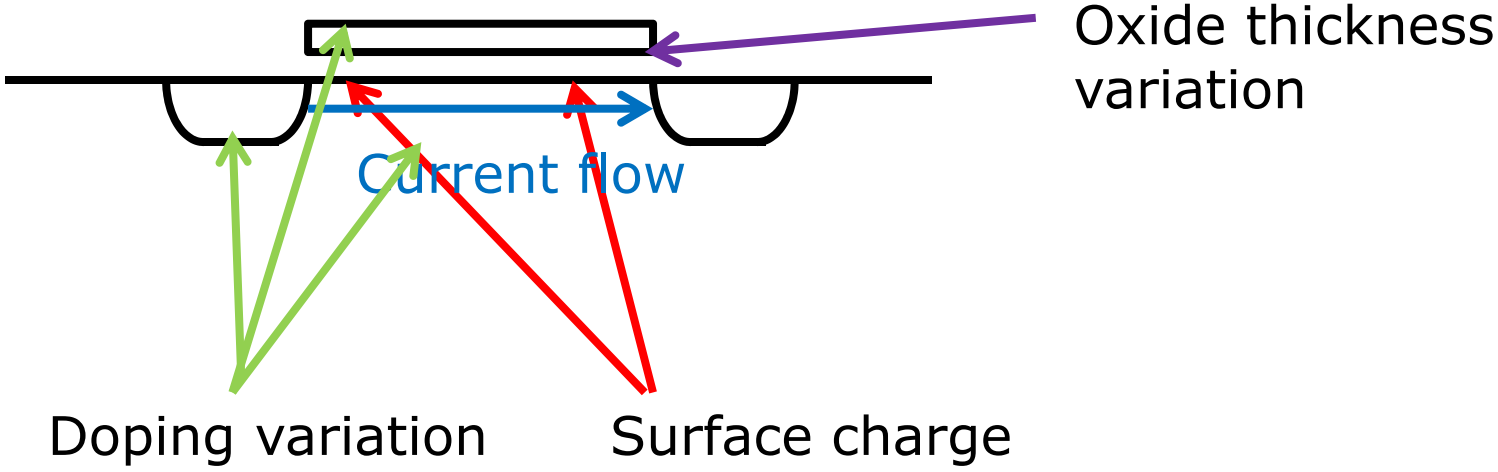
Comparison to a MOS opamp

- MCP6241
- Vos=5mV
- dVos/dT=3μV/C
- Noise density at 10Hz 250nV/rtHz
- Noise spectrum has significantly higher flicker noise corner



Noise spectrum MCP6241

CMOS device characteristics



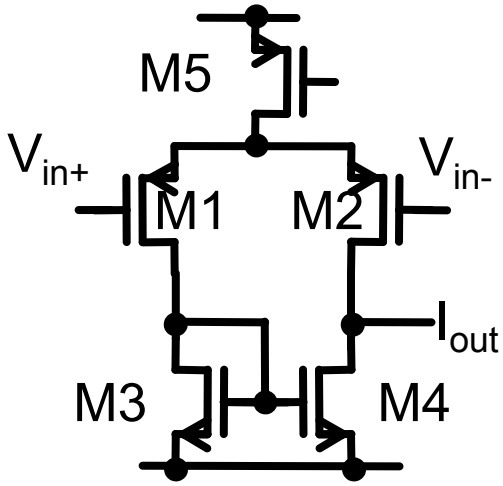
- $V_{T0}=kT/q(\ln(N_D*N_A/n_i^2)+\ln(N_A/n_i)-Q_b/C_{ox}-Q_{ox}/C_{ox}$
- $V_T=V_{T0}+\gamma*\mathrm{sqrt}(V_{sb}+2\Phi_F)-\mathrm{sqrt}(2\Phi_F)$
- V_T depends to first order on doping and oxide thickness, both of which have tolerances.
- The larger the area the more consistent the value, the less variation -> inverse proportional to root of gate area

Offset

- Basic Pelgrom model (Pelgrom et al. 1989)
  - $V_{os}=v_{os1}/sqrt(W*L)$
  - V_{os1} is the standard deviation of a device with 1um gate area
  - Based on characterization from the fab
  - This is the best case
- Offset drift is significant – up to 50% of original offset according to a datasheet survey of uncompensated CMOS opamps
- Additional effects to be considered due to layout
  - Non-identical neighborhoods add to this
    - Specifically distance from active edge
    - Distance from well edge
    - Poly in the neighborhood
    - Active in the neighborhood

Input referred offset example

- Each device has a standard deviation of $\Delta VT=A/\sqrt{(Wn*Ln)}$
- The mismatch is converted to an output current by multiplying with each device $gm=\sqrt{(K'*W/L*I_d)}$.
- The output current is converted to an input signal by dividing with the input device gm1=gm2 (input referred)
- M1 and M2 and devices 3 and 4 each have identical parameters, M5 contribution gets cancelled through symmetry
- Since these are probabilities they sum as rms.



$$V_{os}^2=V_{os1}^2+v_{os2}^2+(v_{os3}^2+v_{os4}^2)*(g_{m3}/g_{m1})^2$$

$$V_{os}^2=A^2*2/(W_1*L_1)+A^2*2/(W_3*L_3)*K'_n/K'_p*(W_3/L_3)/(W_1/L_1)$$

$$V_{os}^2=A^2*2/(W_1*L_1)(1+ K'_n/K'_p*L_1^2/L_3^2)$$

Example $A=4mV\mu m$, $W=40\mu m$, $L_1=0.1\mu m$, $L_3=0.8\mu m$
$K'_{p=}200\mu A/V^2$, $K'_{n=}800\mu A/V^2$

$$v_{os}=4mV/2*(1+1/16)=2.125mV$$

Flicker noise or 1/f noise

- A simple explanation
  - Surface effect – carrier recombination at surface traps
- Basic textbook model – coarse, does not take into account bias dependency etc.
  - KF and AF are model parameters
  - AF is close to 1
  - $Vn=KF/sqrt(W*L)/f^{AF}$
- Offset looks like 'static' 1/f noise – whatever works on 1/f noise works for offset, too.

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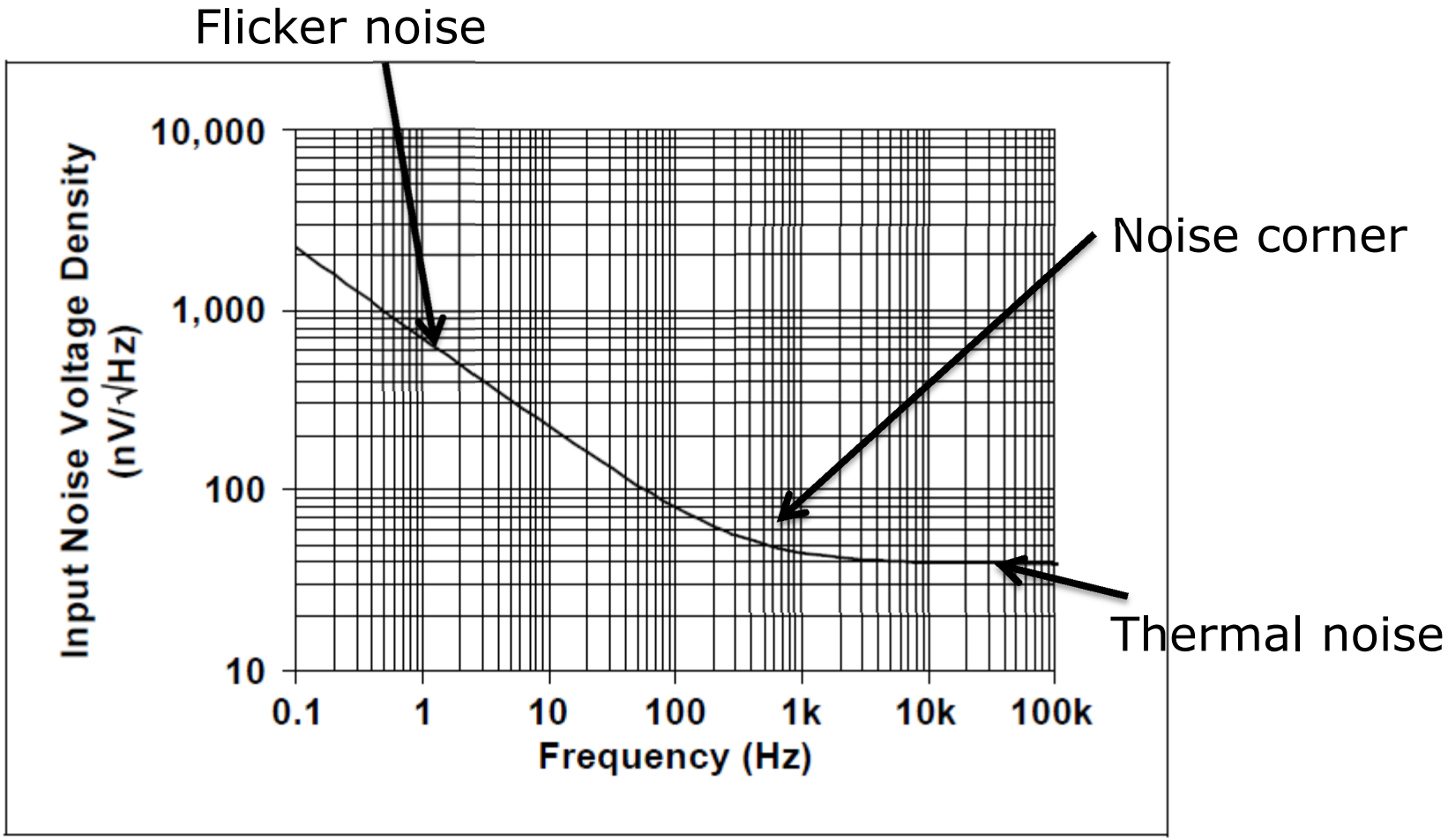
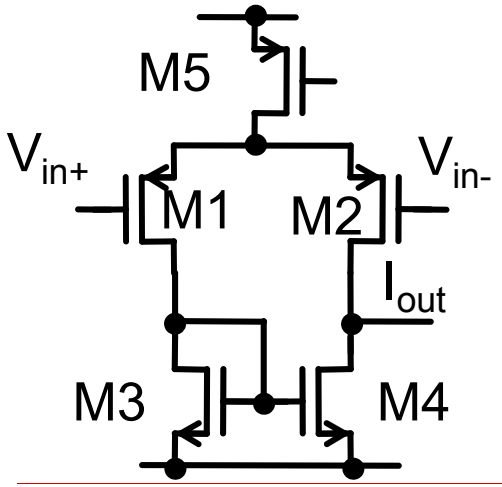
Noise spectrum of MOS device



Flicker noise analysis example

Each device has a flicker noise of $V_n=\mathrm{sqrt}(KF/(W_n*L_n*f^{AF}))$
The voltage noise is converted to an output current by multiplying with each device gm.
The input signal is converted to an output current by multiplying with the input device gm1=gm2
M1 and M2 match, M3 and M4 match, M5 contribution gets cancelled through symmetry
Since these are noise voltages they sum as rms.



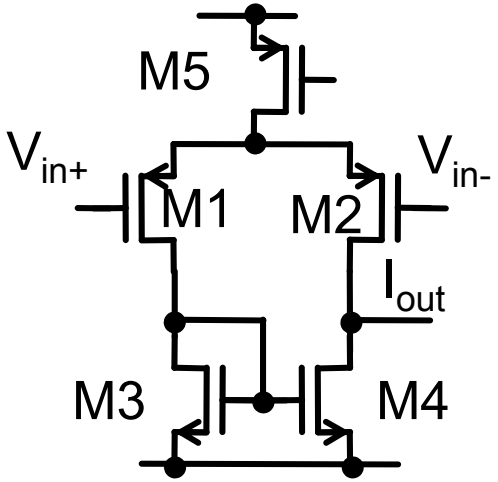
$$V_n^2=V_{n1}^2+v_{n2}^2+(v_{n3}^2+v_{n4}^2)*(g_{m3}/g_{m1})^2$$

$$V_n^2=K_{Fp}/f*2/(W_1*L_1)$$
$$+K'_n/K'_{p*}K_{Fn}/f*2/(W_3*L_3)*(W_3/L_3)/(W_1/L_1)$$

$$V_n^2=K_{Fp}/f*2/(W_1*L_1)(1+K'_n/K'_p*K_{Fn}/K_{Fp}*L_1^2/L_3^2)$$

See Johns/Martin chapter 4

Flicker noise analysis example



$V_n^2=K_{Fp}/f*2/(W_1*L_1)(1+K'_n/K'_{p*}K_{Fn}/K_{Fp}*L_1^2/L_3^2)$

Example

K_{Fn}=2e-23
K_{Fp}=1e-23
$K'_{p=}$200μA/V²
$K'_{n=}$800μA/V²
W=40μm, L_1=0.1μm, L_2=0.8μm, f=1Hz

V_n^2=1e-23/2*(1+1/8)=6.25e-22V²/Hz

V_n=25pV/sqrtHz

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How to manage offset and flicker noise

- AC coupling – for example in audio
- System level planning (e.g. low IF vs. zero IF)
- Upmodulation of the signal above the flicker noise corner – chopper stabilization
- One time offset calibration
- periodic offset calibration – autozero
- Separation of signal and error through correlated double sampling

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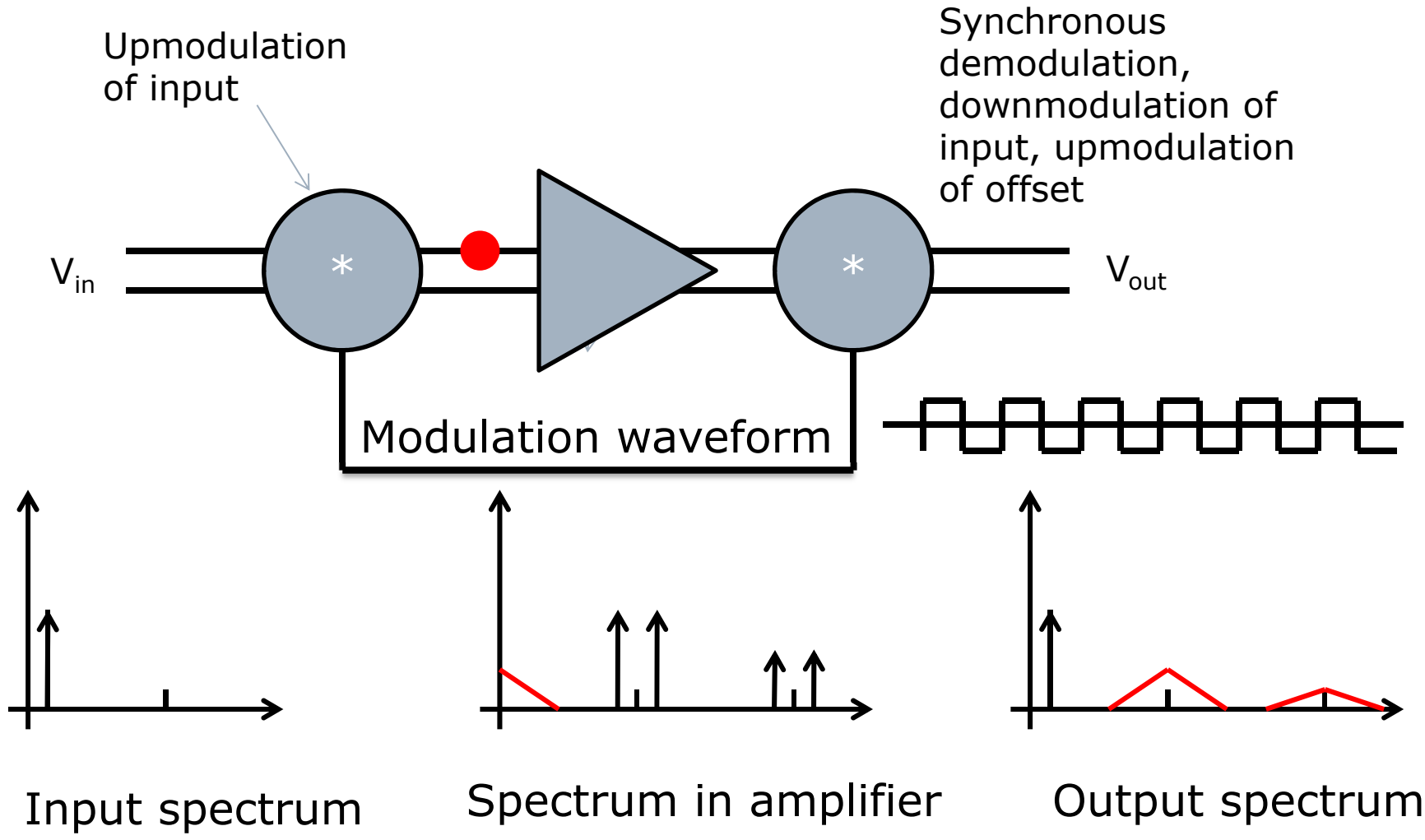
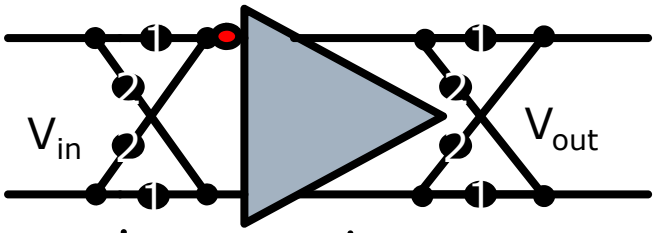
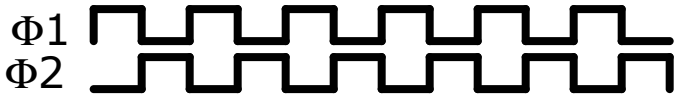
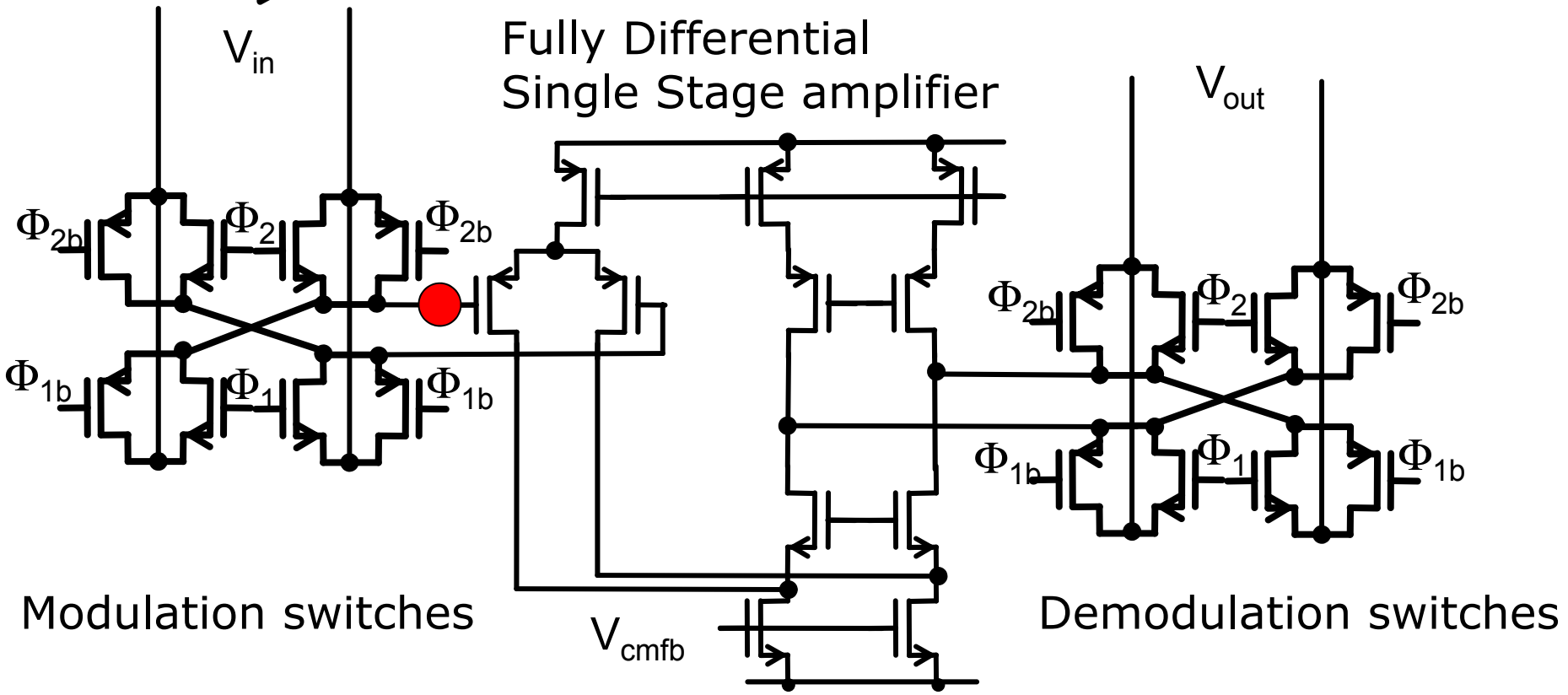
Chopper Stabilization



Transistor implementation



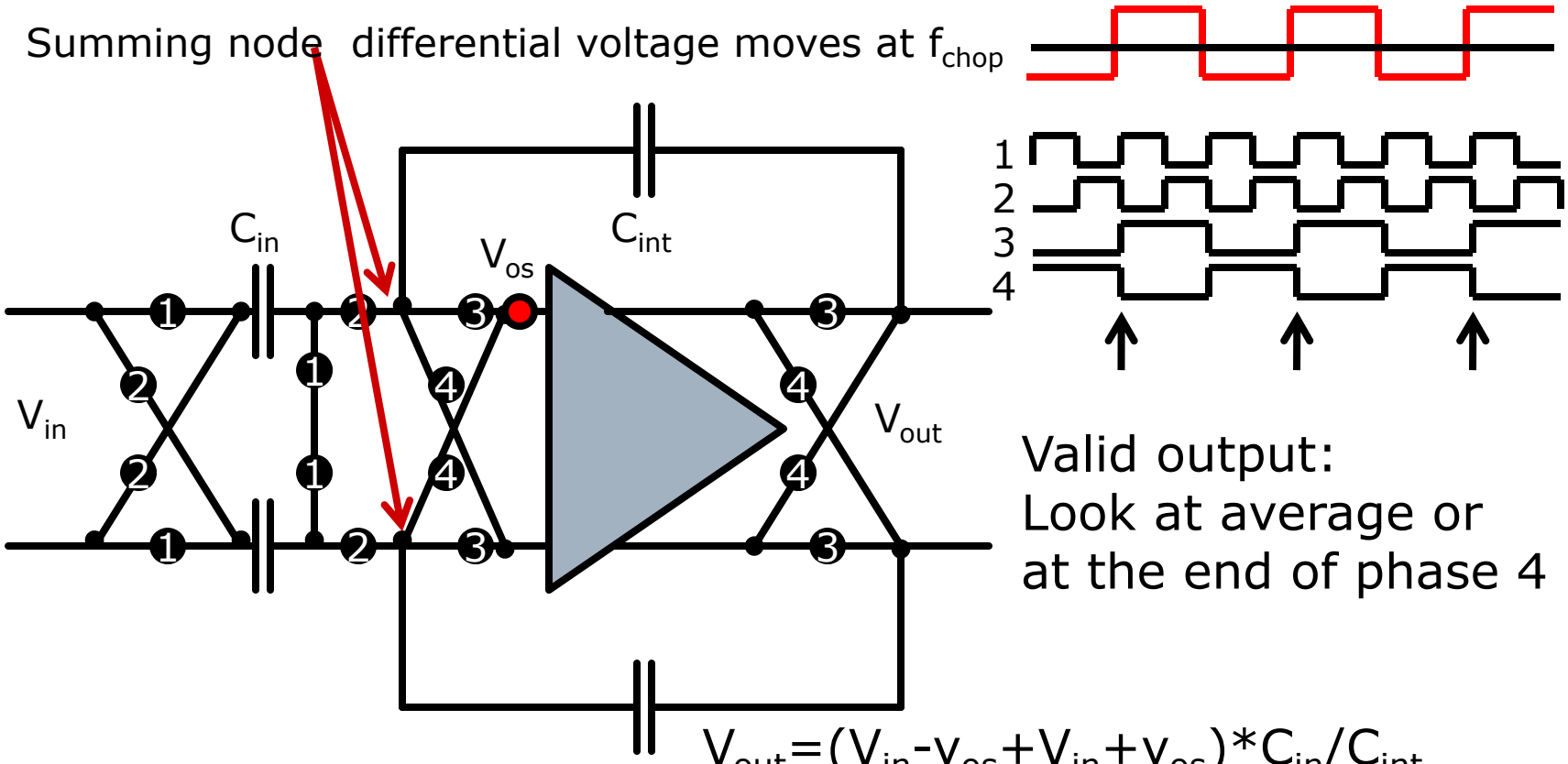




Chopper amp in SC circuit

2 cycles of charge and dump $V_{out}=(V_{in}-v_{os}+V_{in}+v_{os})*C_{in}/C_{int}$

Summing node differential voltage moves at f_{chop}



Valid output:
Look at average or
at the end of phase 4

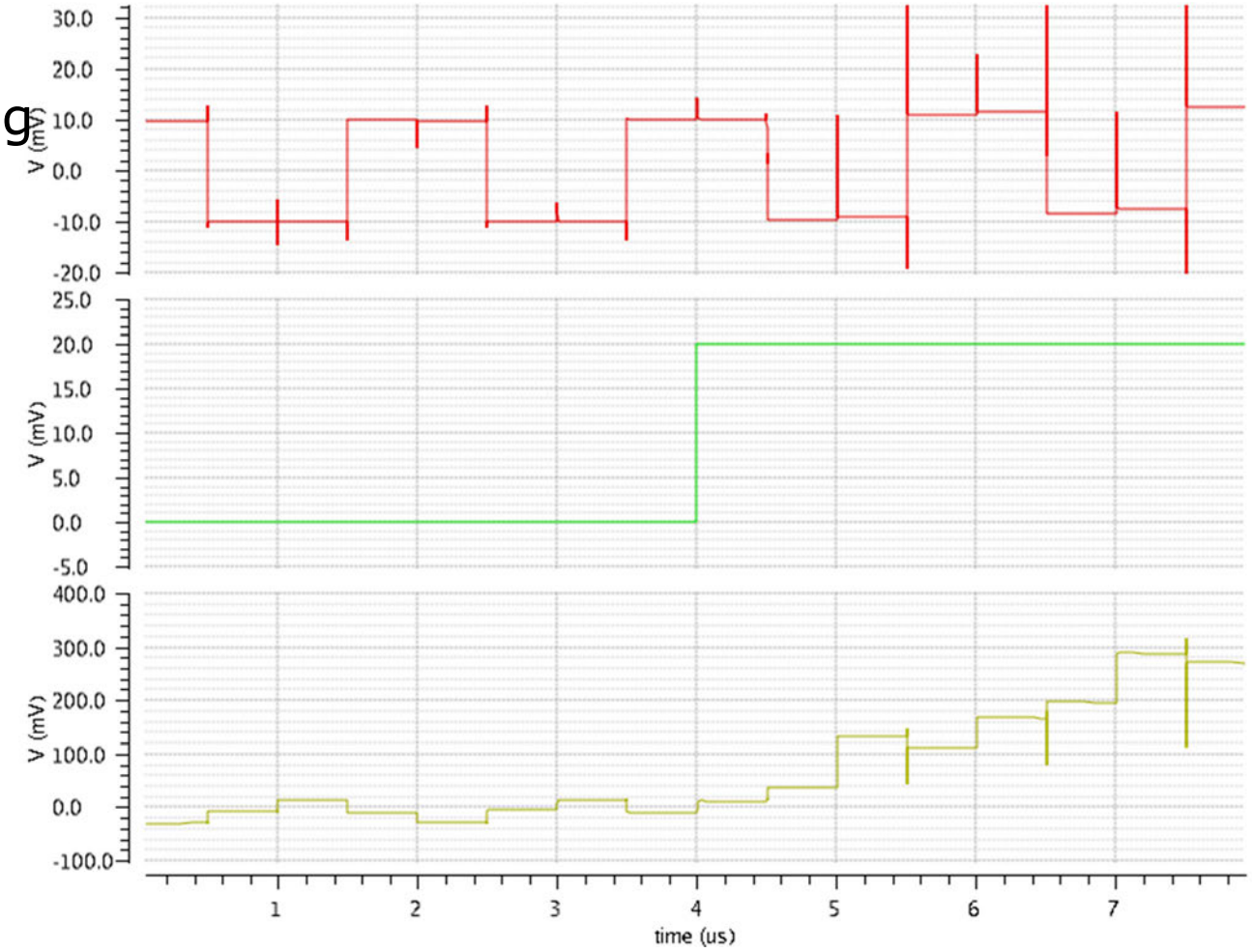
$V_{out}=(V_{in}-v_{os}+V_{in}+v_{os})*C_{in}/C_{int}$

Waveform

Summing node

input node

output node



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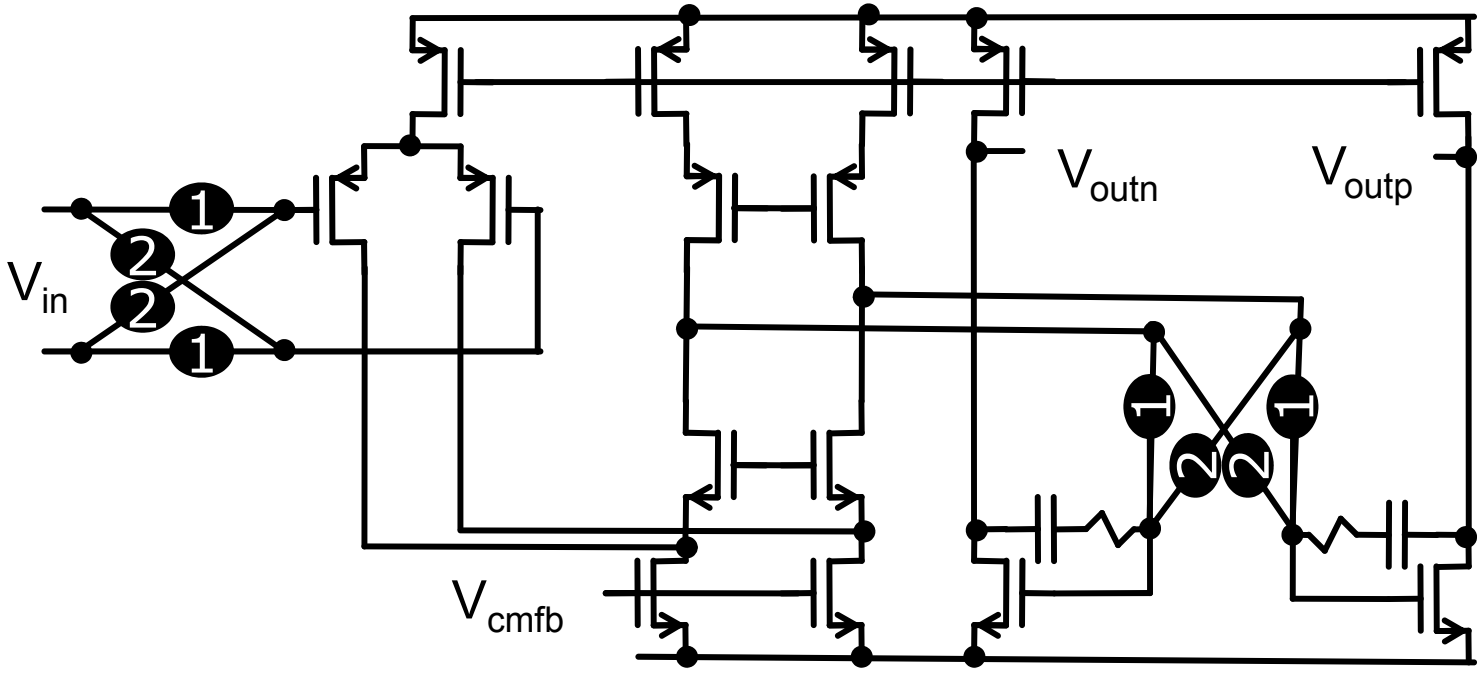
2 stage opamp implementation

Fully differential, completely symmetic
Chopping of first stage only, no capacitors within chopper

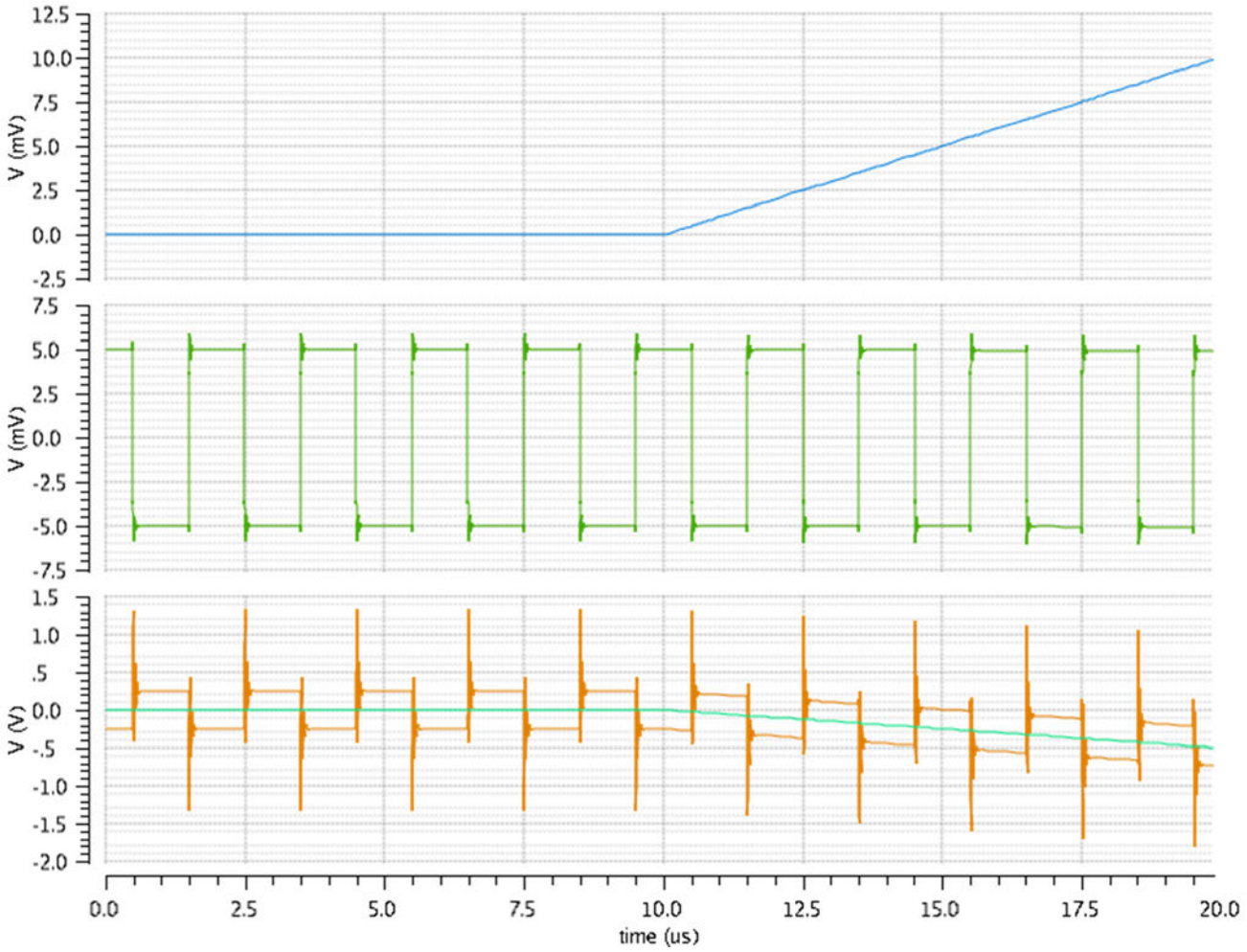


Waveforms (inverting amplifier)

input

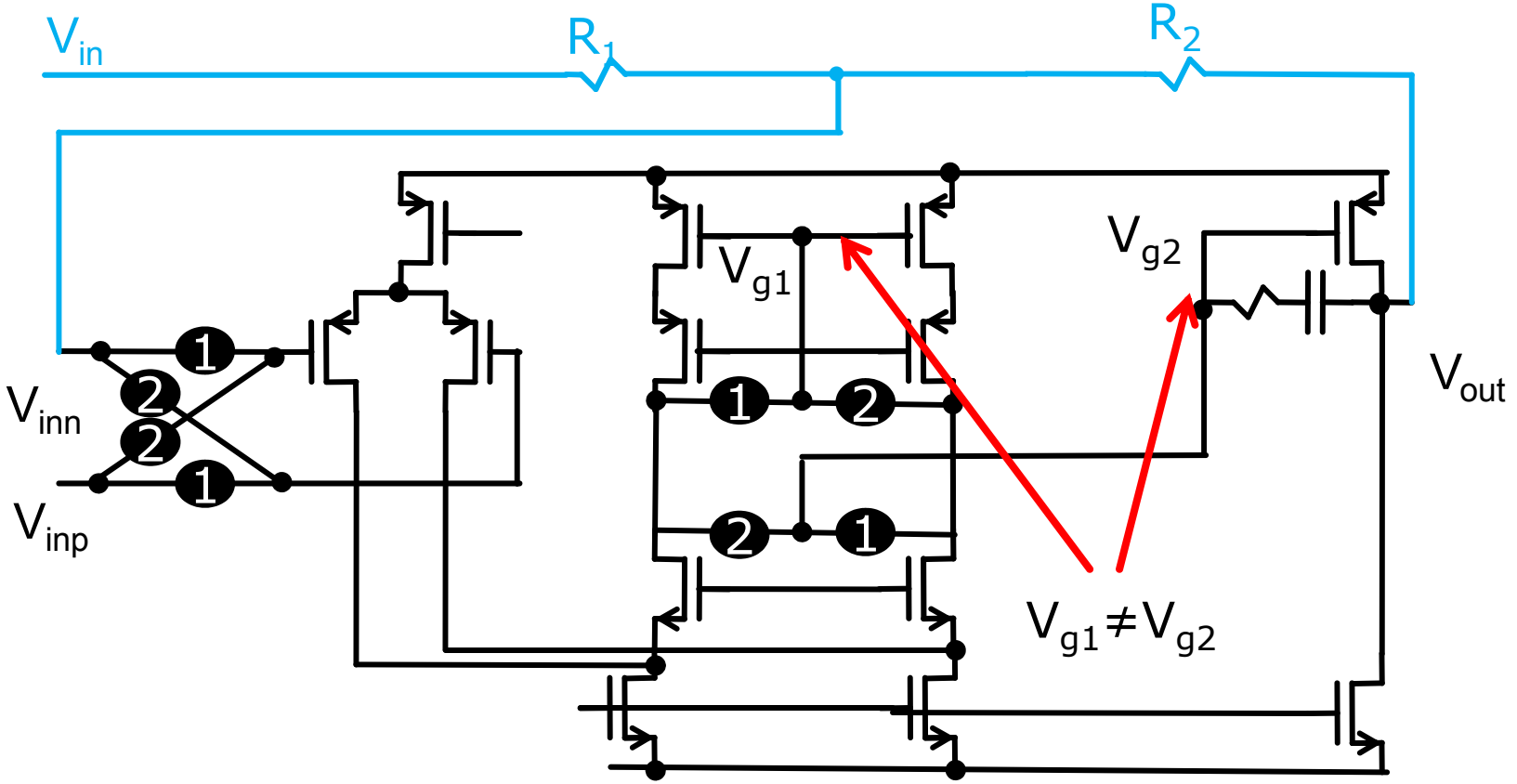
summing node

output



Chopper stabilized 2 stage opamp

Single ended – not fully symmetric
Danger – systematic offset
Chopper cannot help!



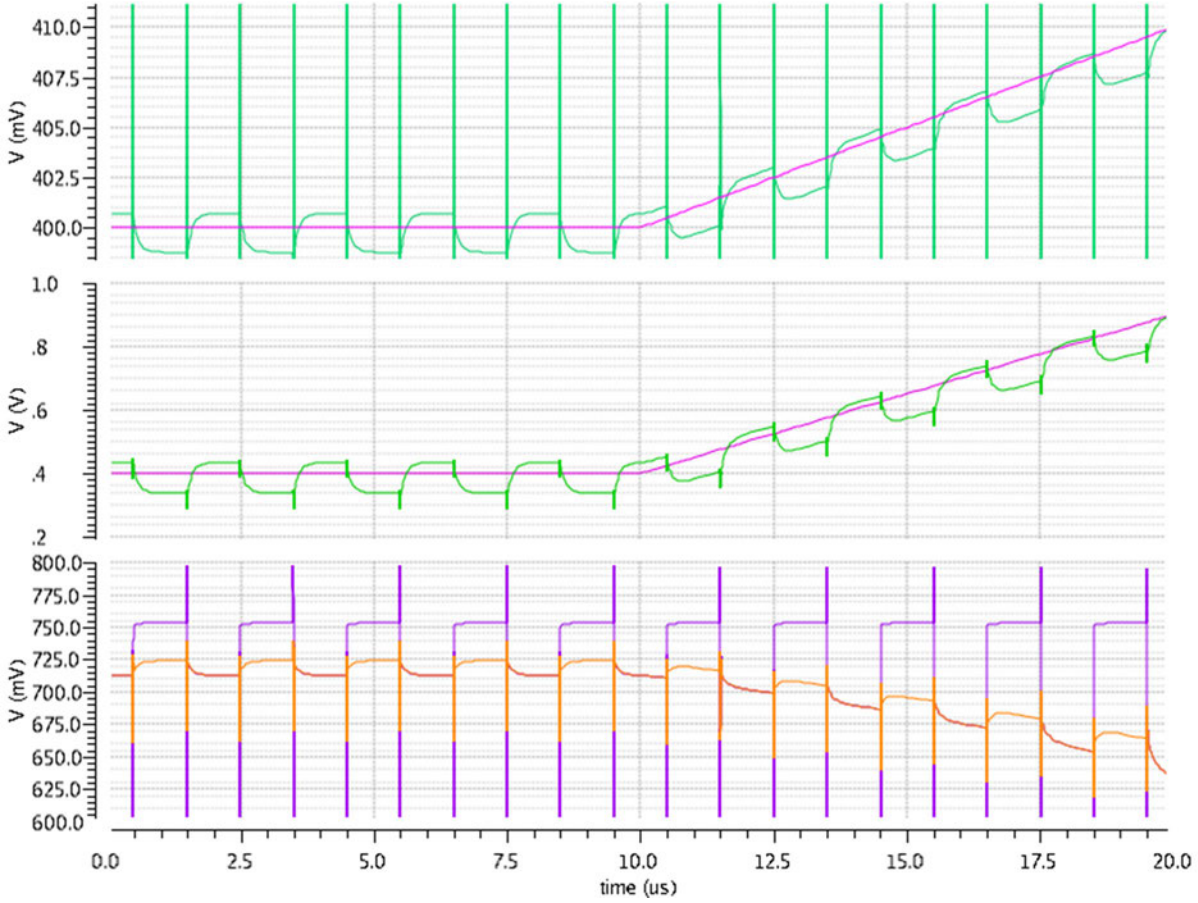
Asymmetry issue – caution!

- Closer look at two stage opamp and limiter of accuracy

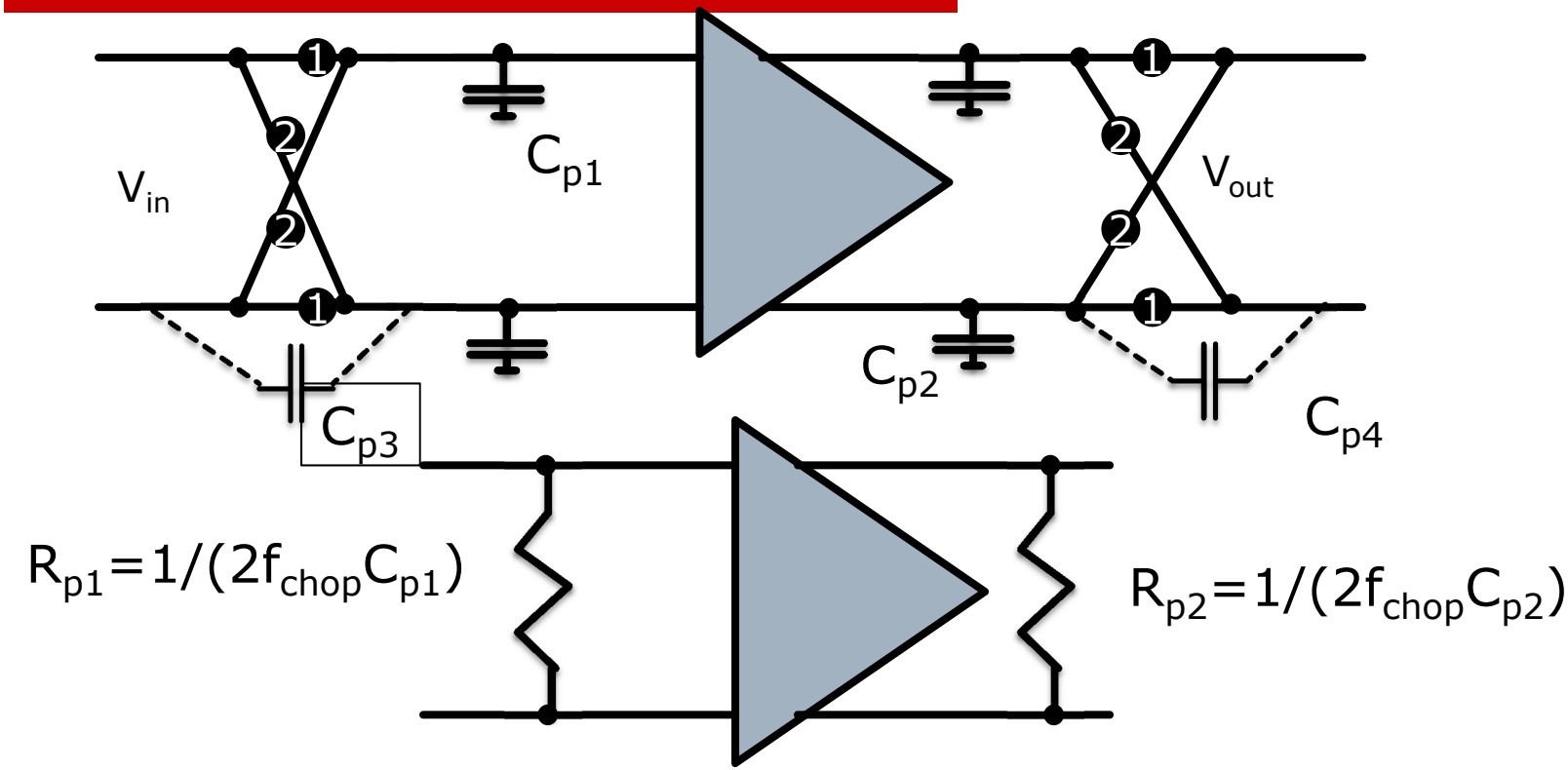
input

output

First stage output



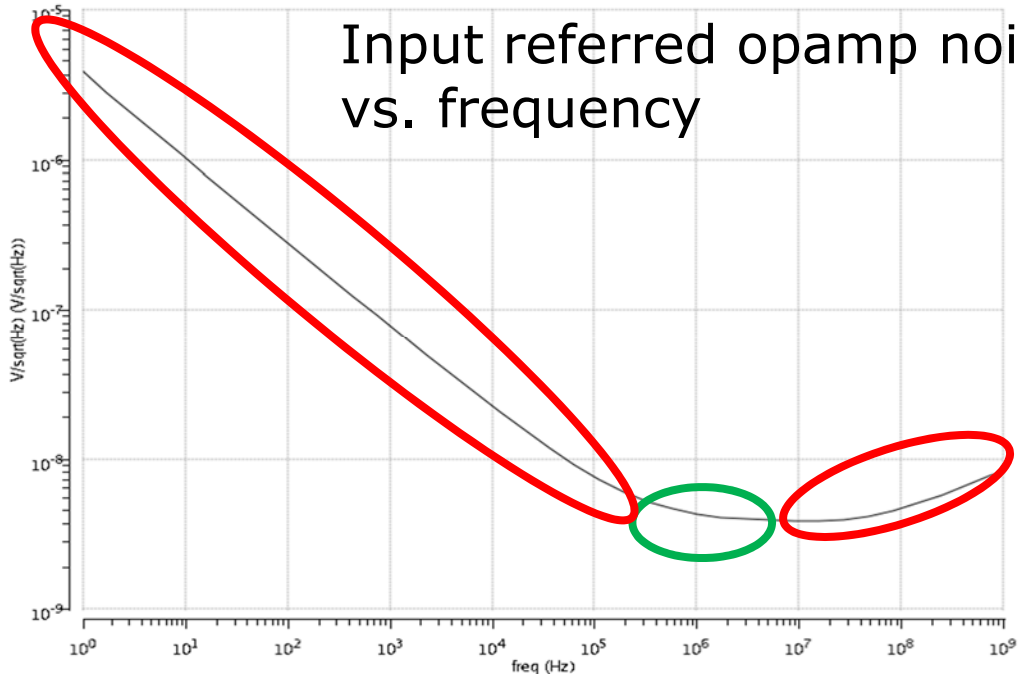
Parasitic switched capacitors



Cp1 and Cp2 are fundamental, must be taken into account
Cp3 and Cp4 must be avoided
Input current associated with these can affect interfaces
– not suitable for very high impedance sensors

Chop frequency considerations

- Chop frequency – best above the noise corner
- Keep it low to minimize the switched capacitor effect
- Must be much faster than amplifier bandwidth



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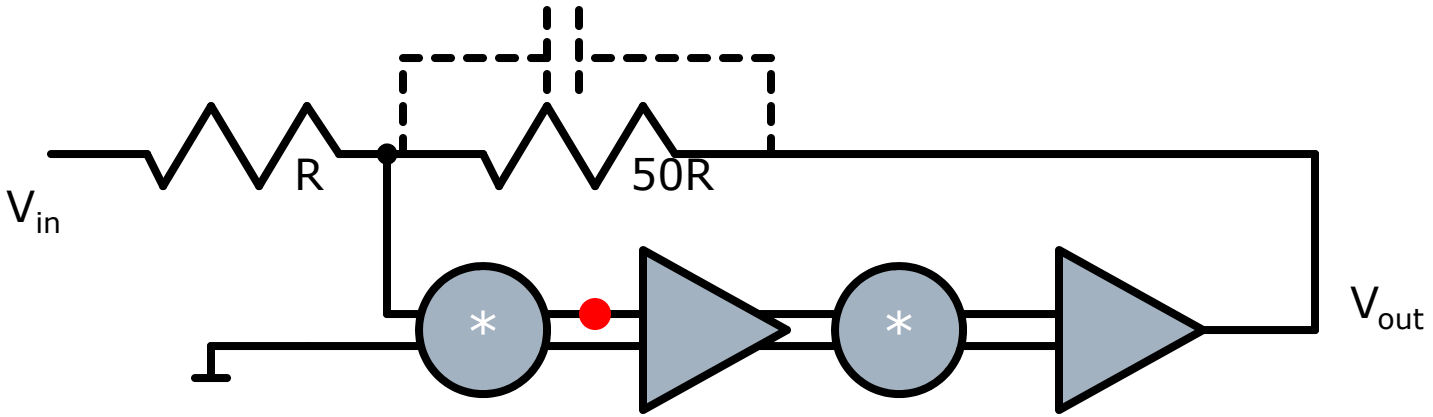
Chop artifacts

- Imagine an opamp in a gain50x configuration
- Vos=5mV, vsignalmax=5mV @10kHz
- 250mV signal @10kHz plus 250mV square wave at 500kHz – the chopper drives the bandwidth, slew rate specs!

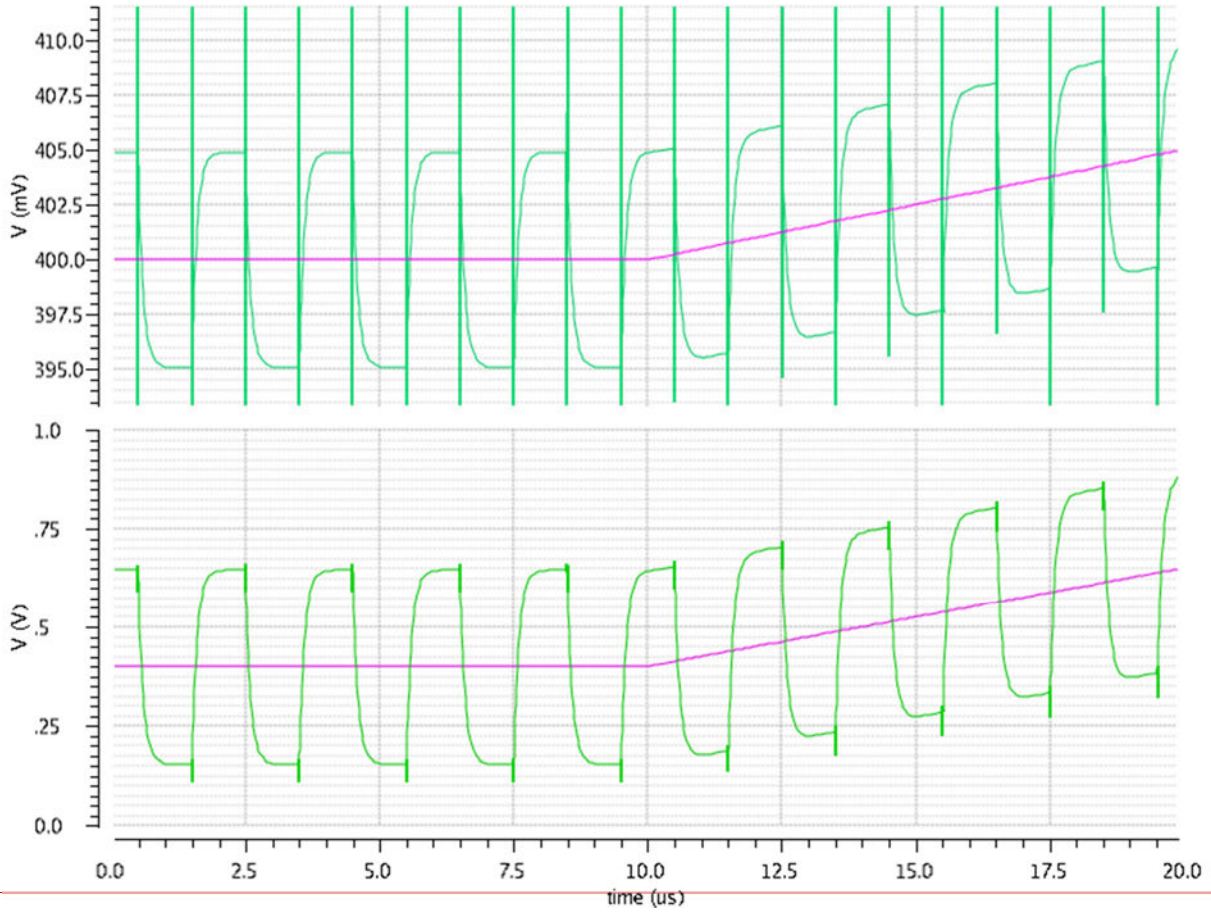


Waveforms of chop artifacts

- Example: offset 5mV, gain of 50

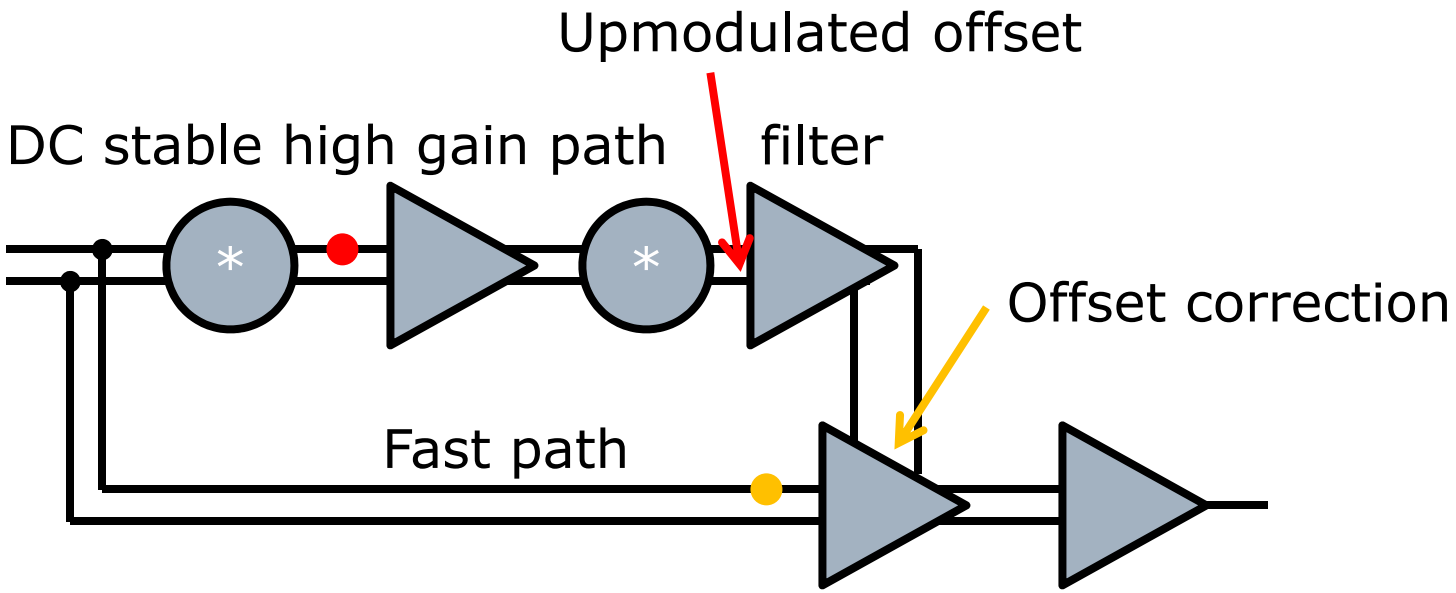
Summing node

output

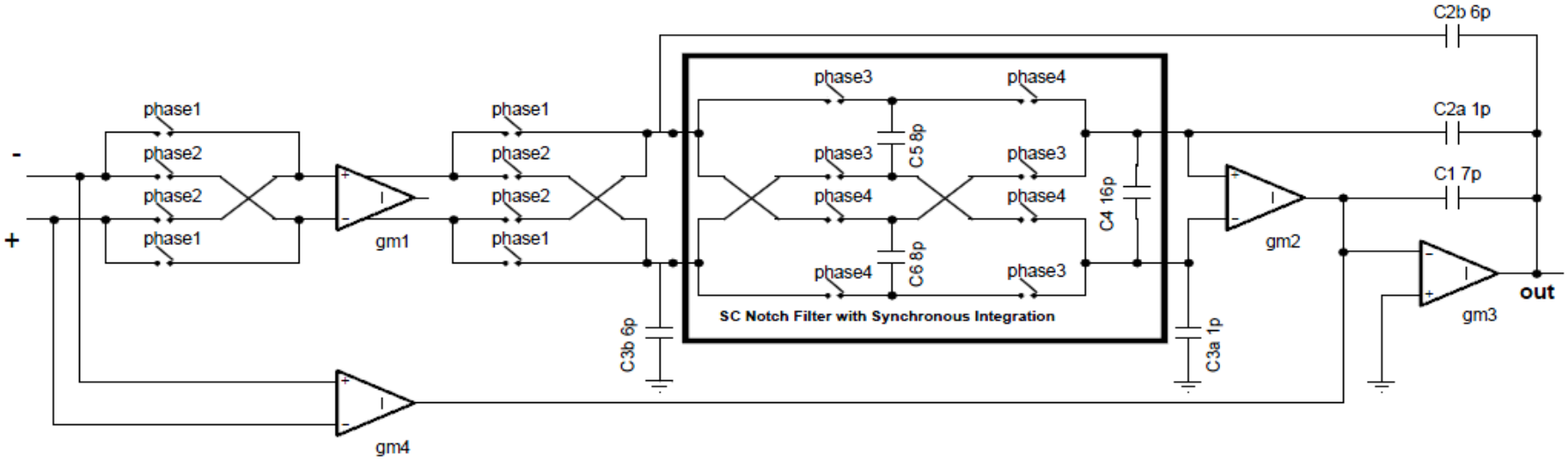


Eliminate the artifacts

- Totally different behavior, square wave is absorbed and summing node acts stable!
- Filter removes upmodulated offset inside the opamp



Removal of the chop artifact



- Notch filter inserted after chopped stage g_{m1}
- Switched capacitor filter is synchronous to chop frequency, so notch is very precise
- Feedforward compensation to maintain stability through g_{m4}

Burt, Zhang, 2006

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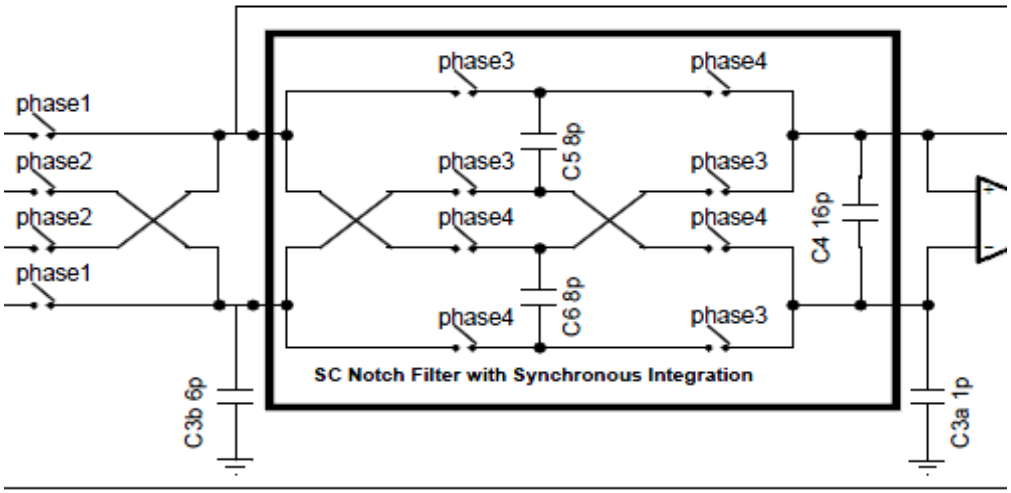
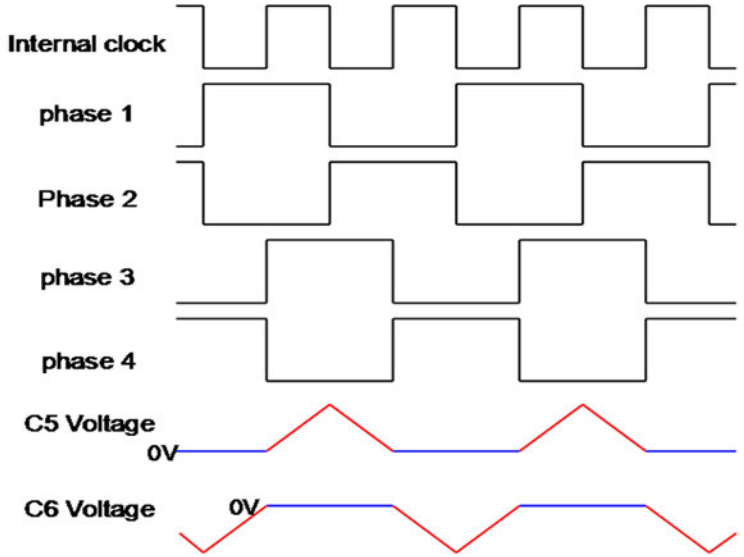
Switched Capacitor Notch Filter





- Phase 3 and 4 are shifted 90^{o} to chop clock
- Integration of two half chop phases on C5 and C6
- Blue waveform drives output stage – no ripple!

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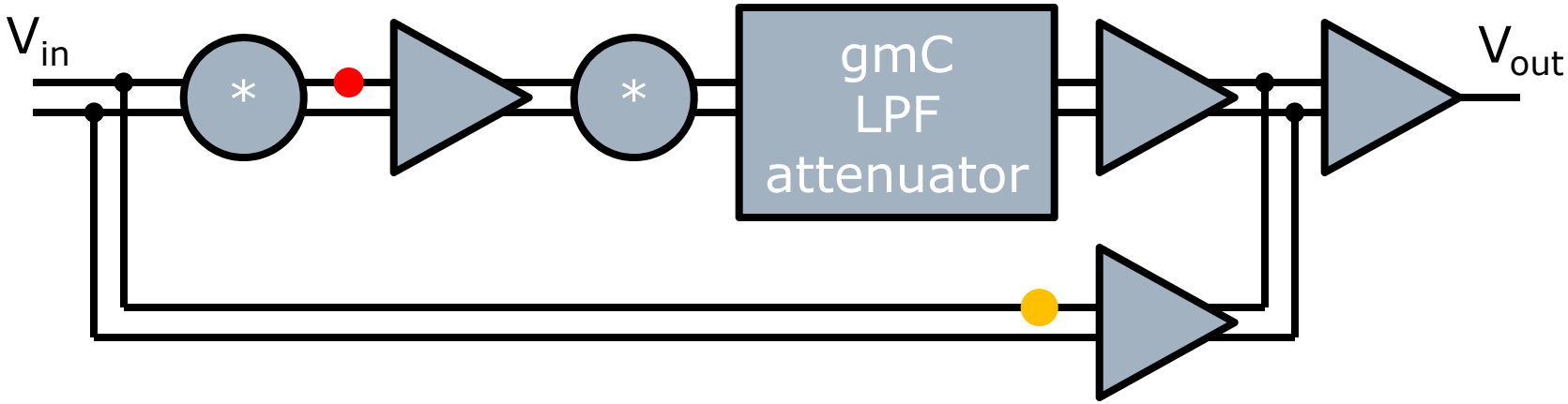
Another implementation

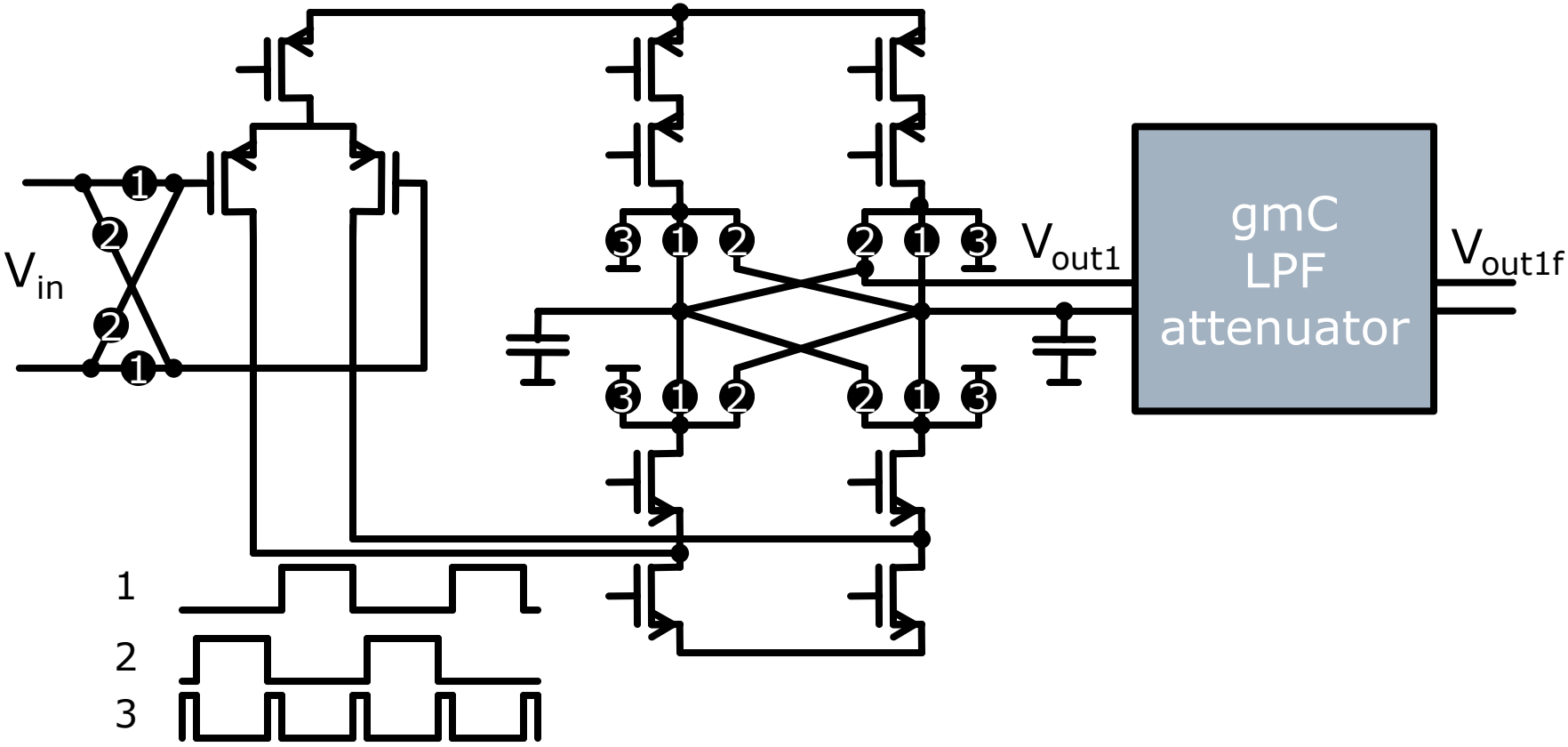


- Similar idea, 1MHz chop frequency, 3 pole 100kHz filter, 1/64 attenuation, removes upmodulated offset by 96dB
- Chop artifacts on output are insignificant

Thomsen, 2000

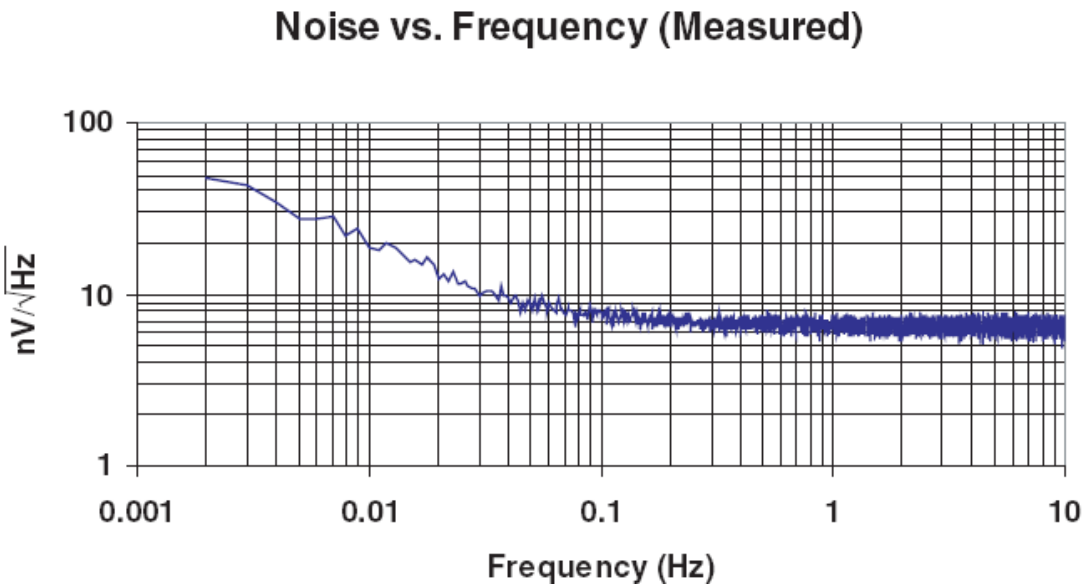
Chopper implementation details

- Current steering at the output



Results for the Cirrus CS3001

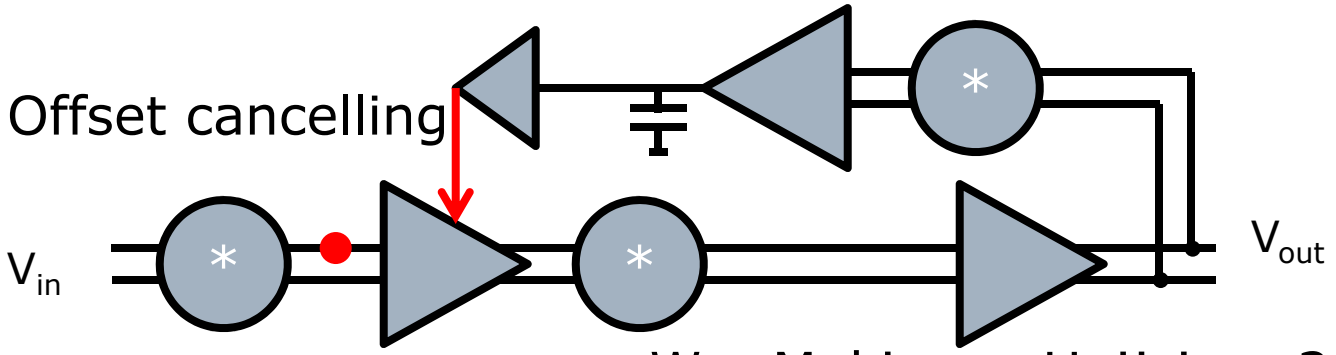
- Low noise in band 6nV/rtHz
- Flicker noise corner 0.05Hz
- Offset <10μV
- Offset drift <50nV/C
- By far exceeds the OP627 example from above



Noise spectrum of CS3001

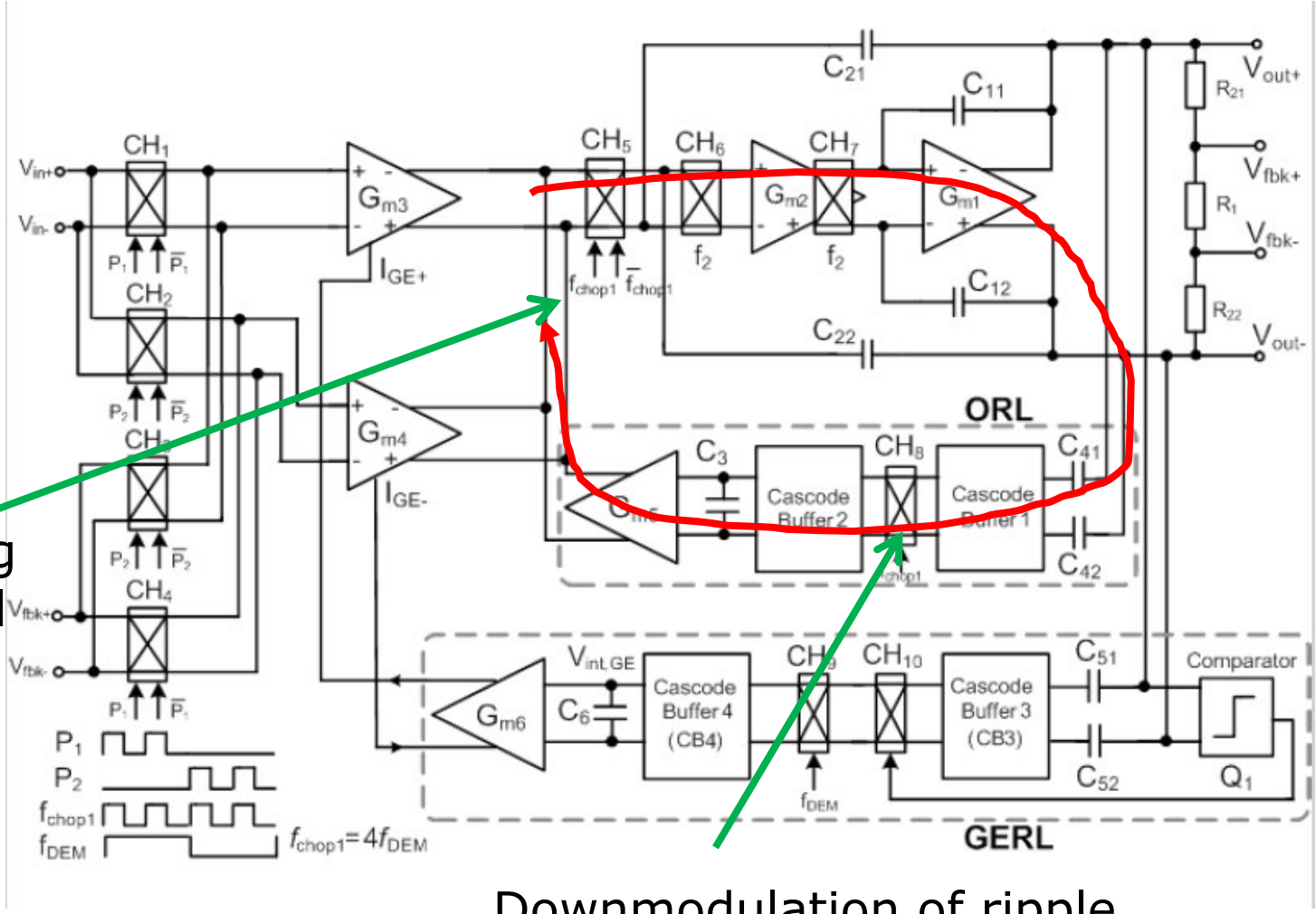
Alternate proposal

- Signal and offset are still separate in frequency
- Detect the presence of ripple at the output of the opamp
- With another modulation step the amplified ripple can be brought to DC.
- Integration of this error can create a cancellation of the offset
- Still a system without sampling, so no significant noise penalty!



Wu, Makinwa, Huijsing, 2009, 2011

Removal of chop artifacts



Noise Analysis: PSS/PNOISE

- Periodic Steady State Analysis followed by PNOISE
  - The simulator finds a repetitive transient waveform (here the chop frequency period)
  - A noise analysis is performed at many timesteps along the way
  - The transfer function and the output noise are calculated as the sum of all these solutions
  - Large signal effects such as modulation and sampling are captured!
  - See cadence Application note in References

Noise Analysis: PSS/PNOISE

- Simulation setup:
  - PSS beat frequency ‘500kHz’, ’10’ harmonics, ‘shooting’ method
  - Pnoise ‘1 to 250kHz’, maximum sidebands ’10’
  - Output node: amplifier output
  - Noise type ‘sources’
  - Input signal grounded for noise measurement

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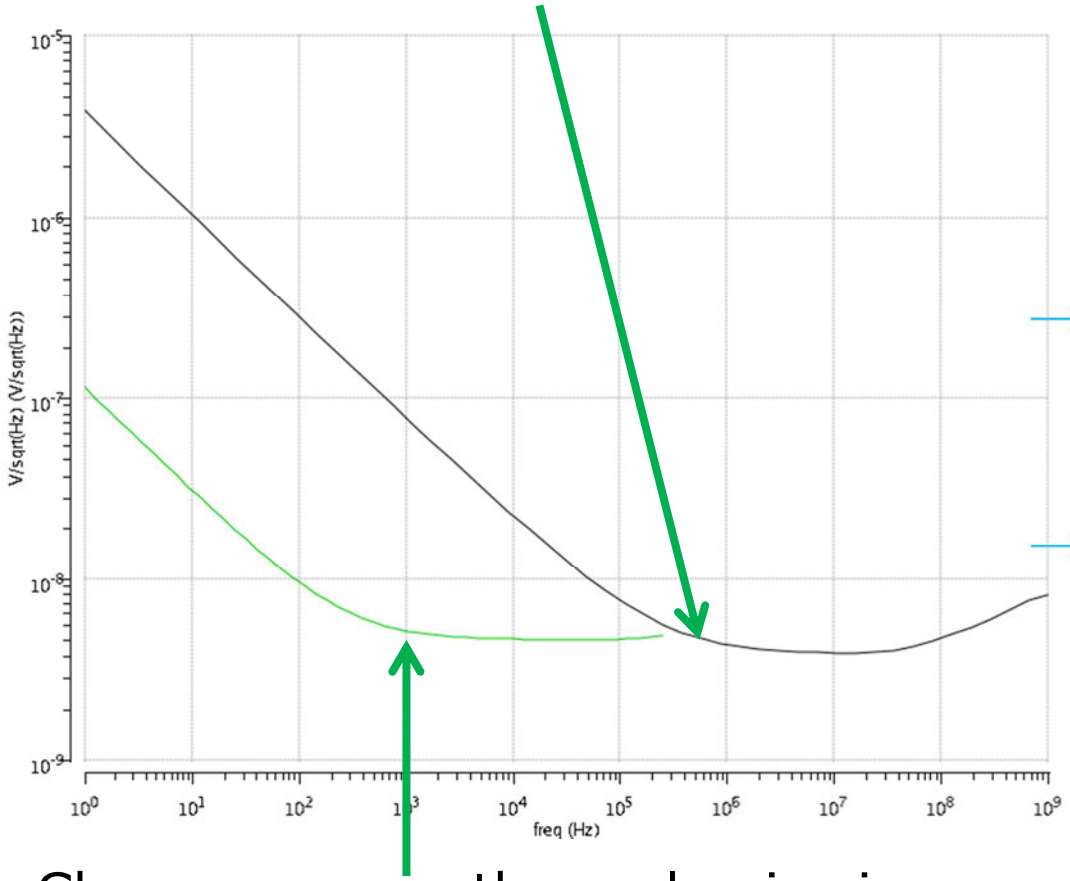
Noise simulation results

Chopper off – noise corner 500kHz



Chopper on: no thermal noise increase

List of noise contributors

No chopping – all flicker noise

Device	Param	Noise Contribution	% Of Total
/M122	fn	1.02594e-08	30.24
/M123	fn	1.02547e-08	30.22
/M125	fn	2.3545e-09	6.94
/M124	fn	2.29332e-09	6.76
/M116	fn	2.18637e-09	6.44
/M117	fn	2.13138e-09	6.28
/M118	fn	1.65962e-09	4.89
/M119	fn	1.64596e-09	4.85
/R48	rn	7.03901e-10	2.07
/M120	fn	8.89083e-11	0.26

chopping – thermal noise

/R48	rn	7.74774e-09	63.17
/M116	id	4.4507e-10	3.63
/M117	id	4.45055e-10	3.63
/M122	id	4.00054e-10	3.26
/M123	id	3.99021e-10	3.25
/M123	fn	3.26811e-10	2.66
/M122	fn	3.26735e-10	2.66
/M124	id	3.13567e-10	2.56
/M125	id	3.13498e-10	2.56
/M117	fn	2.53907e-10	2.07

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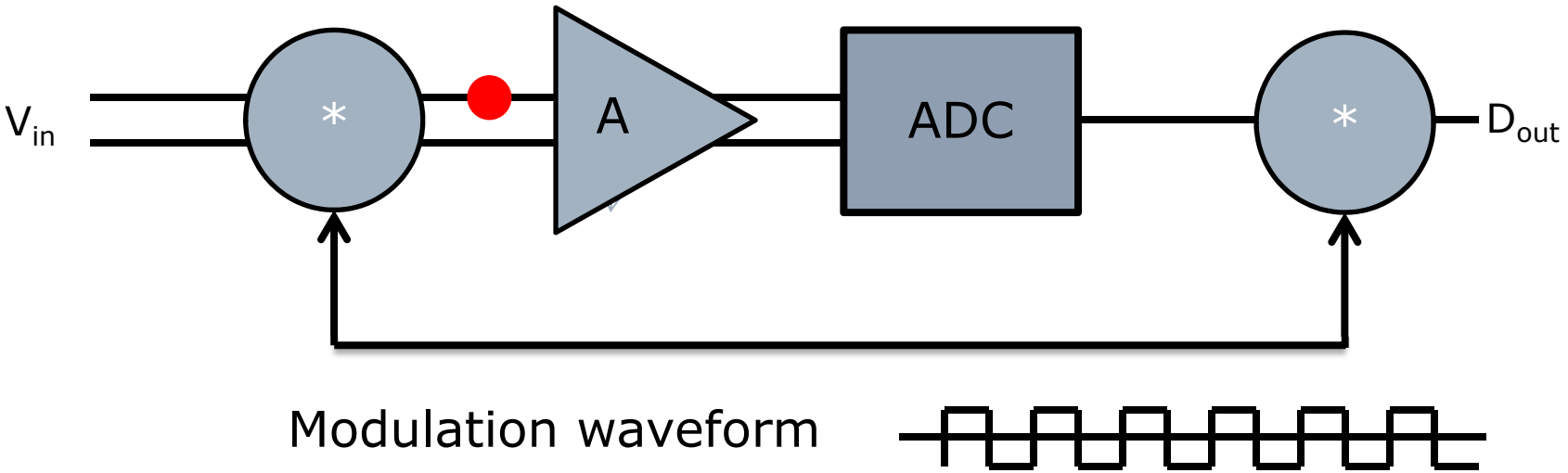
mixed signal implementation?

- The demodulation can happen in the digital domain
- All bandlimiting effects within the chopper are harmful
- Like to use slow chop frequency – effective offset removal, limited 1/f noise removal



Summary

- Chopping can greatly improve offset and 1/f noise through symmetry
- No noise penalty
- In continuous time application, watch or remove the chop artifacts
- Remaining transients limit accuracy
- Low risk in a switched cap application
- Watch out for switched capacitor connections limiting impedance on input and output
- Watch out for sampling/aliasing of a chopped signal – remove artifacts first

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Outline

- Motivation and history
- Offset and flicker noise background
- Techniques to manage offset and flicker noise
  - Chopper Stabilization
    - Basic idea
    - Switched capacitor and continuous time implementations
    - Chop artifacts and their removal
    - Second order effects
  - Autozero
    - Basic idea
    - Implementation examples
    - Second order effects
  - Correlated double sampling
    - An extension of Autozero into switched capacitor circuits
- Conclusion

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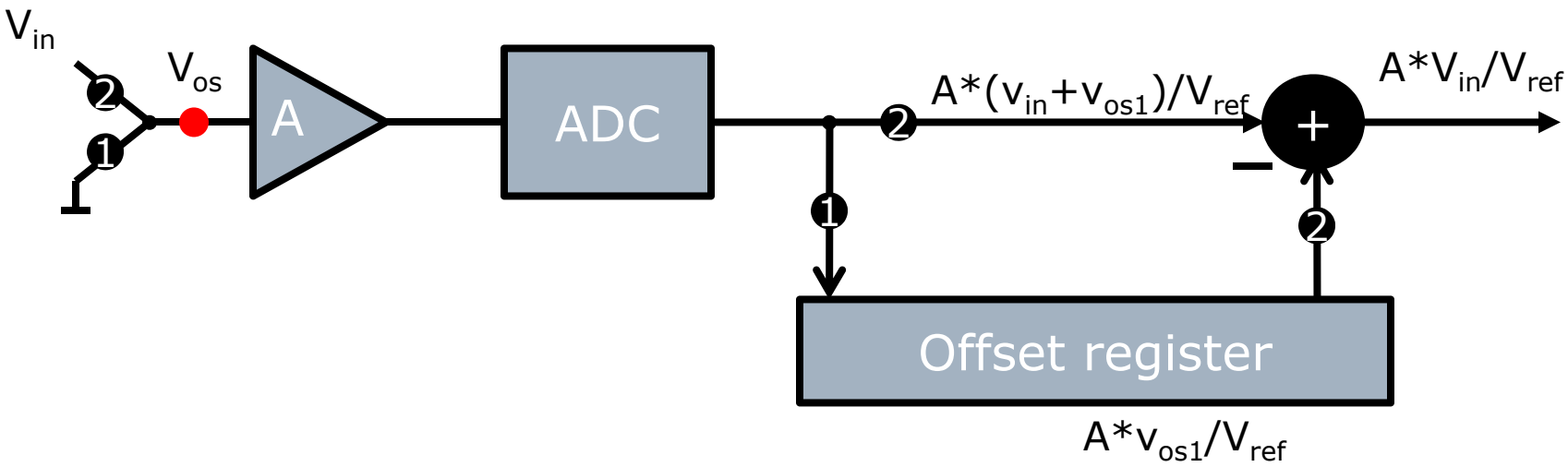
Definition of autozero

- Phase 1: Measure and store offset
  - Circuits are taken 'off line' to calibrate offset
  - Results of calibration are stored digitally or analog

- Phase 2: Measure signal, subtract offset
  - Calibrated circuits used for measurement
  - A means to subtract has to be provided – digitally or analog

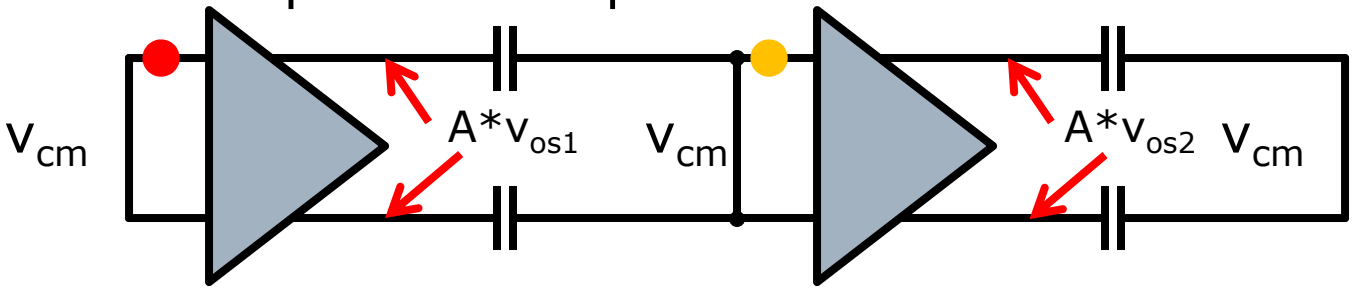
Autozero ADC example

- Short the input to ground
- Take a measurement of the error and store it
- Measure the input
- Subtract the offset – result is offset corrected

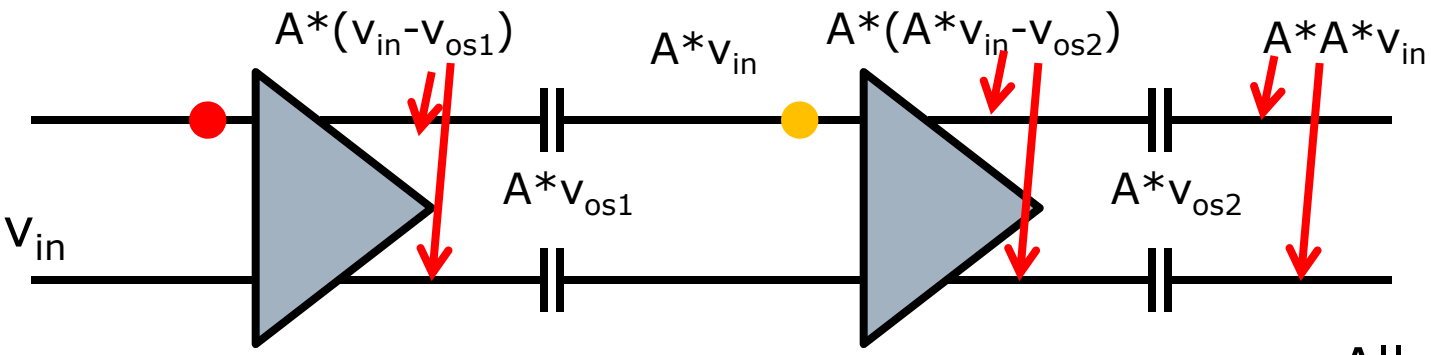


low gain comparator example

- Low gain = gain * offset within output dynamic range
- Auto zero phase: Sample and store error



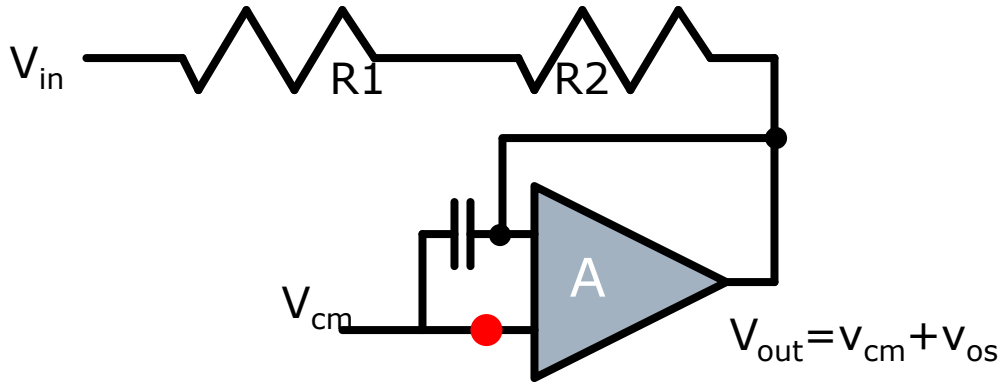
- Operation phase: Amplify signal , subtract error



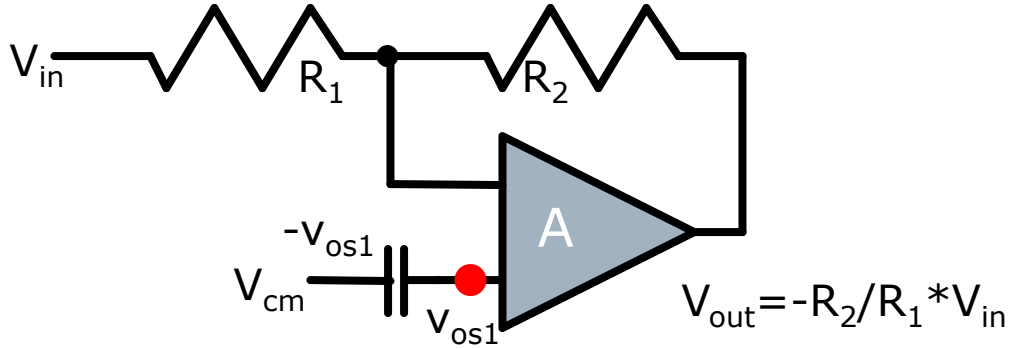
see Allen/Holberg

high gain opamp example

- High gain – residual error V_{os}/A is small enough
- Auto zero phase – sample and store offset



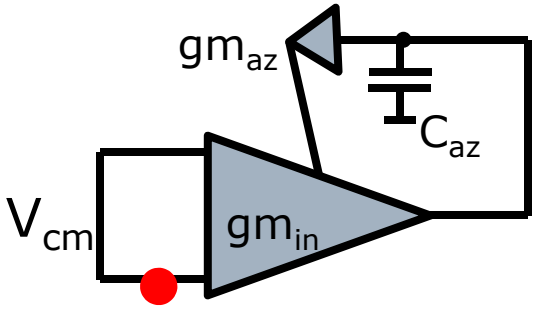
- Operation phase: Amplify signal , subtract error



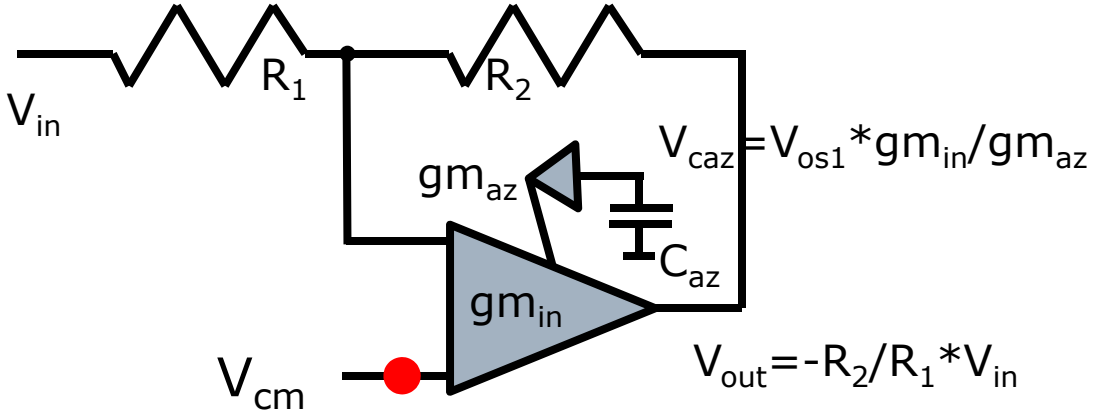
see Allen/Holberg

Another opamp example

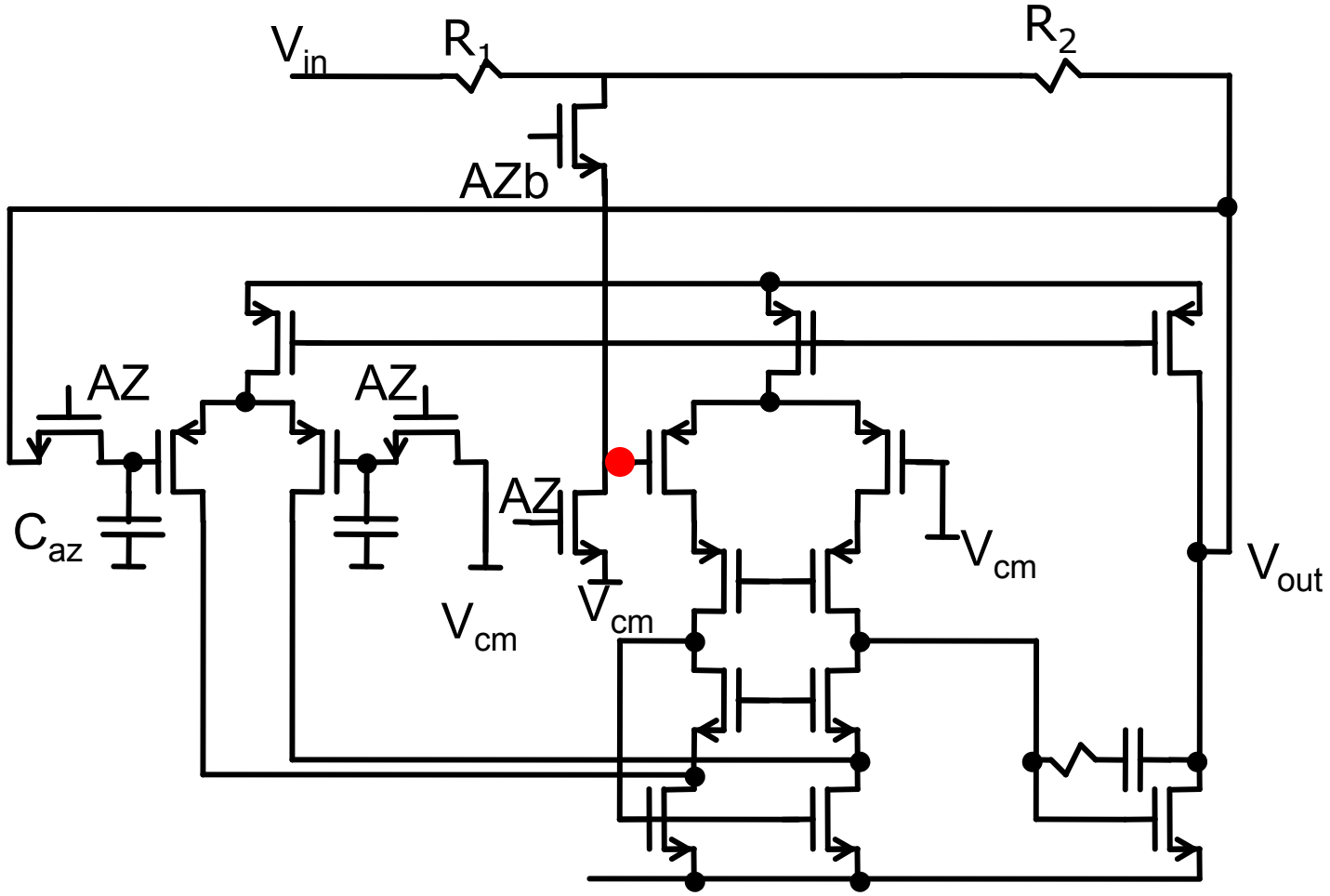
- Autozero phase: measure the offset and store it



- Operation phase: amplify signal and subtract offset

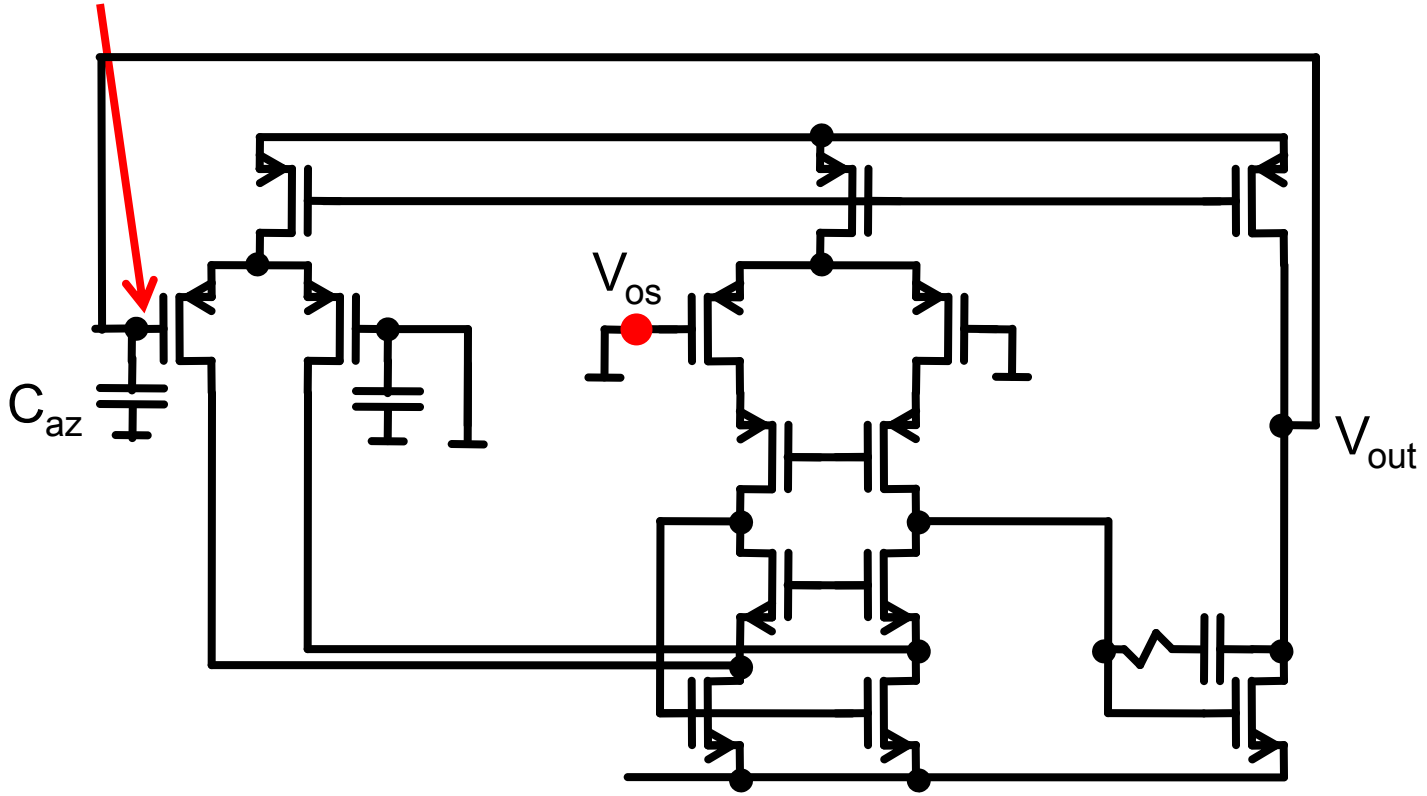


Transistor level example

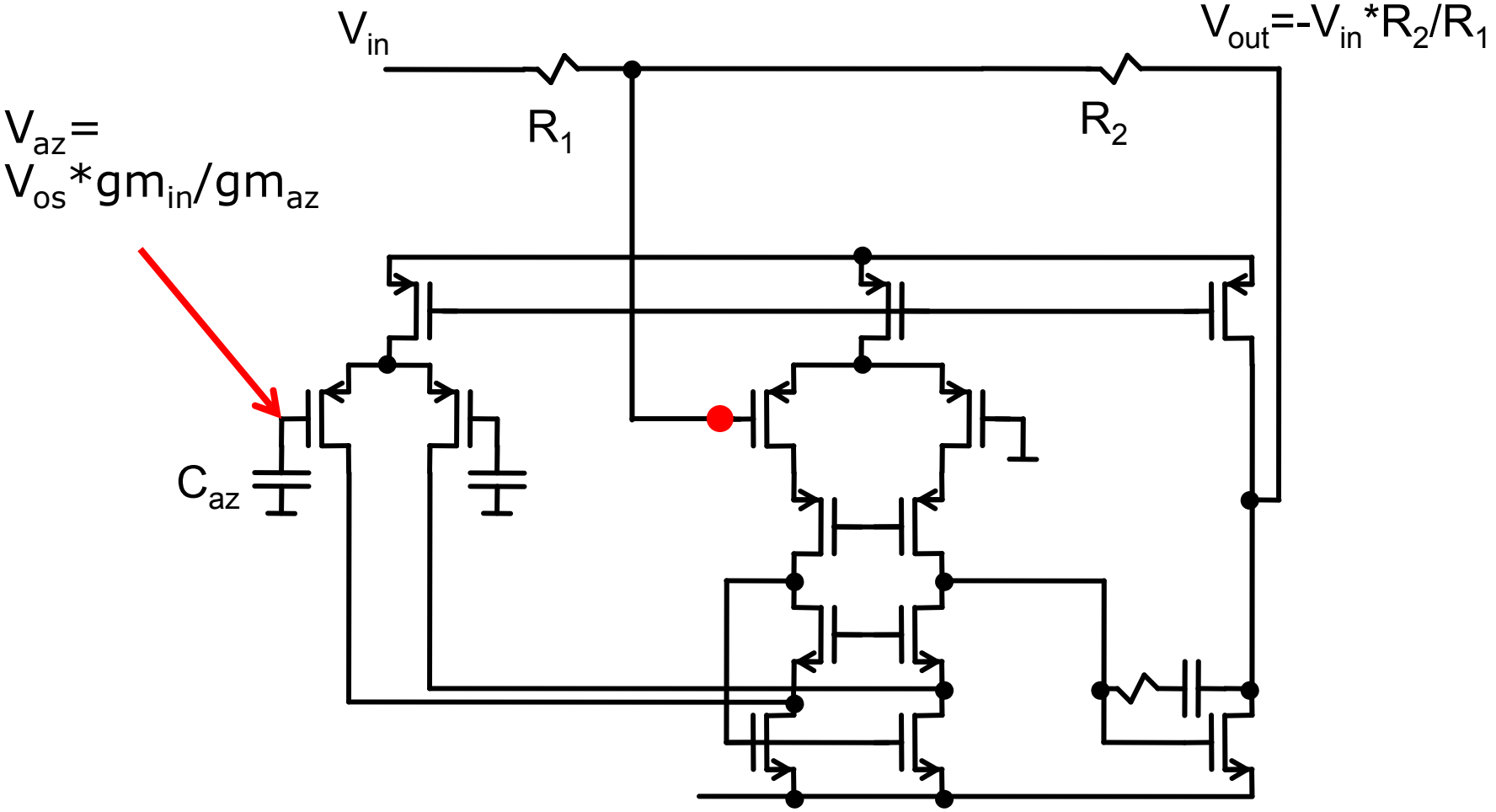


autozero phase

$V_{az}=V_{os}*gm_{in}/gm_{az}$



operation phase

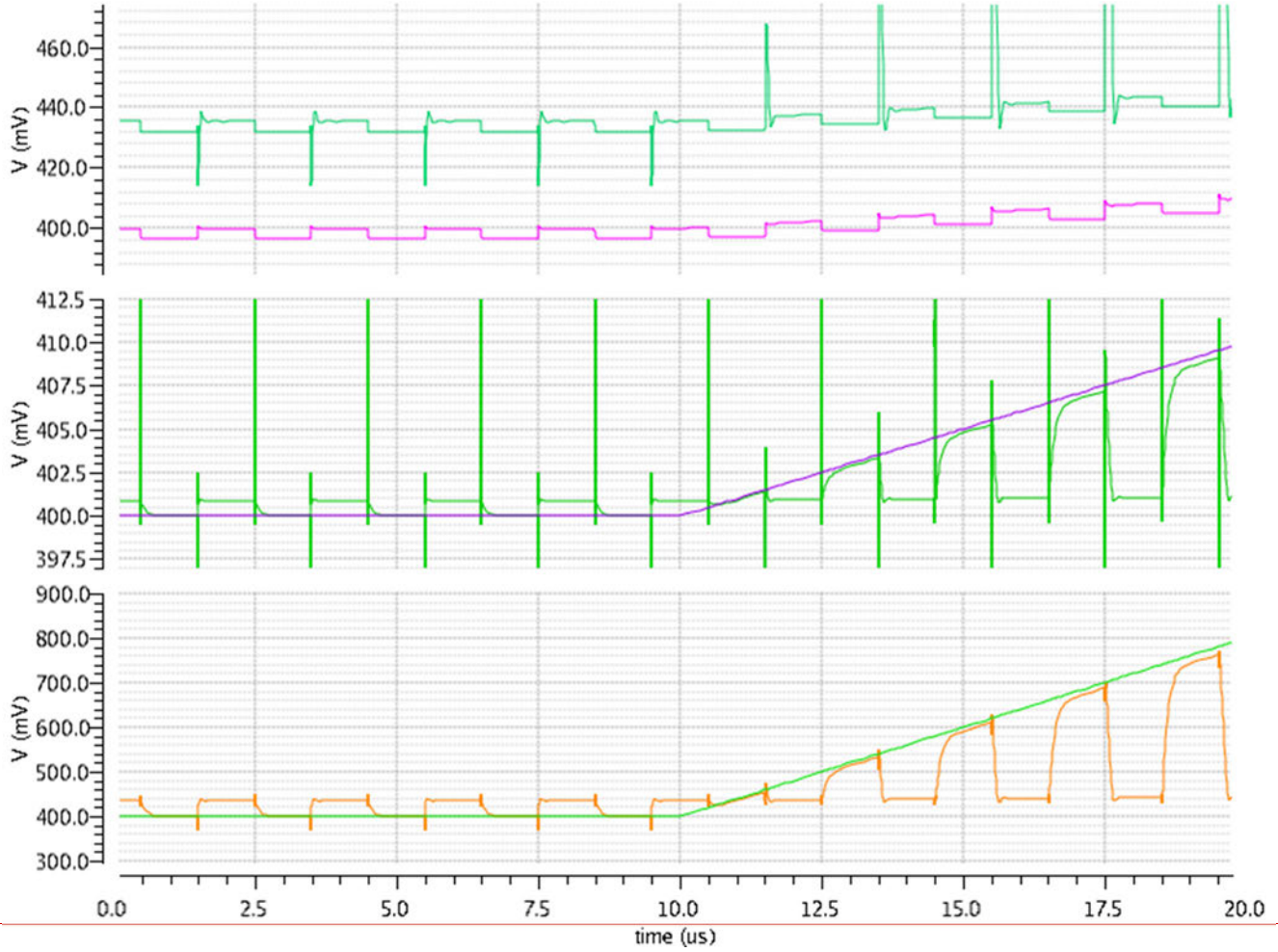


Waveforms

Autozero nodes

input nodes

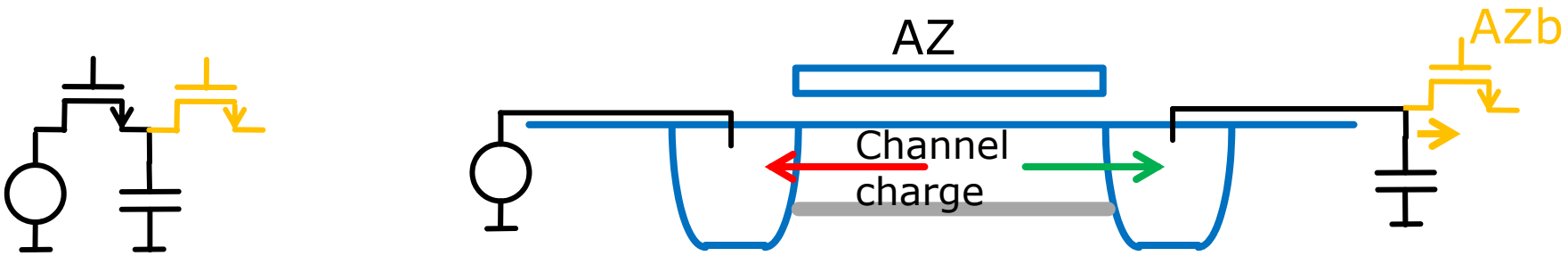
output node and ideal



Error sources

- Noise penalty - Stored offset has noise, signal measurement has noise. Increases noise voltage by 3dB
- Autozero phase ≠ Operating phase. Switches are in different positions, different currents flow, different glitches may be present. Careful design required.
- Storage error – digital storage is perfect, Analog storage has errors. Clock feedthrough, charge injection, leakage. Differential implementation helps a lot.

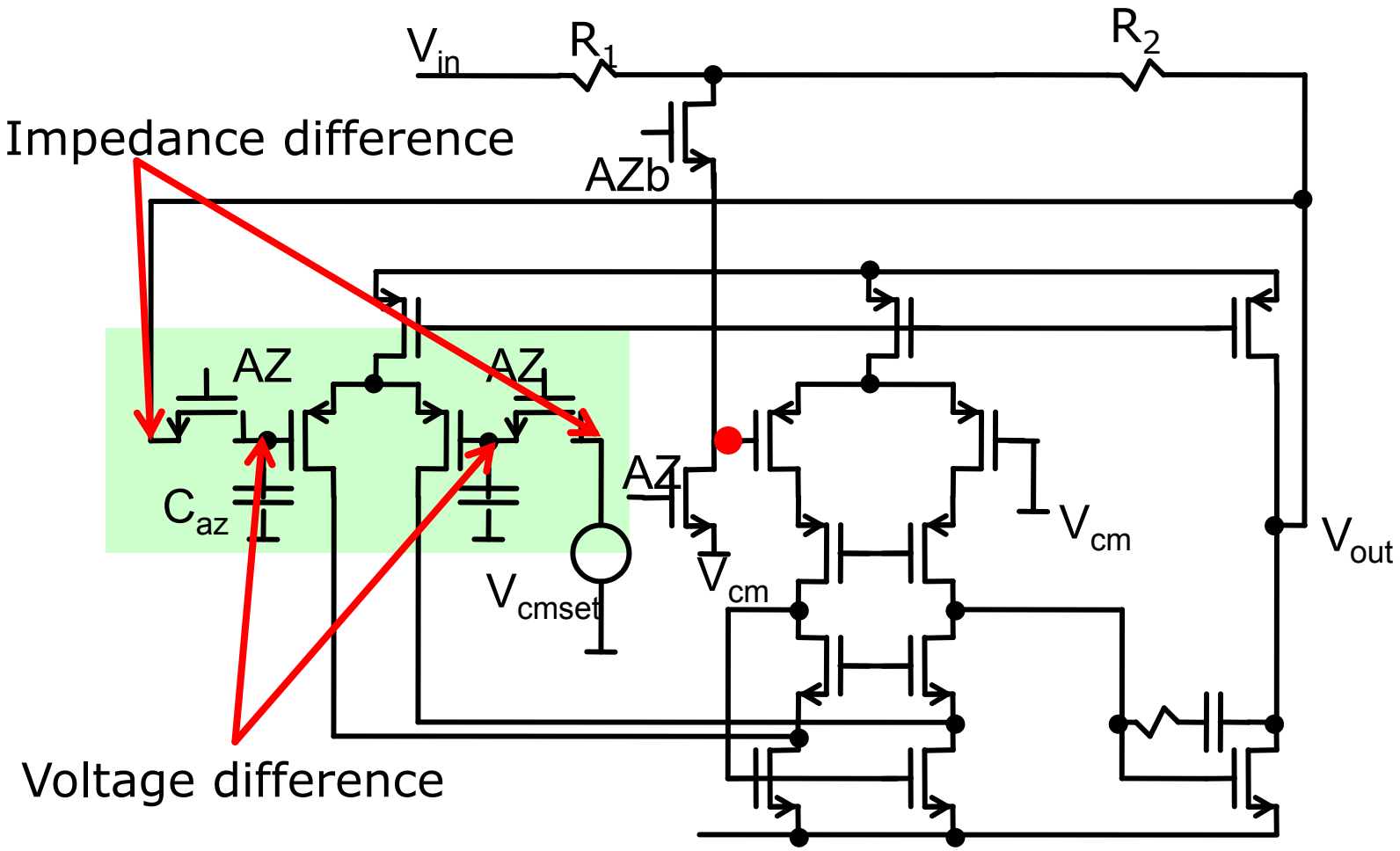
Charge Injection



- Channel charge depends on the gate to channel voltage
- Charge distribution depends on the impedance seen
- Charge injection onto the cap can ruin the accuracy of the auto zero operation
- Differential operation recommended
- Cancellation techniques are known but are not very robust – see orange transistor

Eichenburger, Guggenbuhl, 1990

Charge Injection

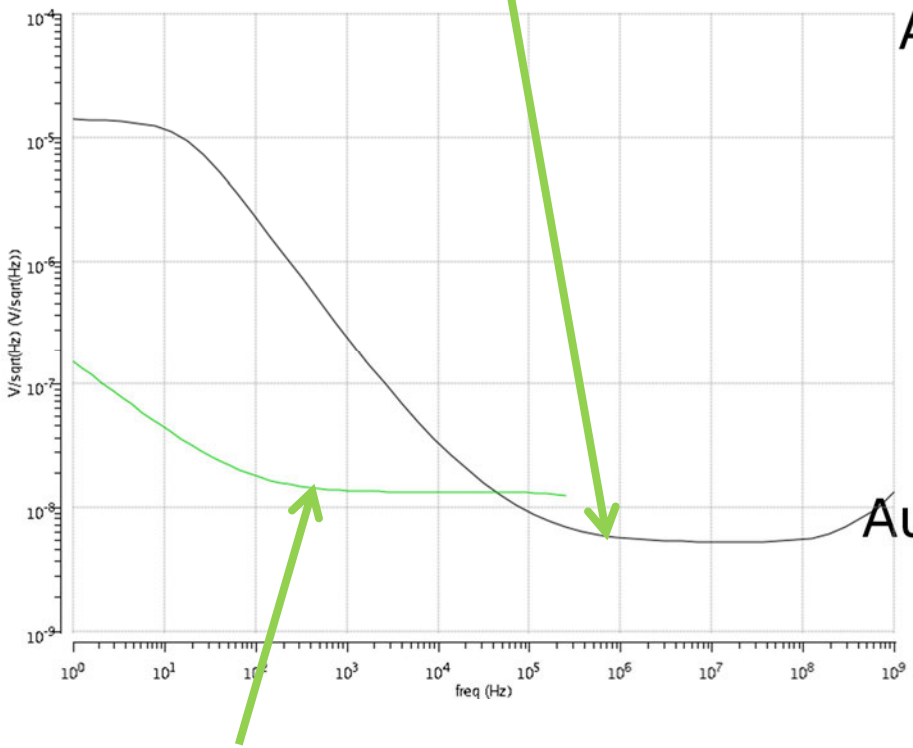


Noise analysis: PSS/PNOISE

- PSS settings
  - Fundamental frequency 500kHz (autozero clock)
  - Harmonics 10 (it pays to vary this, to find sensitivity)
    - Look at the noise spectrum that is sampled, this will indicate where the significant noise is
  - Shooting technique
- PNOISE settings
  - Fundamental frequency 500kHz (autozero clock)
  - Sidebands 10 (similar to harmonics)
  - Look at noise spectrum
  - Look at noise report
    - Integrated noise in the band of interest
    - See that noise contributors are those that you would expect!
- Input grounded, Noise observed at amplifier output

Results of PSS analysis

AZ off: noise corner 500kHz



AZ on: Elevated thermal noise

List of noise contributors

Autozero disabled – flicker noise

Device	Param	Noise Contribution	% Of Total
/M186	fn	3.03006e-09	6.24
/M184	fn	2.95966e-09	6.10
/M193	fn	5.29306e-10	1.09
/M188	fn	5.1566e-10	1.06
/M180	fn	5.14673e-10	1.06
/M189	fn	2.72912e-10	0.56
/M191	fn	2.7031e-10	0.56
/M192	fn	2.46558e-10	0.51
/M187	fn	2.28352e-10	0.47
/M179	fn	6.82412e-11	0.14

Autozero enabled – thermal noise

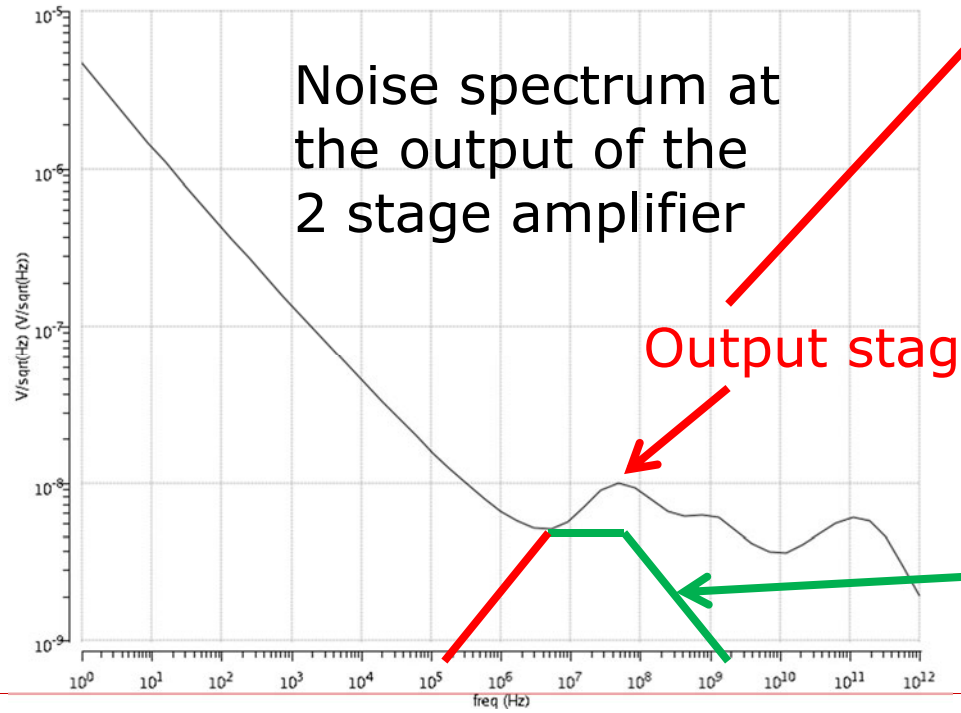
Device	Param	Noise Contribution	% Of Total
/R50	rn	1.33245e-11	6.96
/M189	id	1.06653e-11	5.57
/M191	id	1.03514e-11	5.41
/M184	id	9.74716e-12	5.09
/M186	id	9.2109e-12	4.81
/M157	id	8.92213e-12	4.66
/M161	id	8.65251e-12	4.52
/M68	fn	8.24145e-12	4.31
/M156	id	8.19282e-12	4.28
/M154	id	7.67705e-12	4.01

Autozero considerations

- Requires a reset phase – no processing of the signal part of the time
- Additional circuitry – noise penalty from extra diffpair, noise on cap
  - Minimize g_m of offset cancellation circuits to reduce its extra noise
- Sampling of offset can trap additional noise

Autozero considerations

- Careful - Multistage amplifier will add extra noise to sampled offset
- Use NOISE, PSS and PNOISE analyses to understand the noise impact!



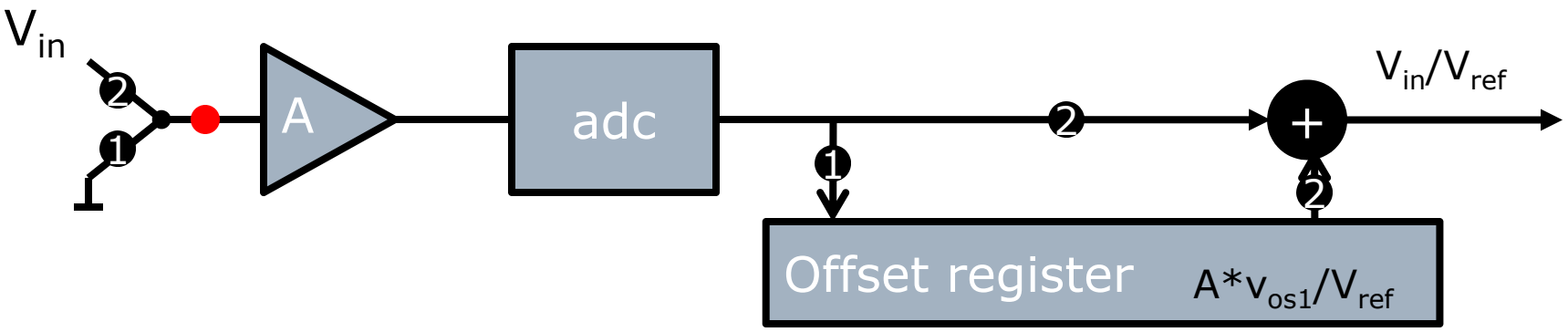
/R47	in	7.21348e-09	68.46
/M152	id	1.49422e-09	14.18
/M153	rgbi	3.91976e-10	3.72
/M64	id	2.61017e-10	2.48
/M153	id	2.00075e-10	1.90
/M152	rgbi	1.8992e-10	1.80
/M162	id	1.37854e-10	1.31
/M161	id	1.08258e-10	1.03
/M157	id	7.48798e-11	0.71
/M163	id	6.75291e-11	0.64

Output stage contribution – dominates!

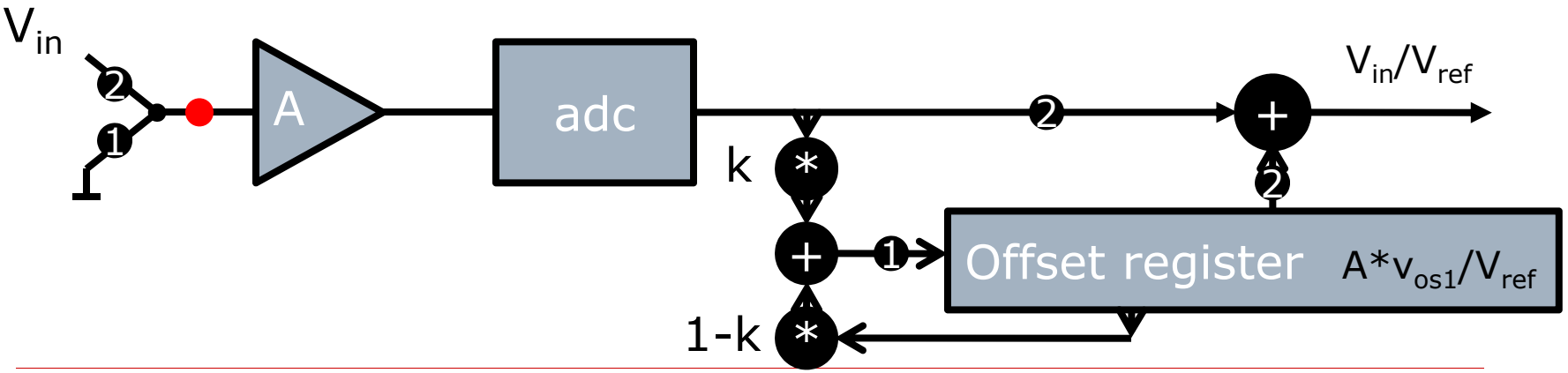
Input stage noise floor

Reducing autozero noise

Case 1: sample offset, sample signal, subtract – noise penalty 3dB

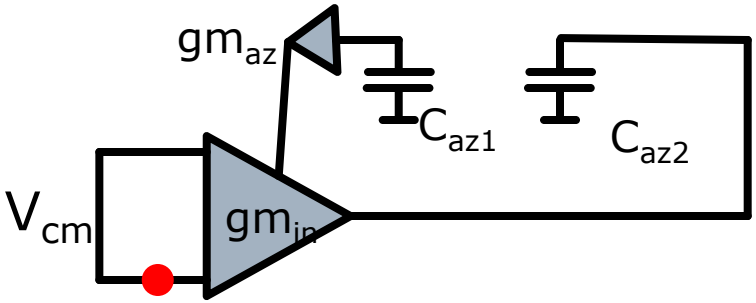


Case 2: sample offset, integrate/average with previous samples sample signal, subtract – noise penalty reduced, bandwidth reduced

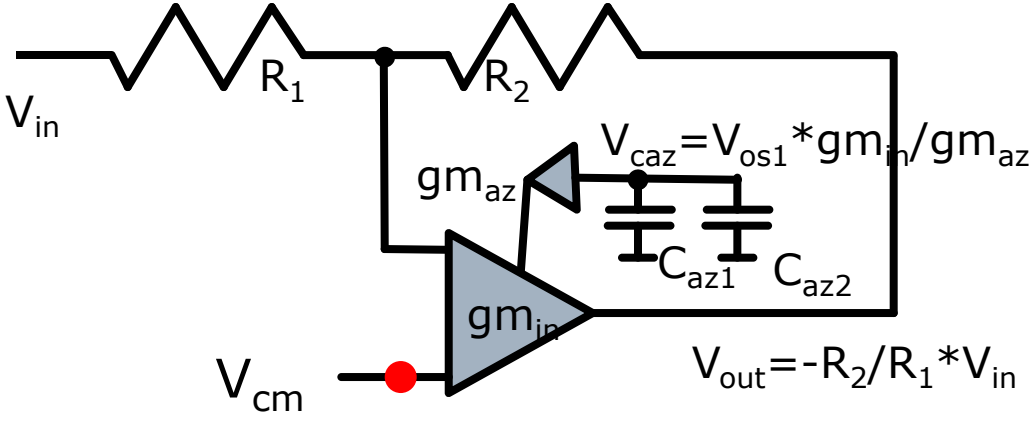


Analog implementation

- Autozero phase: measure the offset and store it



- Operation phase: amplify signal and subtract offset

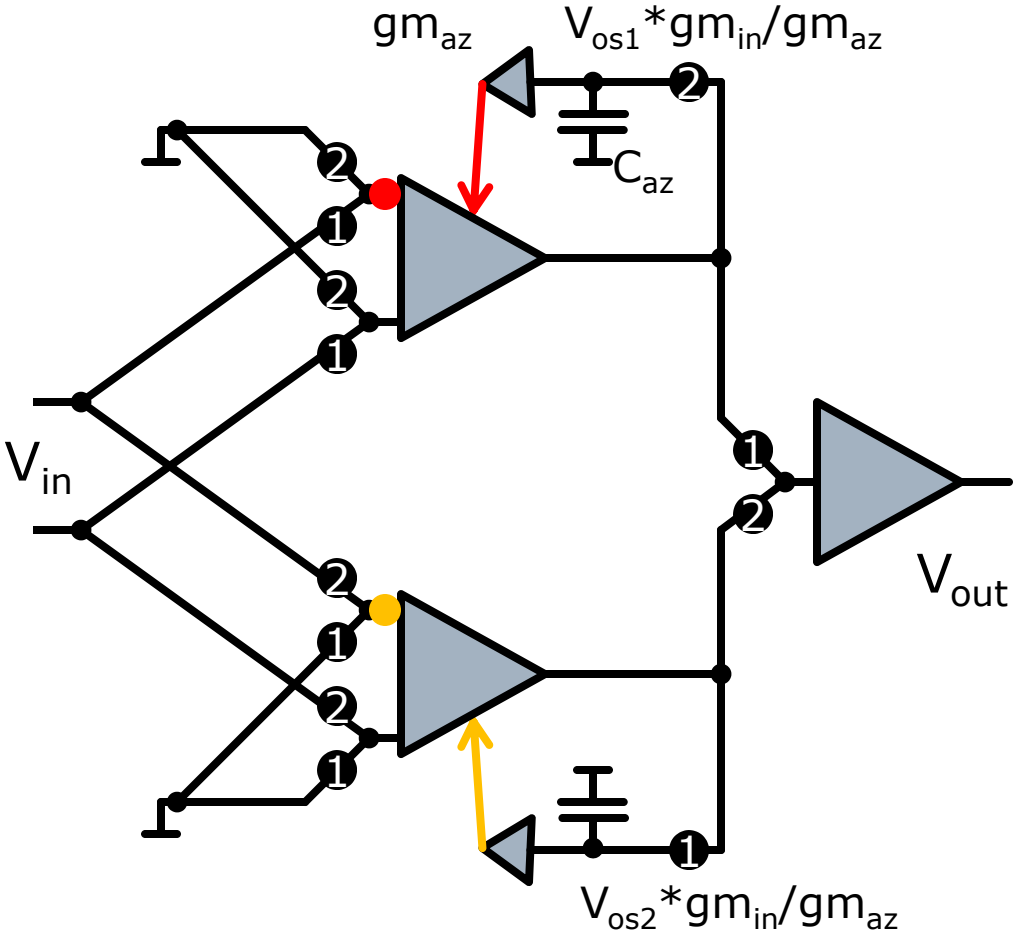


Caz1>>Caz2
Implementing a low pass filter (leaky integrator)

Reduced bandwidth and noise

- Don’t measure instantaneous offset, but average the most recent offset measurements.
- Reduces the cancellation bandwidth
- Reduces the noise – can make it a much less significant noise source
  - No averaging 3dB noise penalty
  - 4 times averaging, 1dB noise penalty
  - 32 times averaging 0.1dB noise penalty
  - …unless we are starting to lose flicker noise cancellation.

AZ in a continous time opamp 1



- Autozero 'reset time limitation' overcome by ping pong mode of two stages
- No chop artifacts, but glitches at switch-over
- Noise disadvantage – due to gm_{az} and C_{az}
- Twice the input stage power

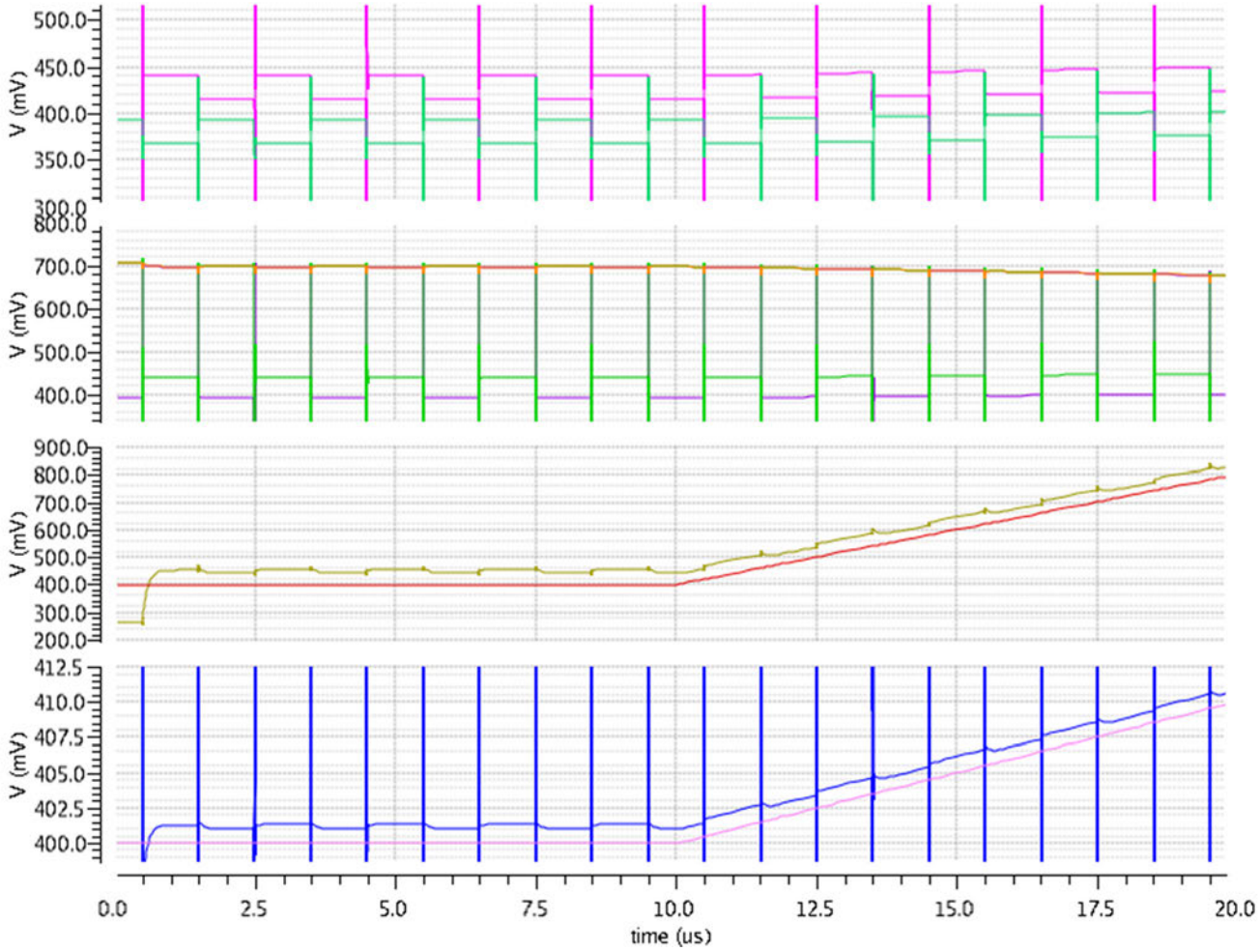
Waveforms

Az nodes

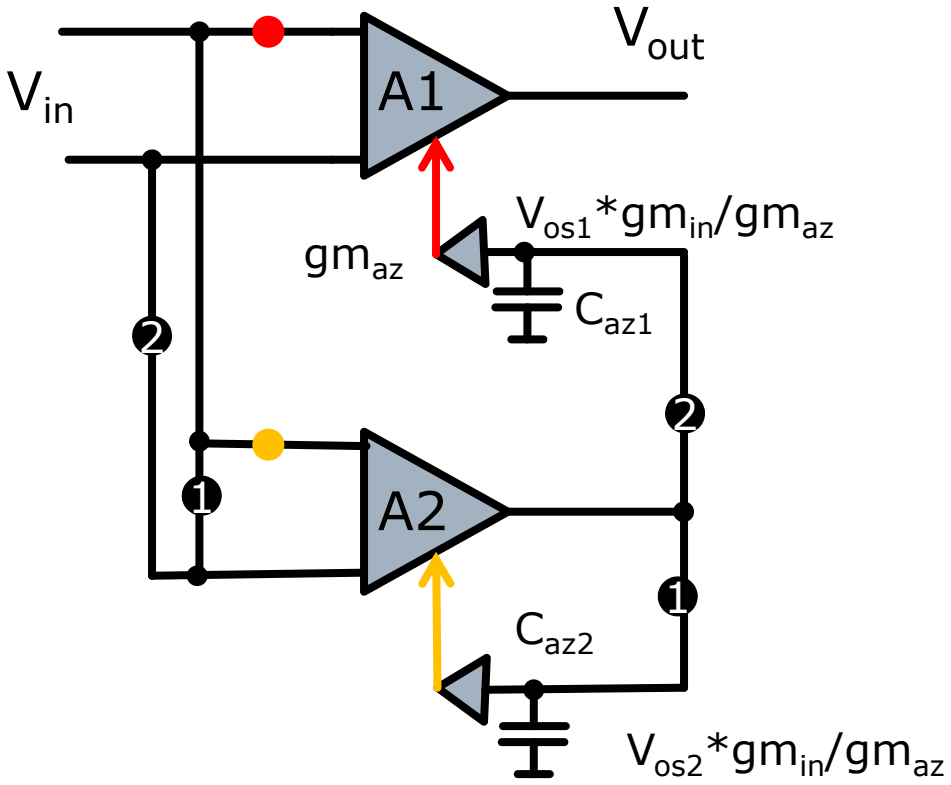
Output first stage

Output second stage

summing node



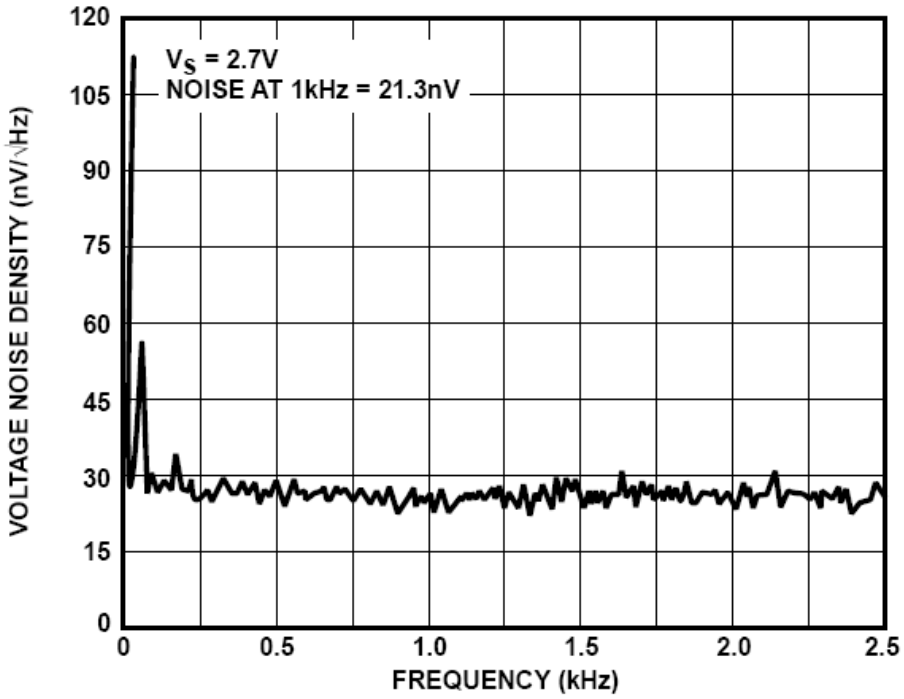
AZ in a continous time opamp 2



- Autozero 'reset time limitation' overcome by sample and hold of auto-zero voltage
- Phase 1 samples offset of A2 on C_{az2}
- Phase 2 refreshes A1 offset stored on C_{az1}

Performance data AZ-opamp

- ADI AD8628
- Offset <1μV
- Offset drift 2nV/C
- Noise floor 22nV/sqrtHz



Autozero summary

- Sampled system
- Sampling has noise and aliasing issues
- Devices are taken ‘offline’ to calibrate – amplifier is not continuously available
- Storage of offset required
- Storage is perfect in digital
- Analog storage is imperfect. Charge injection is the biggest issue, modern processes also present leakage challenges

Outline

- Motivation and history
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- Techniques to manage offset and flicker noise
  - Chopper Stabilization
    - Basic idea
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    - Chop artifacts and their removal
    - Second order effects
  - Autozero
    - Basic idea
    - Implementation examples
    - Second order effects
  - Correlated double sampling
    - An extension of Autozero into switched capacitor circuits
- Conclusion

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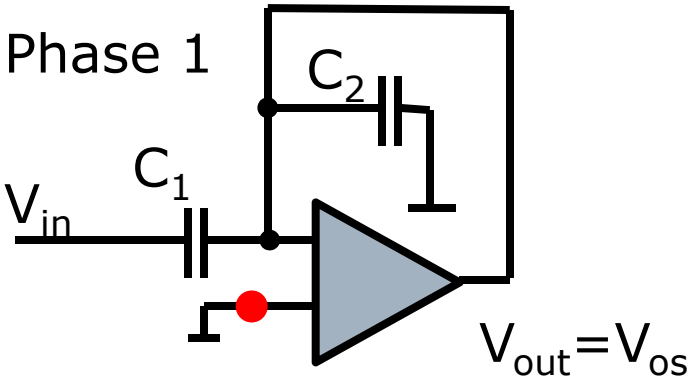
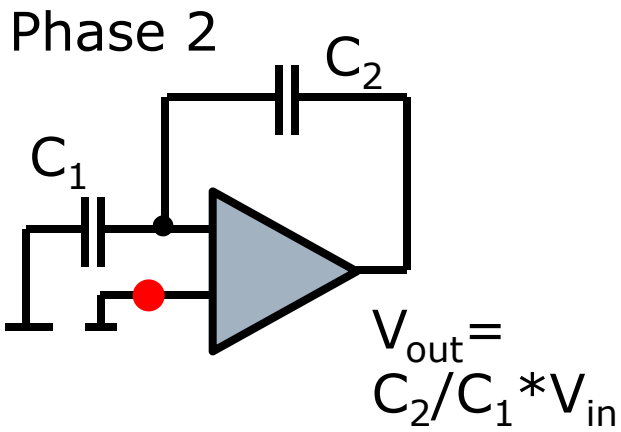
Correlated Double Sampling

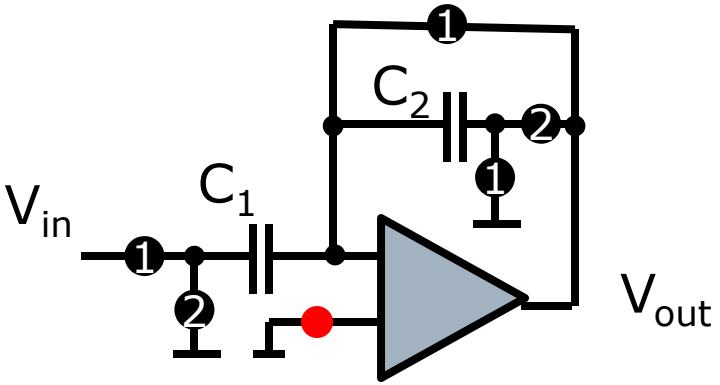
- Switched capacitor Sampling systems
- Extension of Autozero technique into the world of switched capacitors
- Capacitors are already present, introduce switch phasing to take advantage and store offset voltage
- Take advantage of finite gain error storage

Offset compensated SC amplifier



- Phase 1 similar to autozero – stores offset on the caps
- C_1 and C_2 serve both as offset storage and gain elements
- Inverting input always sits at V_{os}





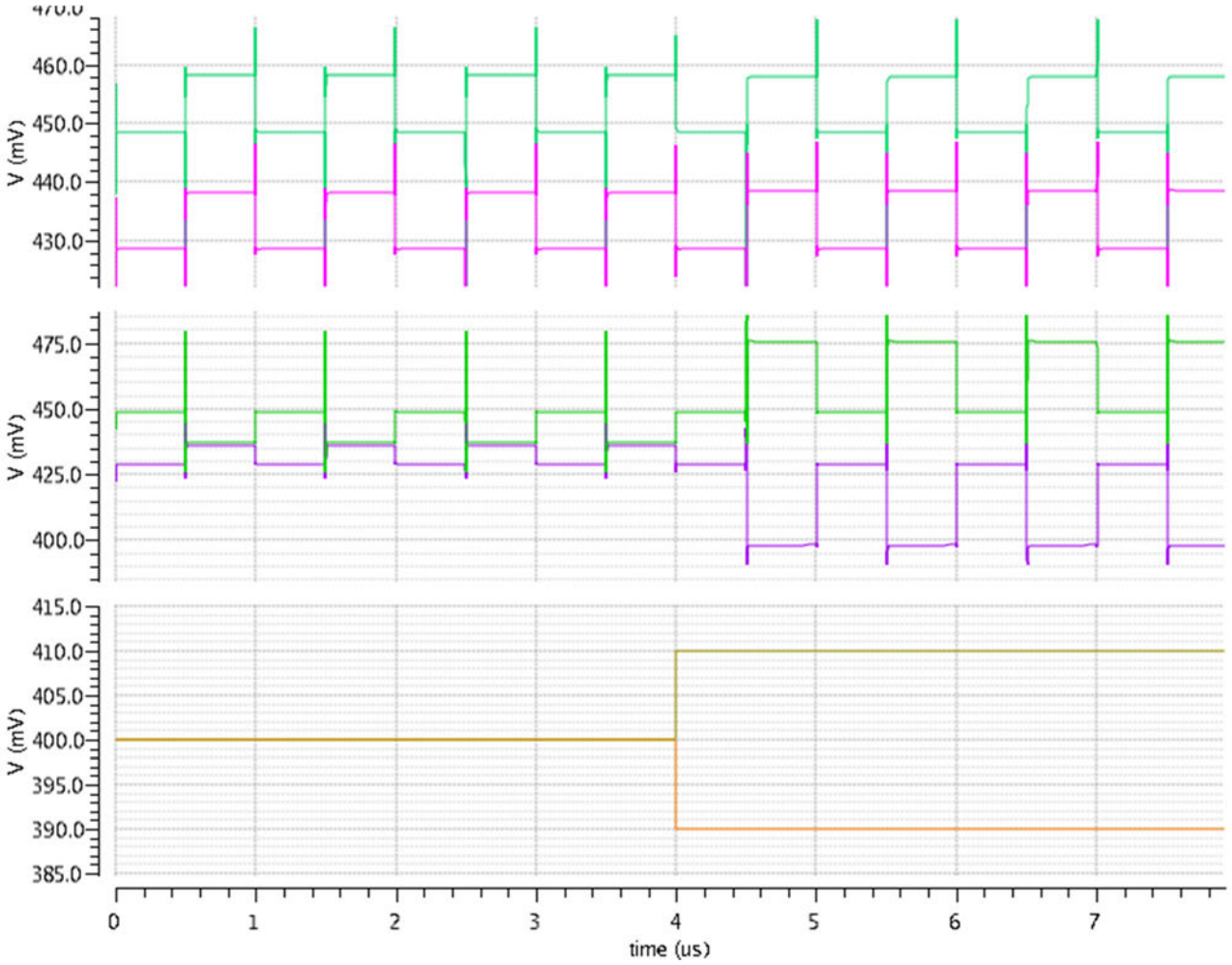
Gregorian, 1981

Waveforms

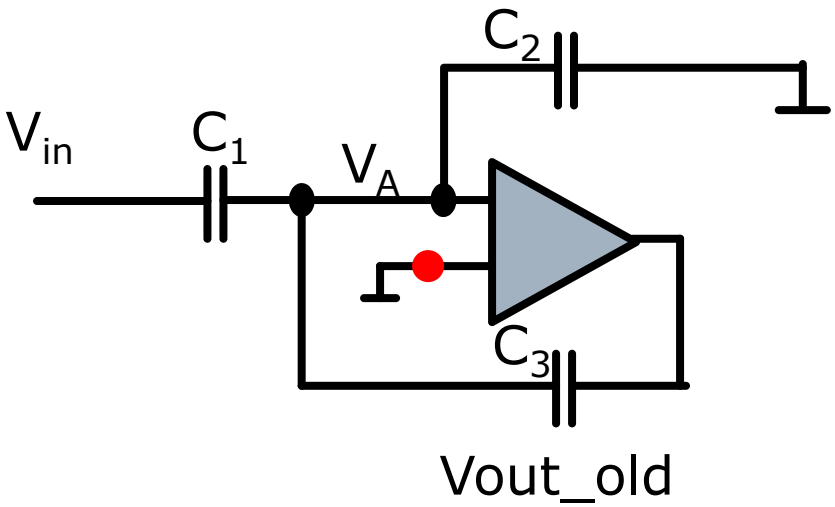
Summing node

Opamp output

Input node

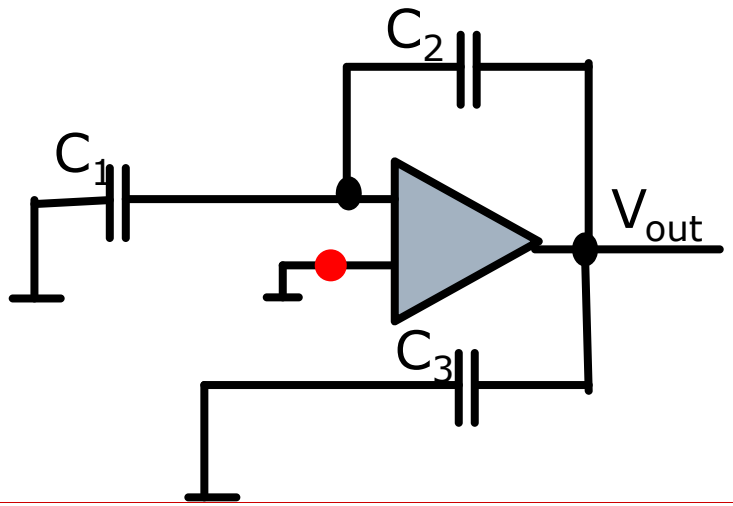


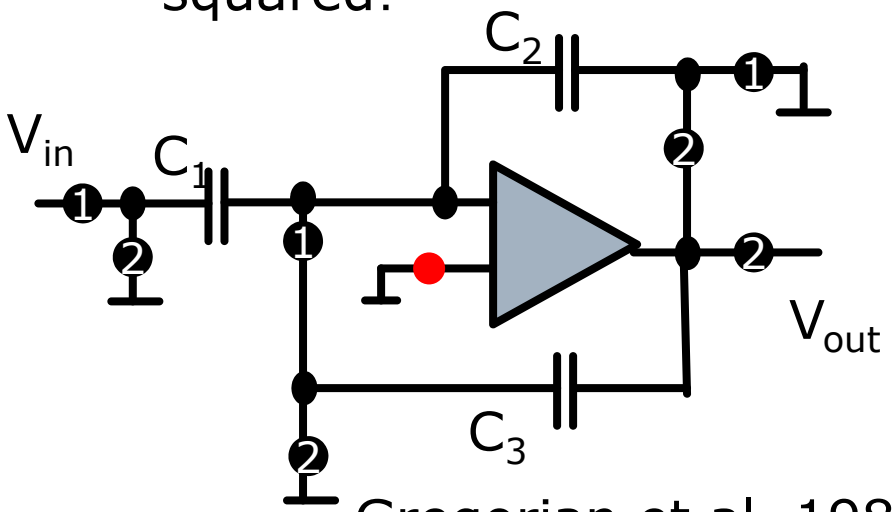
CDS for gain error correction



Vout_old

- The addition of capacitor C_3 keeps the output of the opamp at $V_{out\_old}+V_A$
- $V_A=V_{os}+V_{out\_old}/A$ where A is the gain of the opamp
- Acts like we have gain squared!





Gregorian et al, 1984

Error sources in CDS

- Charge injection – fully differential implementations are preferred
- Sometimes a noise penalty – little noise penalty in first example, noise penalty for storing charge on C3
- Ability to take out gain error related problems if V_{out} does not change much from cycle to cycle.

CDS summary

- Look for opportunities to store offset on exiting capacitors in switched capacitor circuits
- Taking the Autozero idea and applying it in circuits that already have capacitive charge transfer.
- Ability to store and subtract gain error related offset voltage can be added – very attractive in modern technologies where gain is hard to come by.

Comparison

Chopper Stabilization	Autozero	Correlated double sampling
Modulation, no sampling	Sampled system	Sampled system
No noise penalty, best noise performance	Increased noise	Increased noise
Output cannot be sampled easily		Also compensates for gain error
Accuracy limited by transients, best offset	Accuracy limited by sampling process	Accuracy limited by sampling process
Recommended for continuous time applications	Applicable in many discrete time systems	Suitable for switched capacitor systems

Conclusion

- Good low frequency and DC performance has a lot of value in applications such as sensor interfaces
- Although MOS devices have poor matching and flicker noise, several techniques are available to improve this performance
- Noise, power, and area penalties are manageable
- Modern simulation tools can fully support this
- The resulting noise and offset performance can be world class

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Papers to see

- 21.8 KU Leuven Chopping and dynamic element matching for low offset and high gain accuracy
- 21.9 TU Delft chopper amplifier across isolation barrier
- 21.10 Analog Devices chopper amplifier across isolation barrier

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