T4: Layout: The other half of Nanometer CMOS Analog Design

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INTRO

Acknowledgements

- Willy Sansen - KULeuven
- Bill Redman White, Hans Tuinhout, Marcel Pelgrom, Nicole Wils - NXP
- Seyed Danesh, Keith Findlater and all the Gigle Analog Design team
- Ian Clifford, Gordon McKinnon, Cadence Design Systems
- Kofi Makinwa and Kamran Souri- TUDelft
- Anthony Walton and Robert Henderson – Edinburgh University

Tutorial Aims

- What we'll try to cover
  - Introduce some of the physical effects that cause transistors to change properties in nanometer CMOS
  - Introduce issues associated with metallisation
  - Introduce approaches to layout and design that can help minimise these effects
  - Use examples to show why every design is different and paranoia is the only way to feel in control.
- What we'll not cover
  - Passives
  - RF
  - Noise
  - How to develop PCELLS
  - <40nm technology

Disclaimer 1

- Every circuit is different
- Every technology is different
- Every requirement spec is different
- Every CAD flow is different
- Every designer is different

- It's your problem – the layout you need to make your circuit work is your responsibility

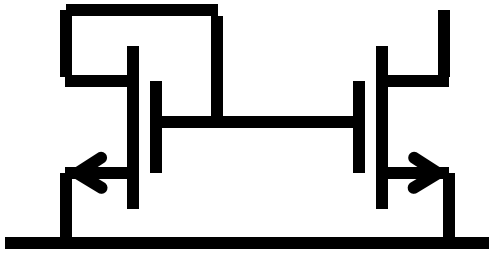
  – This tutorial only hopes to enlighten some of the layout issues that affect nanometer analog circuits.

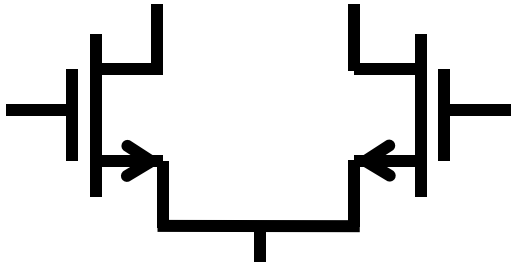
BACKGROUND

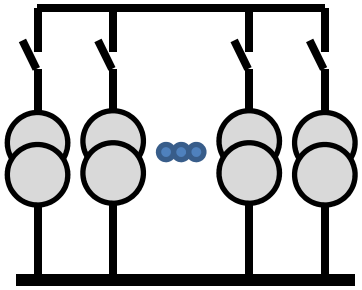
Why is layout important to a designer

- High performance analog
  - Power, speed and precision is not all about 'design'
  - Layout is a major contributor to headroom, systematic mismatch, crosstalk and Gain Bandwidth
- Risk
  - It's not the 100 reasons why it works that matter, its the 1 reason why a circuit fails that needs to be identified .
  - Not everything is modelled, extractable or simulatable
- Design time
  - It's not how quickly you go through the path, it's how many times you need to go around the loop that determines design time
  - Being right 1st time saves more time and money than any design-time productivity
- Area
  - Pushing things to be too small can be equally problematic as relaxing things to make them too large

CMOS analog design relies on matching







Biasing

- PVT sensitivity
- Operating headroom
- Quiescent Control
- Safe Operating Area

Offset

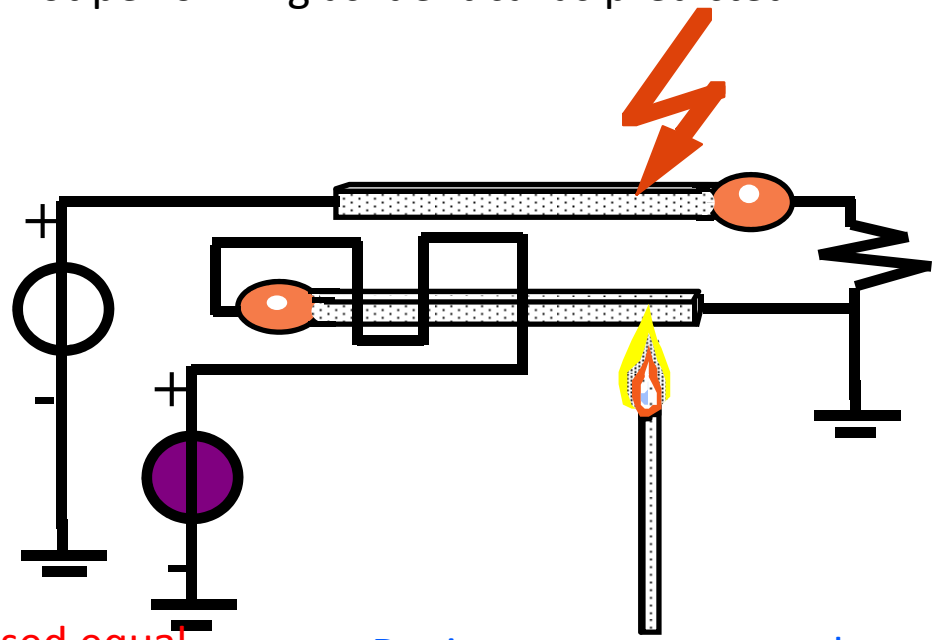
- Input pairs
- Common Mode
- Range
- CMRR
- PSRR

Precision

- Converter resolution
- INL
- DNL
- SFDR

mismatch is NOT ONLY caused by microscopic device fluctuations

Many (first layout) mixed-signal circuit realizations FAIL because supposedly identical components are not performing as identical as predicted



Devices are not used equal

- bias (parasitic resistances)
- temperature
- electrical disturbances (X-over)

Layout / design challenge !!!

Devices are not as equal as expected

- orientation
- environment
- metallization

Characterization / Modeling also layout challenge !!!

Courtesy of Hans Tuinhout, NXP

what do we want to know about mismatch?

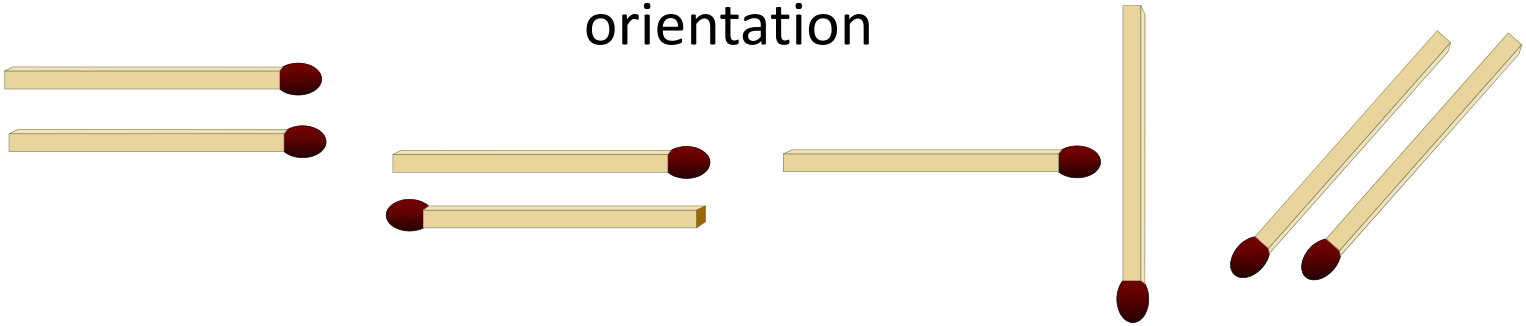
mismatch study categories:

- A-factor determination (for analogue and/or digital circuit design)
- Fluctuation reduction studies (digital circuits; yield improvement, product engineering)
- Layout design rule and design guideline studies: orientation, mirroring, folding, dummies, distance effects (????): “what if rules”
- Special constructions, high precision pairs (QUADs, common centroid matrices, high precision ladders, etc.)
- Dedicated mismatch investigations (product disasters)

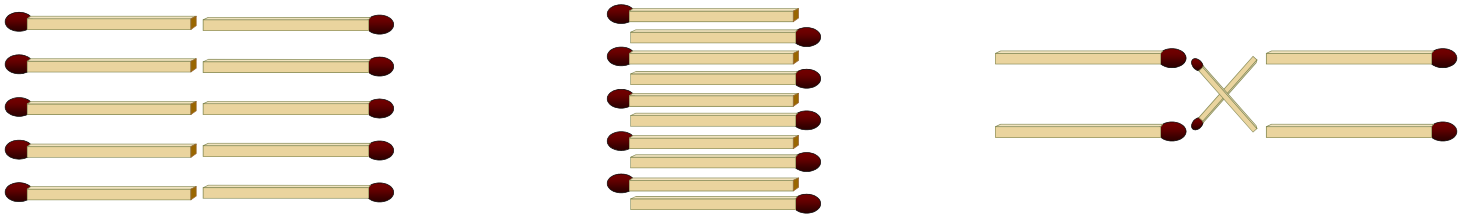
Courtesy of Hans Tuinhout, NXP

What affects matching ?

orientation

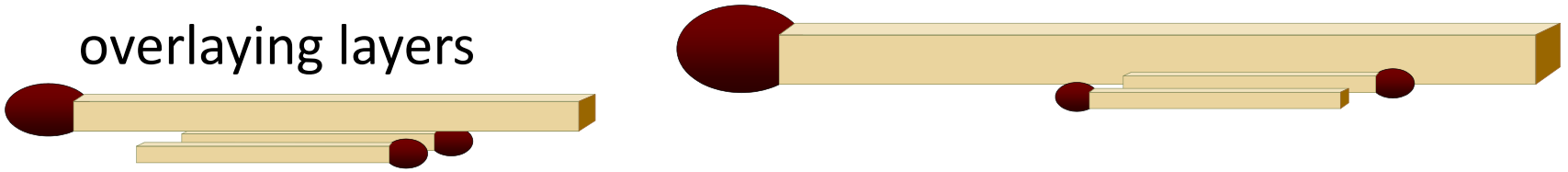


multiple fingers / common centroid / QUADs



distance

overlaying layers

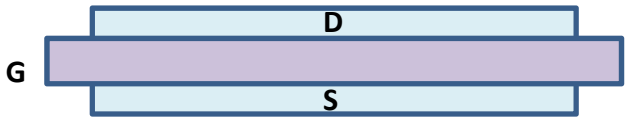


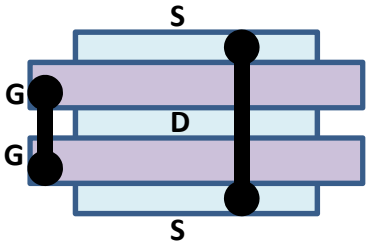
adjacent layout

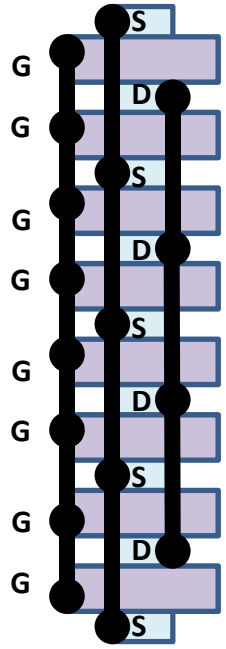
Courtesy of Hans Tuinhout, NXP

Layout can affect power efficiency

- Gain BW for a given current is dominated by
  - Gm
  - Cs/Cd - Primary/secondary pole capacitance
- Layout can alter both of these







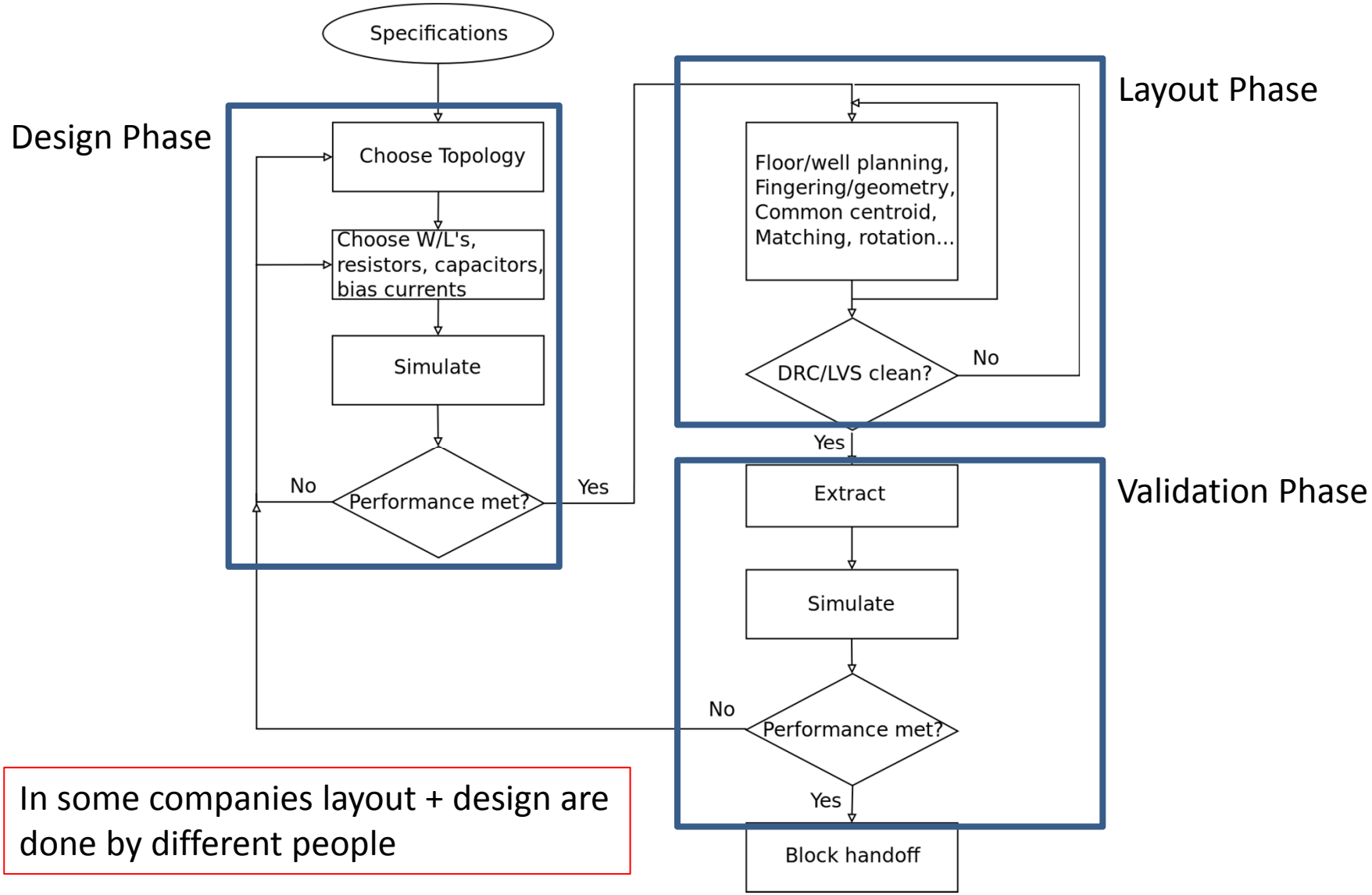
- All the same overall W/L but differing Gm, Cs and Cd

What a designer should really care about

- What he designed is what he'll get
- What he didn't design and just assumed wouldn't affect him, won't affect him
- He'll get the matching he needs to make the circuit work
- How long will it take to get the design ready for tapeout
- Will the design work when it comes back
- Will the design have issues when it goes through qualification and production

Classic Layout Techniques

Classical analog design flow

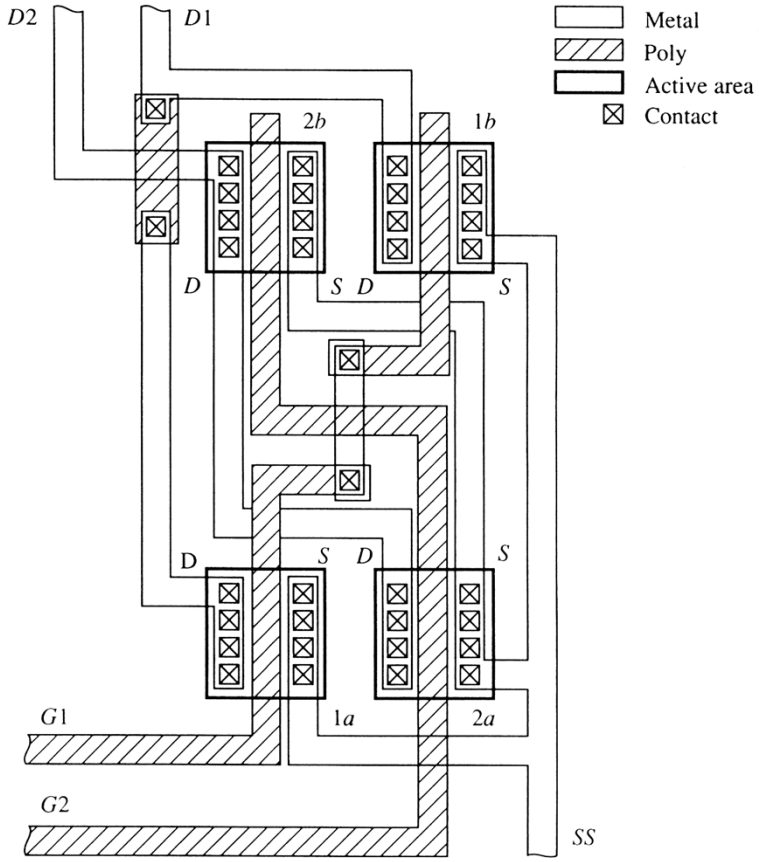


In some companies layout + design are done by different people

Classical analog layout techniques

1. **Equal nature**
2. **Same temperature**
3. **Increase size**
4. **Minimum distance**
5. **Same orientation**
6. **Same area/perimeter ratio**
7. **Round shape**
8. **Centroid layout**
9. **End dummies**
10. **Bipolar always better !**

(Analog Design Essentials, Sansen)



Courtesy of Willy Sansen, KULeuven

Classical analog layout techniques

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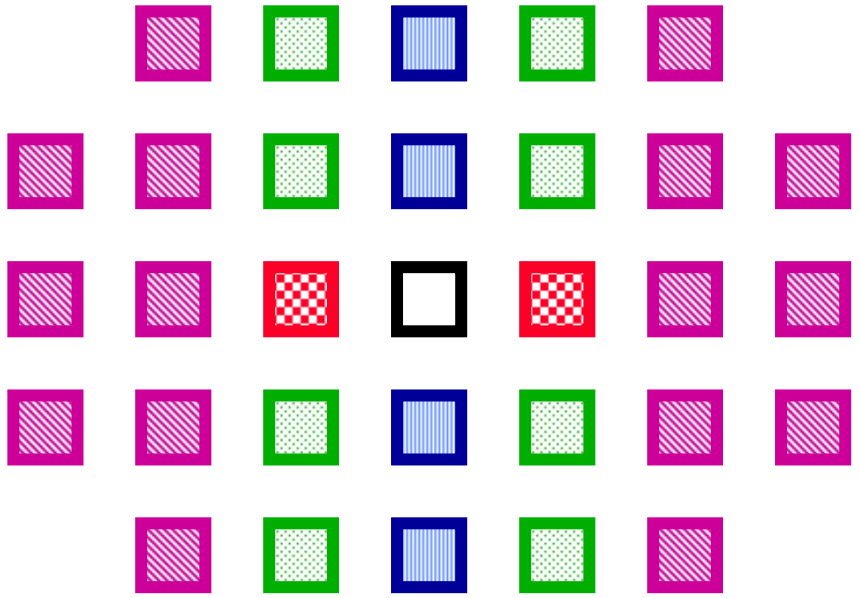
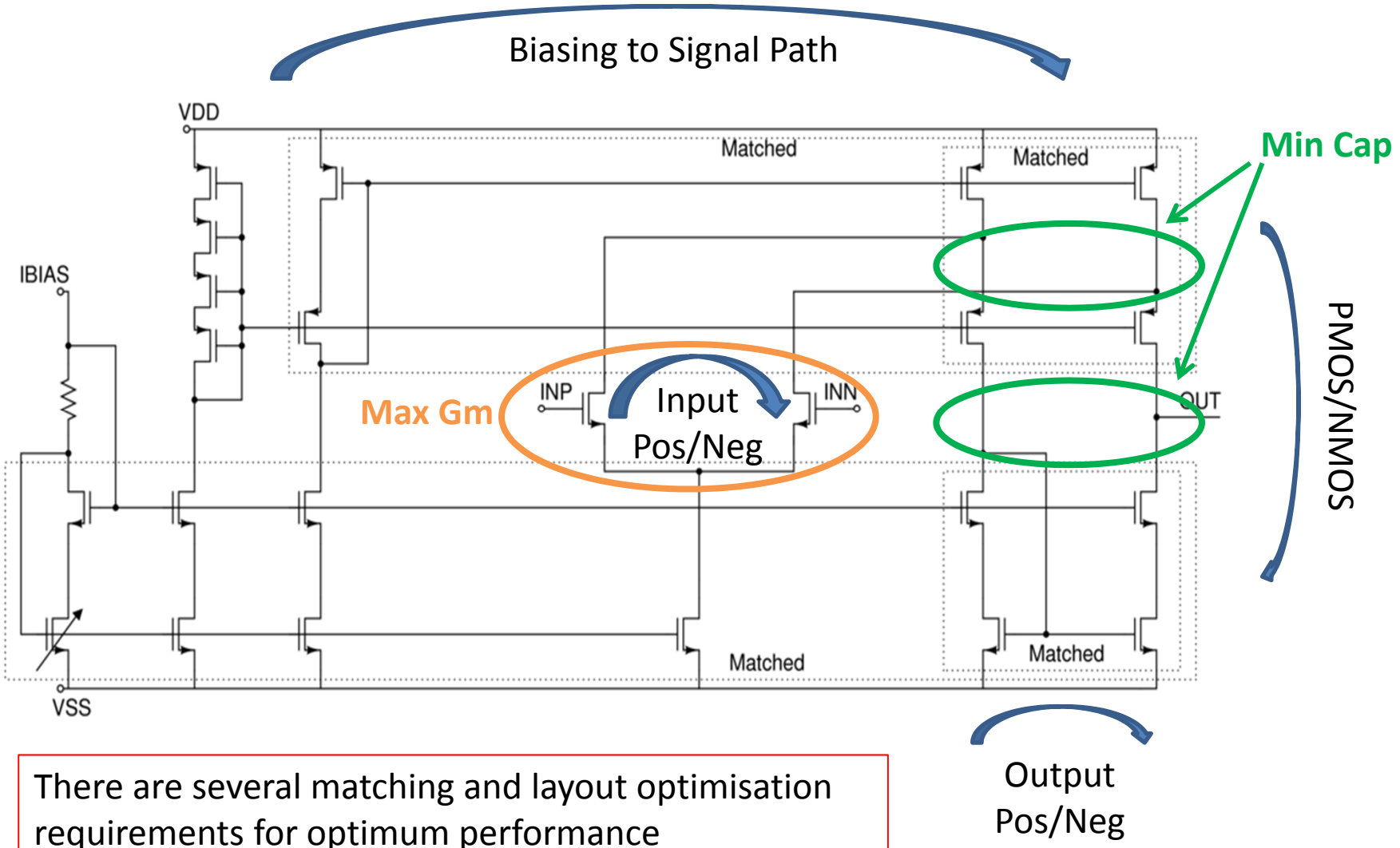


(Analog Design Essentials, Sansen)

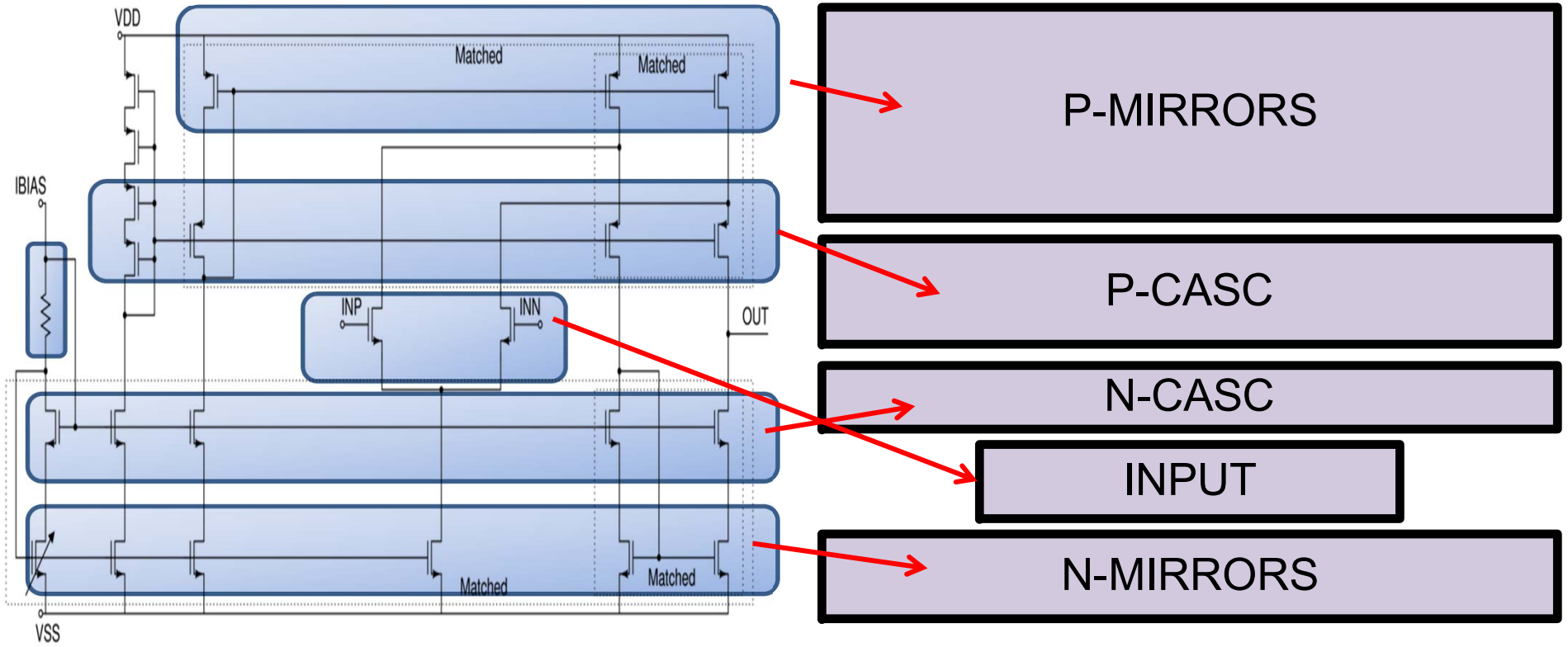
Courtesy of Willy Sansen, KULeuven

The folded cascode example (1)



There are several matching and layout optimisation requirements for optimum performance

Matching a topology to a layout



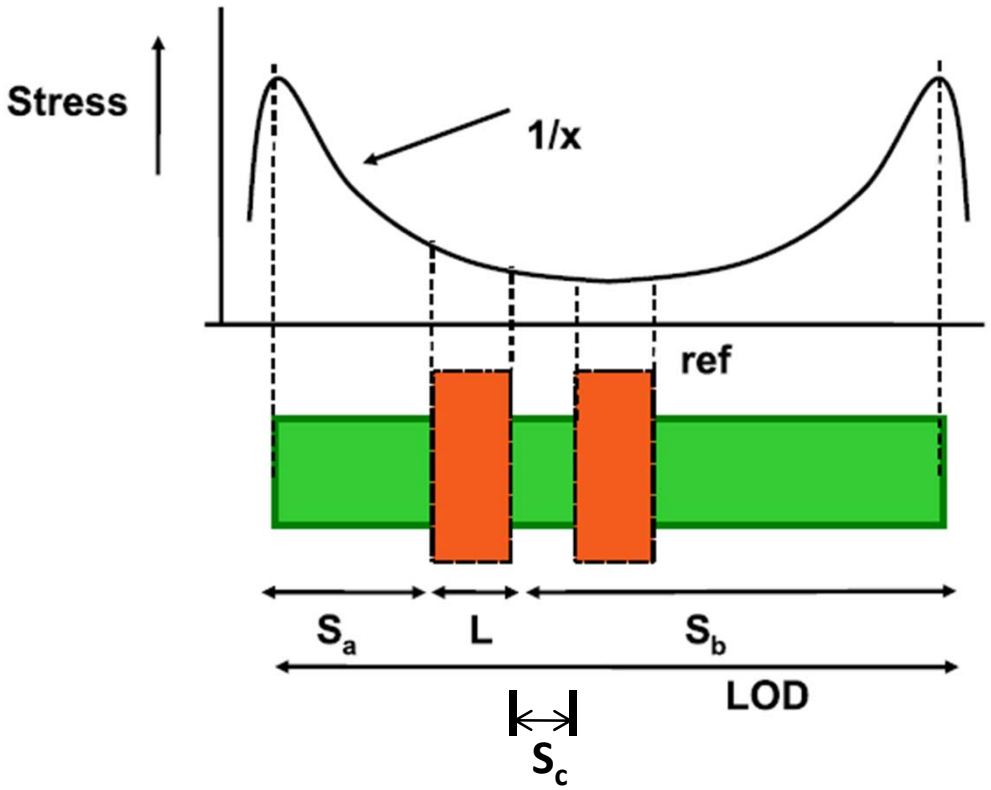
Does it remind you of a space invader ?

What happens in Nanometer CMOS to make the layout more challenging

- More pronounced physical effects
  - STI stress effects
  - Well Proximity
  - Poly Proximity
  - Metal overlap
- Metal/contacts more resistive
- Lower Electro-migration and current handling capabilities
- Additional DFM flows (Metal/Poly/OD fill, Litho Correction)
- Lower voltage headroom, Smaller SOA window
- Greater use of digital assisted analog
  - More signals, mixtures of wells, supplies

Things about Nanometer you need to know

Shallow Trench Isolation - stress effects (1)



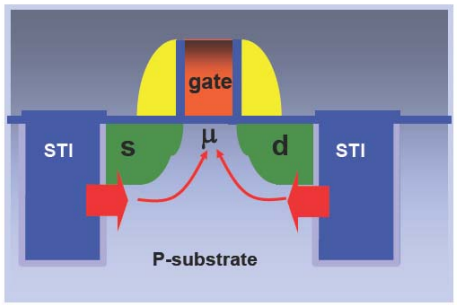
- For nanometer CMOS the most common isolation scheme is STI
- Stress is caused by thermal expansion of various materials, it affects the electrical properties of the silicon (e.g. mobility) and hence Idsat, gm and Vth
- Has been incorporated into existing BSIM4 SPICE models (SA, SB, SC)

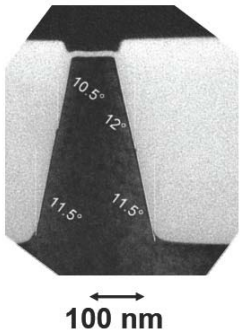
Diagrams Courtesy of Marcel Pelgrom, NXP

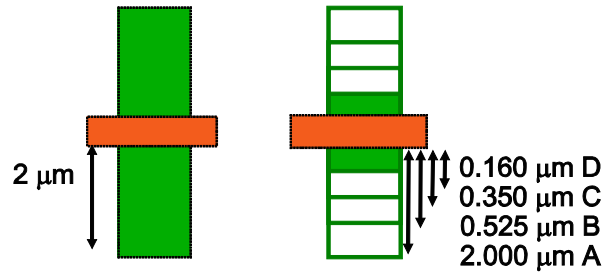
Shallow Trench Isolation - stress effects (2)

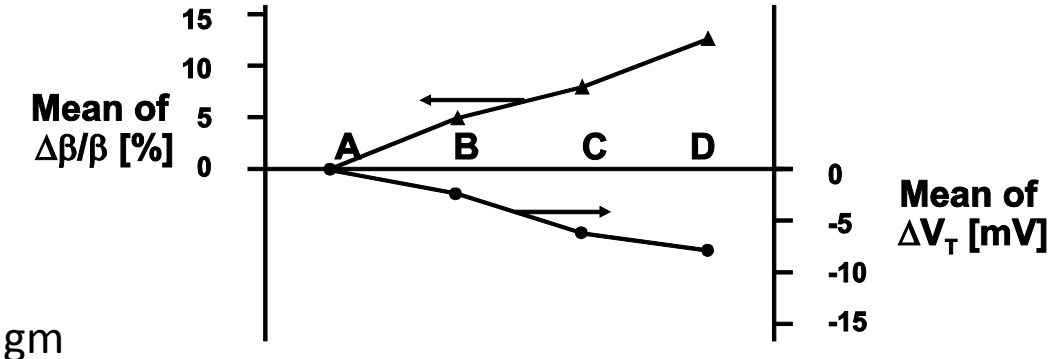
- The drivers of the stress and corresponding shift in electrical performance can be qualitatively described by two geometric parameters, Sa and Sb in SPICE.
- They represent the distance from the gate to the edge of the OD on either side of the device.
- Stress = $1/ (Sa + L/2) + 1/(Sb+L/2)$

Shallow Trench Isolation - stress effects (3)









Can have a huge effect – up to 20% gm

Can be extracted so

i) don't leave it to the end of the design/layout cycle to check

ii) Make it part of the design flow, i.e. should check layout meets design

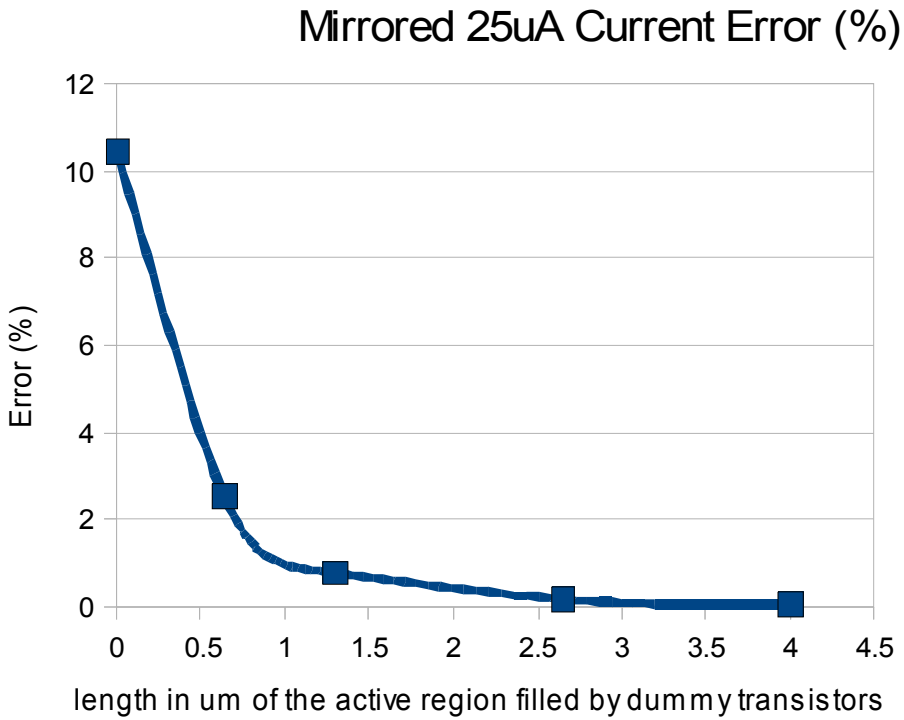
Can be used to optimise the transistor for the applications

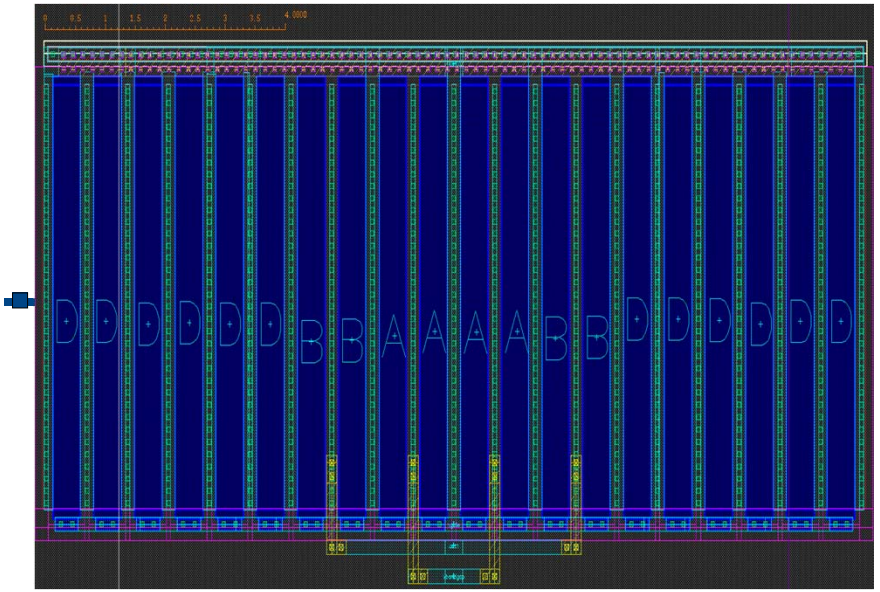
Input pair + switches need high Gm

Current sources need low gm

Diagrams Courtesy of Marcel Pelgrom, NXP

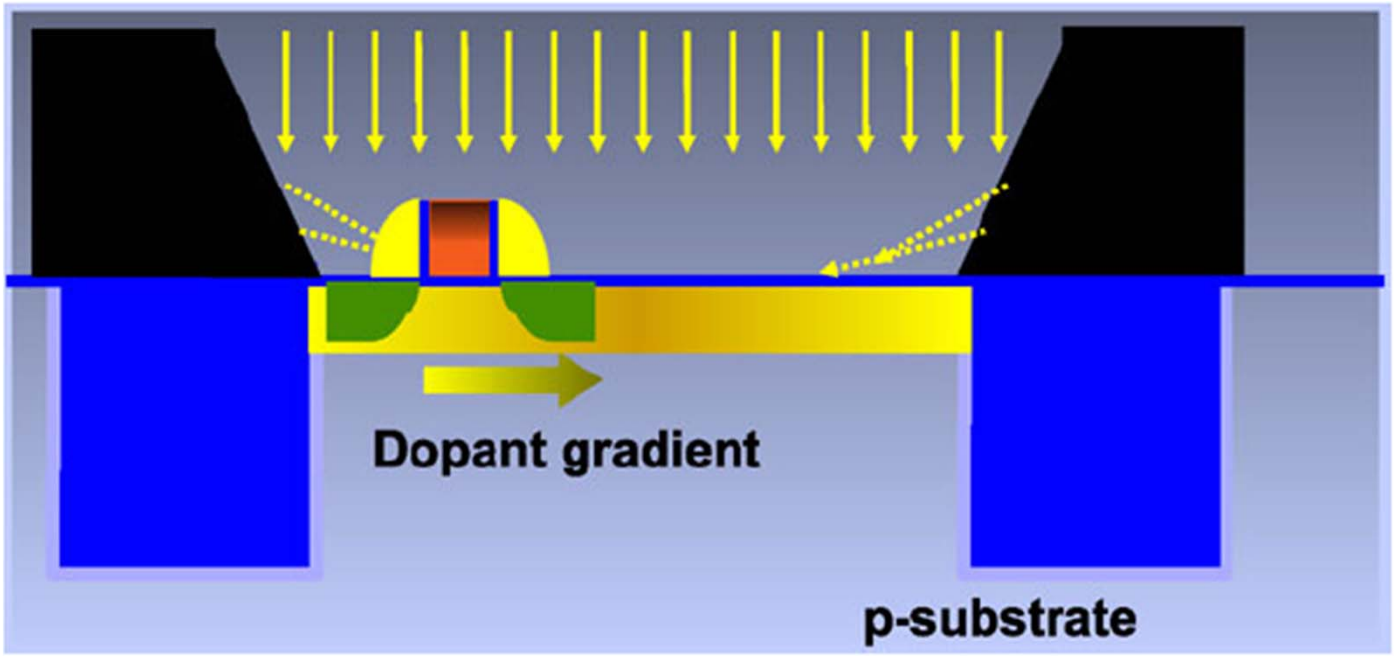
Can dummies solve - Shallow Trench Isolation - stress effects?





- Yes/No - this study shows 4um of dummy transistors are needed to minimise the effects of STI

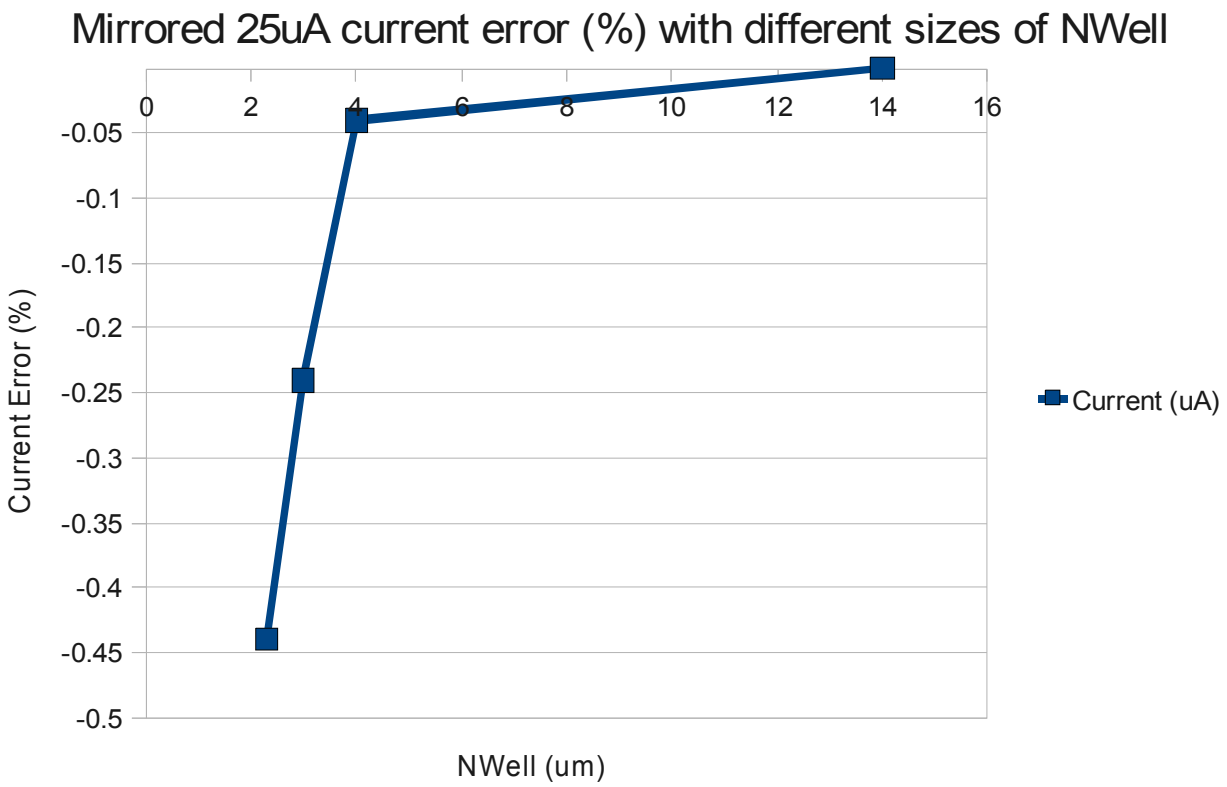
Well Proximity Effects (WPE) (1)



Transistors close to the well edge will exhibit a difference in Vt and Id compared to devices located far away from well edge.

Diagrams Courtesy of Marcel Pelgrom, NXP

Well Proximity Effects (WPE) (2)



BSIM models include the WPE effect using the SCA, SCB and SCC parameters.

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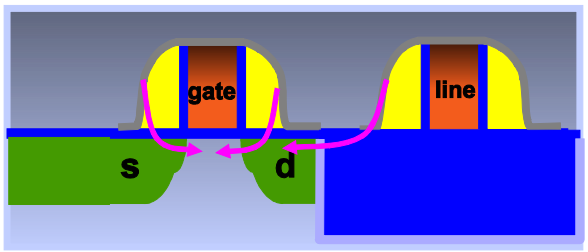
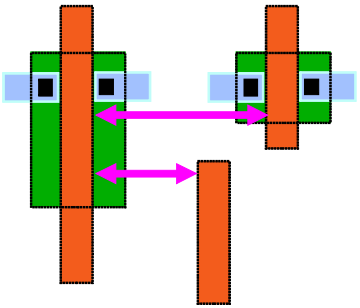
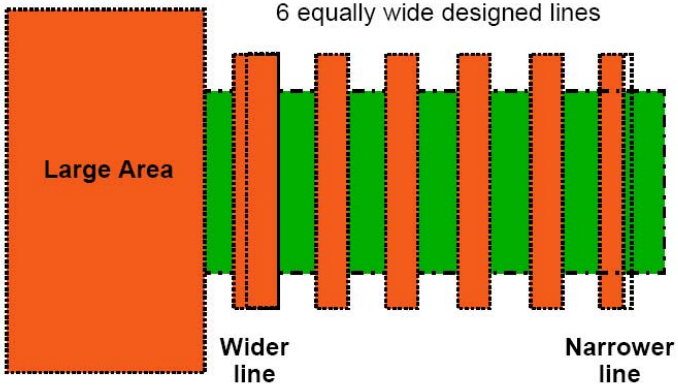
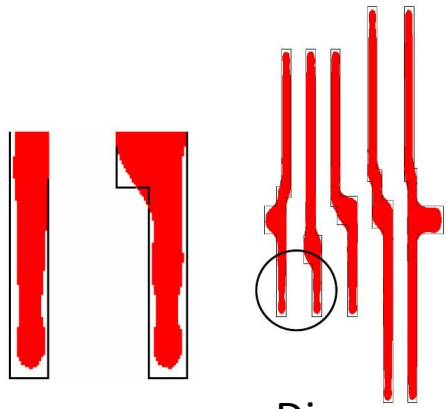
Poly Proximity Effects







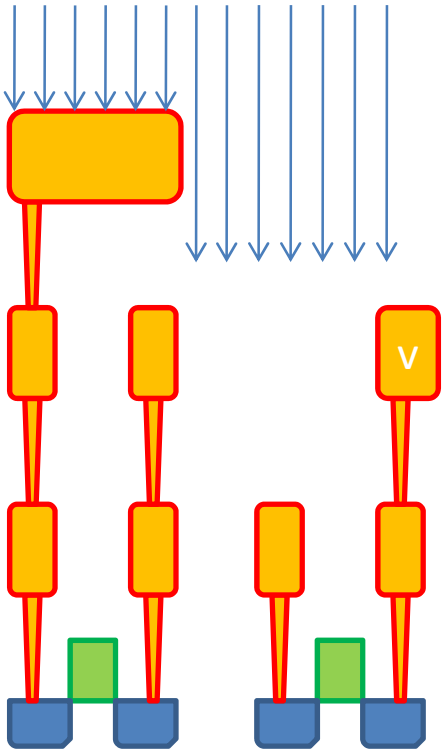


- Poly Near transistors can
  - Induce strain
  - Influence etch uniformity
  - Alter lithography
- Some effects are compensated for at mask prep/making, but …
  - you can't control it
  - always a concern that pushes transistor below 'min'

Diagrams Courtesy of Marcel Pelgrom, NXP

Metal over transistor

Hydrogen released at final process anneal can be blocked by the metal



- Metal over transistor can
  - Prevent annealing
  - Introduce stress
- Not much study available, but is an observable effect
- Not just limited to the lower layers
- Not extracted or modelled

Metal Resistance, Time Constant and Electro migration

- Can't just treat metal as 'metal'
  - IR drops & RC delays & Cross-coupling interaction
    - It's really easy to have a problem in all of these
  - Do the tools help you ?
    - Yes & No – challenge is the extraction
    - It is a complex problem - resistance and capacitance a function of surrounding topologies
- Comparison from 90 to 40 nm
  - Blocks using IO transistor are still a similar size, but resistance of tracks has increased
  - Be careful with signal lines

	90nm	40nm
Contact resistance (ohms/contact)	18	50
Metal 1 min width track resistance (ohms/um)	0.6	5
Metal1 inter track min space capacitance (fF/um)	0.1	0.09
Via 1-4 resistance (ohms/via)	1.5	15
Metal 2-5 min width track resistance (ohms/um)	0.45	4.5
Metal2-5 inter track min space capacitance (ff/um)	0.1	0.09
Top metal min width track resistance (ohms/um)	0.05	0.06

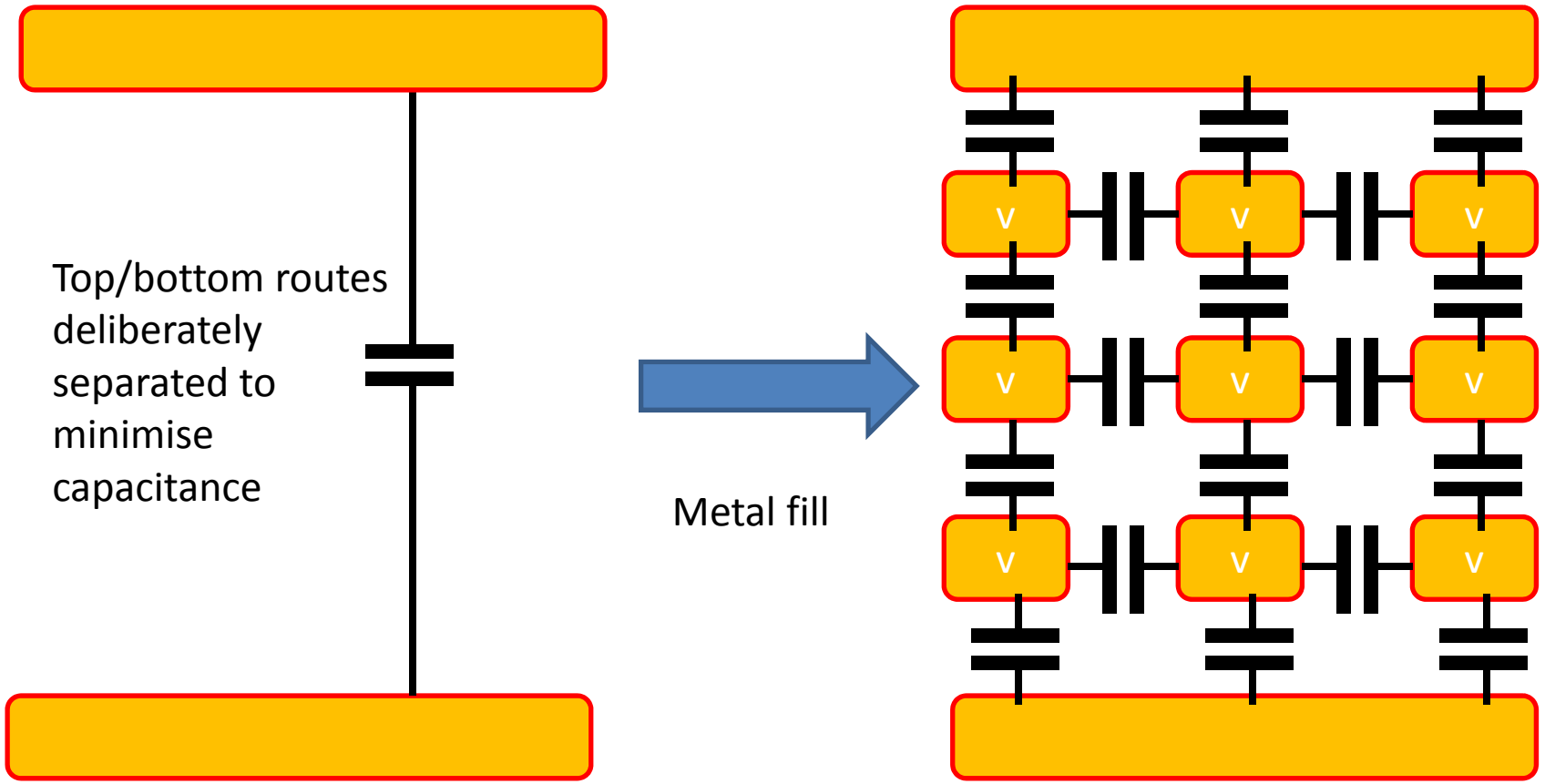
Poly/Active/Metal density & other litho effects

- To control the process and improve uniformity there are design rules for density of poly, active and metal.

- In nanometer CMOS the density rules are extremely strict:
  - Checked on poly and active as well as metal
  - Checked on different sized windows (>100 x 100 um, and < 100 x 100 um) with different density limits
  - Can alter depending on starting point of 'search'
  - Auto fill tools available to help ?

- Why is this an issue
  - Need to make sure the block doesn't change when placed inside the macro OR if Auto fill tools are turned on

What happens to the Metal Fill, do you get extra capacitance ?

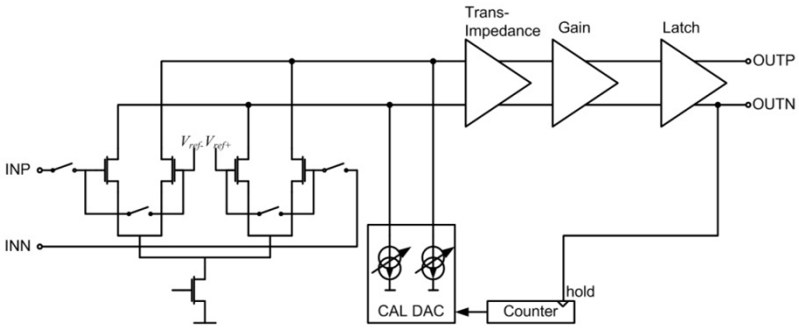


If you want to know the capacitance, put it the metal there yourself, don't let the tools fill it

Summary – How are these effects covered

	Modelled	Extracted
Stress Effects	Yes	Yes
Well Proximity	Yes	Yes
Poly Proximity	No	No
Metal over transistor	No	No
Transistor Orientation	No	Yes (can validate for it)
Track/Contact resistances	Yes, Not easily	Yes, Not easily
Inter Track Capacitance With metal fill	Yes, Not easily	Yes, Not easily

Digitally assisted analog



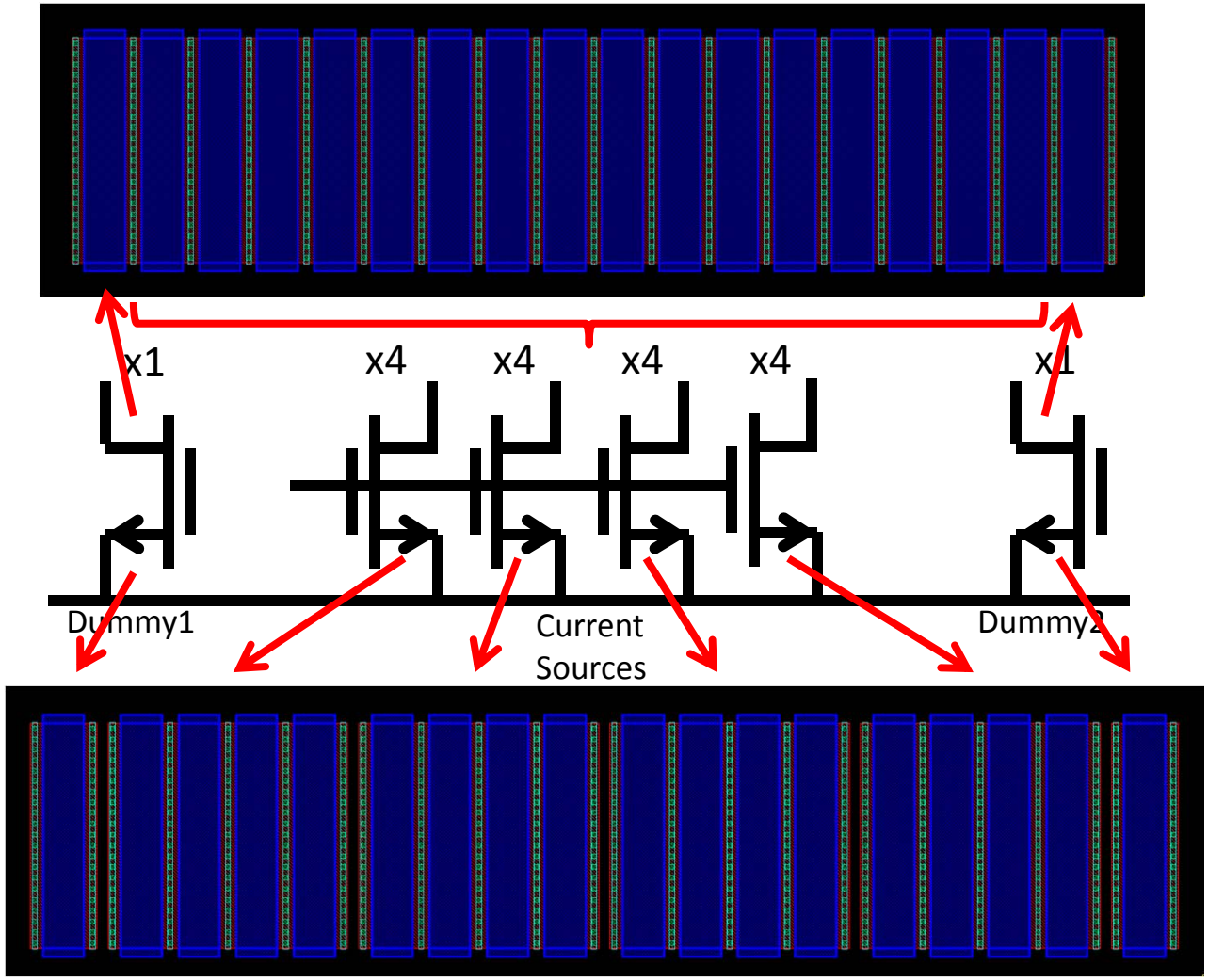
- Change of design style,
  - more digital/analog block,
  - E.g. Trim bits for offset/biasing
- Why it's important for layout
  - Lots of signal lines
  - A Converter or AFE can have 100's of control signals
- Dilemma
  - Do you use digital or analog tools for including the digital
- Danger
  - Letting an analog designer check timing
  - Letting a digital designer in your analog layout
  - Just because its a 'static' control signal does not mean it is not important or sensitive

Sub-block layout strategies

Transistor/Sub-block Layout style

- Split transistors into multiples of ‘2’ to minimise area and capacitance of critical nodes
  - Split into greater binary ratios if you plan to do interleaving with biasing or scaling within the macro
- Consider using Single units of multiple transistors
  - Easier to match stress effects
- Transistor vs Top Level Symmetry
  - Transistor Level Symmetry
    - layout groups of associated transistors together
  - Top Level Symmetry
    - layout one half and mirror

Arrays of transistor vs Array of M units



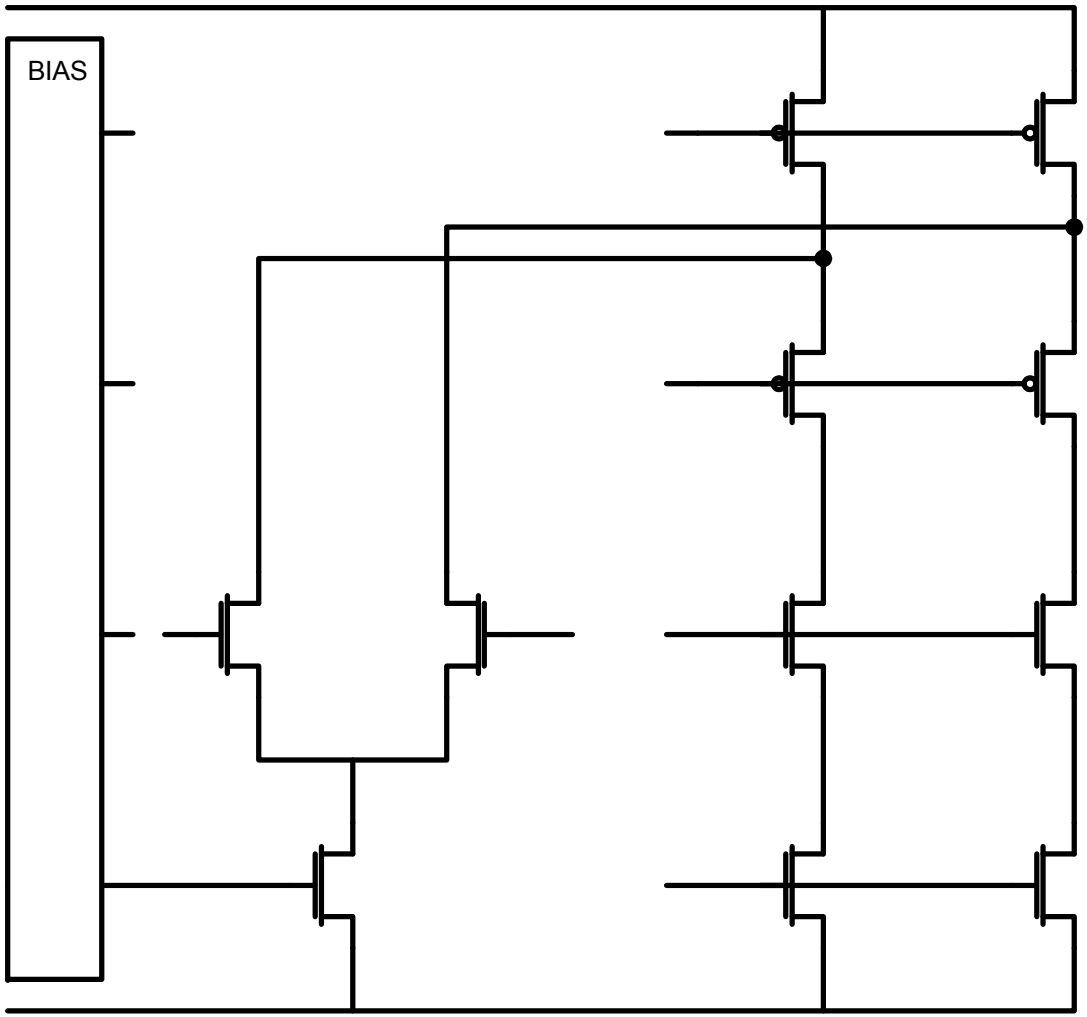
Array of transistors makes it easier to inter-digitate if needed

There is not much penalty in layout area between the two strategies

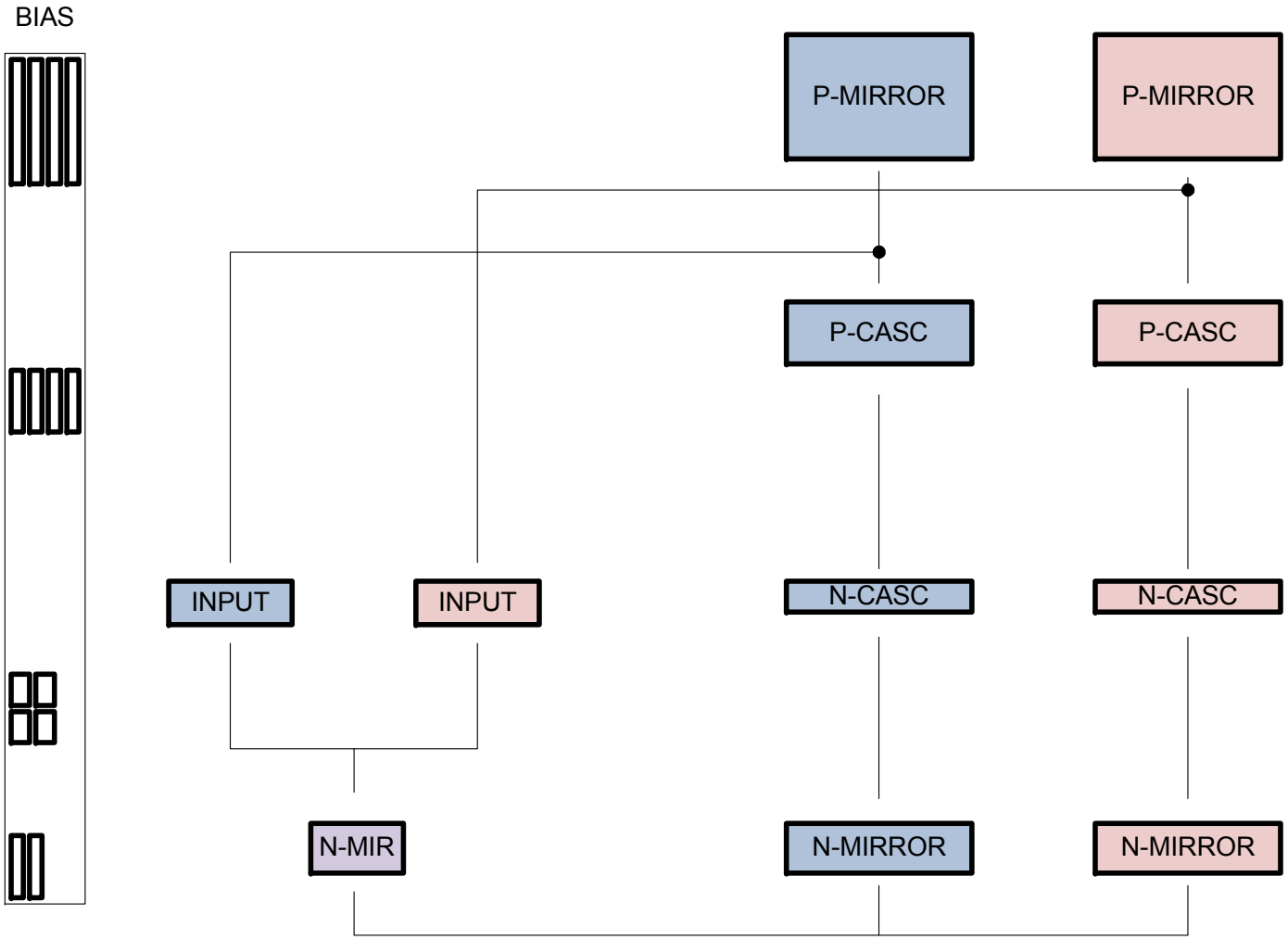
Array of 'M' units easier to match stress effects and reduces metal routing

Comparison of symmetry at transistor vs symmetry at top level for a Folded Cascode Amplifier

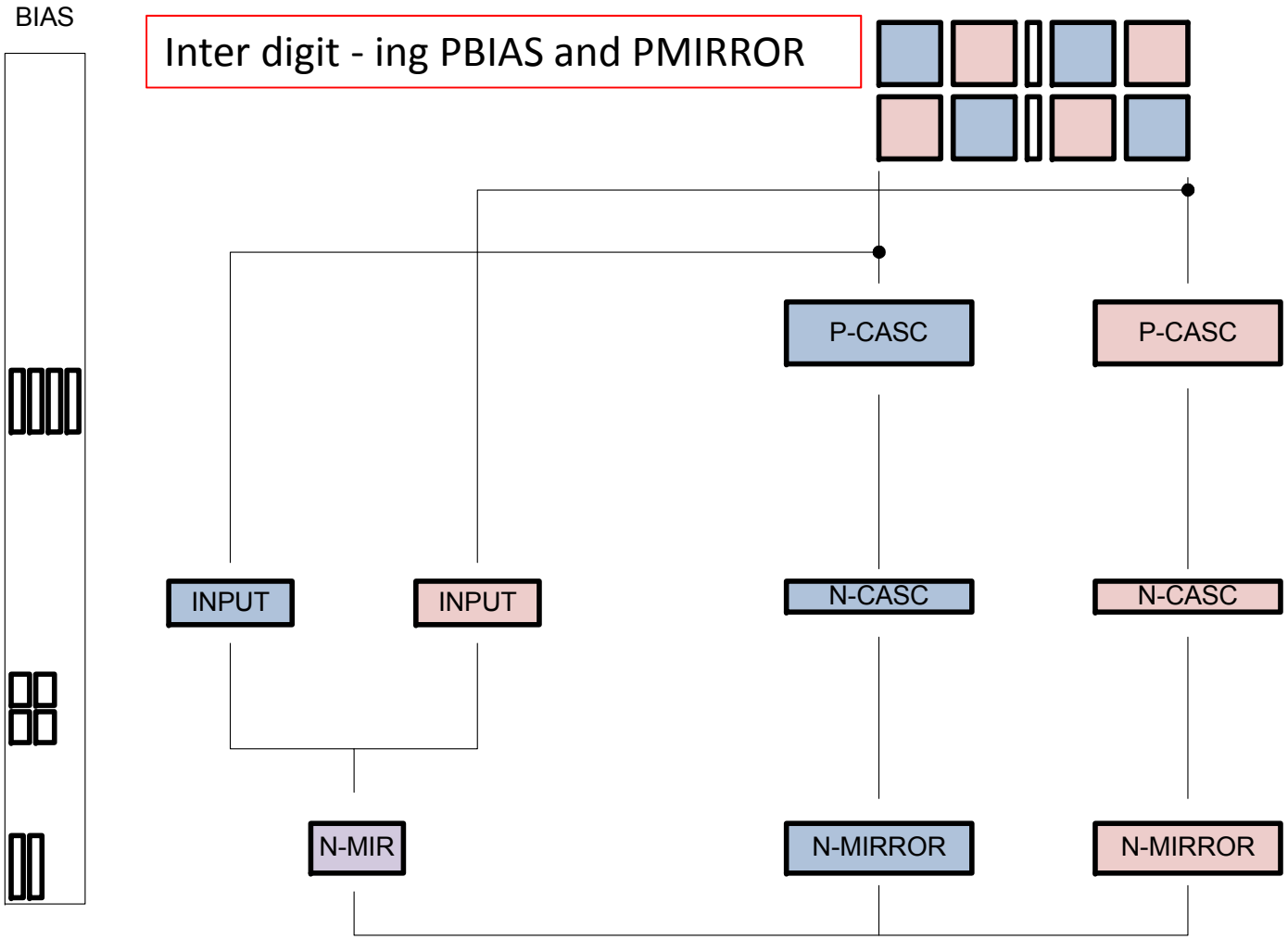
The Amplifier (schematic)



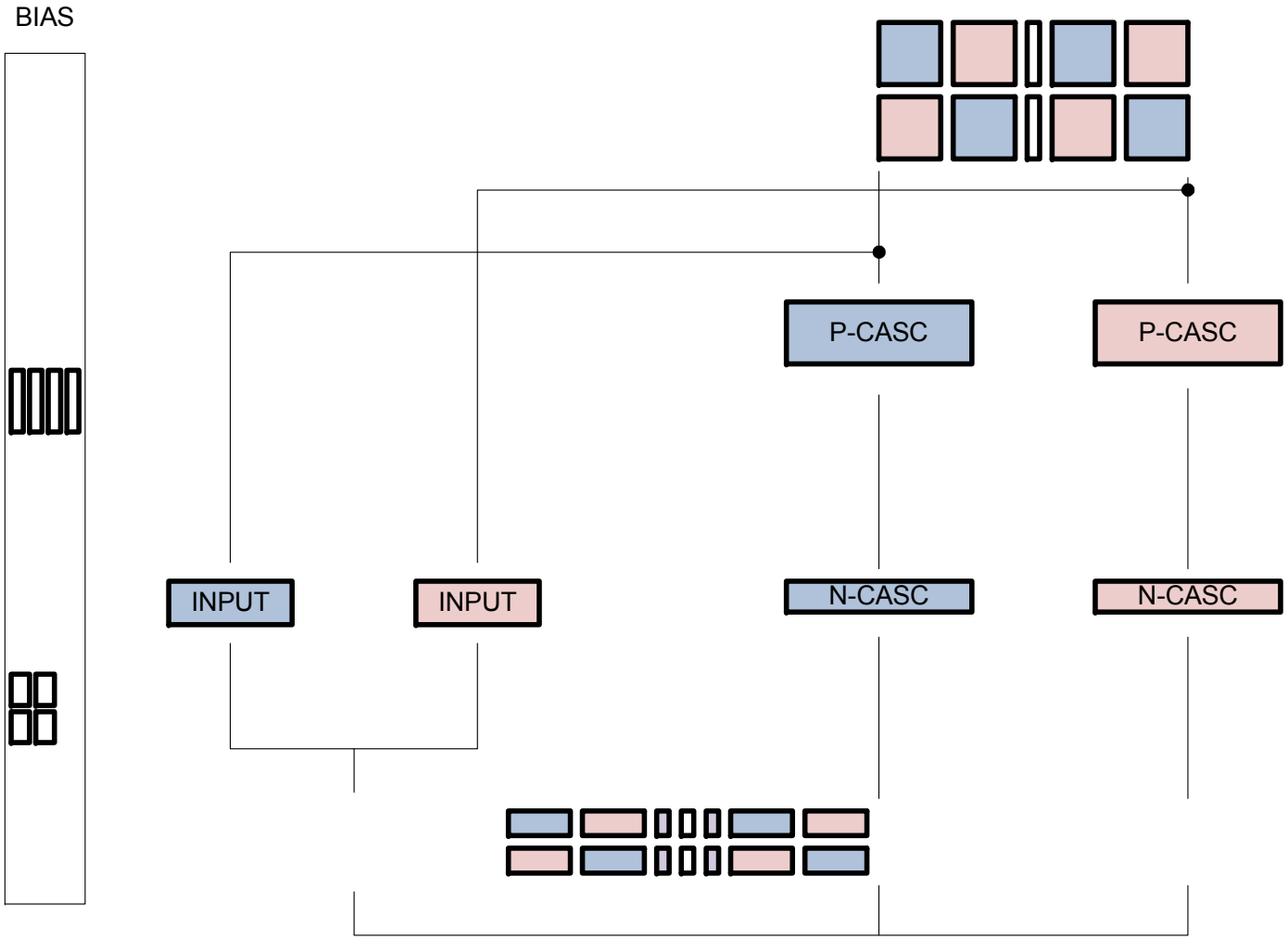
The Amplifier (Starting Components) Symmetry at Transistor Level (1)



Symmetry at Transistor level (2)

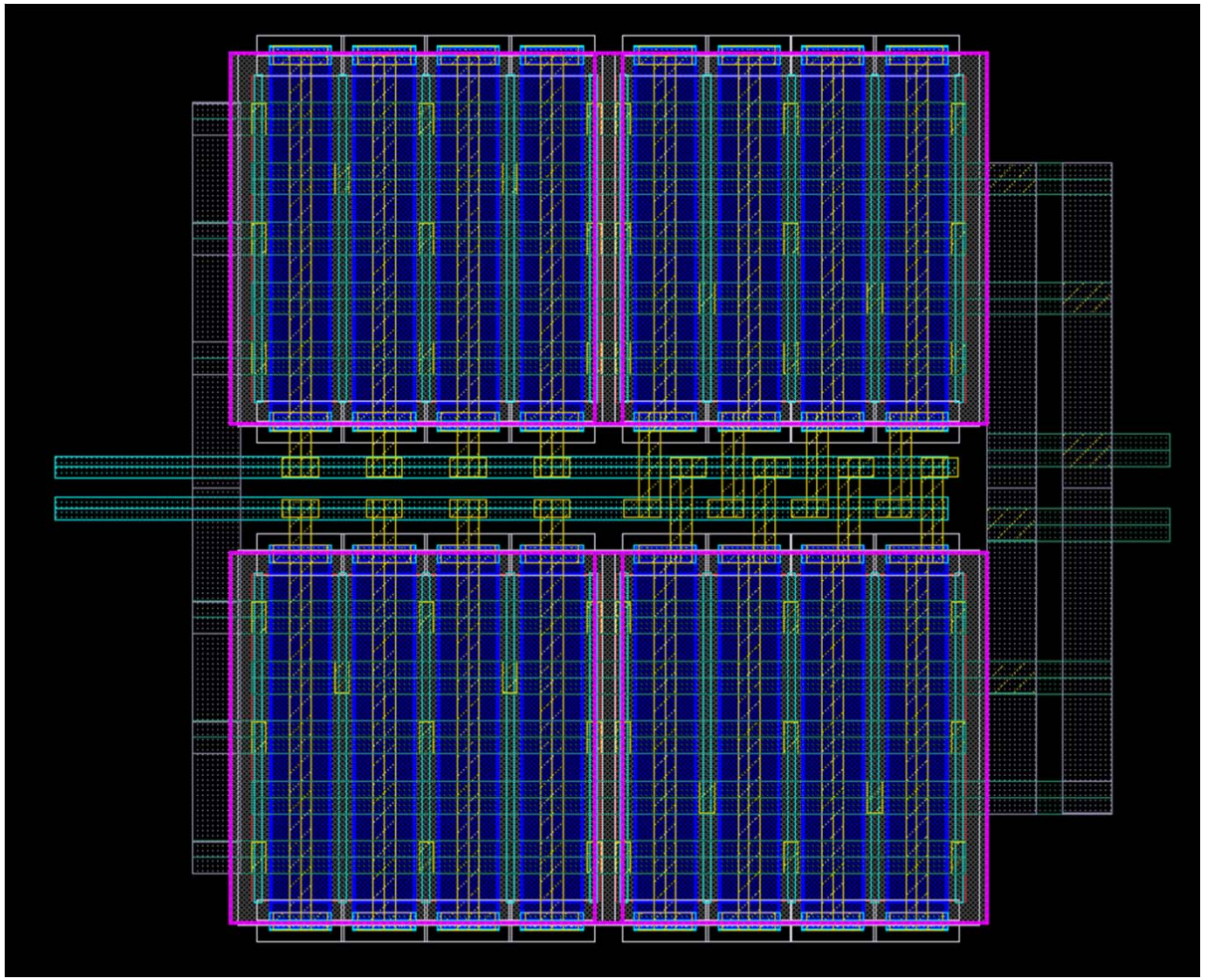


Symmetry at Transistor level (3)



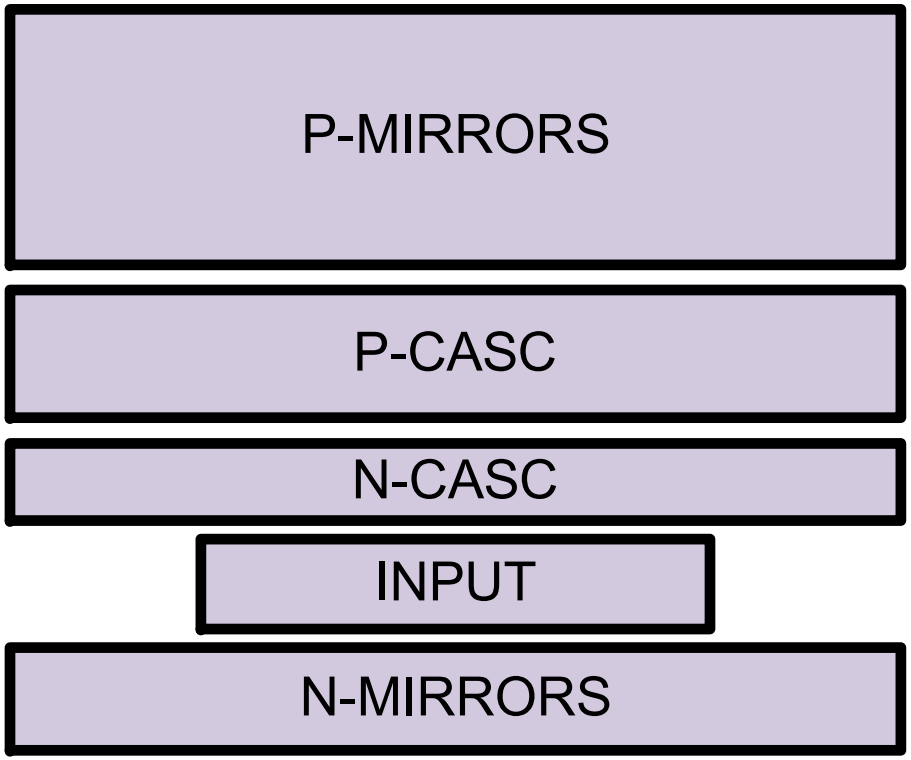
Inter digit - ing NBIAS and NMIRROR

Metal Matched Cross Quad



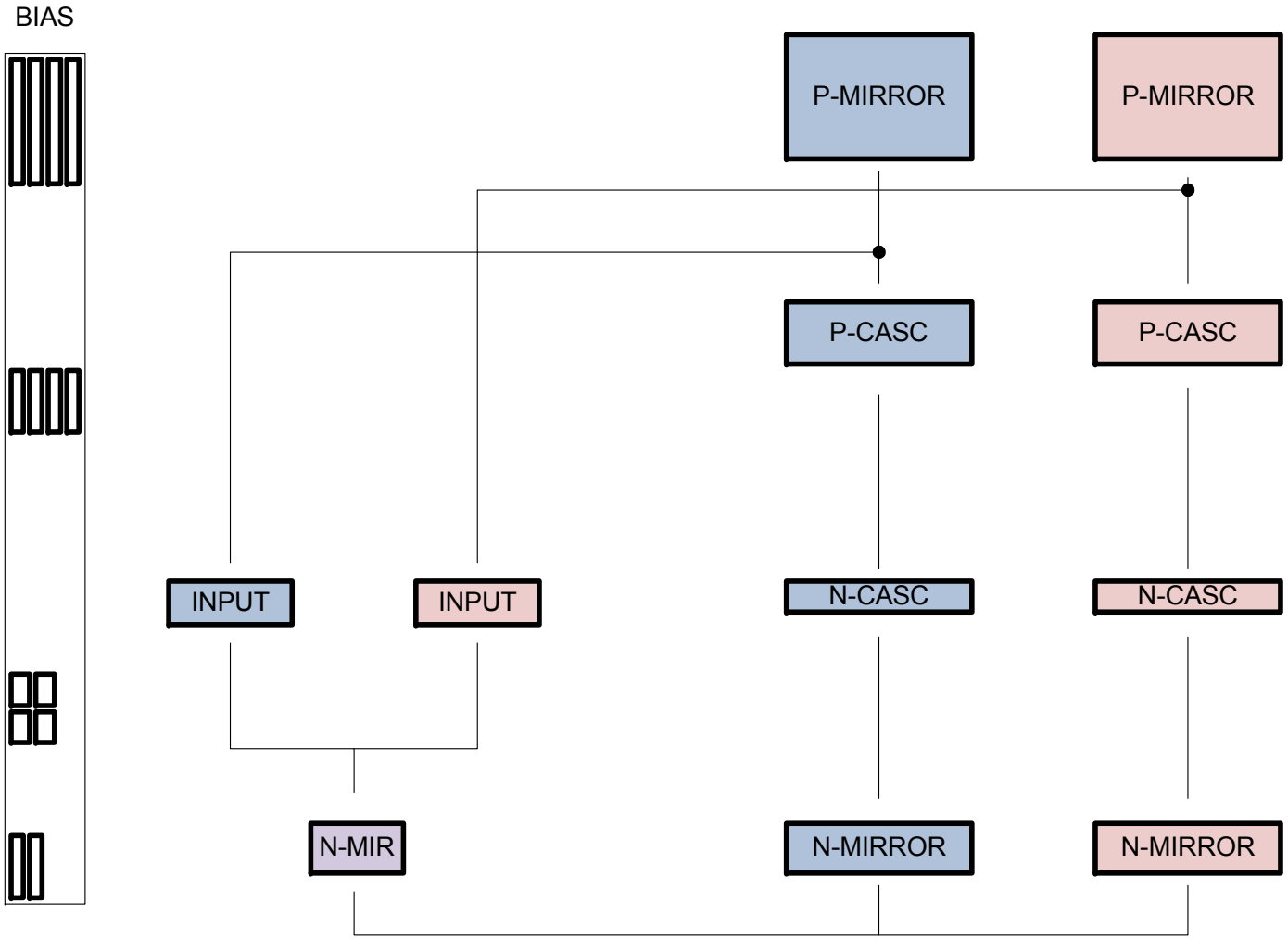
Common Centroid input pair ...

Symmetry at Transistor Final Layout

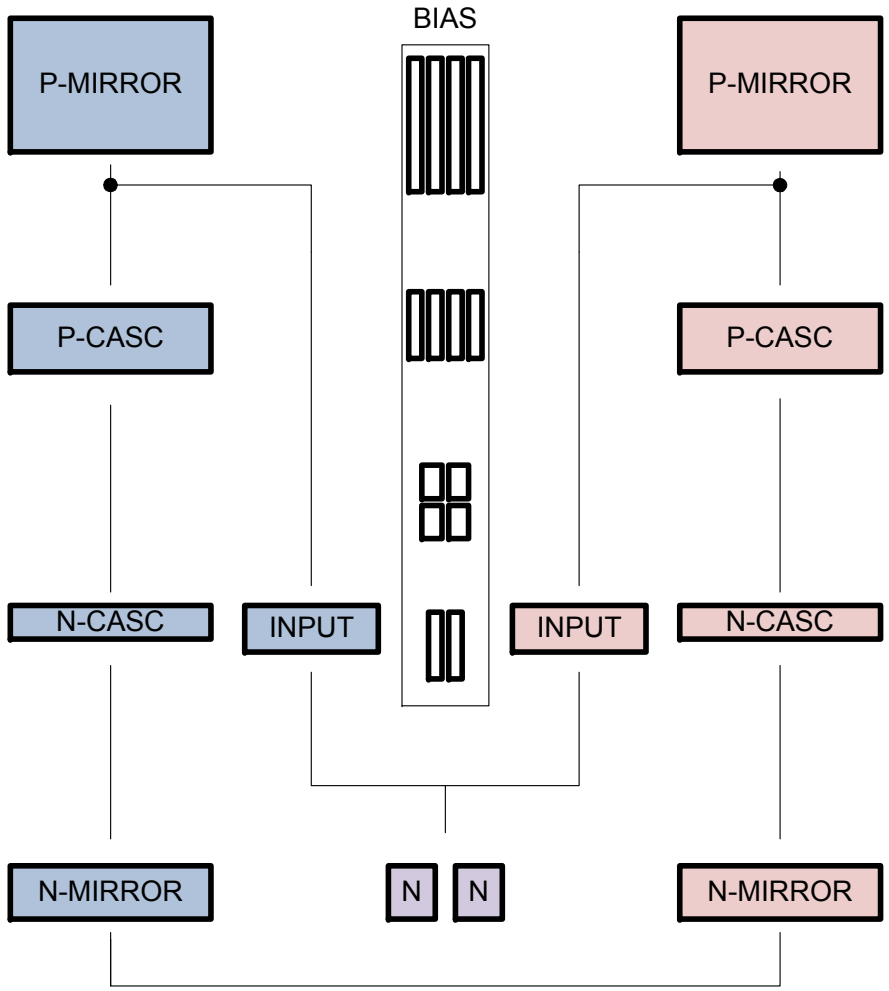


All transistors interlinked
+ Good matching
- Poor parasitics

The Amplifier (Starting Components) Symmetry at Top Level (1)

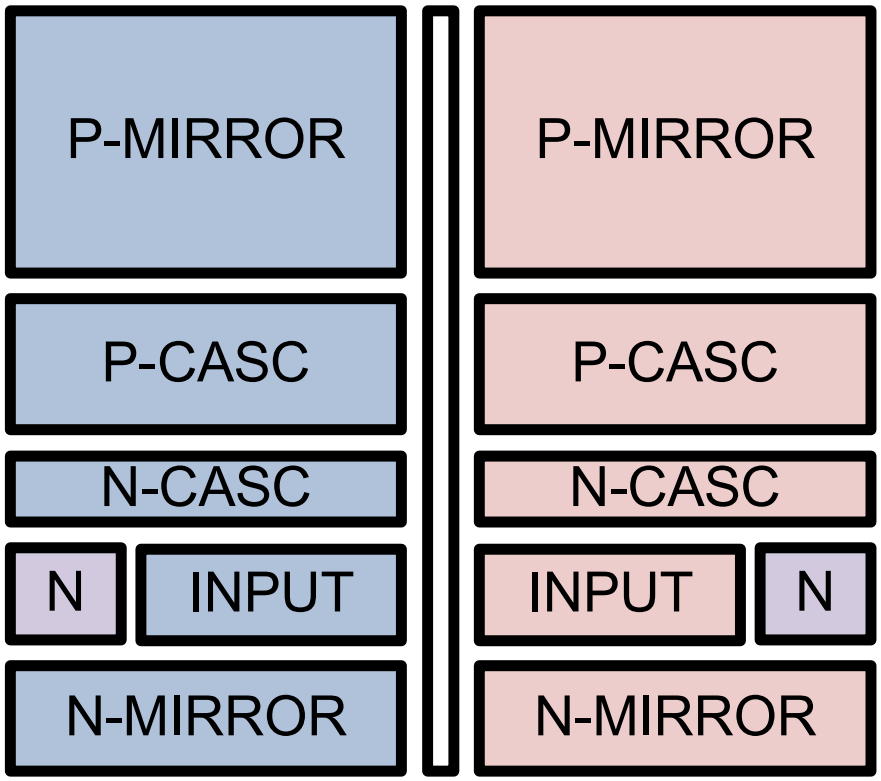


Symmetry at Top-Level (2)



Biasing Placed in the middle of identical POS/NEG blocks

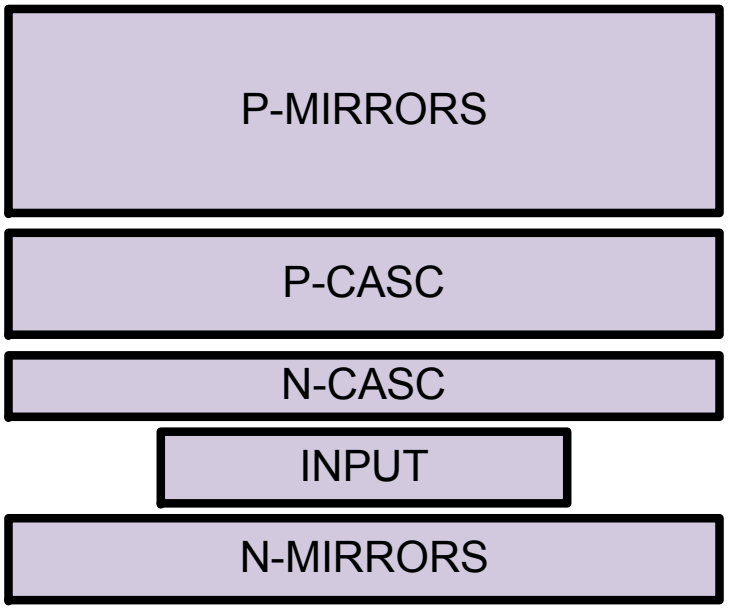
Symmetry at Top-Level Final Layout



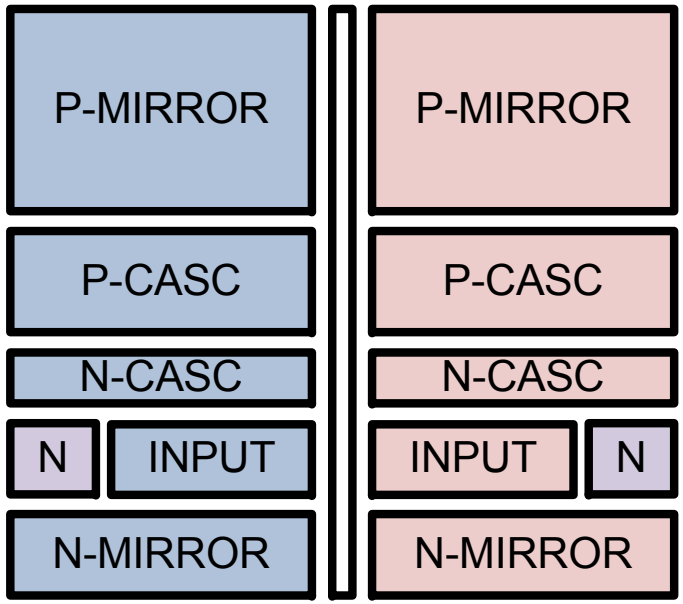
"Pseudo" differential
Mirrored Layout
+ Good parasitics
- Poor gradient matching

To flip or not to flip

Symmetry at Transistors



Symmetry at Top-Level

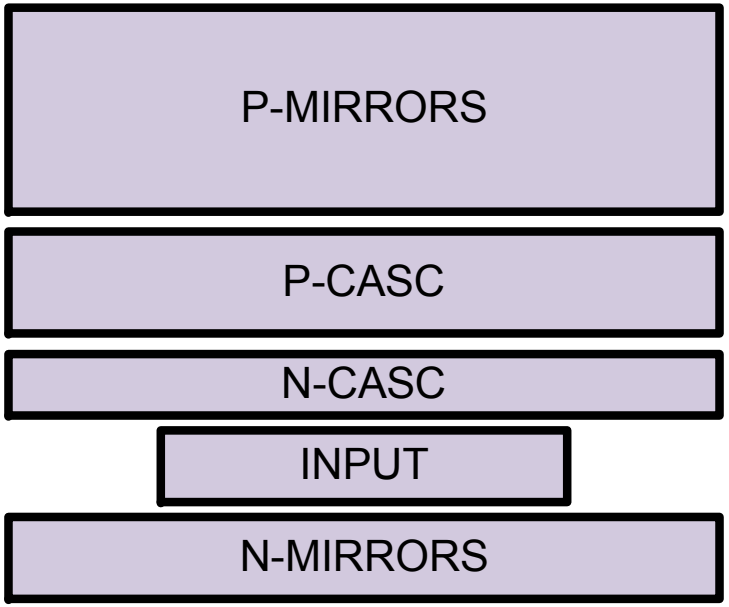


Sometimes you can mix ‘n’ match

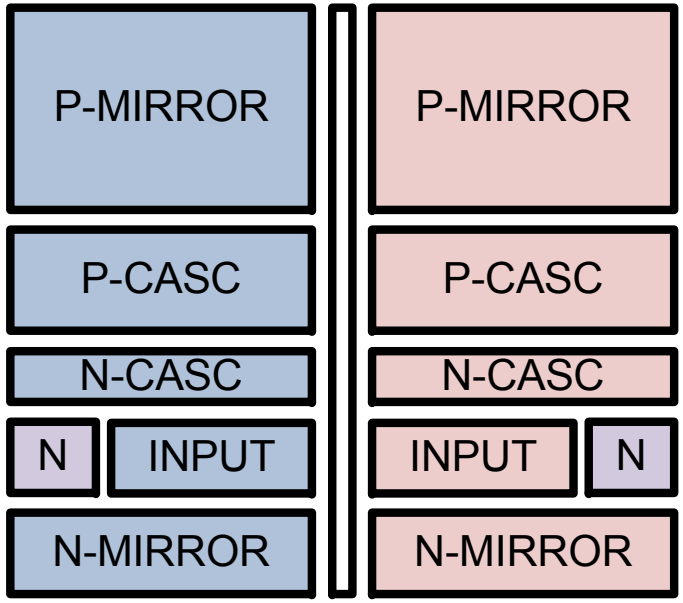
Which to Use?

0.75u 0.5u 0.35u 0.25u 0.18u 0.13u 90n 45n

Symmetry at Transistors



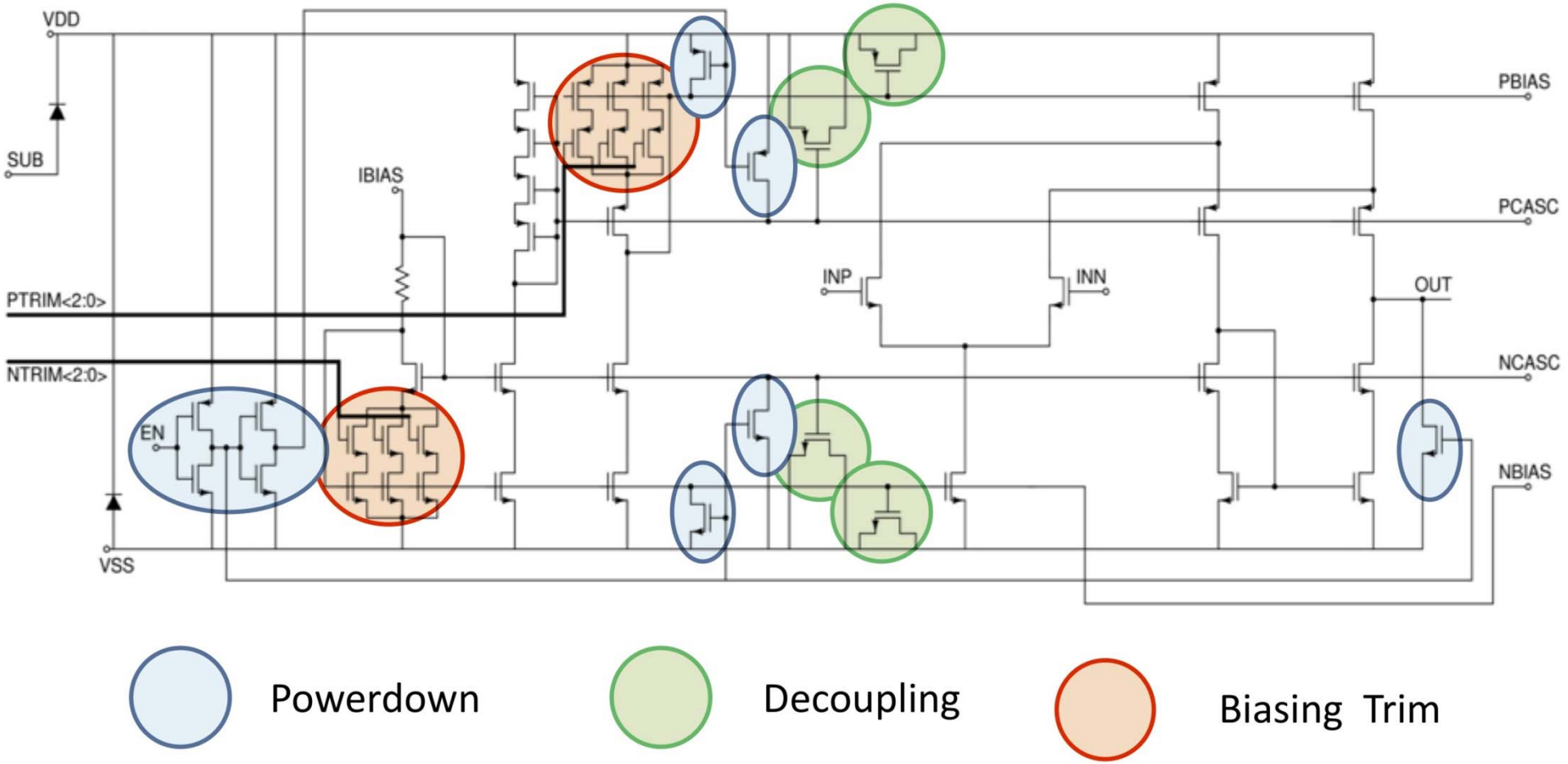
Symmetry at Top-Level



Include ‘sundries’ at block level before starting layout

- Easier than going back and retro fitting at macro level. Example sundries :-
  - Decoupling
  - Power down
  - Trim
  - Test
  - Debug signals or blocks
  - Get out of jail functions
    - Put in spares
    - Bring key signals to top metal (plan for FIB)

Example: Getting Ready for Layout

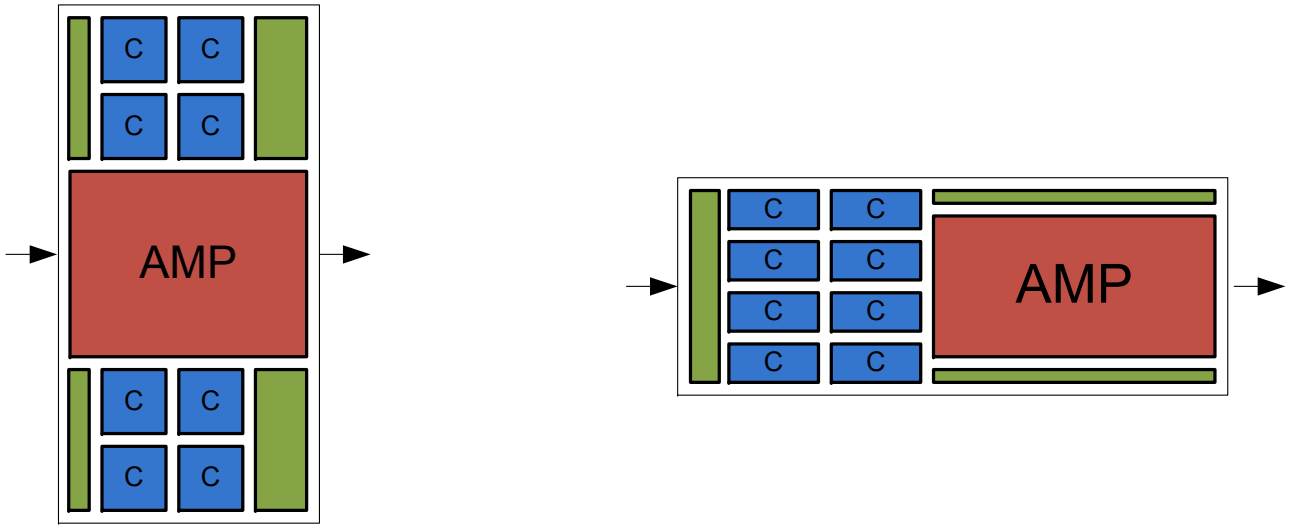


Block floorplan

- Signal flow
  - Need to consider the routing around the sub block
    - E.g. feedback network
    - Minimise input-output and stage-stage crosstalk, particularly around blocks with high gain or delay
  - What to do across the block (Eg Analog, digital, references)
    - Where do the signals arrive, where does it leave?
    - Don't create a problem for someone else to solve
- Power supplies
  - What is the global strategy and what metal layers will be used?
- Wells
  - Organization, well spacing and overlap is the largest design rule
  - Deep Nwell, not always compatible with sub-blocks,
    - strategy to use deep nwell needs to be decided early on

Building up a macro-block
Example Pipelined ADC

Within one stage of the pipelined ADC, the amplifier, the capacitors and the other circuitry can be arranged in different ways.

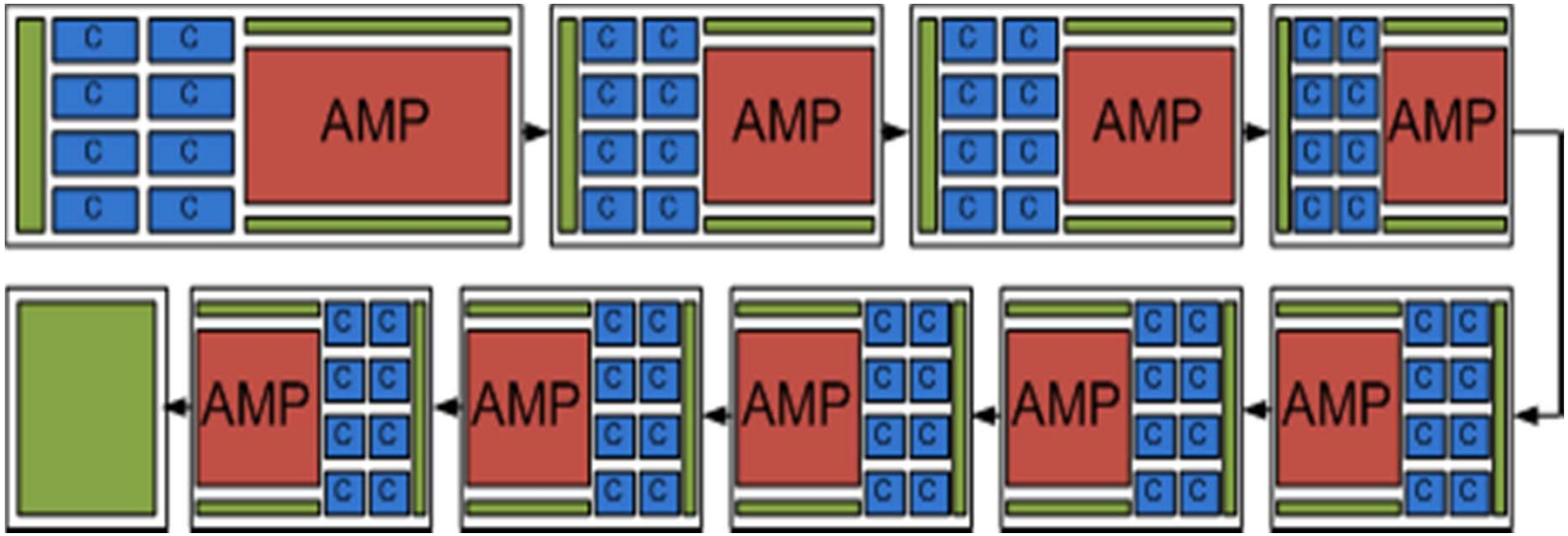


Things to consider within the Stage:

- Compactness of Stage Layout
- Critical Signal routing inside the stage
- Effect of Parasitic

Example (1) 12bit pipeline ADC Floorplan

The 'U' Shape

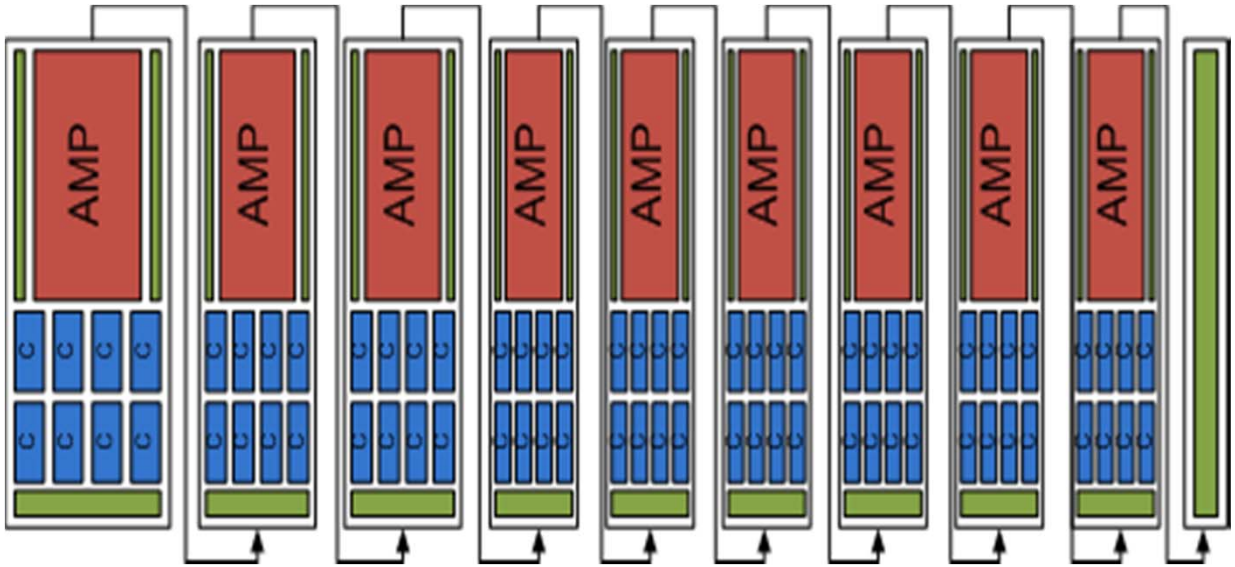


+ Results in simple layout of each stage
+ It can be easier to scale the stages

- The low res stages are close to the front end
- Distribution of the clock can be difficult

Example (2) 12bit pipeline ADC Floorplan

The ‘up-down’ floorplan

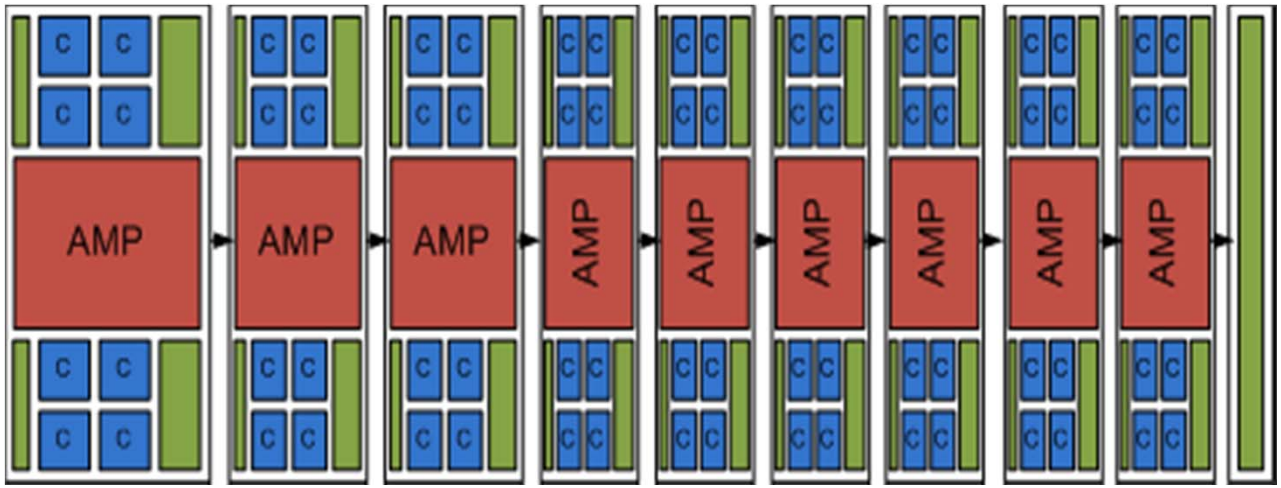


+ Distribution of clock is simple
+ Uniformity between the stages can be maintained
+ High-Res is far away from Low-Res

- Scaling of stages is difficult
- It’s difficult to balance the routing between Pos and Neg in a differential system
- In practice managing unwanted parasitic can be difficult

Example (3) 12bit pipeline ADC Floorplan

The ‘left-right’ floorplan



+ Distribution of clock is simple
+ Uniformity between the stages can be maintained
+ High-Res is far away from Low-Res
+ cross stage parasitic are minimized

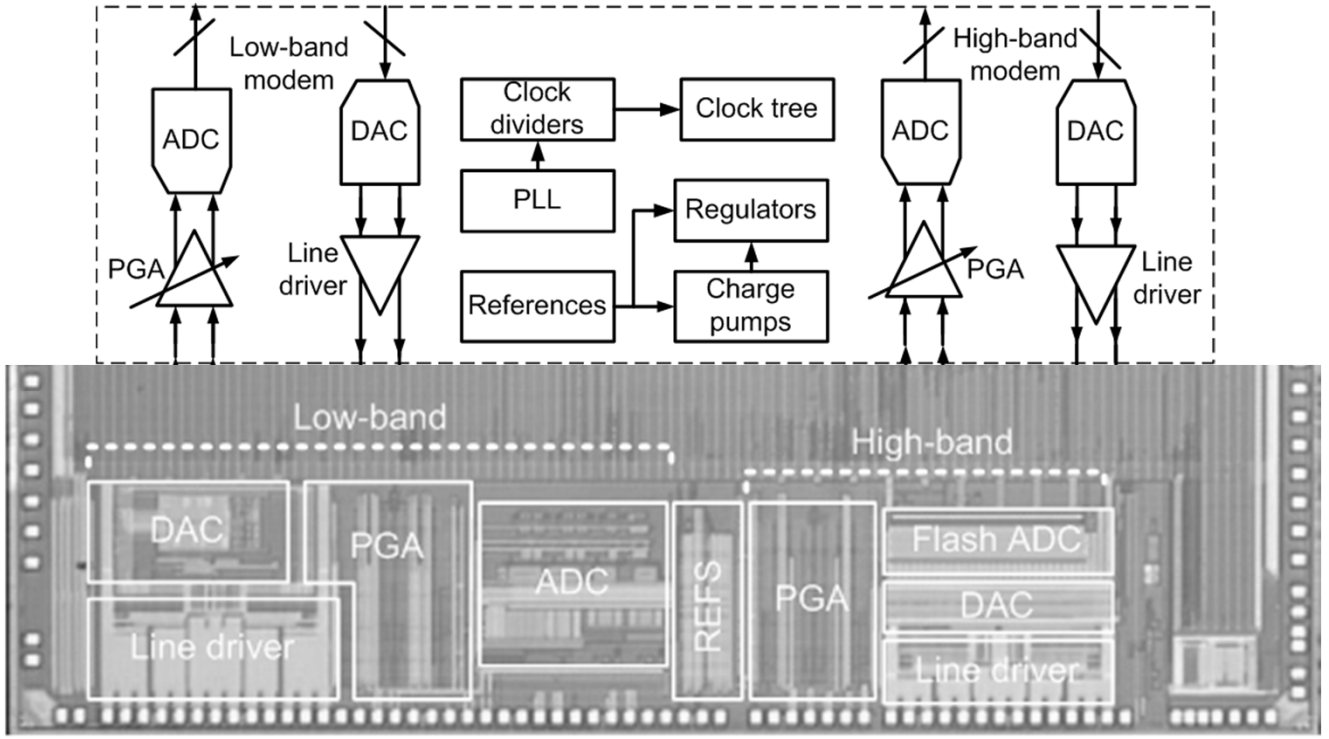
- Internal routing and layout of each stage can be very difficult
- Scaling of stages for power can require major rework.

Handling density

- The temptation exists to use the auto-fill method to meet density guidelines, but:
  - You don't know where it will place the dummy metal in your sensitive analog circuit
  - It will not take care of matching and above metal effects on devices
  - The only way to check the performance of the new parasitics is to extract and simulate, with very large netlists and run times.
- If you have a sensitive circuit:
  - Fill by hand, observing matching and symmetry
  - Use the dummy as shielding for sensitive nets
  - Exclude the auto-fill
  - Check the density in DRC with difference origin points (someone will drop in your block in a different place to where you ran DRC from!)

Chip/Macro level considerations

Analog macros/AFEs in SoC



- Need to consider
  - Separation of functions (e.g. RX/TX or bands)
  - Alignment to pins/pads
  - Power routing
  - Reference routing
  - Clock routing
  - Form factor
  - Signal flow
  - Proximity effects
  - Crosstalk
  - Gradient effects
  - Stress effects

Clock/digital

- Include known timing cells (buffers) at interfaces
  - At edge of AFE/DFE
  - At edge of each sub-block
  - Make sure there are known constraints on clock jitter, delay
  - Make sure the interface is insensitive to an asynchronous timing error.
- Factor in noise and mismatch into clock jitter, delay and duty cycle
  - Shield if necessary
  - Consider Including dedicated supply for clock
  - Use specialist buffer cells, or chains of inverters or differential buffers for distributing clocks
  - Watch for analog tracks crossing the clock, introducing noise

Handling Sensitive Analog

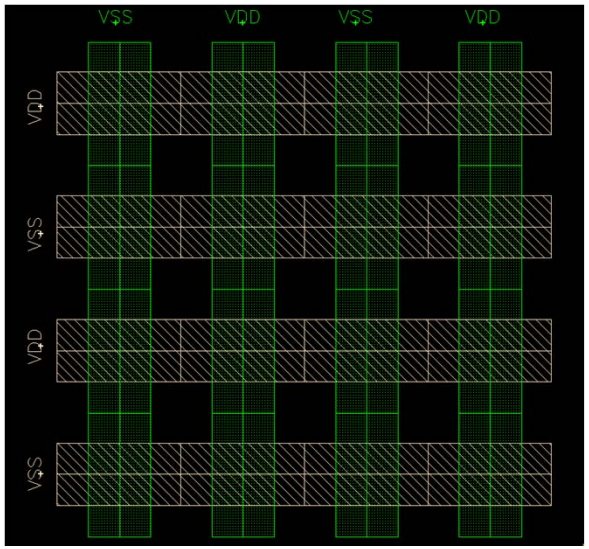
- Create separate shielded routing channels for
  - References (voltage and currents)
  - Analog signals
  - Clocks
  - Datapaths
- Use known ‘clean’ supplies for shields
- Distribute decoupling

SI (Signal Integrity)

- Definition:
  - http://en.wikipedia.org/wiki/Signal_integrity
  - The influence of neighbouring tracks on a digital signal
    - digital timing
    - glitches
- Causes of SI
  - Crosstalk
  - Power/Ground Noise
  - Reflection Noise
- Just because a signal is static does not mean that it can not be subject to SI
  - What would happen if 'PowerDown' got a glitch
- Why is it an issue?
  - Lots of digital signals 'routed/timed' by hand

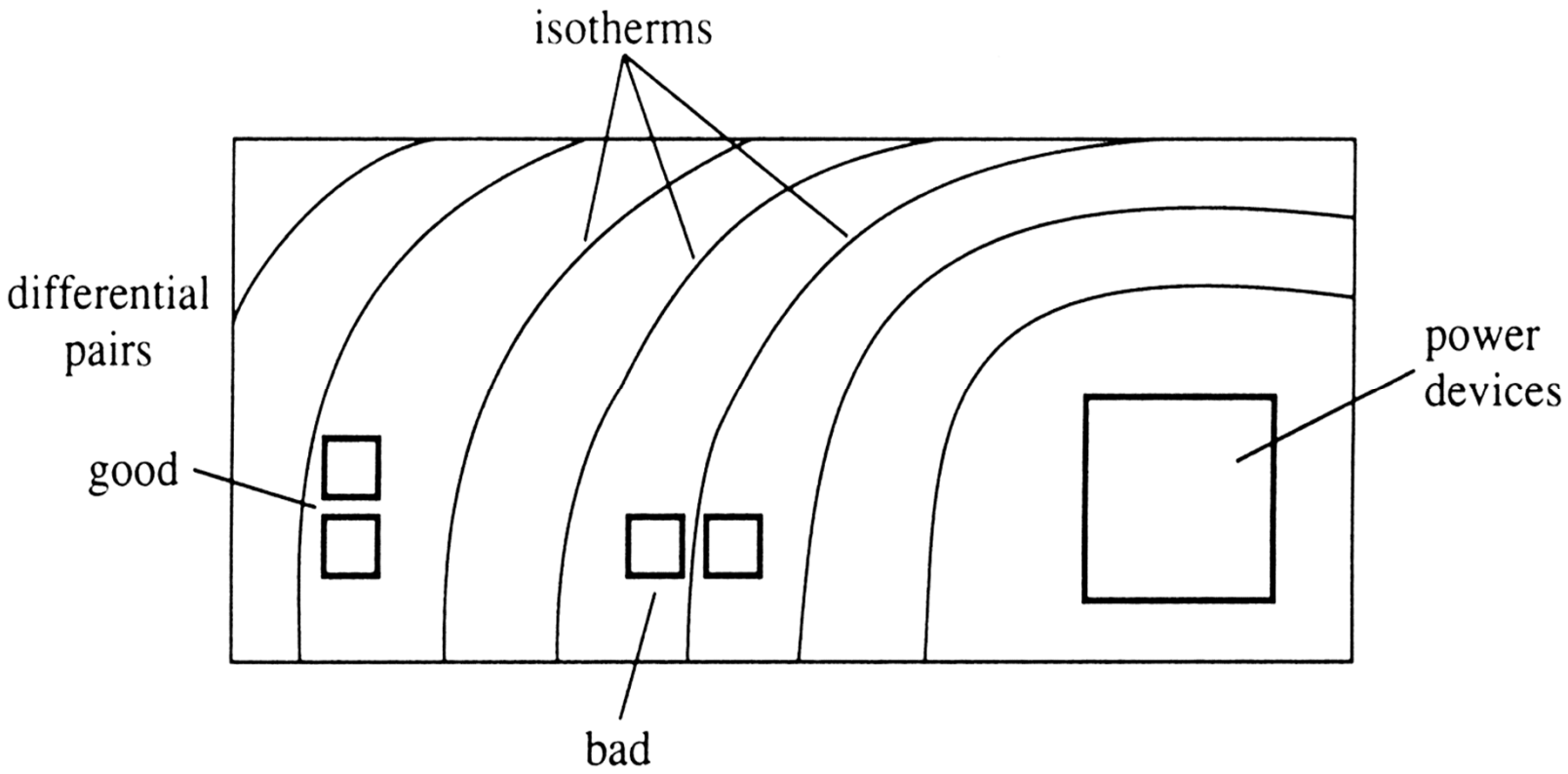
Handling Power Routing

- Try to get ‘thick’ top metal or RDL for Power routing
- Consider a grid
  - Define it upfront
  - Make sub blocks fit into it
  - Align within sensitive ccts



- Ensure symmetric positioning of power pads
- Model bond wire and pin inductances and resistances

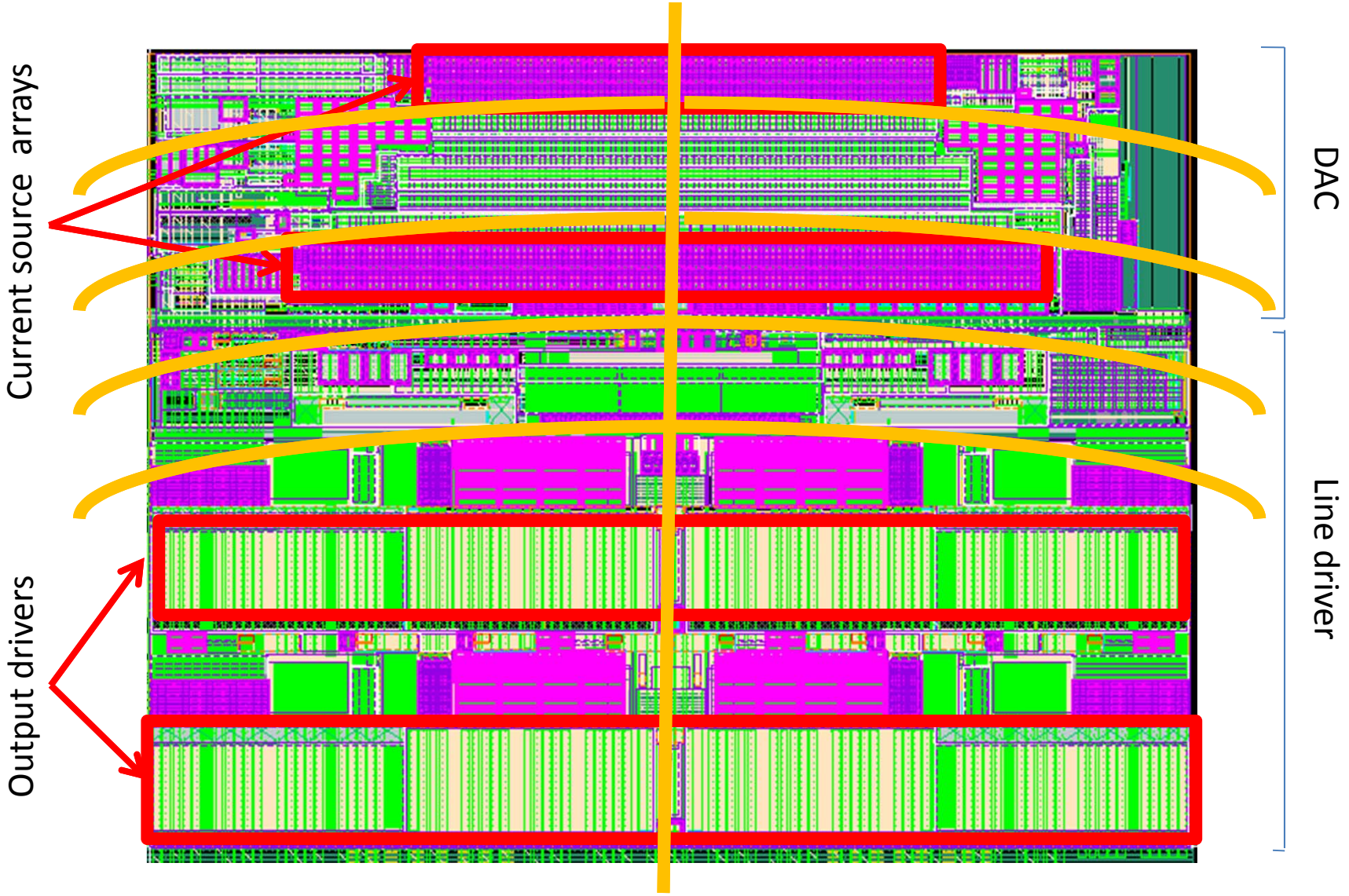
On same isotherm



Solomon, JSSC Dec 74, 314-332

Courtesy of Willy Sansen, KULeuven

Example: DAC + line driver symmetry on isotherms



Optimising your Design Flow

Layout Driven Schematic

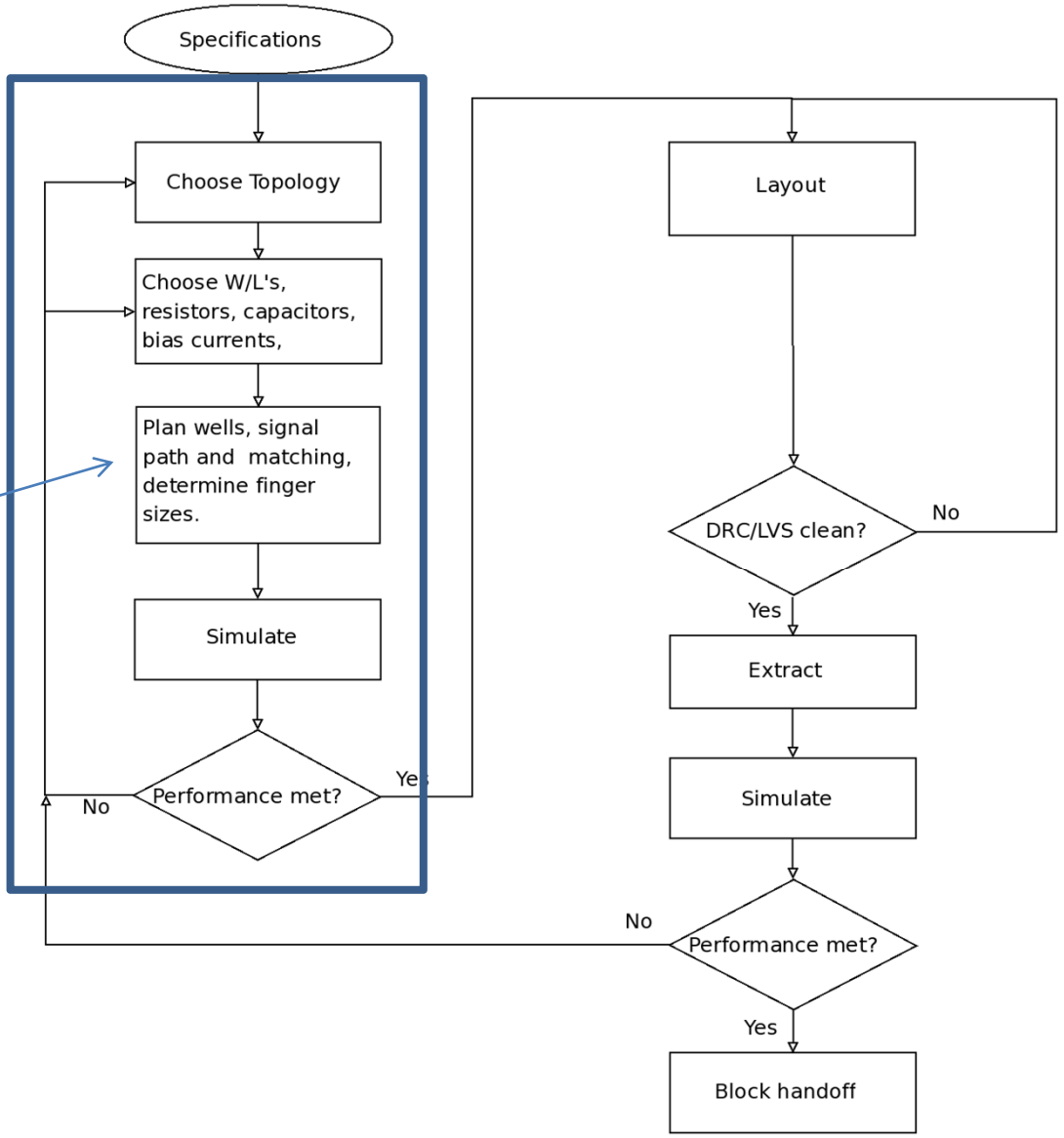
- What and Why
  - Early in process define transistors from what they will be like in layout
    - (A) Ensure SA,SB,SC, Capacitance, well effects (SCA,SCB.SCC) are what they will be in layout, not just W/L, M, NF
    - (B) Make the correct 'unit' size (plan ahead for any scaling/replica)
    - (C) Include 1st order routing parasitics
  - Use a flow that tries to 'match' A/B/C of your layout to be in your schematic pre-layout
  - Make your schematic like your layout floorplan
    - Can help lvs, extraction, iteration
    - All routing should be part of the sub-block layout,
    - This means that hierarchy can be used correctly when extracting, and performing extracted simulations.
- Latest evolution of CAD tools are at least recognising the designers 'intent' with constraint entry and checks

Layout Driven Schematic Flow

Increased Design Phase

Include as many effects as possible in here

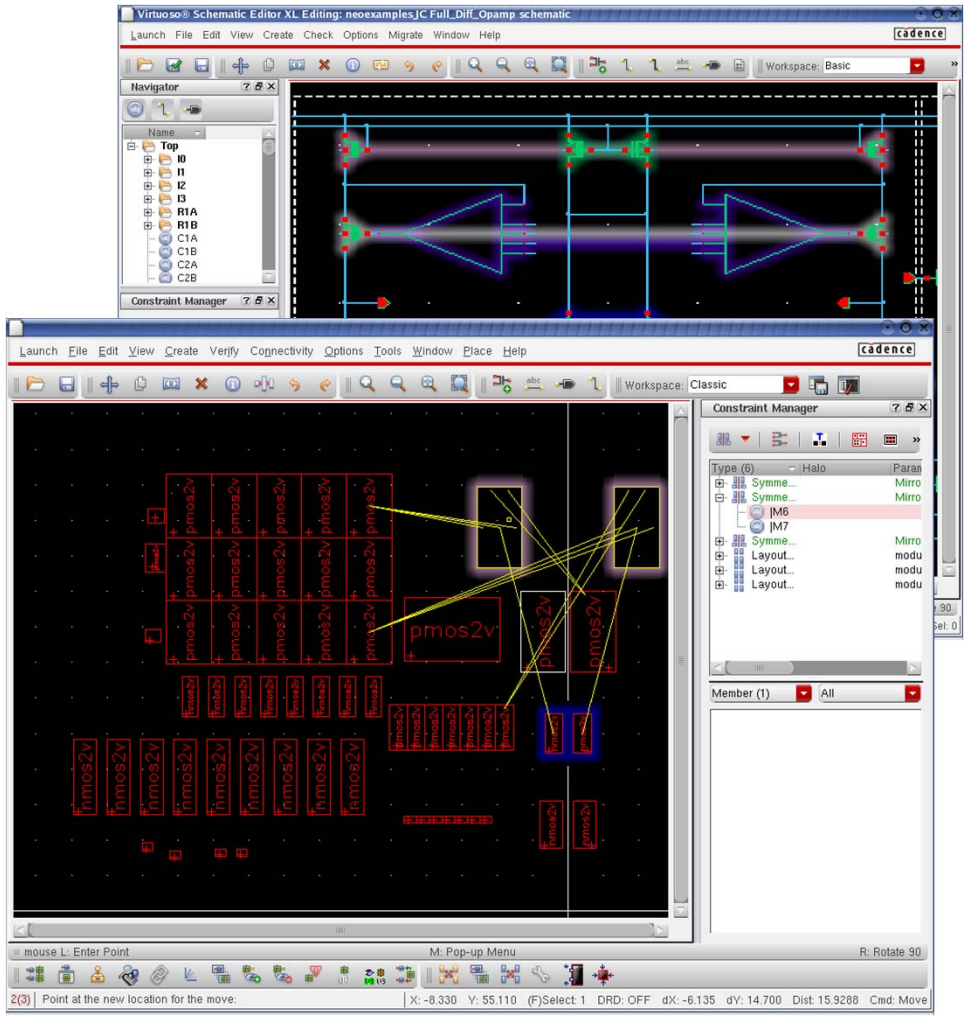
Try to match hierarchy of layout with schematic



Connectivity & Constraint Driven Layout

Superior Communication of Design Intent

- Constraints formally capture and maintain *designer intent* throughout the entire design cycle and across all the design teams
- Common Constraint Manager
  - Common entry and visualization across platform tools
  - Easy and fast constraint creation
  - Automatic transfer from schematics
- Circuit Prospector
  - Automated constraint capture using default and user defined templates
- Constraint Aware Layout Editing
  - ~20x improvement over IC 6.1.1

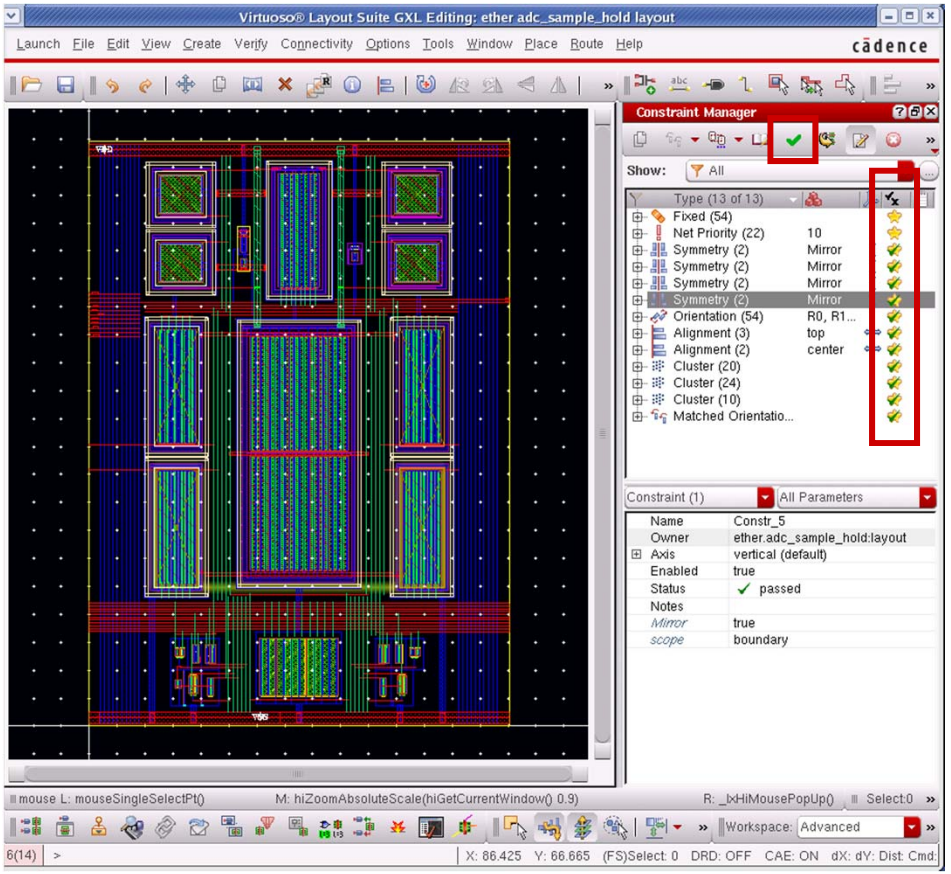


Courtesy of Cadence Design Systems

Fast Validation of Design Intent

Built in “1-Button” Constraint Verification

- Capture and validate your design intent as constraints on the schematic or layout
- What used to require visual inspection taking hours, can now be complete in minutes
  - Can be done before, during or after physical implementation
- Constraint entry takes less time than adding schematic notes
- Constraint Verification
  - Constraint checker accessible from a single button to verify all constraints



Captures, Track, and Verify constraints

Courtesy of Cadence Design Systems

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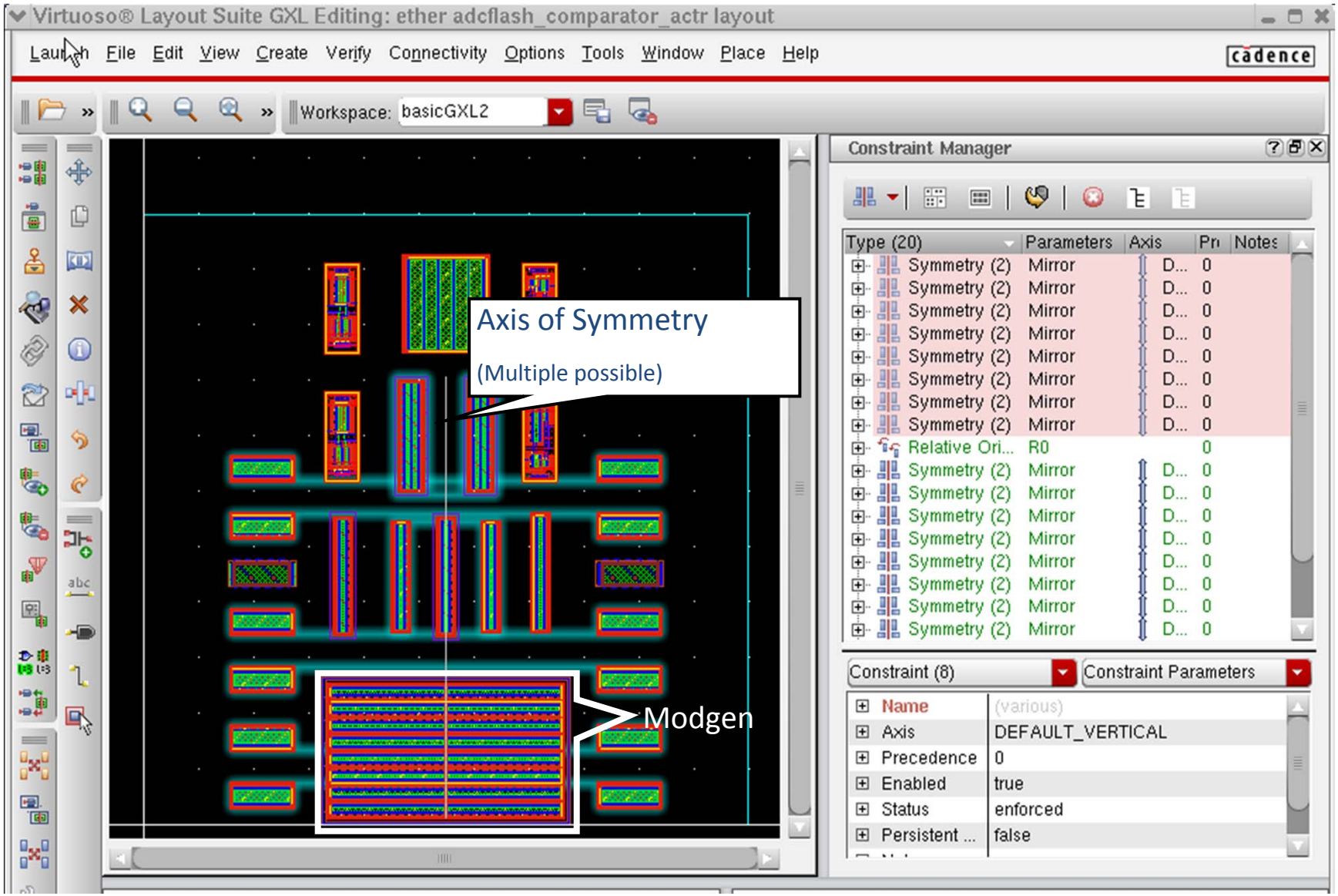
Constraint Compliance: Analog Placement



Courtesy of Cadence Design Systems

Set-up the flow correctly

- Most CAD flows are set-up for digital
  - The accuracy of the results for analog depends on
    - The tools
    - The PDK
    - The parameters chosen
    - The user procedures
    - The number of users (= amount of debug) !!!
- If in doubt (or do it anyway)
  - Put down dummy test structures in layout, and extract, check AD/AS, PD/PS, SA, SB, SC, etc are extracted correctly (manually check the netlist)
  - Put down test structures for metal resistance and metal capacitance matching those shown in the DRM, extract them and compare to the DRM number

Understanding the Optimization

- Most extraction tools have reduction algorithms:
  - Removing Minimum R and Minimum C
  - Merging Parallel R
  - Merging Series R
  - Frequency dependent RC reduction
- Understand in what order these occur.
  - If MinR removal is happening before merging, you could lose a much bigger effective resistance.

Example, CAD Tool set-up challenges - IR Drop - Extraction

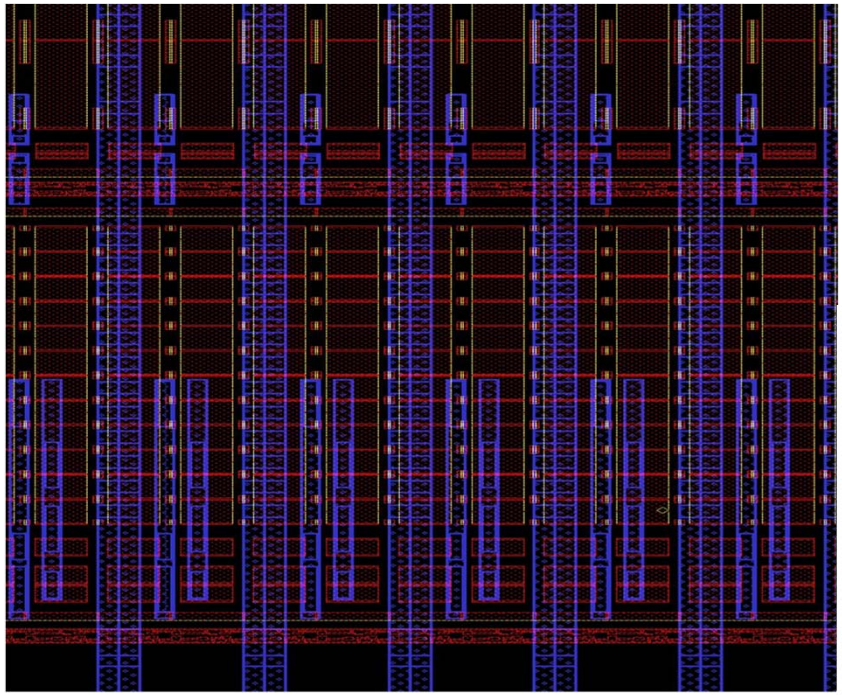
- Using the Extraction Tool correctly is critical in catching problems due to IR drop.
  e.g. unwanted IR drop in a regulator feedback path.

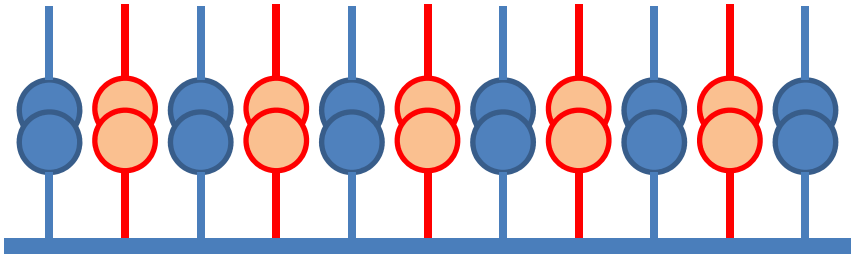
- Choose correct min R
  - too small and you get too many nodes to simulate
  - too large and you miss the important resistances
- Position of labels extremely important!!
  - Labels can short out IR drop at a particular layout level!
- Don't ignore supplies (don't assume they are perfect!)
  - Need to place labels to replicate all the supplies to a block
    - e.g. can have non-functioning circuit with an extracted netlist if only one label on a small piece of metal one at a corner of a block.

Some Examples of Layout Issues

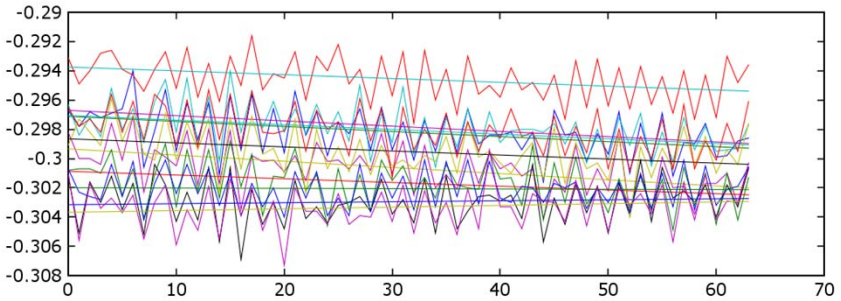
1. Metal effect DAC current source matching
2. Metal-metal capacitance degrading a S/H circuit
3. Common Centroid degrading a precision switch cap integrator gain stage
4. SI issue on a DAC control bit when placed inside an AFE

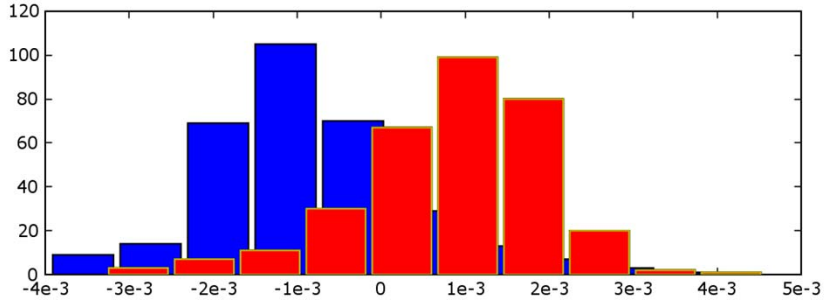
(1) Metal induced error in DAC current source array





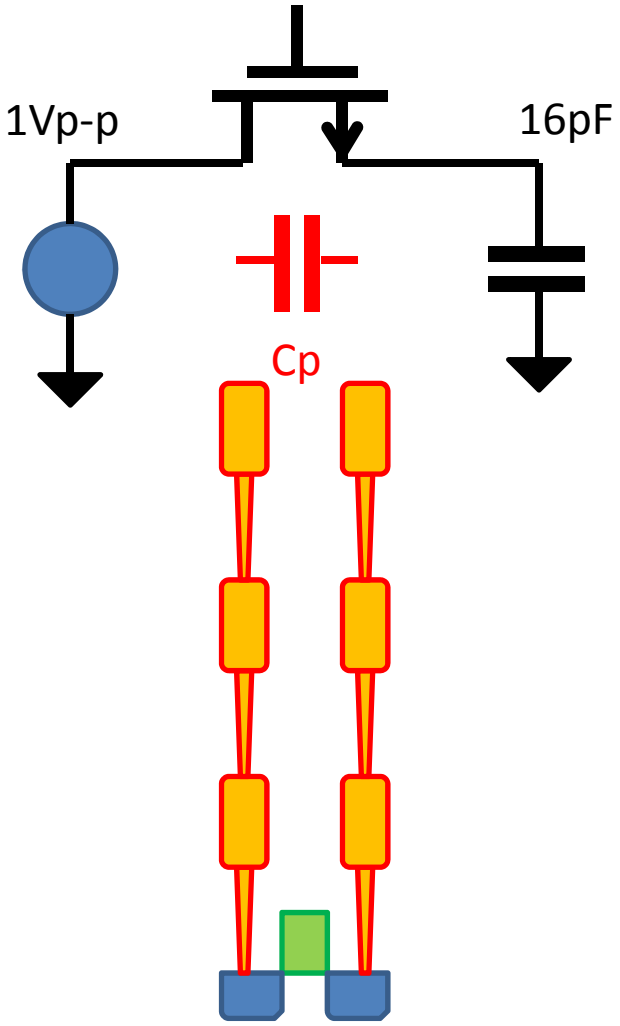
- Current sources were 100% identical
  - EXCEPT Metal 5 which has a delta for odd/even current sources
  - Measured delta ~1% !!!
- It is not only bottom metal that matters





Solution: Replicate Metal 5 pattern over all current sources

(2) S/H leakage capacitance issue



- What could be so difficult
  - Depends on accuracy and BW
- For 16b accuracy
  - Cp needs to be < 120aF
  - Easily generated by parasitic metal across the switch (~1u wide metal)
- Easily missed as the value of capacitance is often ‘filtered’ or ‘lumped to GND’ by the extraction tool
- Compounded by dummy switches and complementary switches and common centroid layout

Solution: Increase M1 spacing ,fan out after M1, and insert GND shield

(3) A Precision SC Integrator with Variable Gain (Cap-DAC)

Application:

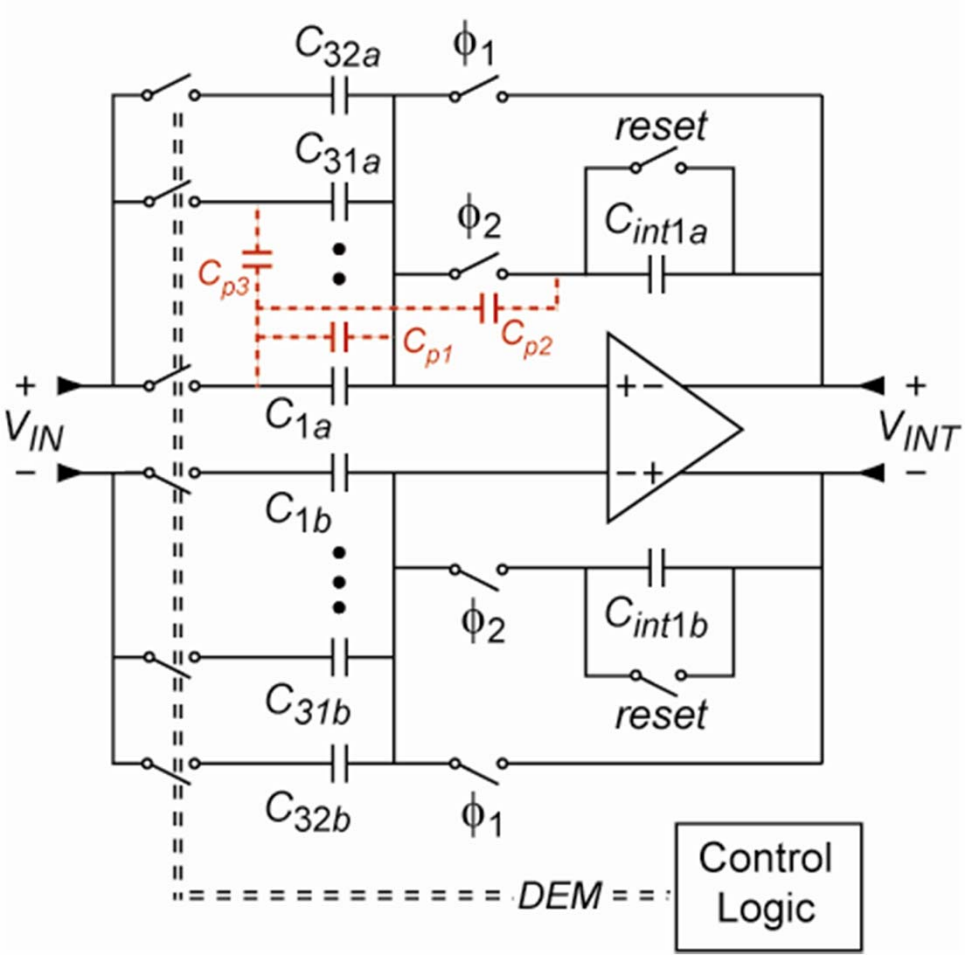
precision smart temperature sensors

Requirement:

accurate (up to 16 bit) gain

Approach:

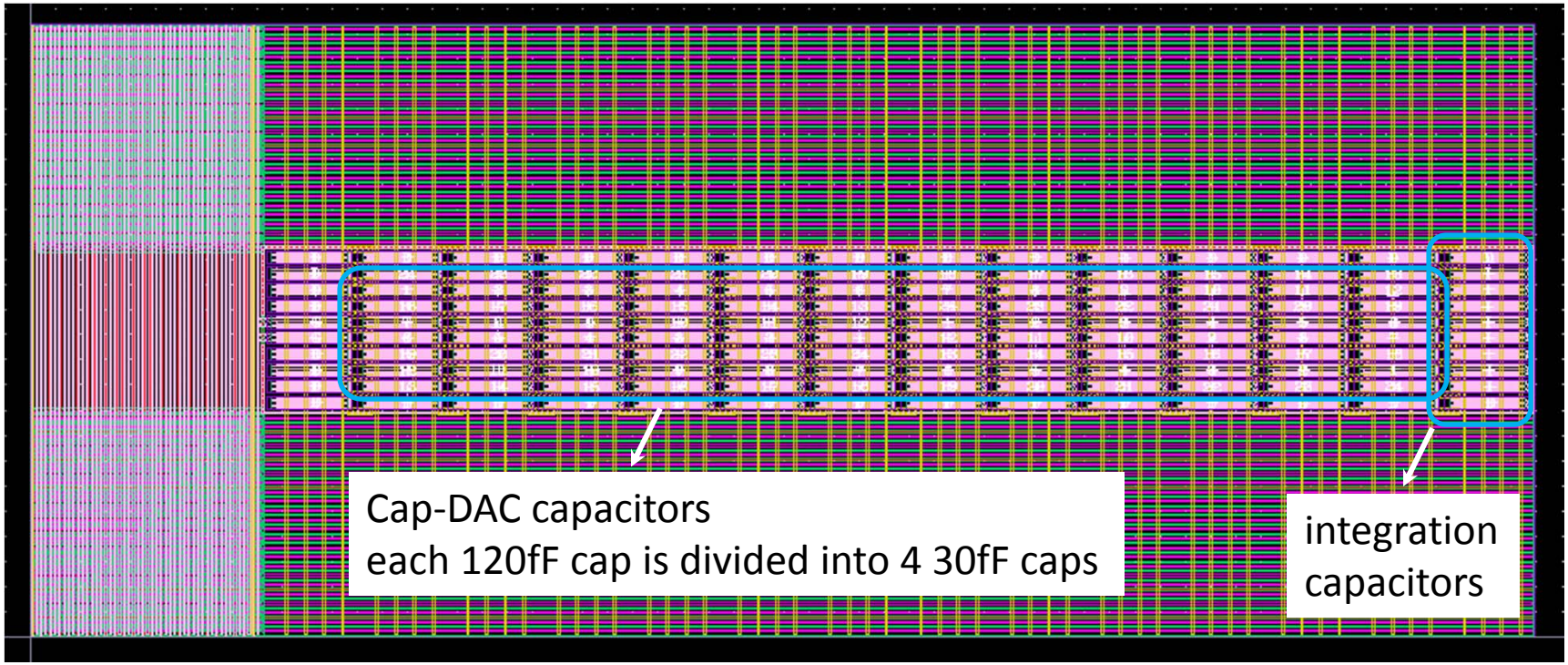
- Initial accuracy (up to 11 bit)
  - sizing
  - common-centroid layout
- Use of DEM



A 5-bit Cap-DAC

Courtesy of Kamran Souri, TUDelft

Is Common Centroid always a good idea
Initial Layout



Common-centroid pattern (Each cap = 4 unit elements): for better matching, but

- long interconnects ⇒ large cross-coupling, mismatch
- cross-coupling ⇒ shield needed for the interconnects, caps
- mismatch ⇒ use the same metal layer for interconnects

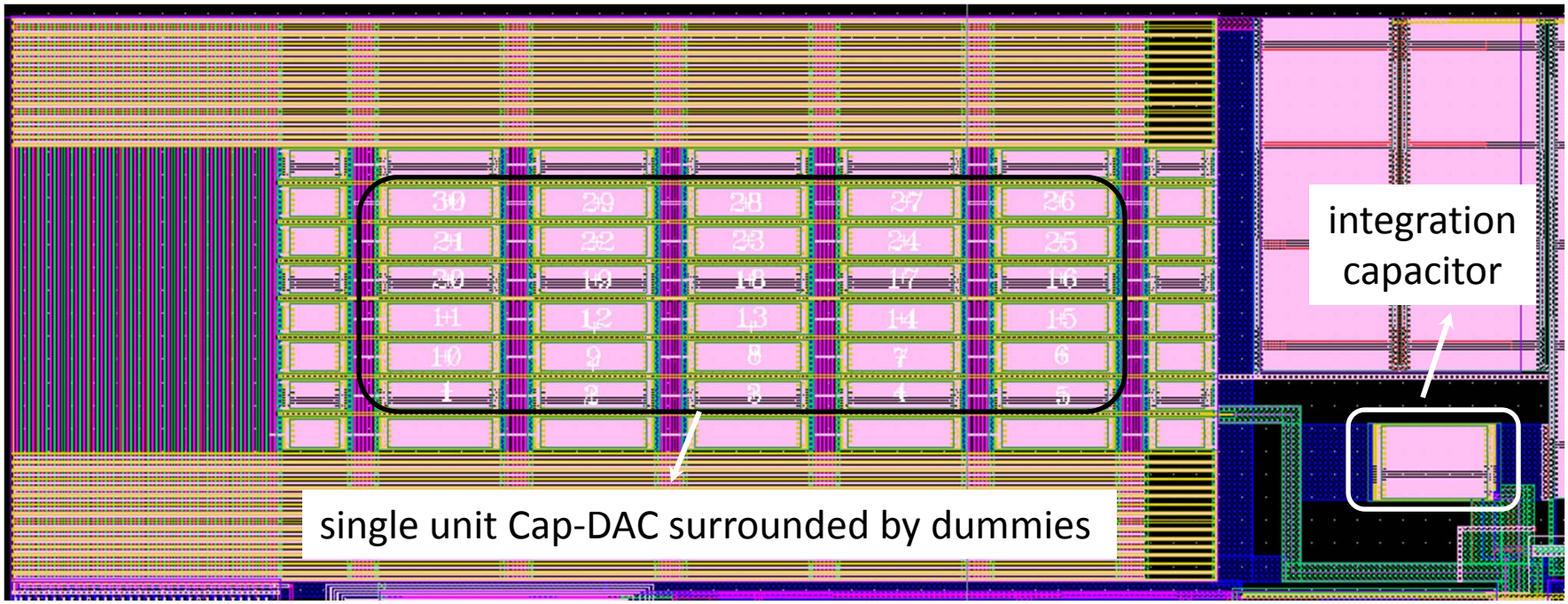
Co-located Cap-DAC and integration capacitors for better matching, but

- Cross-talk gives input dependant gain ⇒ large non-linearity

Result: large area for interconnects (70% of total), and poor matching , and inaccuracy

Courtesy of Kamran Souri, TUDelft

Improved Layout



Single unit cap instead of common-centroid pattern

⇒ shorter interconnects ⇒ less area

Perfect shielding of capacitors and sensitive nodes

⇒ much less cross talk

Separate integration capacitor

⇒ no leakage from the input to integration cap ⇒ accurate gain

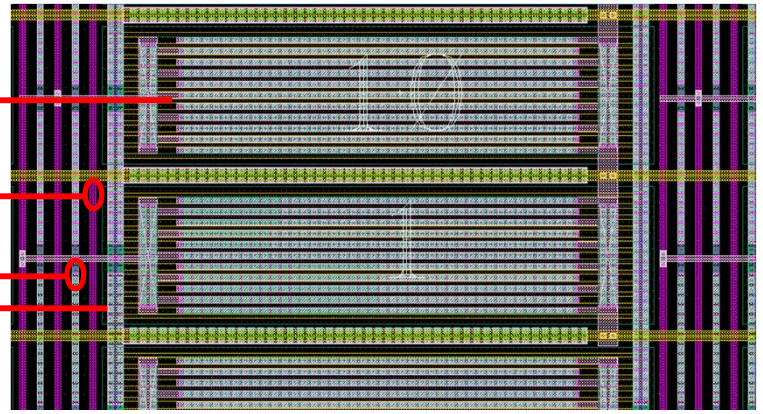
Courtesy of Kamran Souri, TUDelft

Additional Layout Details

Shielded fringe capacitor

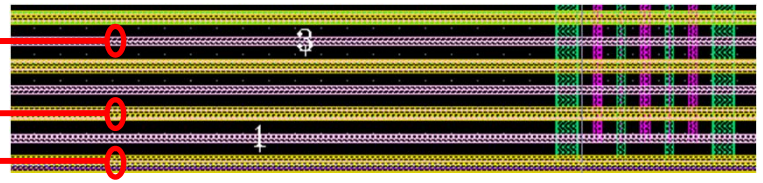
Interconnect

Shields (M_1-M_4)



Interconnect

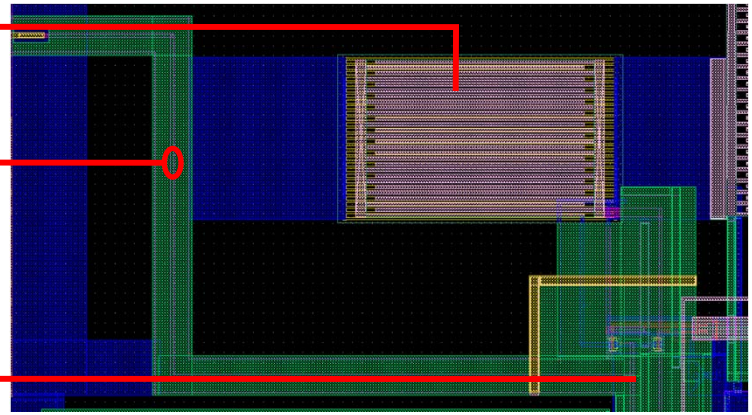
Shields (M_1-M_5)



Isolated C_{int}

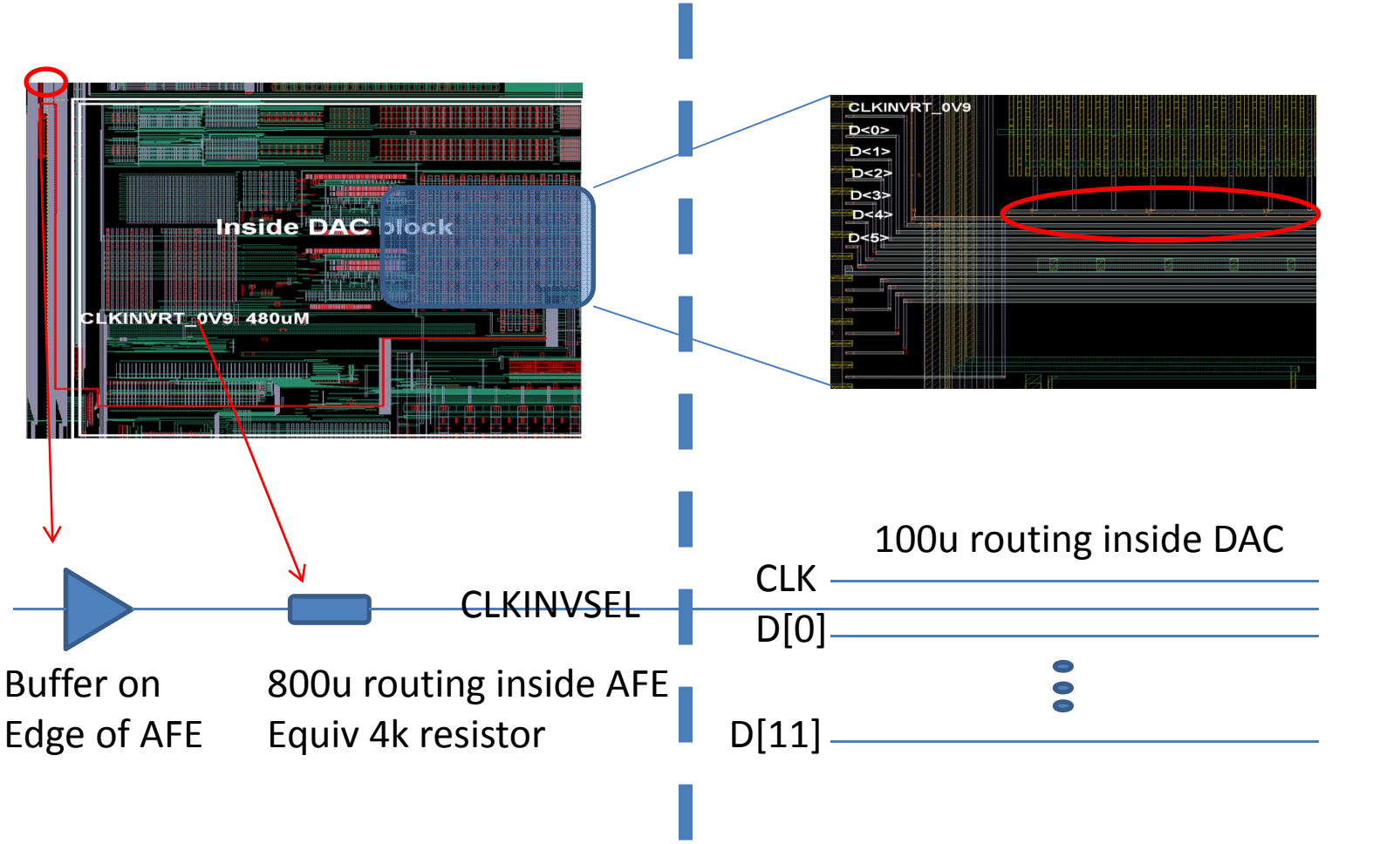
Shielded
virtual ground

Shielded switch-capacitor
interconnects



Courtesy of Kamran Souri, TUDelft

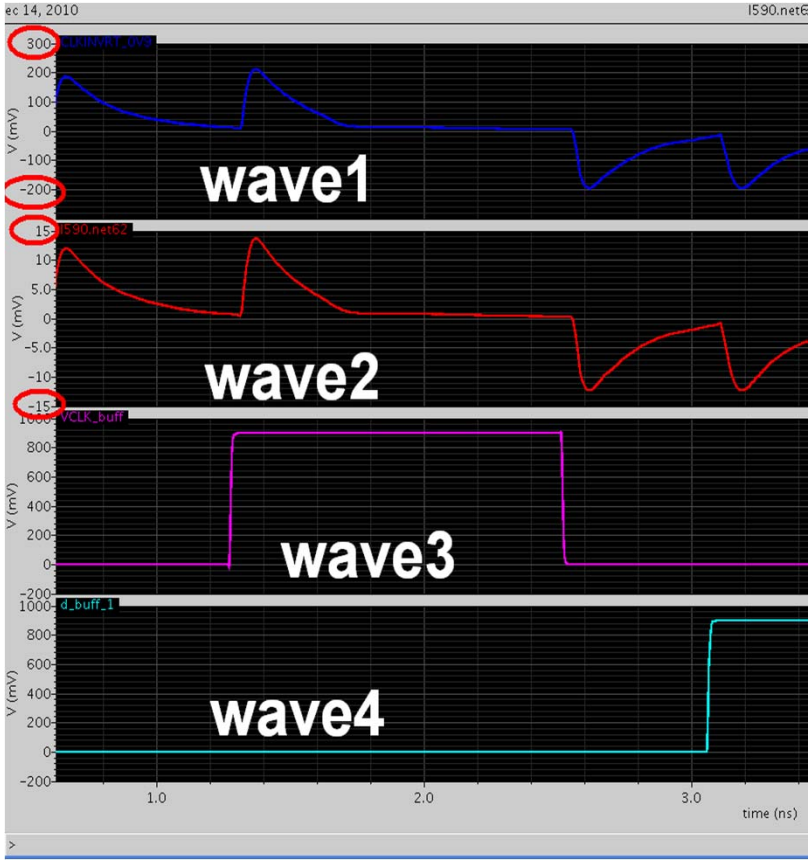
(4) DAC SI issue when placed in AFE

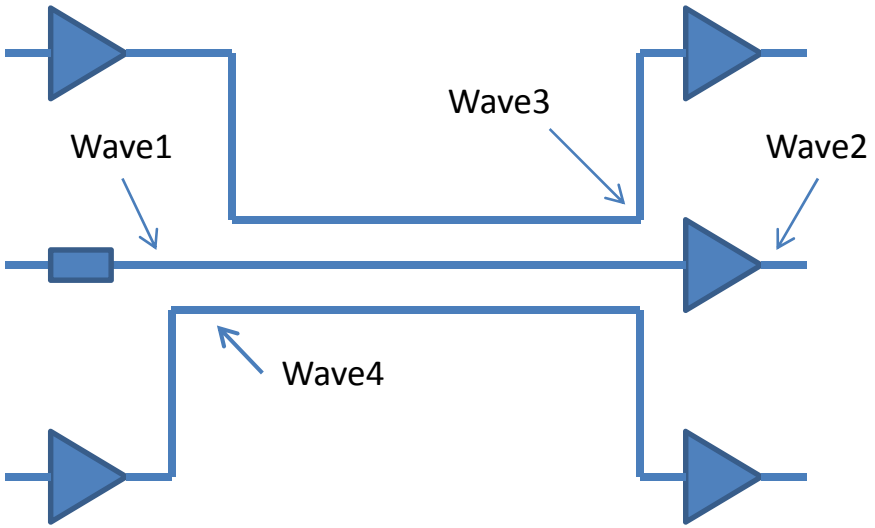


SI issue when extracted/simulated at top level

NO SI issue when extracted/simulated at block level

DAC control bit Example





- Solution:
  - Buffer at the edge of the DAC block
  - Separate tracks by more than min spacing

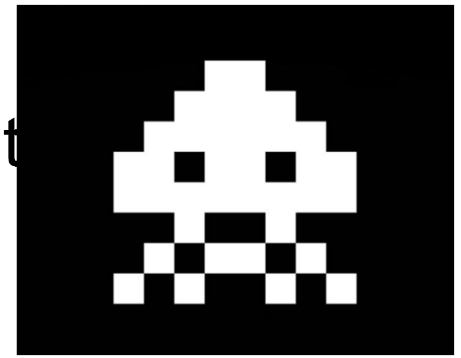
Summary

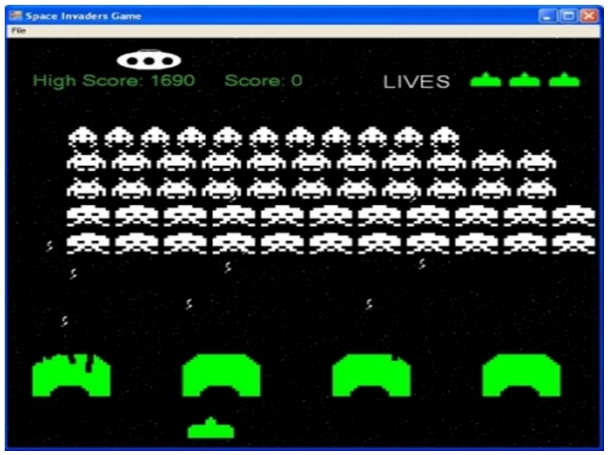
Advice

- Everyone is a novice in a new technology.
  - Be paranoid (especially about CAD and CAD setup)
  - Predict parasitics and transistor partitions in the topology, don't believe the results unless you expect them
  - Decide 'WHAT' is important for your circuit
  - Don't be afraid to rip it up and start again
  - Floorplan, power, clock, signal flow early in planning
  - Modular schematics to match modular layout
  - Symmetry is only perfect with a repeated block
    - There is a reason many layouts look like space invaders
  - Dont be a slave to the automated tool

Disclaimer 2

- I'm sure there are other effects and approaches not covered here
  - it is all born from my 'collective' experience, it is not a definitive list
  - There will always be new ones
  - Every 'circuit/technology' is different
- So ...
  - Its **still** your problem
- But
  - **Good** luck.





I'm serious about the space invaders, just in case some of you didn't know what they are