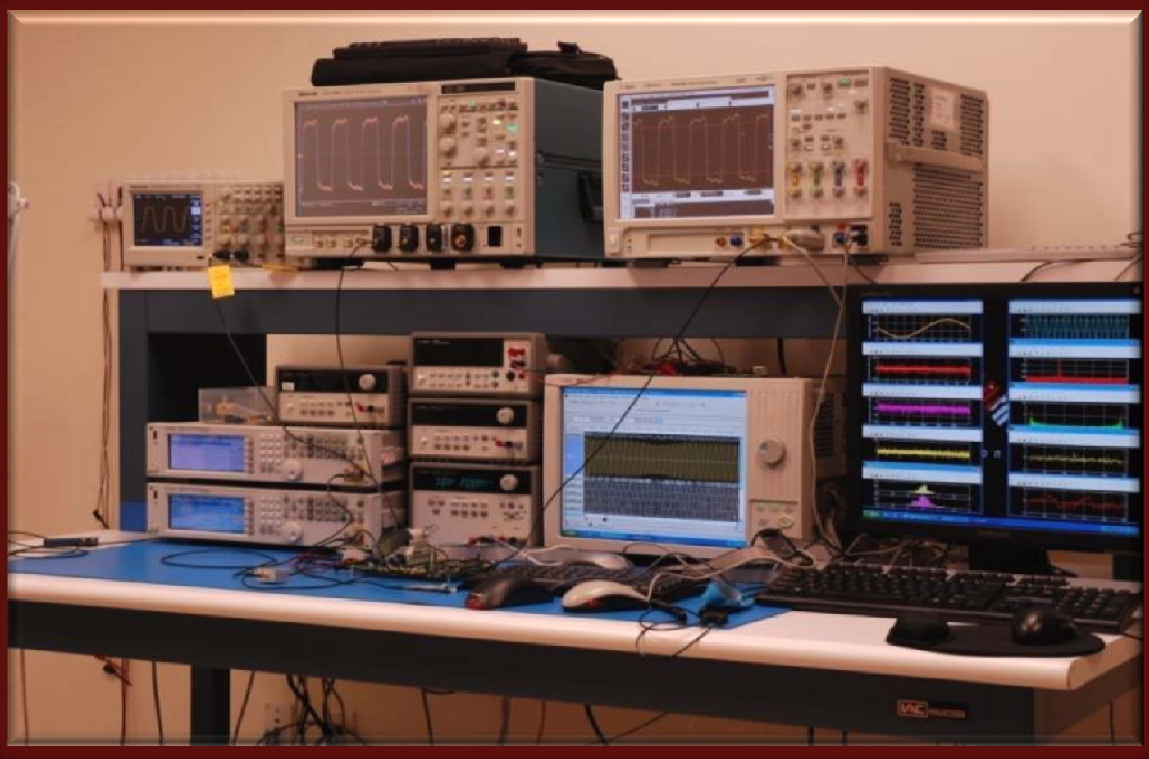
Seamlessly Blending Analog and Digital

TUTORIAL

ISSCC 2010

Specifying & Testing ADCs

Aaron Buchwald, PhD



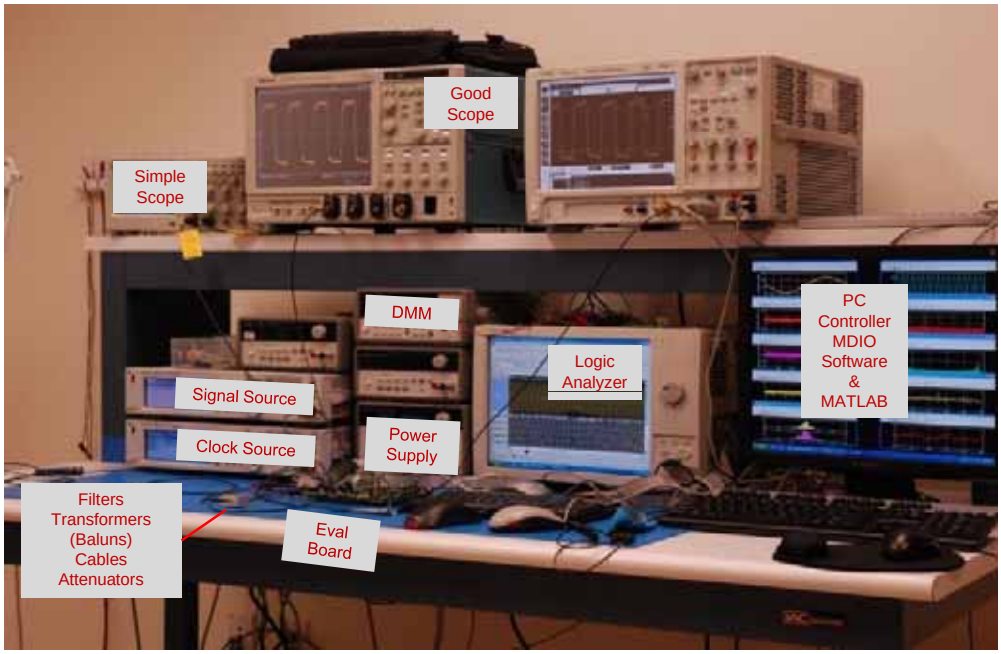
Mobius Semiconductor Inc.

Tutorial #3:
Specifying and Testing ADCs

Aaron Buchwald, PhD
Mobius Semiconductor

Sunday
07 Feb 2010

Let's Get Started: What Should I Measure?



Does someone have a list of specs?

List of Specifications

ADC Specs (some)
Offset
Gain Error
Missing Codes
INL
DNL
SNR
SFDR
THD
SNDR
NPR
MTPR
IM2
IM3
IP3
ERBW
BER
Aperture uncertainty
Aperture delay
Power
FoM

Lets take these specs one at a time and read the definitions:

IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters

IEEE Std 1241-2000

OK. Lets NOT

I'm more concerned with debug, understanding and gaining insight to improve the next generation of designs rather than just verifying information on someone's data sheet

Puzzle Solvers

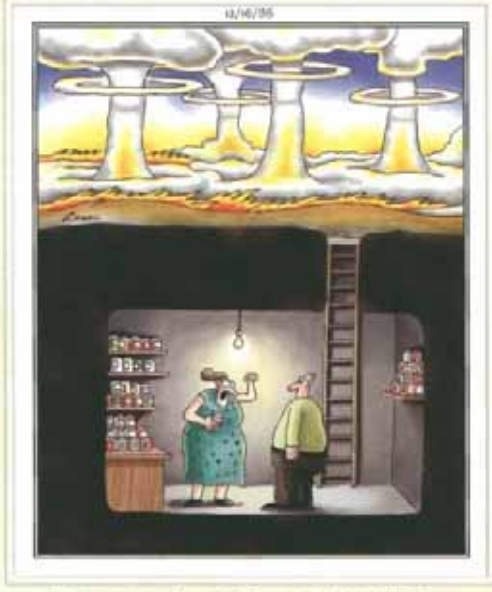
- ADC Testing is like solving a puzzle
  - Methodically and calmly extract and analyze data
  - Design experiments to isolate problems
  - Similar to solving mysteries, or determining a diagnosis

- One big difference with respect to puzzles – in ADC testing you don't know, a priori, if a "solution" exists

First Lesson: ADC Testing Starts in the Beginning

Know your specs and metrics

Know how to measure them



"How many times did I say it, Harold? How many times? 'Make sure that bomb shelter's got a can opener—ain't much good without a can opener,' I said."

Know how to observe and control all key aspects of the circuit for debug & optimization

Gary Larson, ***The Complete Far Side 1980-1994 (2 vol set)*** Andrews McMeel Publishing; 1st edition (October 2003). **ISBN-10:** 0740721135

180 Seconds of Philosophizin'

1st Silicon Success

- First-Silicon Success
  - To the audience: Who here gets first silicon success all the time?
  - Raise your hand
- Optimal specification for every application
  - Audience: Who here knows the set of specifications to achieve optimal system performance at minimal cost area and power?
  - Raise your hand
- Welcome to the real world
  - You people who answered, “Yes” can leave
  - This course is for the rest of us who occasionally encounter problems and need to test and debug

The “Worked in First-Silicon” Lie

- Goals are
  - Solve existing problems, most efficiently
- Tools cost several $100k, manyear ~ $300-500k
  - A year of simulation is not necessarily a good idea
- New issues are only discovered when trying something new
- New techniques only get invented when trying something new

“Hey! Look what Zog do!”

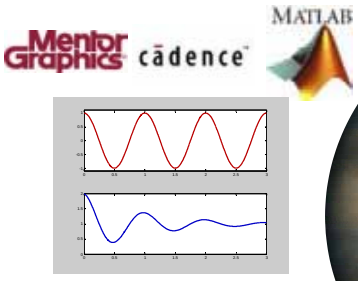
Gary Larson, ***The Complete Far Side 1980-1994 (2 vol set)*** Andrews McMeel Publishing; 1st edition (October 2003). **ISBN-10:** 0740721135

Testing and Specifying are In "The Real World"

Hemisphere of Design ⟵ ⟶ Hemisphere of Experience

Most of the IC Design world (Especially Digital) Doesn't like it over here

Simulations



I'm uncomfortable with ambiguity

Shouldn't everything be either "1" or "0"

Books and papers

Testing and Specifying are In "The Real World"

It was at that precise moment Stanley realized that he may very well be a brain in a vat.

Philosophy of Science: What is Knowledge?

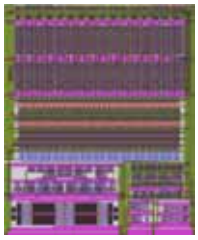
Brain in a Vat

Online available http://en.wikipedia.org/wiki/Brain_in_a_vat

I used to work here BROADCOM Now it's BLIZZARD

The idea that we can leave our vulnerable bodies while preserving relevance, learning, reality, and meaning has permeated society

Internet social networking
Long distance learning

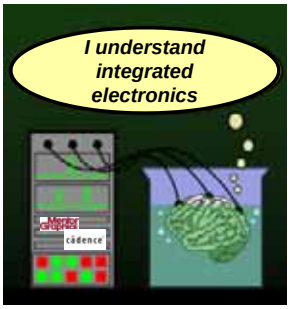


Making These

They make this

Disconnect from Reality in IC Design Industry

Brain in a Vat



Online available http://en.wikipedia.org/wiki/Brain_in_a_vat

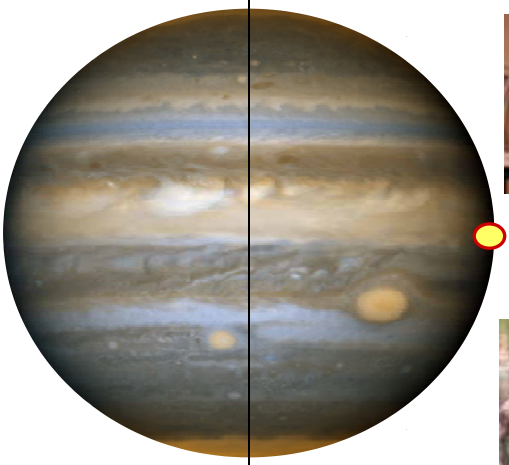
Fabless Semiconductor companies with hierarchical design groups and more reliance on CAD tools means very few people actually make the vital connection with reality

"The difference between the mathematical mind and the perceptive mind: the reason that mathematicians are not perceptive is that they do not see what is before them….. the mind …. does it tacitly, naturally, and without technical rules.

-- Pascal

Spend Some Time on the Dark Side

Hemisphere of Design ⟵ ⟶ Hemisphere of Experience



Experience is what you get when You don't get what you wanted.

Finish, Testing

Start, Specs

This is the most satisfying task in engineering

The Path to Enlightenment: Specs, Design & Testing

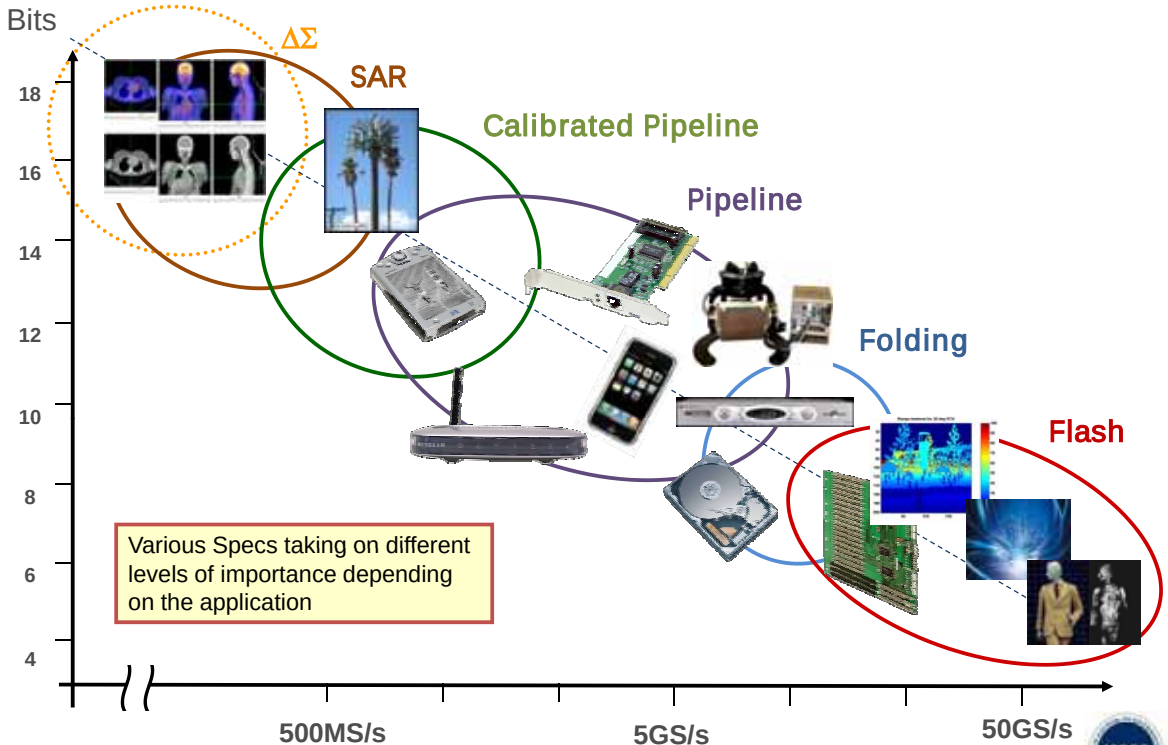
Sagrada Familia, Staircase
Barcelona, Spain
Antoni Gaudí

Staying in the comfort-zone between 90^0 and -90^0 without entering into the world of testing and specifying limits any real progress

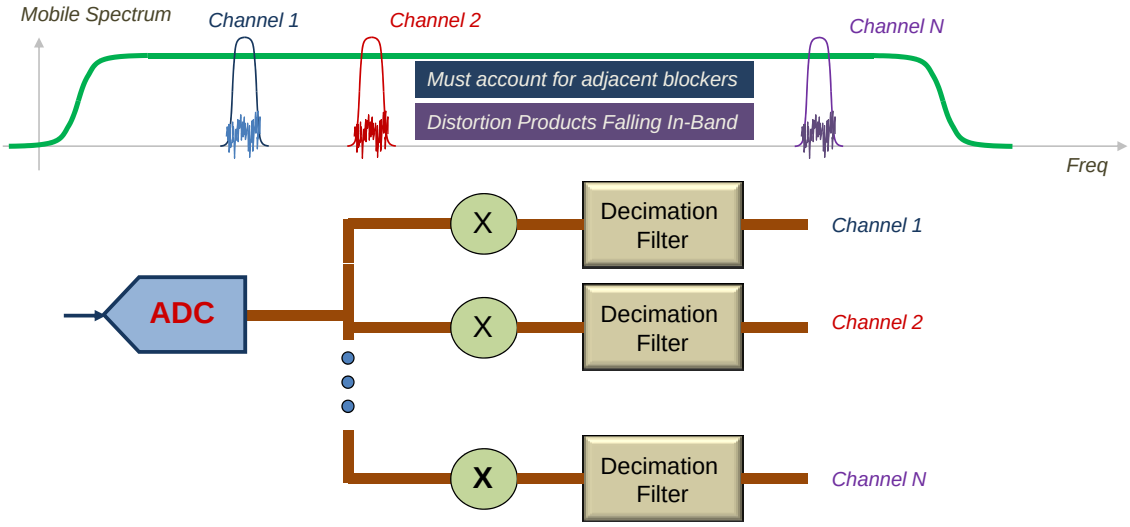
The path to progress is like a DNA spiral. By traversing the circle from 0^0 to 360^0 many times, we gradually ascend

Specifying ADCs

Architecture vs. Speed and Resolution

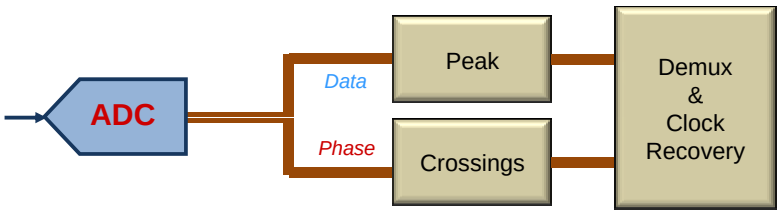


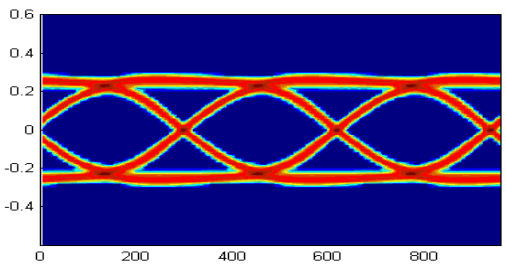
Requirements Differ in Various Systems: Narrowband

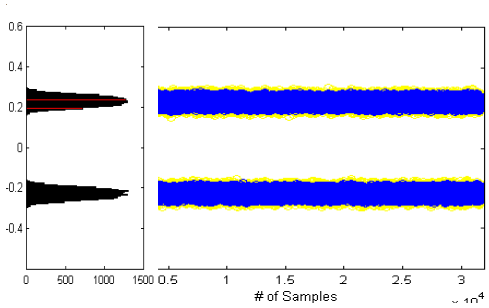


- **Linearity High**
  - Prevent nonlinear mixing products from falling in-band
- **Noise Less Important**
  - Processing gain due to narrowband filtering
- **14-16 bit linearity with 12-bit noise (typical)**

Requirements for Broadband







- **Linearity Low**
  - System is forgiving of smooth nonlinearities
- **Noise & Metastability Important**
  - Noise impacts BER directly
  - BER (Metastability) in ADC = BER in data

What are the Important Specifications?

SFDR
MTPR
NPR

Base Stations

SerDes

BW
BER
SNR

BER
Metastability

Scopes

Optical

Aperture
Jitter
SNR

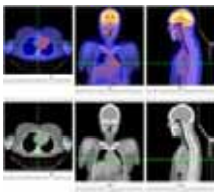
Power
THD
IP3

Mobile

Audio
Video
Touch

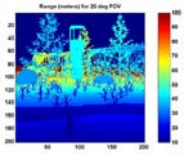
Power
INL
SNR

SNR
INL
THD



Medical

Radar

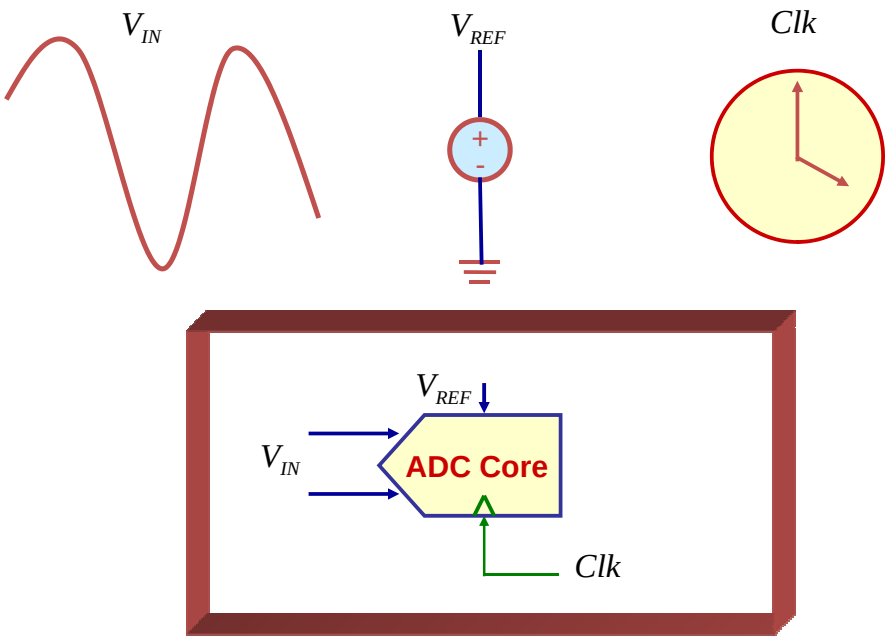


BW
Aperture

From faculty.washington.edu/kinahan/petct.html

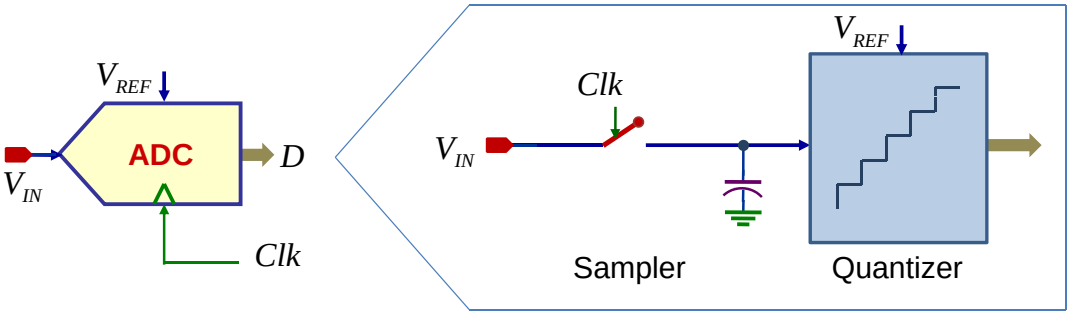
Preliminary Considerations

ADC is a Three-Input Circuit



ADC Performance depends on ALL THREE inputs

Sampler & Quantizer

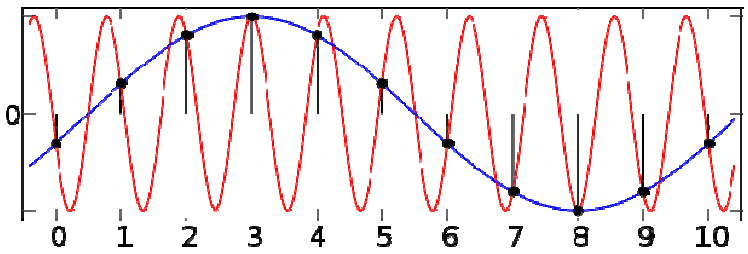


Primary functions of the ADC consists of sampling and quantizing. These can be treated separately

Note: Not always, non-uniform time-stamp ADC does NOT have typical aliasing characteristics

[1] Yannis Tsividis, Data Conversion and Digital Signal Processing without Sampling, "*ISSCC SE4: Unusual Data-Converter Techniques*, Feb, 2008.
[2] B. Schell and Yannis Tsividis, A Clockless ADC/DSP/DAC System with Activity-Dependent Power Dissipation and No Aliasing, "*ISSCC Digest of Tech. Paper 30.6, Feb, 2008*.

Sampling Can Cause Aliasing



Two input signal frequencies occupy same sampled frequency

Red is aliased
Blue is not aliased

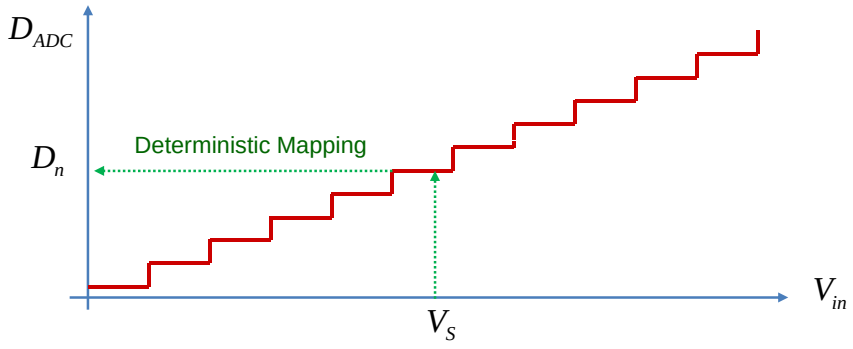
Aliasing in spacial domain

Moiré pattern

Not Aliased

From http://en.wikipedia.org/wiki/Nyquist%E2%80%93Shannon_sampling_theorem
http://en.wikipedia.org/wiki/Aliasing

Quantization is NOT Noise

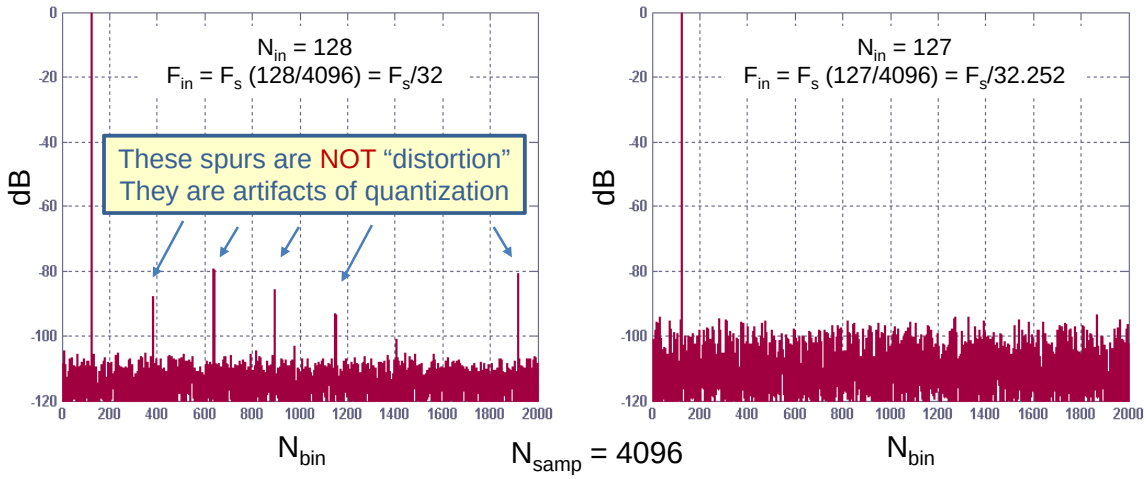


- Mapping from V_s to Codes is completely deterministic
  - No Random Noise
- All spurs are harmonically related to the signal
  - No random modulations
- For uniformly distributed "ideal" quantization, all frequency content is NOT equal in power
  - Spectrum is NOT "white"
- Difficult to model and track high-order nonlinearities due to quantization
  - We assume the noise is "white"
  - Consider only first 10-20 harmonics as "distortion"

Harmonic Content Example

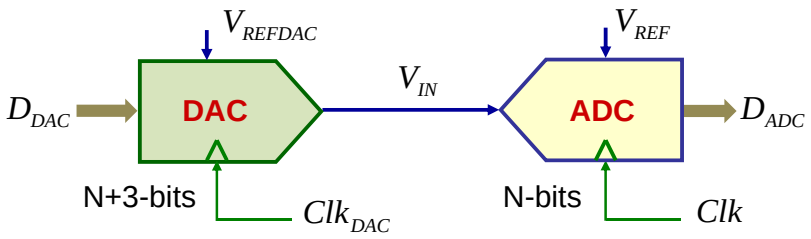
Reference:
The Data Conversion Handbook
Walt Kester (Editor) *page 87*

- Same "ideal" ADC
- Same sample rate
- Same # of samples
- Different input frequency

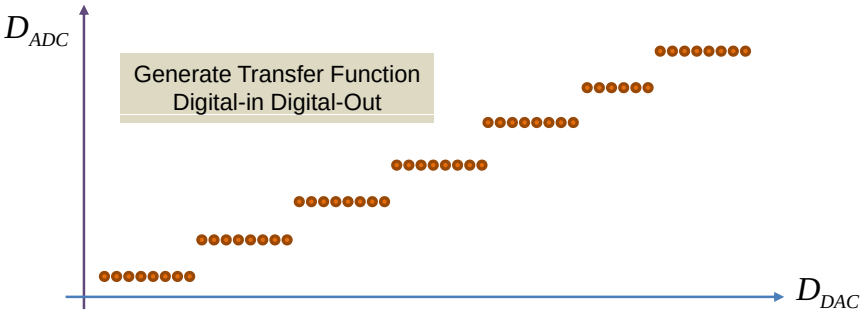


DC Testing

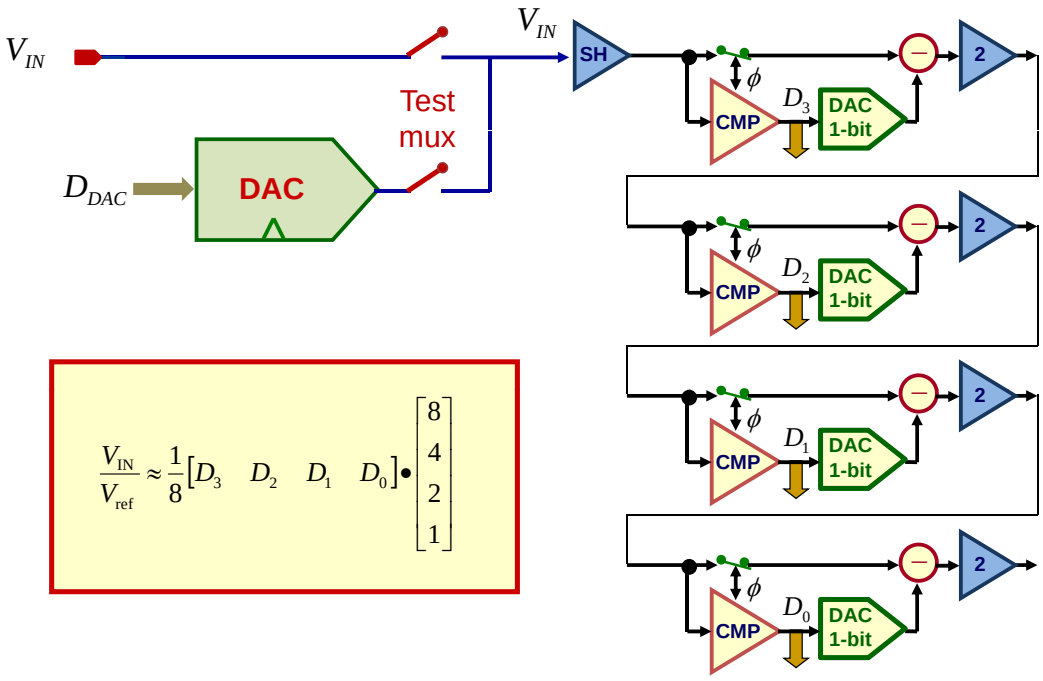
DC Testing



- Use DAC with much higher accuracy than the ADC. Assume it's accurate
  - This replaces servo-loop testing
  - Can require board modification if AC coupling caps are used

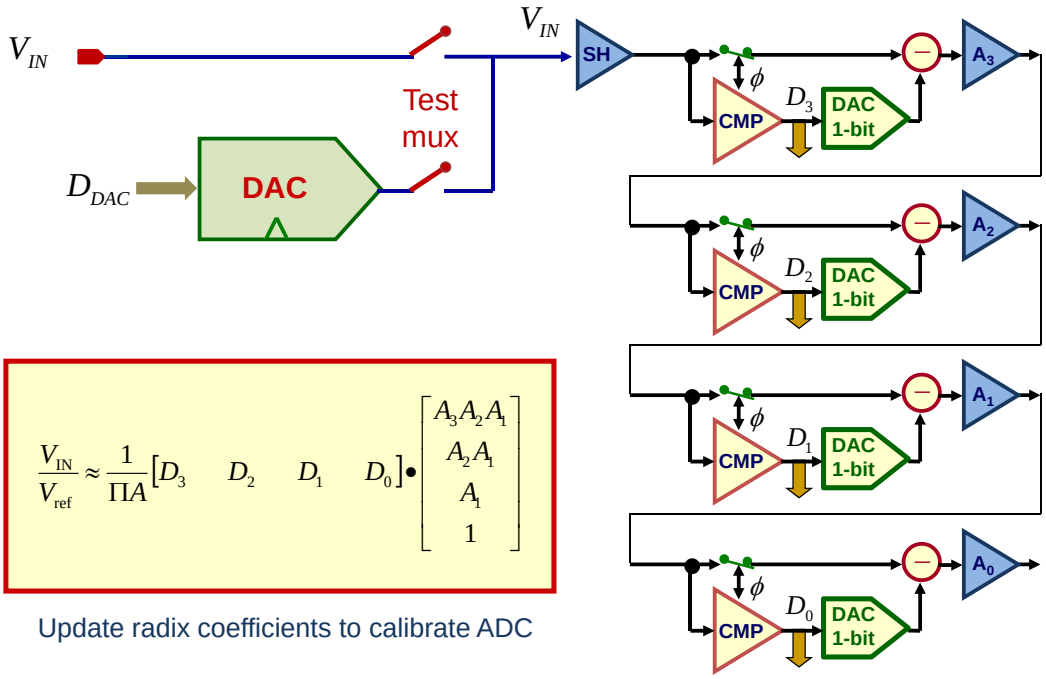


DC Testing: Ideal for BIST



$$\frac{V_{IN}}{V_{ref}} \approx \frac{1}{8}\begin{bmatrix} D_3 & D_2 & D_1 & D_0 \end{bmatrix} \bullet \begin{bmatrix} 8 \\ 4 \\ 2 \\ 1 \end{bmatrix}$$

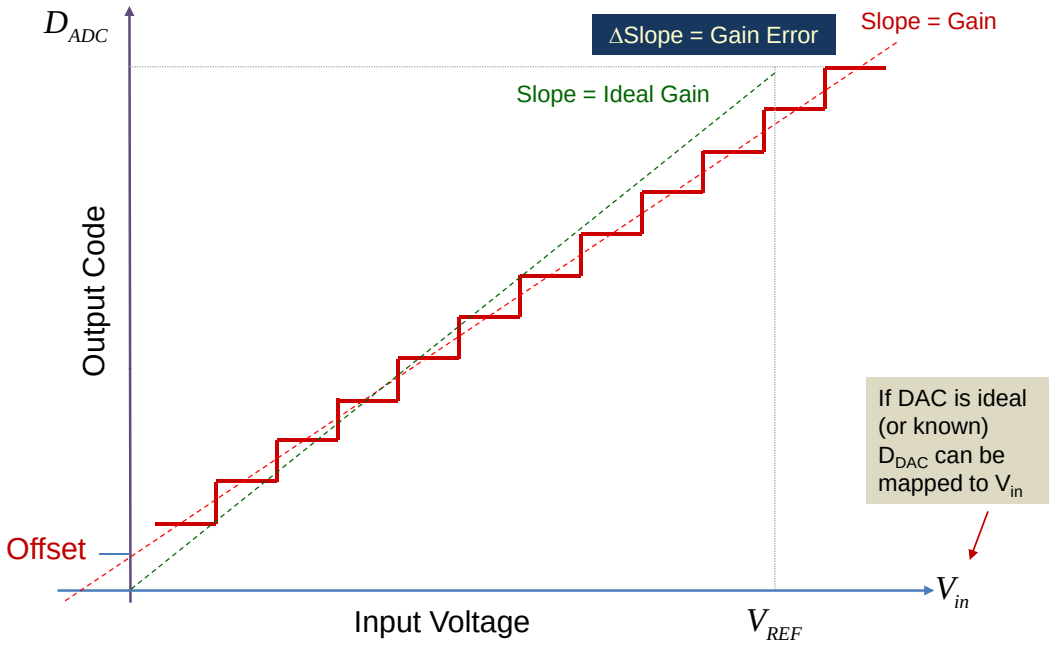
DC Testing: Foreground Calibration



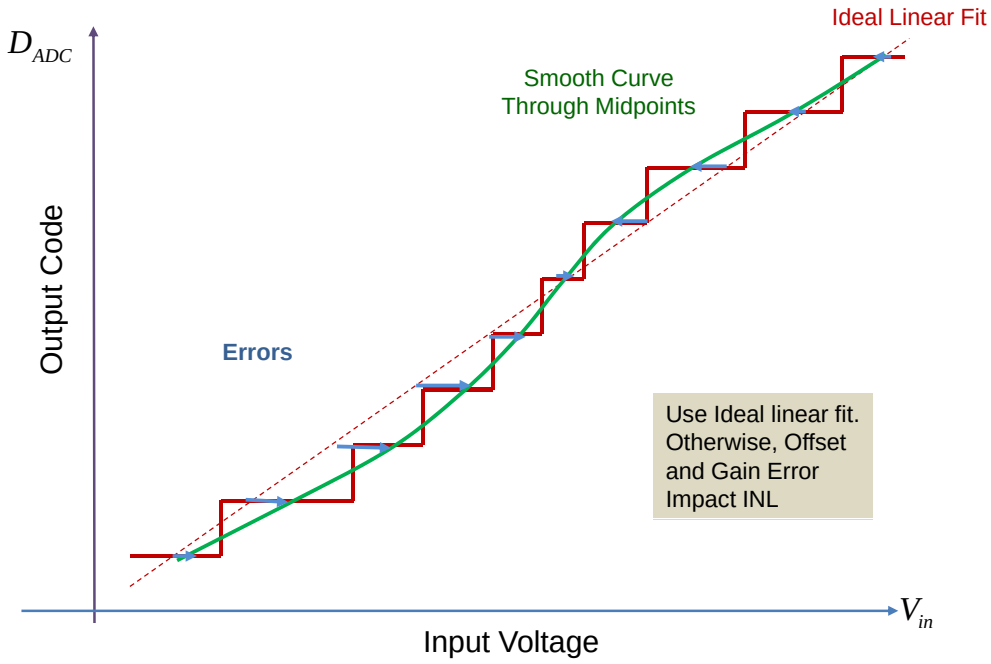
$$\frac{V_{IN}}{V_{ref}} \approx \frac{1}{\Pi A}\begin{bmatrix} D_3 & D_2 & D_1 & D_0 \end{bmatrix} \bullet \begin{bmatrix} A_3A_2A_1 \\ A_2A_1 \\ A_1 \\ 1 \end{bmatrix}$$

Update radix coefficients to calibrate ADC

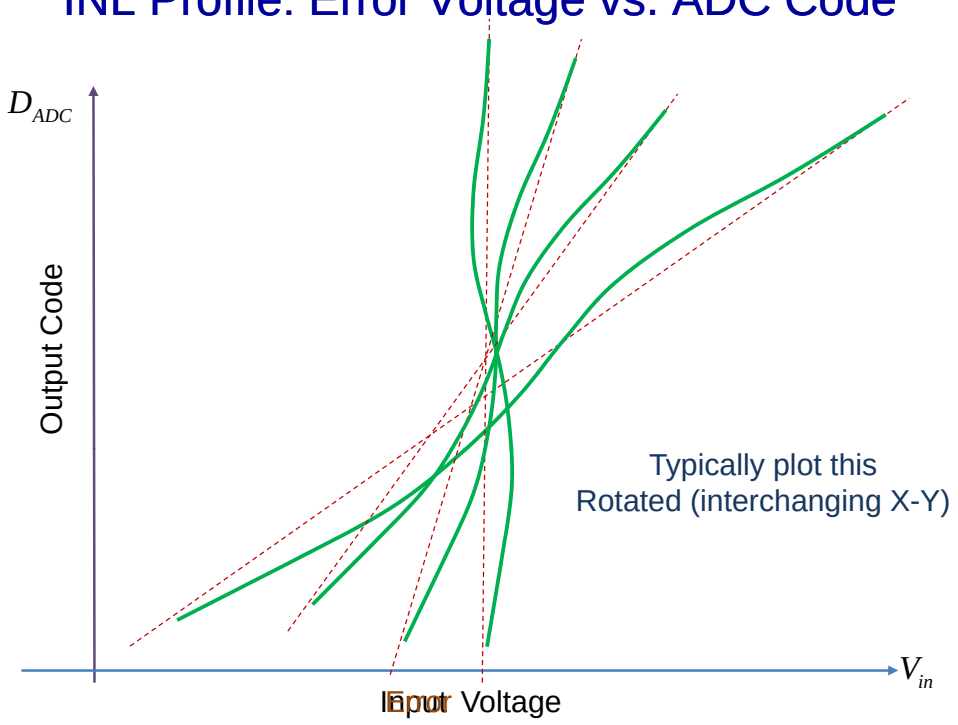
DC Testing: Transition Levels



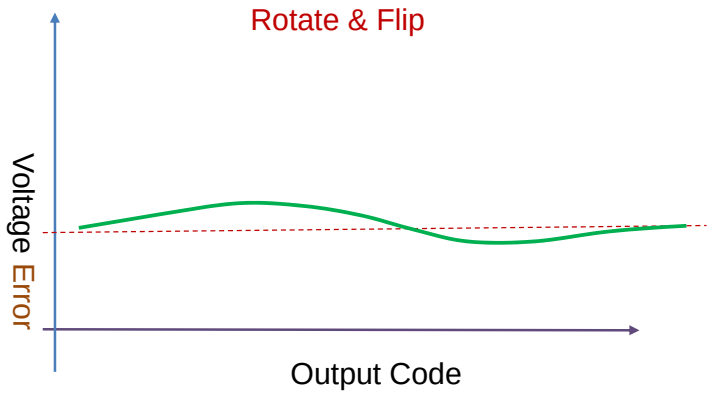
DC Testing: INL



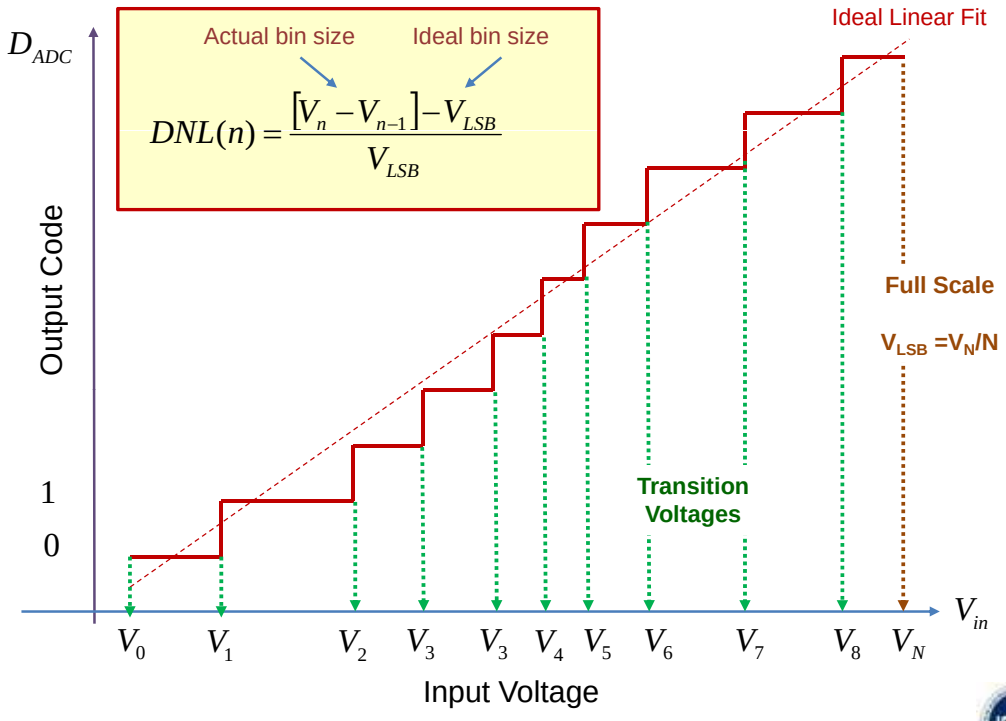
INL Profile: Error Voltage vs. ADC Code



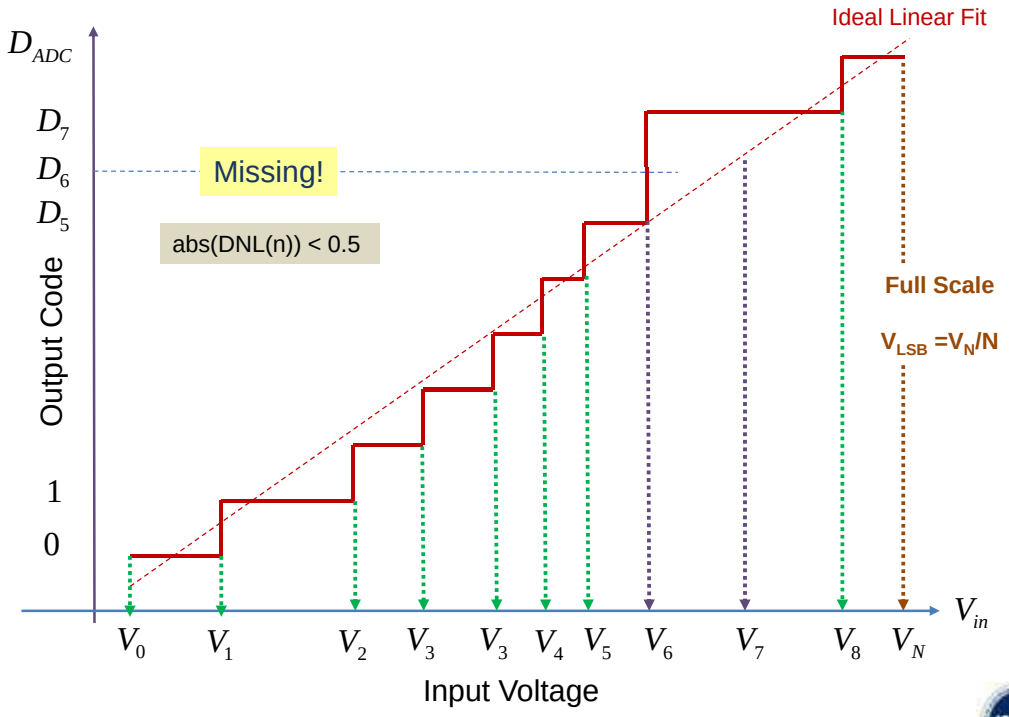
INL Profile: Error Voltage vs. ADC Code



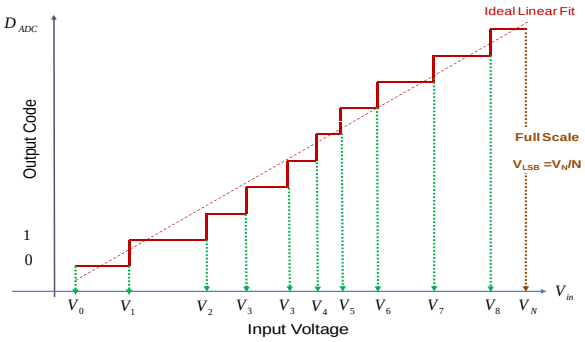
DC Testing: DNL



DC Testing: DNL & Missing Codes



DC Testing: DNL & Relation to INL



Actual bin size — Ideal bin size

$$DNL(n) = \frac{[V_n - V_{n-1}] - V_{LSB}}{V_{LSB}}$$

- DNL and INL contain the "same" information
- Integrate (Sum) DNL to see this explicitly

$$\sum_0^n DNL(m) = \frac{1}{V_{LSB}}[V_0 - 0 + V_1 - V_0 + V_2 - V_1 + \cdots + V_{n-1} - V_{n-2} + V_n - V_{n-1}] - n$$

Error Voltage relative to best-fit straight line

$$INL(n) = \sum_0^n DNL(m) = \frac{V_n - nV_{LSB}}{V_{LSB}}$$

ADC Physical Performance Limitations

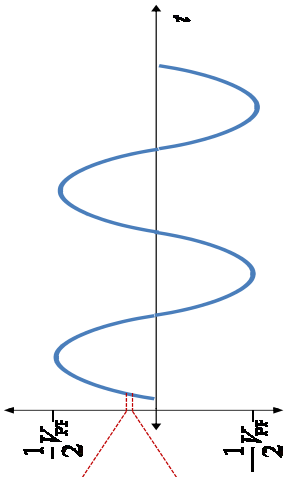
Noise & Aperture Jitter

SNR for Ideal Quantizer

Full-Scale Sinewave Power

$$P_S = \frac{V_{PP}^{\ 2}}{8}$$

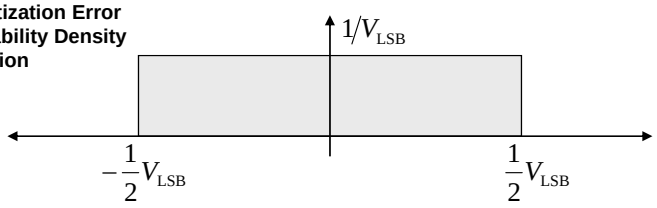
$$V_{S\sigma} = \frac{1}{2}\frac{V_{PP}}{\sqrt{2}}$$



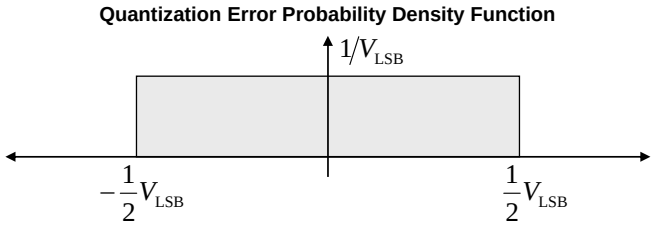
Assumptions

1) Quantization error is noise
2) Noise is uniformly distributed in each code bin
3) Noise in one code bin is independent of noise in any other code bin

Quantization Error Probability Density Function



RMS Quantization Noise



$$V_{Q\sigma} = \frac{V_{LSB}}{\sqrt{12}} = 0.289 V_{LSB}$$

rms Quantization Noise

$$V_{Q\sigma} = \frac{V_{PP}}{2^n\sqrt{12}} = \frac{V_{PP}/2}{2^n\sqrt{3}}$$

Where V_{PP} is the full-scale Voltage and n is the # of bits

SNR and Effective # of Bits (ENOB)

For a full-scale single-tone sinewave input, the signal-to-noise ratio is

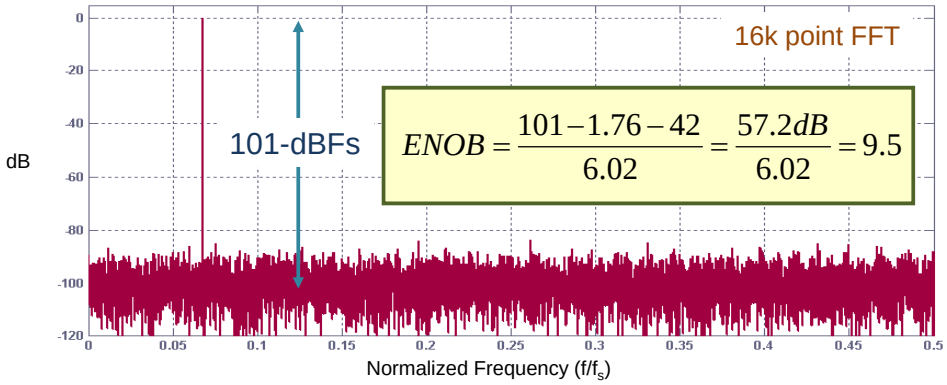
$$SNR = \frac{V_{S\sigma}}{V_{Q\sigma}} = 2^n\sqrt{\frac{3}{2}}$$

$$SNR_{dB} = 20\log\left[2^n\sqrt{\frac{3}{2}}\right] = n\cdot 20\log(2) + 10\log(3/2) = n\cdot 6.02 + 1.76$$

- Solving for "n" given a measured SNR, (or SNDR) gives an expression for ENOB
- Non-ideal ADC generates harmonics, so must use SNDR in place of SNR
- A non ideal ADC can be compared to an ideal ADC, which has the same ENOB
- An ideal ADC will not have ENOB exactly equal n-bits because of violation of noise assumptions

$$ENOB = \frac{SNDR_{dB} - 1.76}{6.02}$$

Estimating SNR from a Glance at the Spectrum



$$ENOB = \frac{101 - 1.76 - 42}{6.02} = \frac{57.2dB}{6.02} = 9.5$$

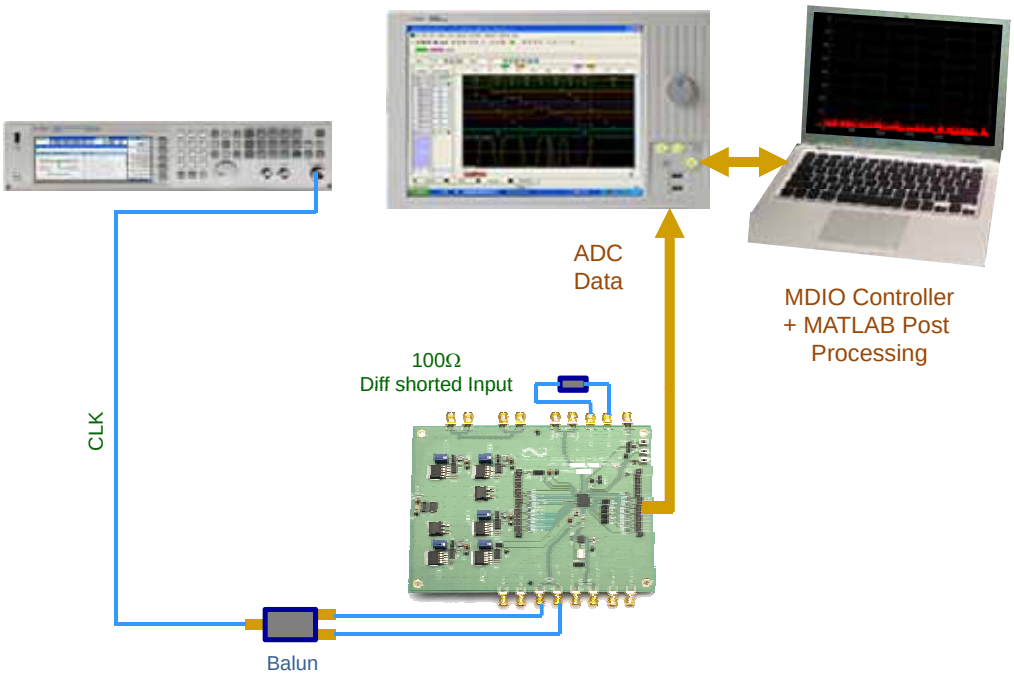
$$10\log\left[\frac{P_{S\sigma}}{P_{n\sigma}}\right] - 1.76 = ENOB \cdot (6.02) \quad » \quad 10\log\left[\frac{P_{S\sigma}}{P_{nFbin\sigma} \cdot N_S}\right] - 1.76 = ENOB \cdot (6.02)$$

Total noise power

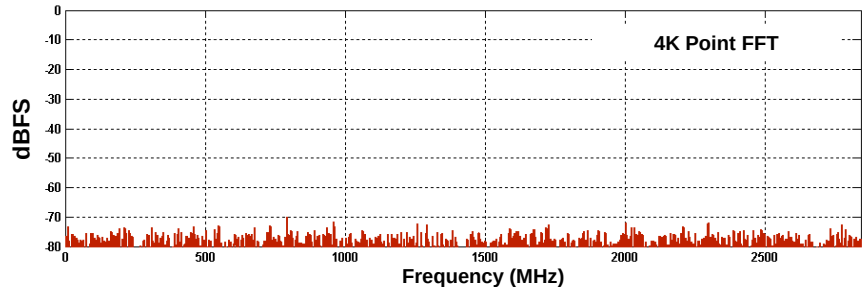
Average noise power per frequency bin

$$ENOB = \frac{10\log\left[\frac{P_{S\sigma}}{P_{nFbin\sigma}}\right] - 1.76 - 10\log[N_S]}{6.02}$$

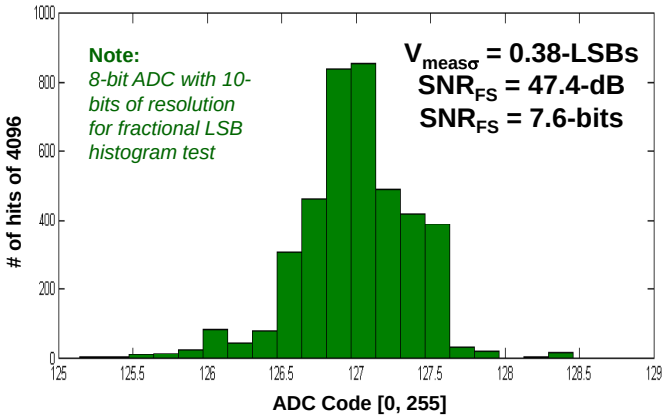
Zero-Input Test



Grounded Input Histogram



Check Frequency Spectrum for any clock-related spurs in the noise floor

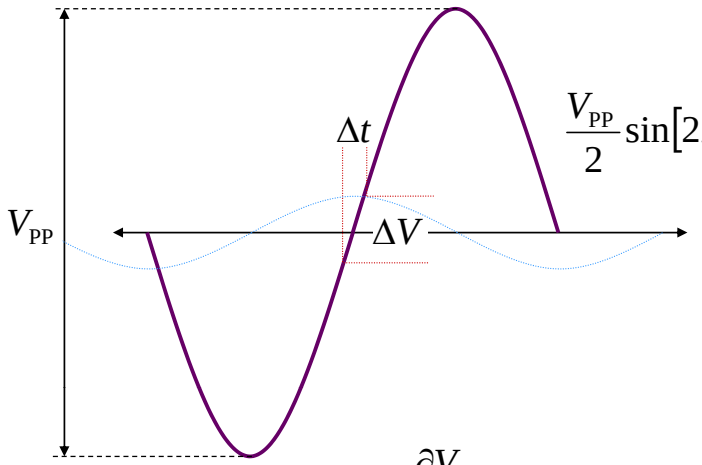


$$V_{n\sigma}{}^2 = V_{meas\sigma}{}^2 - \left[\frac{V_{PP}}{2^n\sqrt{12}}\right]^2$$

$$\left[\frac{V_{n\sigma}}{V_{LSB}}\right]^2 = 0.38^2 - 0.29^2 = 0.25^2$$

$$V_{n\sigma} = \frac{V_{LSB}}{4} = 8.2 \text{ bits}$$

Limitations Due to Timing Jitter for Sine Input

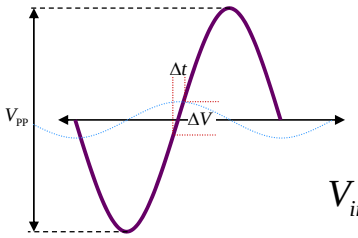


$$\frac{V_{PP}}{2}\sin\left[2\pi \cdot f_{in}(t+\Delta t)\right]$$

$$\Delta V = \frac{\partial V}{\partial t}\Delta t$$

$$\Delta V(t) = \Delta t\left(\pi f_{in}\right)\cdot V_{PP}\cos[2\pi f_{in} t]$$

Expression for SNR due to Jitter



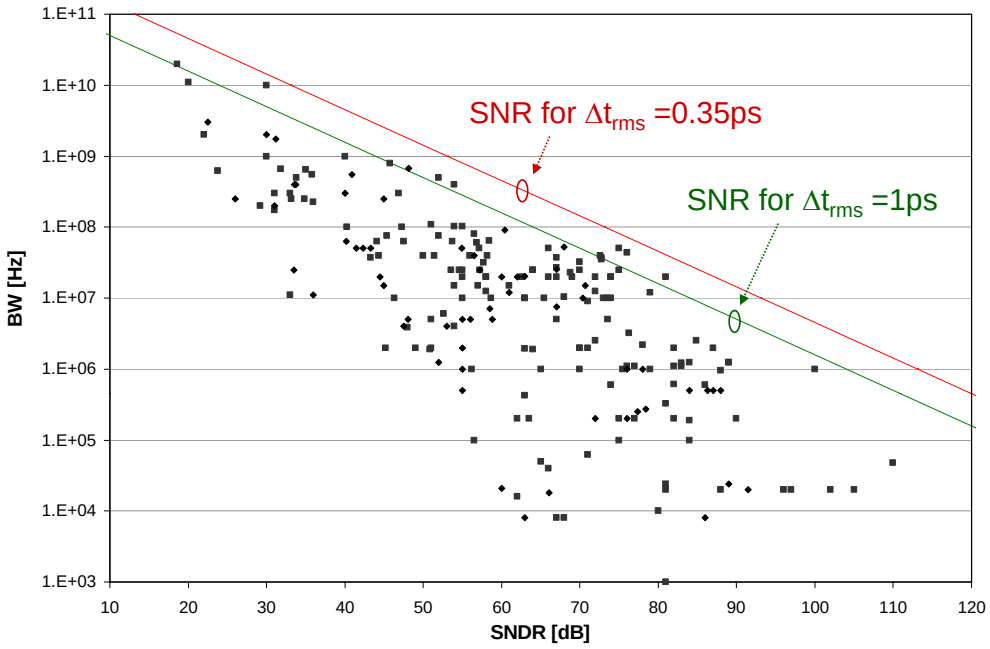
$$V_{inrms} = \sqrt{avg\left[\left(\frac{V_{PP}}{2}\sin\left[2\pi \cdot f_{in}(t+\Delta t)\right]\right)^2\right]} = \frac{V_{PP}}{2\sqrt{2}}$$

$$\Delta V_{rms} = \Delta t_{rms}(\pi f_{in}) \cdot V_{PP} \cdot \sqrt{avg\left(\cos^2[2\pi f_{in} t]\right)} = 2\pi f_{in}\Delta t_{rms}\frac{V_{PP}}{2\sqrt{2}}$$

$$\frac{\Delta V_{rms}}{V_{inrms}} = \frac{1}{SNR} = 2\pi f_{in}\Delta t_{rms}$$

Now find Δt_{rms}

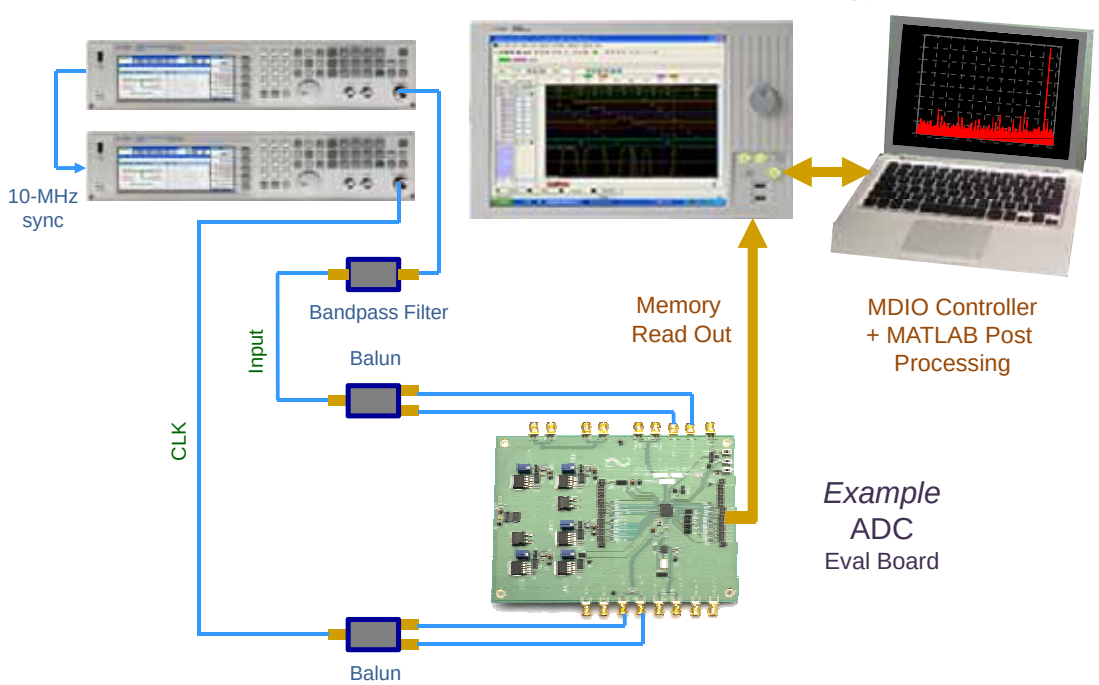
SNR vs. Bandwidth Showing Jitter Limits



[3] Boris Murmann, "*ADC Performance Survey 1997-2009,"* [Online]. Available: http://www.stanford.edu/~murmann/adcsurvey.html

Dynamic Testing

Dynamic Testing: Use a "Known" Input



Coherent Leakage

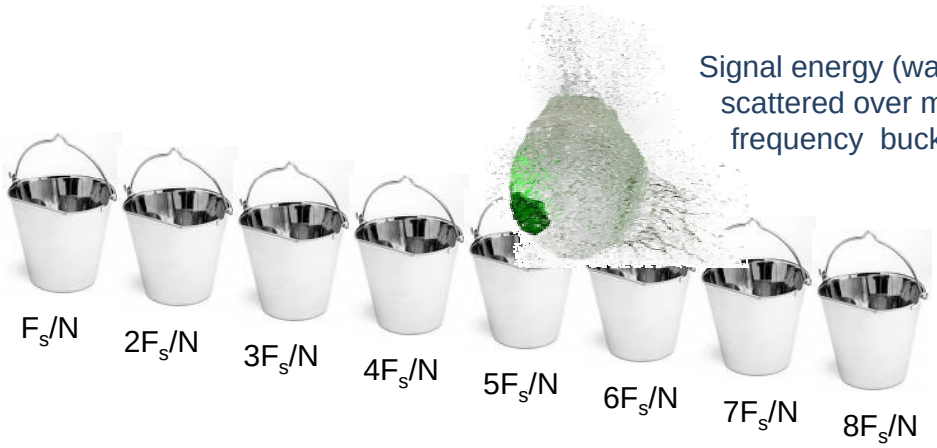
Input signal is exactly centered an a frequency bin

Signal energy (water) occupies only one frequency bucket

Coherent Leakage

Input signal is NOT centered an a frequency bin

Signal energy (water) is scattered over many frequency buckets



Coherent Sampling

Heisenberg Uncertainty Principle

$$\Delta x \Delta p \geq \frac{h}{2\pi}$$

Wave equations in space

Fourier Frequency-Time Analogy

$$\Delta t \Delta f \geq K$$

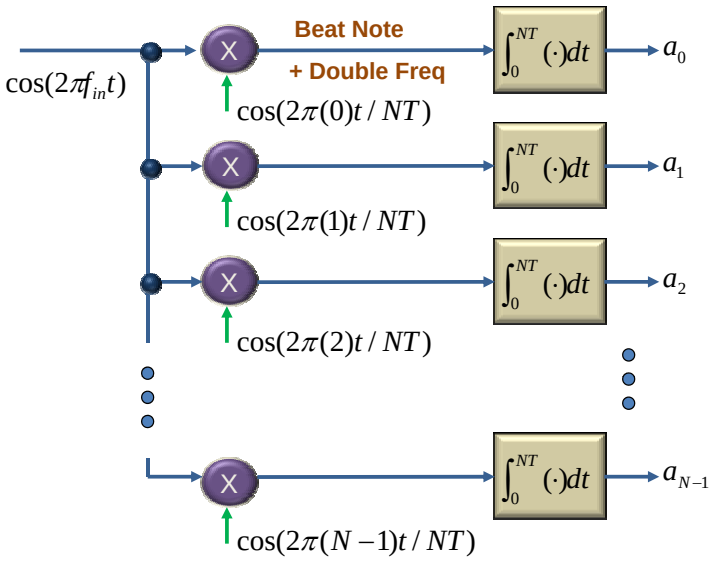
Wave equations in time

If T_s is the sample period and F_s is the sample frequency, then normalizing

$$\frac{\Delta t}{T_s}\frac{\Delta f}{F_s} \geq K \quad \text{or} \quad \frac{\Delta f}{F_s} \geq \frac{K}{N_s}$$

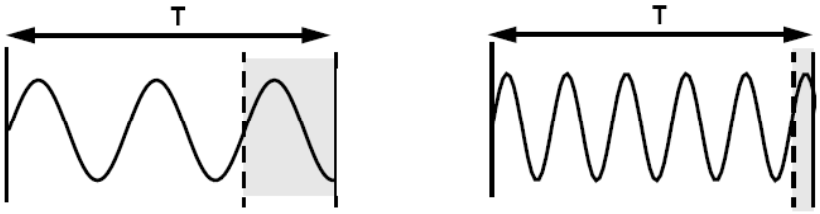
The accuracy in estimating the input frequency is inversely proportional to N_s, the number of samples taken

DFT as a Bank of Mixers and Integrators

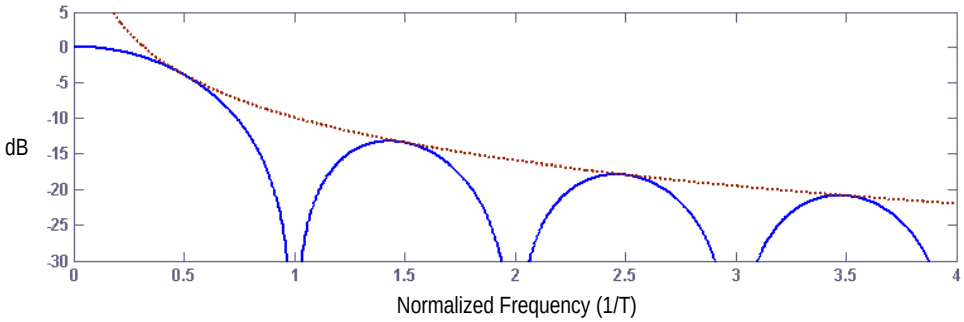


Orthogonality is maintained for any frequency if N_s is very large, or if the input frequency is harmonically related to the sample frequency

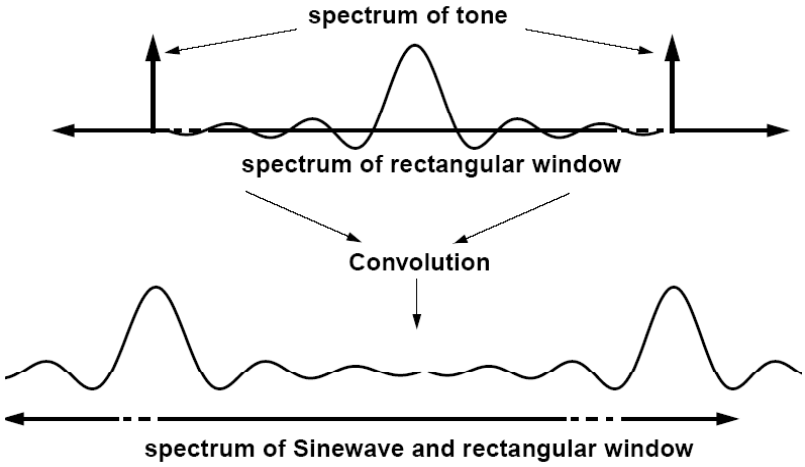
Frequency Leakage: Rectangular Window » Sinc



As frequency increases, the fraction of the signal contributing to the integral decrease. Spectrum as 1/f roll-off with nulls at multiples of 1/T

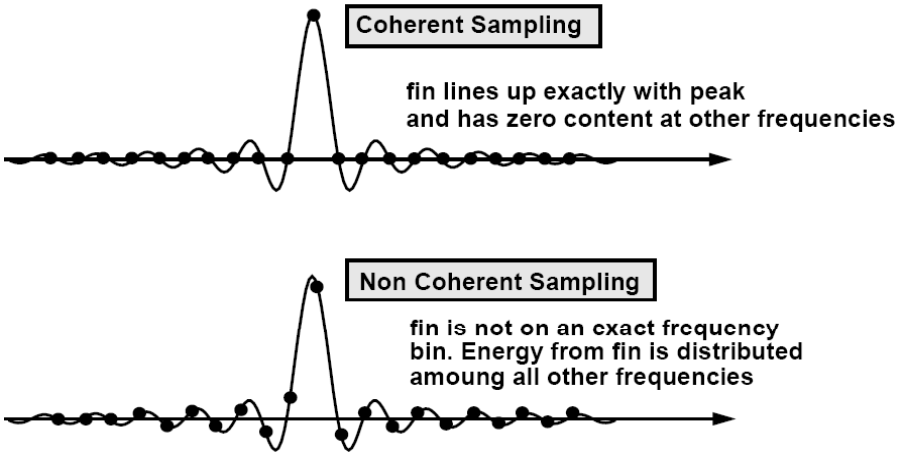


Leakage in DFT



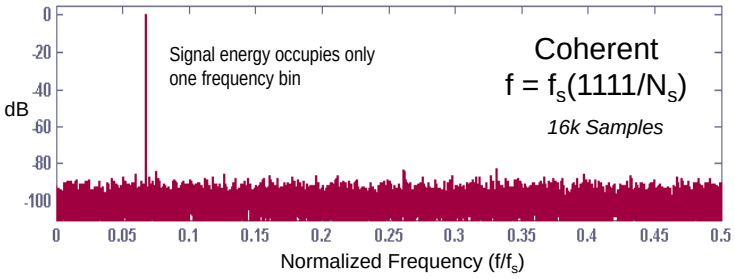
Actual Fourier Transform on the input signal is the convolution of the pure tones from the sinewave and the sinc function from the rectangular window

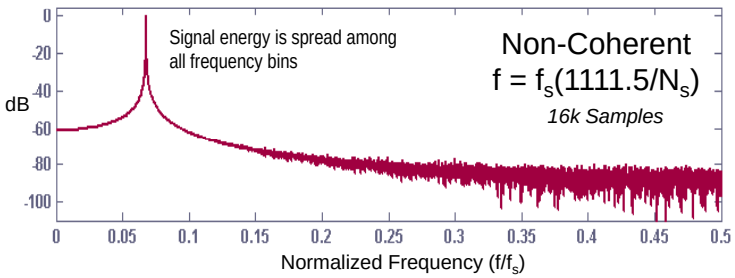
Leakage in DFT: Special Case of Coherent Sampling



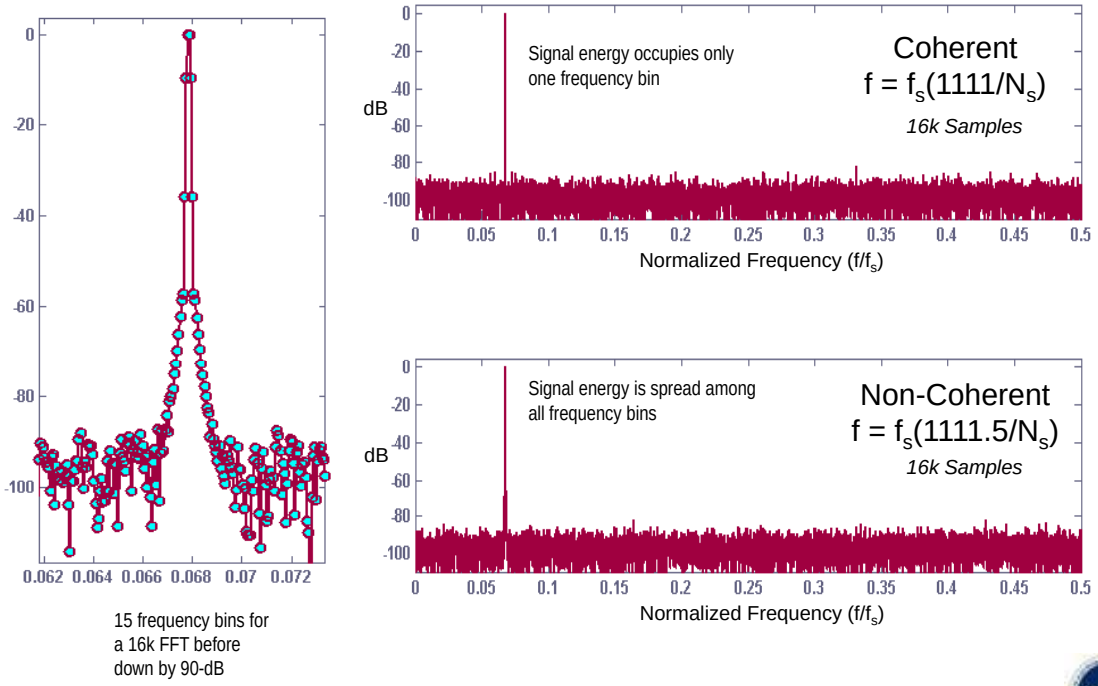
Energy in signal tone is convolved with window function and spreads across frequency band

Eifel Tower Effect for Non-Integer # of Periods





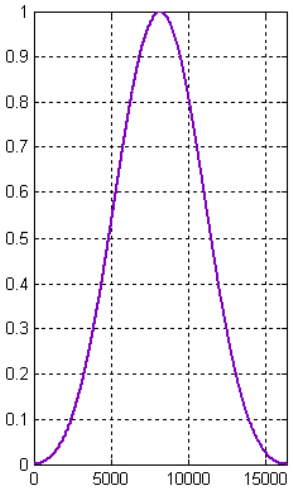
Blackman Windowing



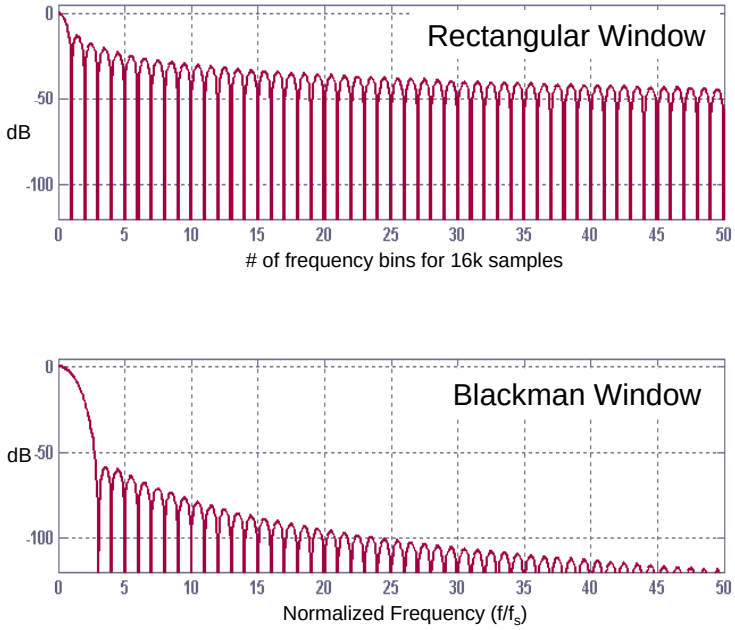
15 frequency bins for a 16k FFT before down by 90-dB

Windowing

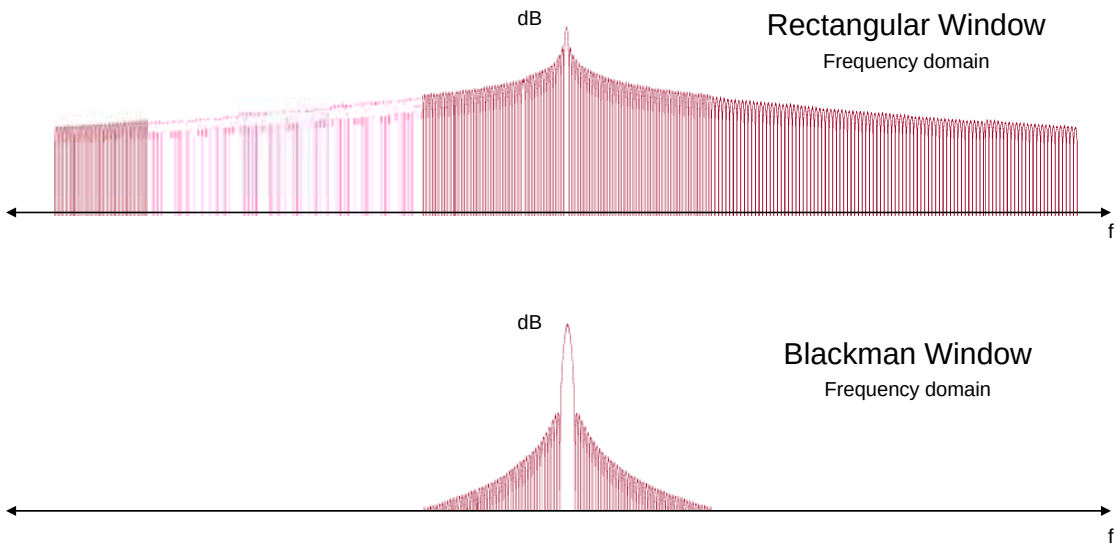
Frequency Response of Blackman / Rect Window



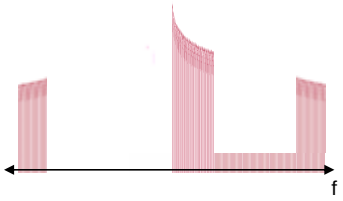
Blackman Window in time domain for 16k samples

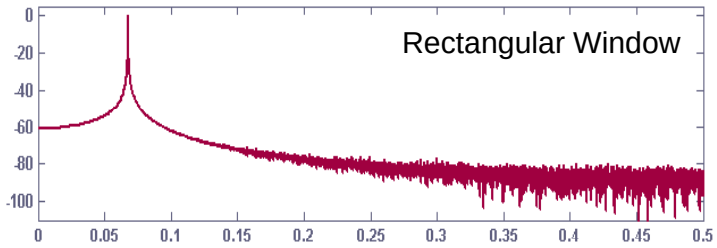


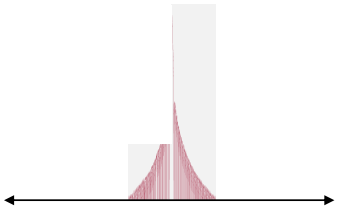
Frequency Response of Blackman / Rect Window

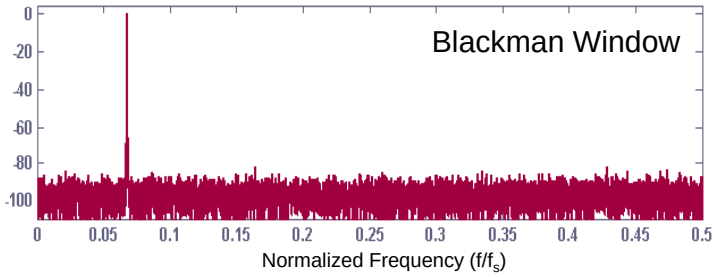


Frequency Response of Blackman / Rect Window





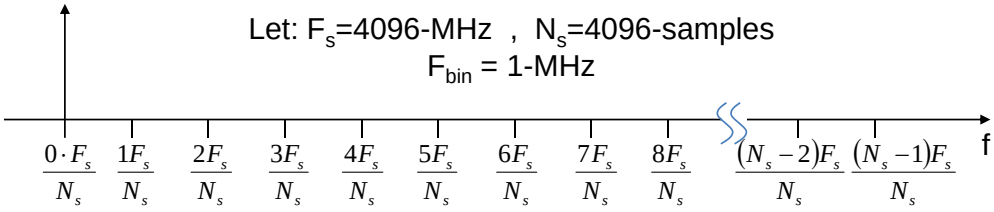


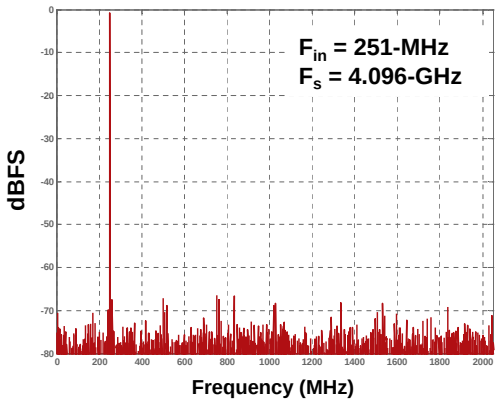


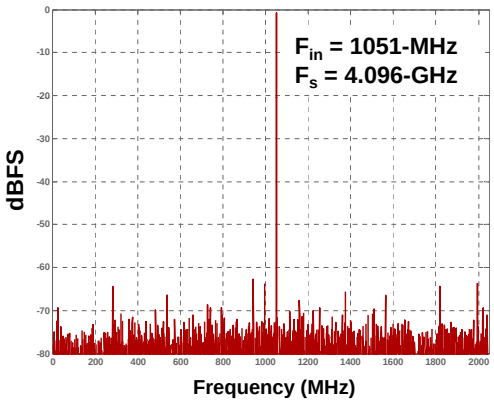
Coherent Frequency: Input Must be in a Freq Bin

Let: F_s=4096-MHz , N_s=4096-samples

F_{bin} = 1-MHz



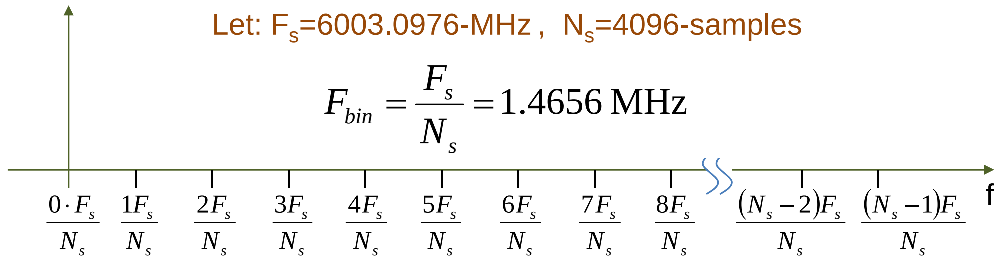




Coherent Frequency: Truncating Long Decimal Values

Let: F_s=6003.0976-MHz , N_s=4096-samples

$$F_{bin} = \frac{F_s}{N_s} = 1.4656\ \mathrm{MHz}$$




```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%     Matlab Script to calculate sample frequencies for ADC
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%---------------------------------------------------------------------
%--- Parameters
%---------------------------------------------------------------------
nsamp = 4096;           % Number for coherent FFT samples
fs_x = 6003;            % Default sample frequency in MHz
nsigdig = 4;            % resolution in frequency selection [0 1 2 3 4...]
sig_factor = 10^nsigdig;  % Factor used to truncate bin freq
%---------------------------------------------------------------------
%--- User input
%---------------------------------------------------------------------
fprintf('\n\n')
fprintf('--------------------------------------------------------------\n')
fprintf('\t\tCoherent Frequency Calculator\n')
fprintf('--------------------------------------------------------------\n')
fs_xin = input('  ---> Input Approximate Sample Clock (MHz) = ');
if fs_xin
   fs_x = fs_xin;
end
```

```
%---------------------------------------------------------------------
%--- Find approximate frequencies
%---------------------------------------------------------------------
fbin_x = fs_x/nsamp;                           % First estimate of bin frequency
fbin = round(fbin_x*sig_factor)/sig_factor;    % Truncate # of digits
fs = fbin*nsamp;
fprintf('\n-------------------------\n')
fprintf('\tfs   = %14.8f\n',fs)
fprintf('\tfbin = %14.8f\n',fbin)
fprintf('-------------------------\n\n')
```

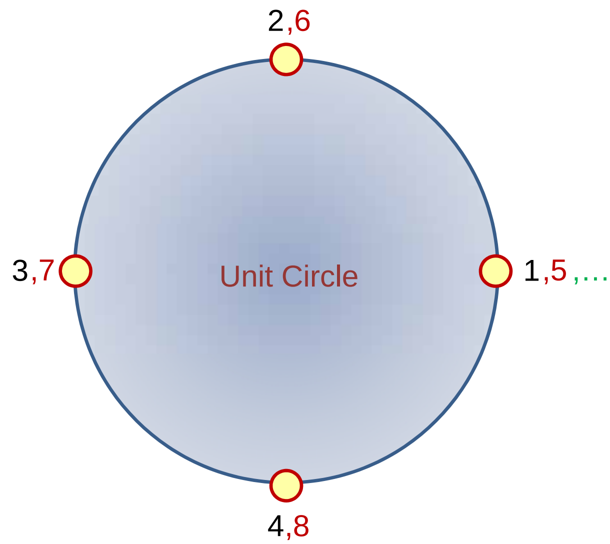
```
-------------------------------------------------------------
     Coherent Frequency Calculator
-------------------------------------------------------------
  ---> Input Approximate Sample Clock (MHz) = 6003

 fs   =  6003.09760000
 fbin =        1.46560000
```


Relative Prime Frequencies for No Repetition

$F_s = N_s F_{bin}$, $F_{in} = N_{in} F_{bin}$

N_s and N_{in} must be relative prime to prevent repetition

Consider
N_s = 32
N_{in} = 8



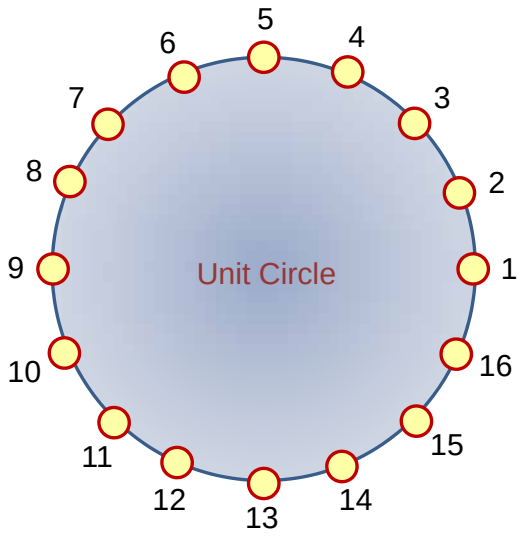
Pattern Repeats
$F_{in} = F_s/4$

Relative Prime Frequencies

$F_s = N_s F_{bin}$, $F_{in} = N_{in} F_{bin}$

N_s and N_{in} must be relative prime to prevent repetition

Consider
$N_s = 16$
$N_{in} = 1$



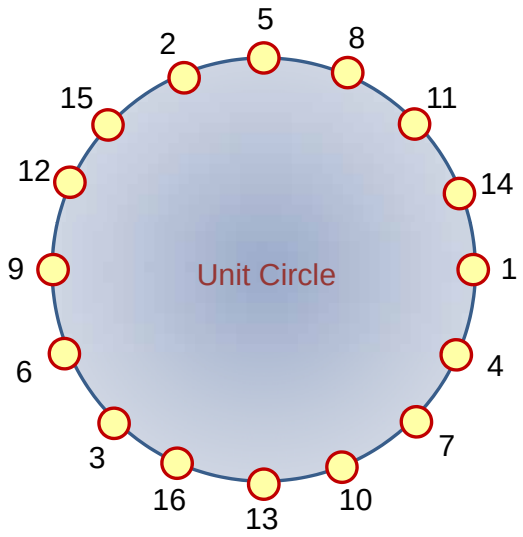
Pattern does not Repeat
$F_{in} = F_s/16$

Relative Prime Frequencies

$F_s = N_s F_{bin}$, $F_{in} = N_{in} F_{bin}$

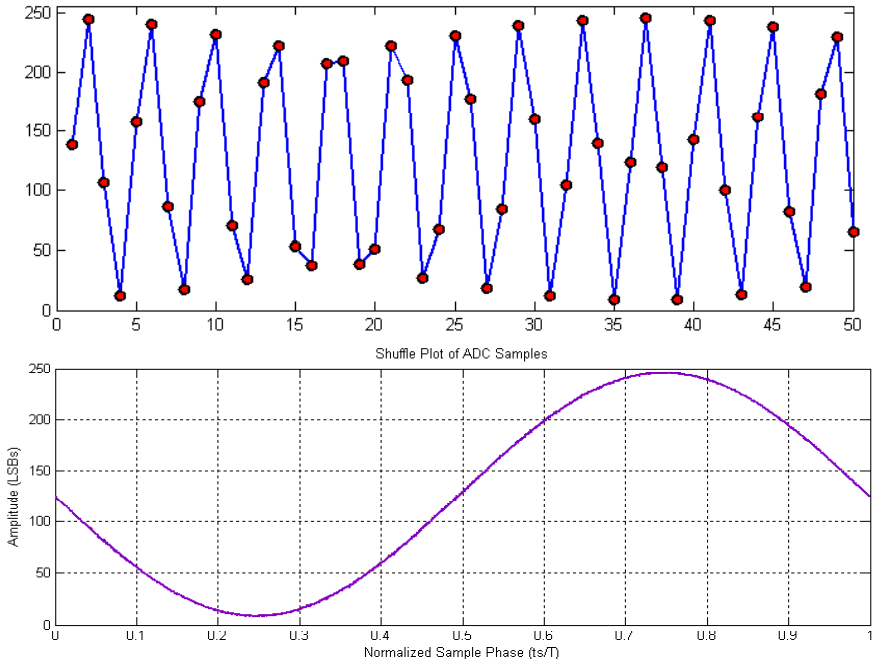
N_s and N_{in} must be relative prime to prevent repetition
For $N_s = 2^n$, condition is met provided N_{in} is an odd integer

Consider
$N_s = 16$
$N_{in} = 5$



Pattern does not Repeat
$F_{in} = F_s/16$

Shuffle-Plot



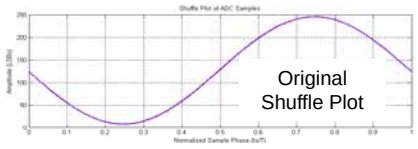
1.05-GHz Input

If input is coherent and relative prime condition is met, the full data pattern will be distributed as $2\pi/N_s$ equal phases around the unit circle

Data can be **"Shuffled"** in order of increasing phase [0, 2π] to show one cycle of the sinewave

Similar to Sampling Scope

Information from Shuffle Plot

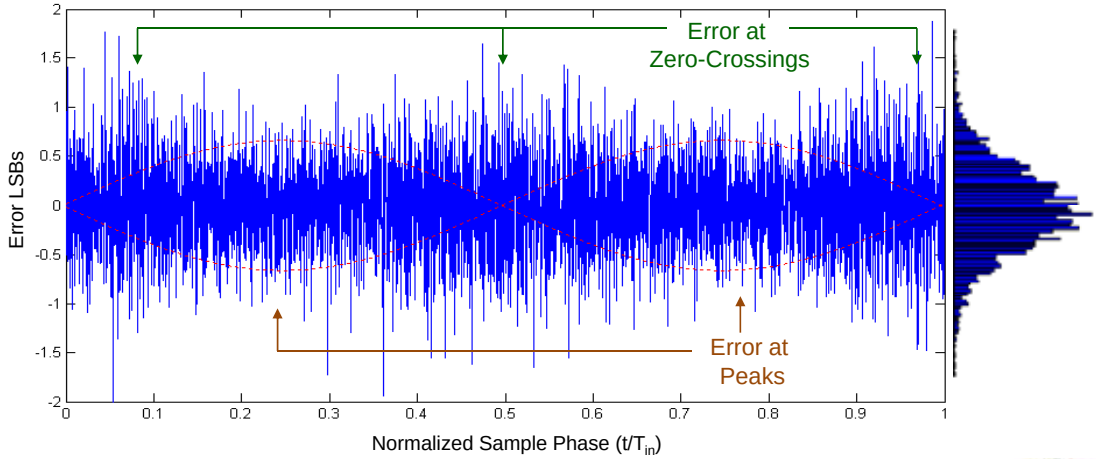


Original Shuffle Plot

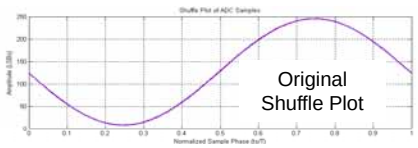
$$V_{peak\sigma}{}^2 = V_{n\sigma}{}^2 + \left[\frac{V_{PP}}{2^n\sqrt{12}}\right]^2 = 0.38^2$$

7.5-bits SNR at Peaks

Error with respect to ideal fit



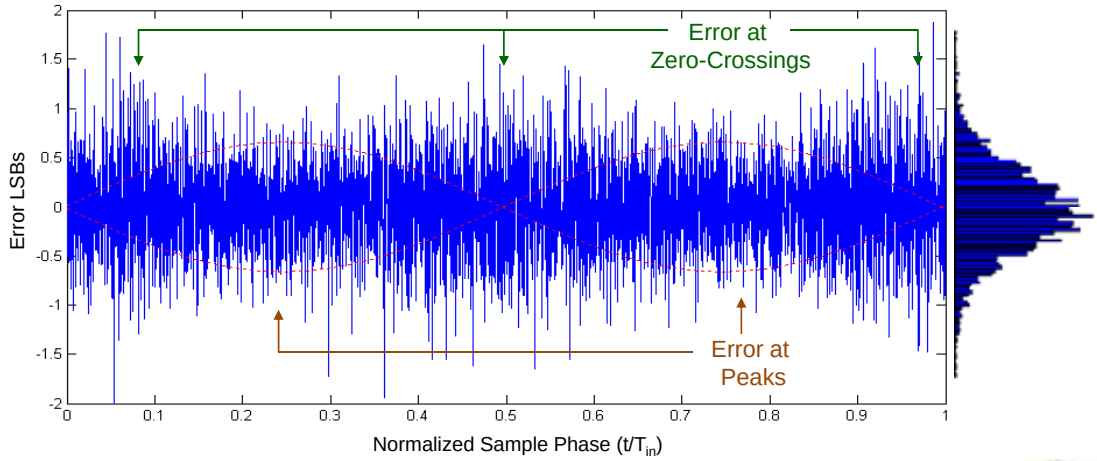
Information from Shuffle Plot: Aperture Jitter



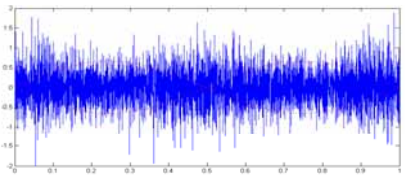
$$V_{zero\sigma}{}^2 = V_{n\sigma}{}^2 + \left[\frac{V_{PP}}{2^n\sqrt{12}}\right]^2 + \left[\pi f_{in} V_{inpp} \tau_{jit\sigma}\right]^2$$

7.1-bits SNR at crossing

Error with respect to ideal fit



Measuring Aperture Jitter From Shuffle Plot



Error with respect to ideal fit

$$\tau_{jit\sigma} = \frac{T_{in}}{\pi}\frac{1}{V_{inpp}}\sqrt{V_{zero\sigma}{}^2 - V_{n\sigma}{}^2 - \left[\frac{V_{PP}}{2^n\sqrt{12}}\right]^2}$$

$$\tau_{jit\sigma} = \frac{T_{in}}{\pi}\frac{1}{2^n}\frac{V_{pp}}{V_{inpp}}\sqrt{x_{zero\sigma}{}^2 - x_{n\sigma}{}^2 - \left[\frac{1}{\sqrt{12}}\right]^2}$$

$$\tau_{jit\sigma} = (303\,\text{ps})\frac{1}{256}\cdot\frac{1}{0.93}\sqrt{0.53^2 - 0.25^2 - 0.289^2} = 467\,\text{fs}$$

- Quantization Noise - LSBs
- Additive Noise –LSBs
- Measured RMS Error at X-ing – LSBs
- Ratio of input wrt Full-Scale
- ADC Resolution
- Period of Input Signal over pi

Optimal Curve Fit

d) Create Matrix (35), Matrix (36), and Matrix (37).

$$y = \begin{bmatrix} y_1 \\ y_2 \\ . \\ . \\ y_M \end{bmatrix} \quad (35)$$

$$D_i = \begin{bmatrix} \cos(\omega_i t_1) & \sin(\omega_i t_1) & 1 & -A_{i-1} t_1 \sin(\omega_i t_1) + B_{i-1} t_1 \cos(\omega_i t_1) \\ \cos(\omega_i t_2) & \sin(\omega_i t_2) & 1 & -A_{i-1} t_2 \sin(\omega_i t_2) + B_{i-1} t_2 \cos(\omega_i t_2) \\ . & . & . & . \\ . & . & . & . \\ \cos(\omega_i t_M) & \sin(\omega_i t_M) & 1 & -A_{i-1} t_m \sin(\omega_i t_M) + B_{i-1} t_m \cos(\omega_i t_M) \end{bmatrix} \quad (36)$$

$$x_i = \begin{bmatrix} A_i \\ B_i \\ C_i \\ \Delta\omega_i \end{bmatrix} \quad (37)$$

e) Compute the least-squares solution, x_i, as shown in Equation (38).

$$x_i = (D_i^T D_i)^{-1} (D_i^T y) \quad (38)$$

f) Compute the amplitude, A, and phase, θ, for the form in Equation (39).

$$y_{ir} = A\cos(\omega t_n + \theta) + C \quad (39)$$

using Equation (40)

$$A = \sqrt{A_i^2 + B_i^2} \quad (40)$$

and Equation (41) and Equation (42).

$$\theta = \tan^{-1}\left[-\frac{B_i}{A_i}\right] \quad \text{if } A_i \geq 0 \quad (41)$$

$$\theta = \tan^{-1}\left[-\frac{B_i}{A_i}\right] + \pi \quad \text{if } A_i < 0 \quad (42)$$

If non-coherent input signal is used, the same information, SNR, THD, Shuffle-domain data, can be obtained if an optimal curve fit is used estimate the following unknown parameters of the sine wave

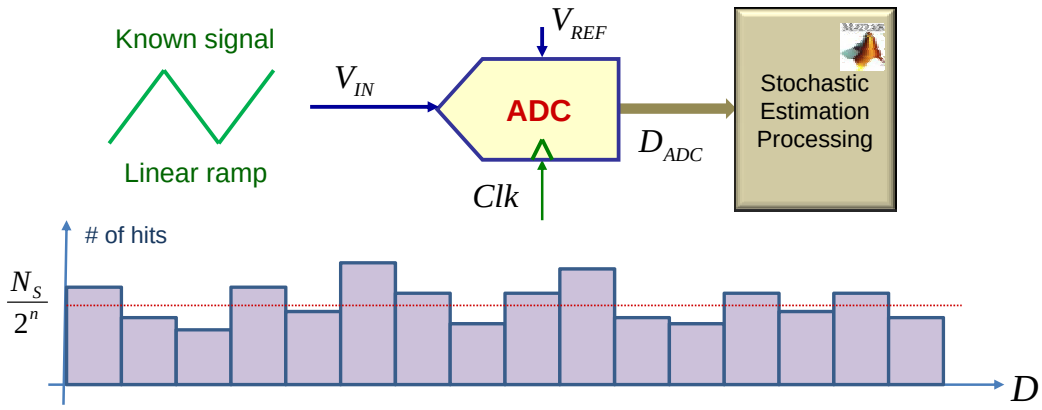
- Frequency
- Phase
- Amplitude
- Offset

IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters

IEEE Std 1241-2000
Page 28

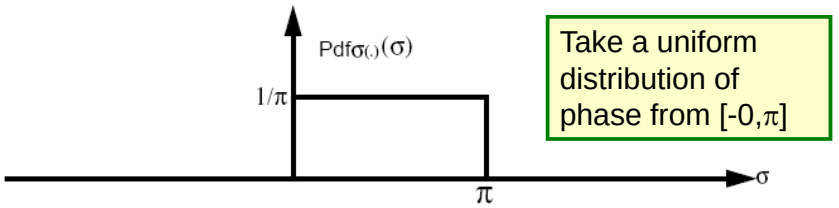
Code Density Testing

Stochastic Estimation: Histogram Techniques



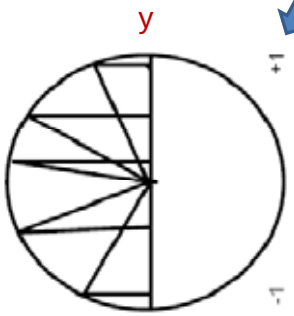
- Statistically estimate the bin width by the # of hits per bin
  - Assumes input has known probability distribution
  - Assumes a sufficient # of samples are taken for statistical accuracy
- Ideal signal is a linear ramp
  - Difficult to generate
- Usually done with a sinusoidal input
  - Need to determine the probability density function of a sinewave

Mapping Uniform Phase to Amplitude



Take a uniform distribution of phase from [-0,π]

Projection on y-axis



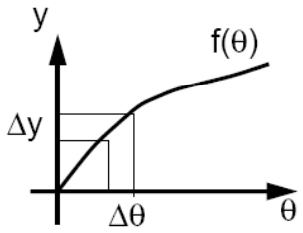
The rotating arm has a projection on the y-axis where the time spent near ±1 is longer than the time spent near 0 due to the velocity of the projection in the y-direction

A Little bit of Math in the "Bathtub" 1 of 2

Consider the general case y = f(θ)

$$|P_\theta(\theta)\Delta\theta| = |P_y(f(\theta))\Delta y| \;\Rightarrow\; P_y(f(\theta)) = P_\theta(\theta)\left|\frac{\Delta\theta}{\Delta y}\right|$$

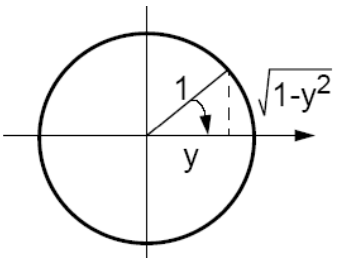
$$P_y(f(\theta)) = \frac{P_\theta(\theta)}{|dy/d\theta|}$$



Reversing the argument to put in terms of y

$$|P_y(y)dy| = |P_\theta(f^{-1}(y))d\theta|$$

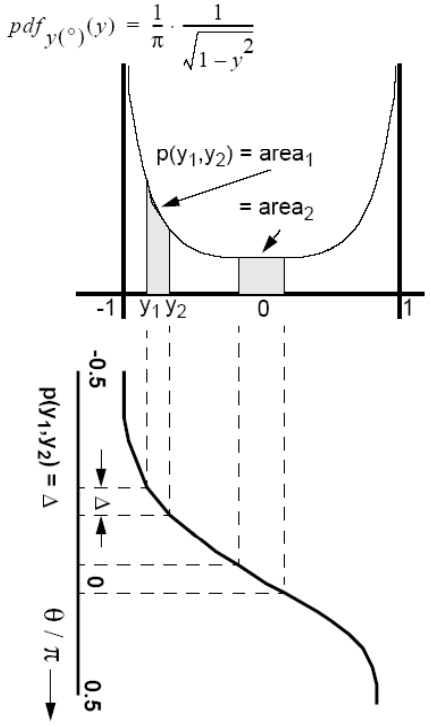
$$P_y(y) = P_\theta(f^{-1}(y))\left|\frac{d\theta}{dy}\right|$$



y = f(θ) = cos(θ), so dy/dθ = -sin(θ)

$$P_y(y) = \frac{1}{\pi}\left|\frac{d\theta}{dy}\right| = \frac{1}{\pi}\cdot\frac{1}{\sin\theta} = \frac{1}{\pi}\cdot\frac{1}{\sqrt{1-y^2}}$$

A Little bit of Math in the "Bathtub" 2 of 2



Find

$$Pr(y_1 \le y \le y_2) = P(y_1, y_2)$$

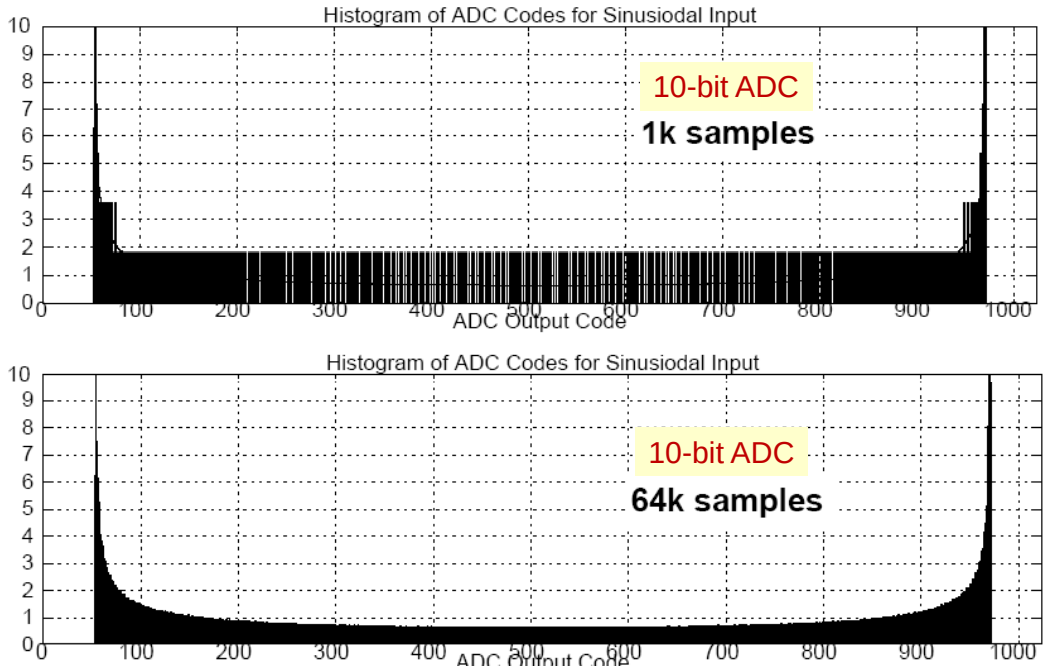
$$P(y_1, y_2) = \frac{1}{\pi}\int_{y_1}^{y_2}\frac{1}{\sqrt{1-y^2}}dy$$

$$P(y_1, y_2) = \frac{1}{\pi}\int_{\text{asin}(y_1)}^{\text{asin}(y_2)}\frac{\cos(\theta)}{\sqrt{1-(\sin\theta)^2}}d\theta$$

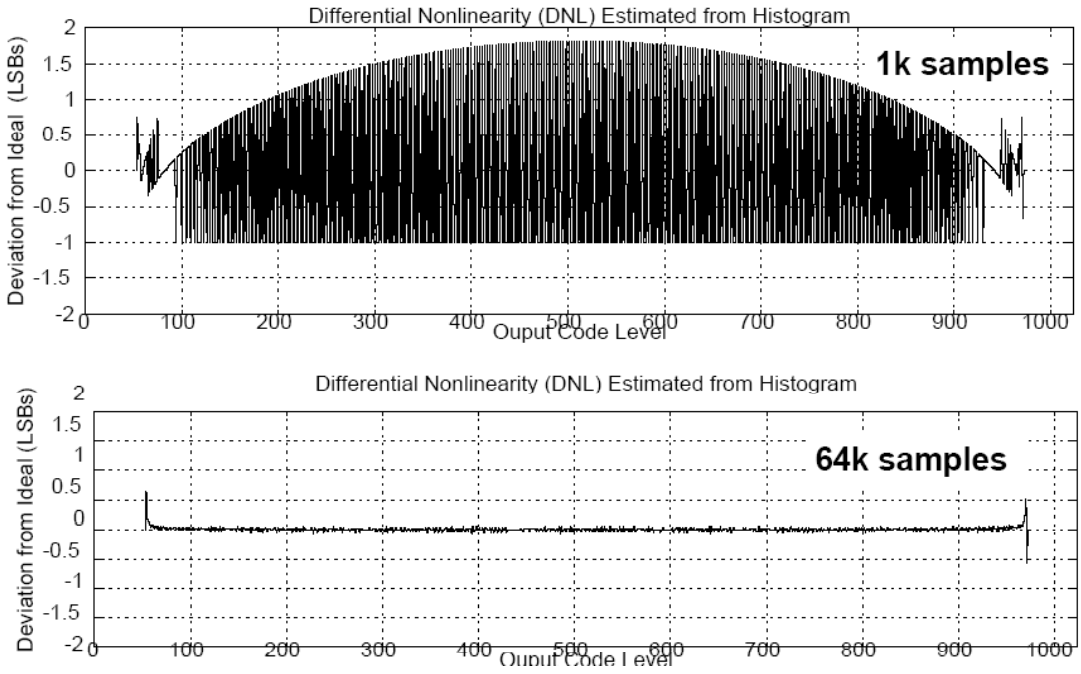
$$P(y_1, y_2) = \frac{1}{\pi}[\text{asin}(y_2) - \text{asin}(y_1)]$$

$$P(\theta_1, \theta_2) = \frac{1}{\pi}(\Delta\theta)$$

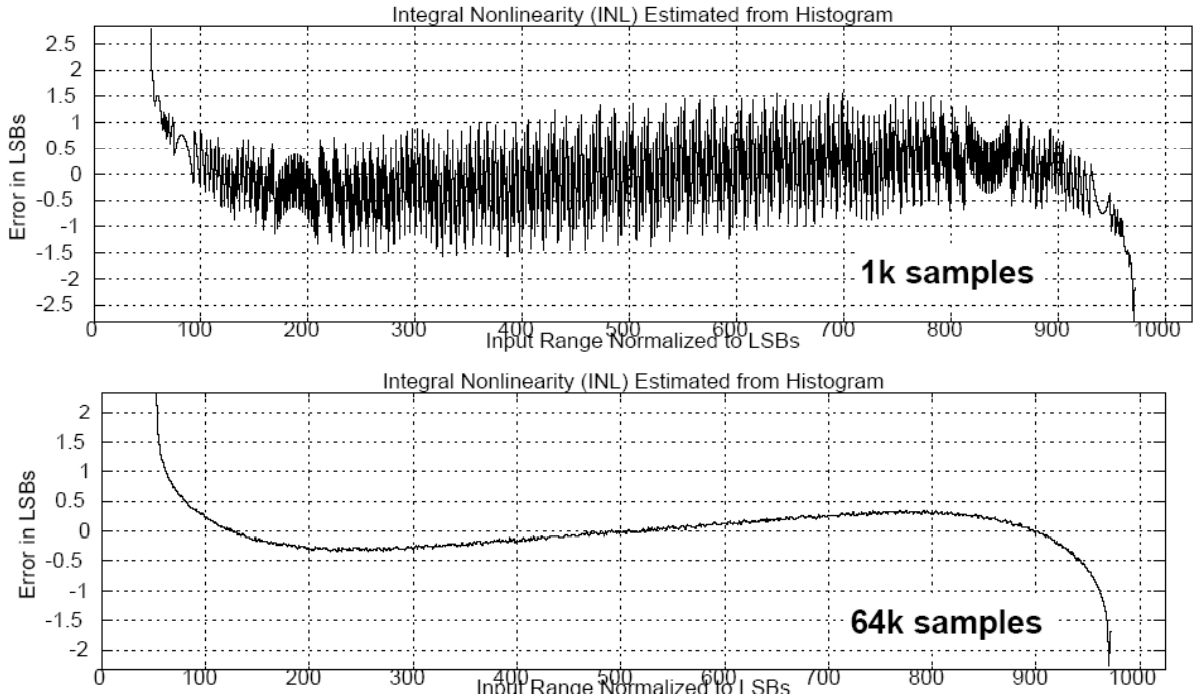
Histogram Technique vs. Sample Size



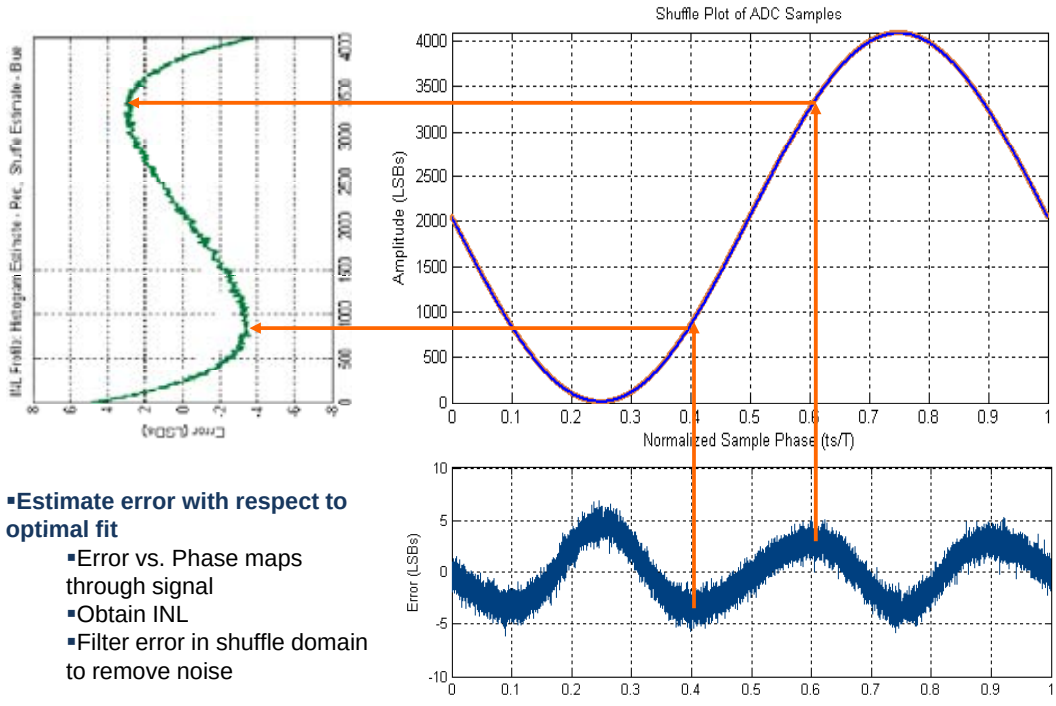
Estimation of DNL vs. Sample Size



Estimation of INL vs. Sample Size

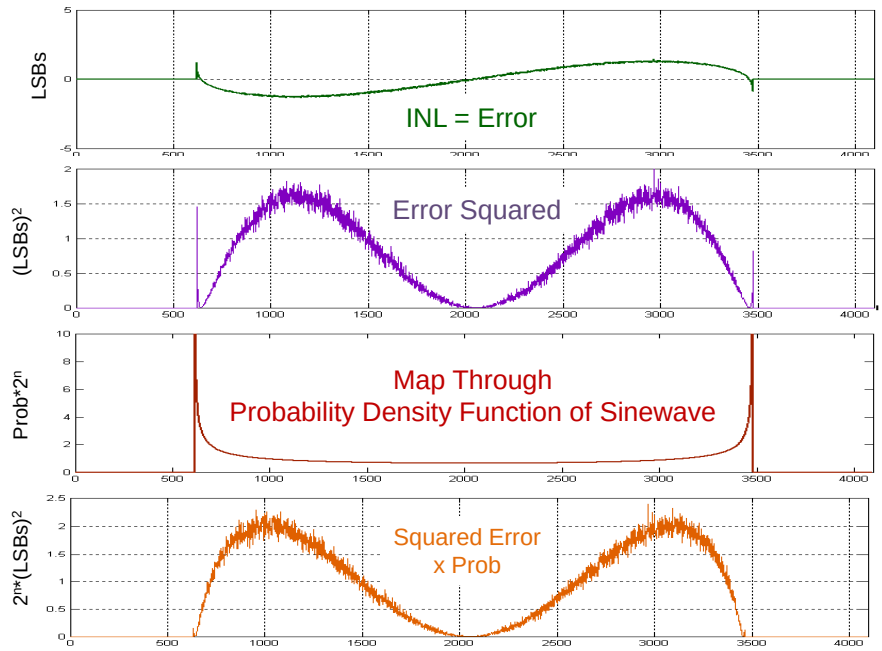


INL from Shuffle Plot



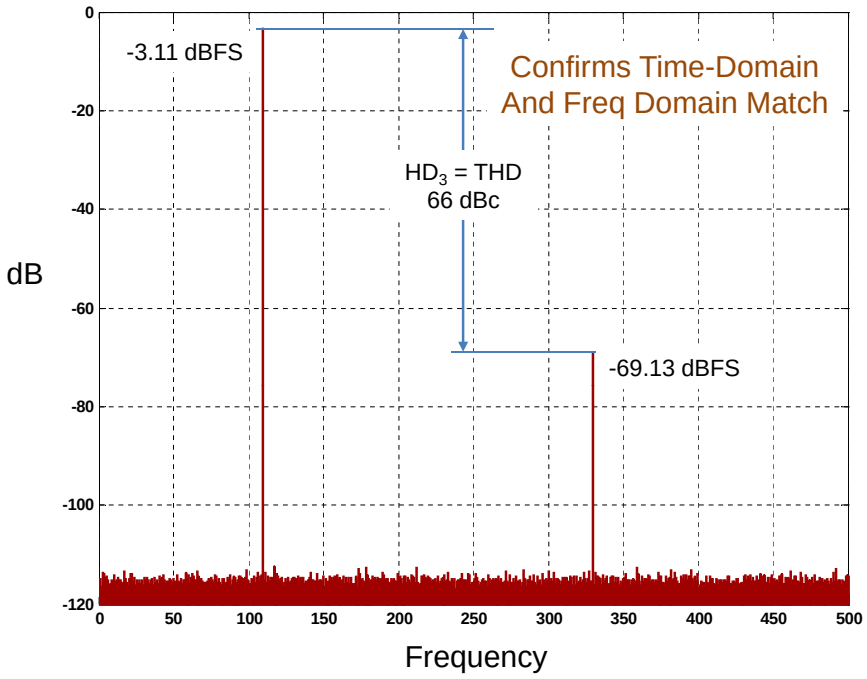
- **Estimate error with respect to optimal fit**
  - Error vs. Phase maps through signal
  - Obtain INL
  - Filter error in shuffle domain to remove noise

INL Relationship to THD



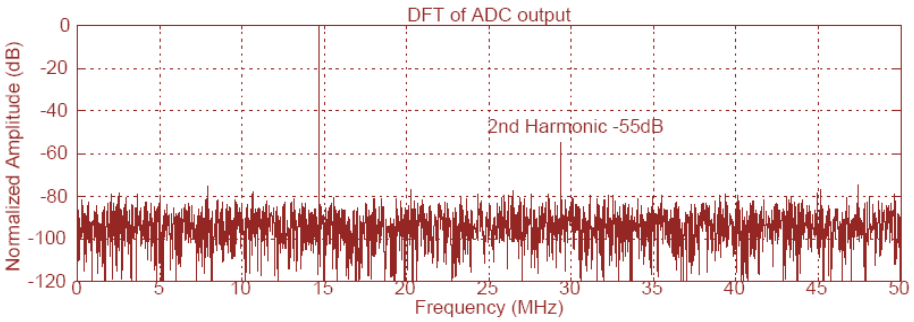
$$\left[\int INL^2(y)P_y(y)dy\right]^{\frac{1}{2}} = 0.5\,\text{LSBs}$$ THD = 66-dBc @ 70% Full-Scale

INL Relationship to THD

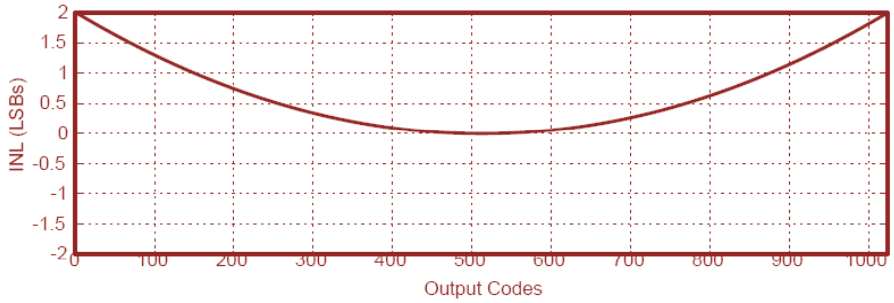


Interpretations of Distortion

INL with Even-Order Distortion

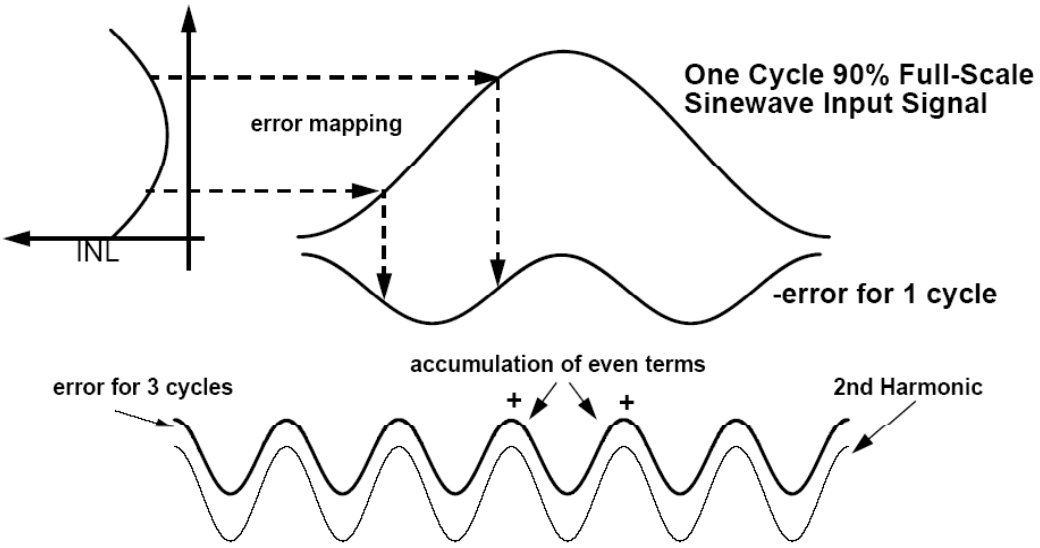


THD = 8.9-bits
90% loading



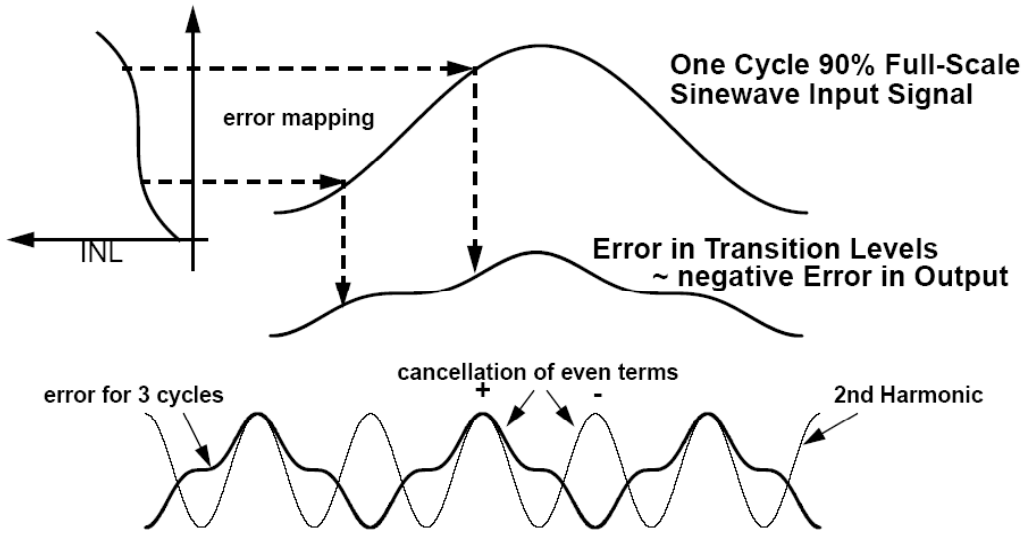
INL ± 1

Error vs. Time for 2nd-Order Distortion



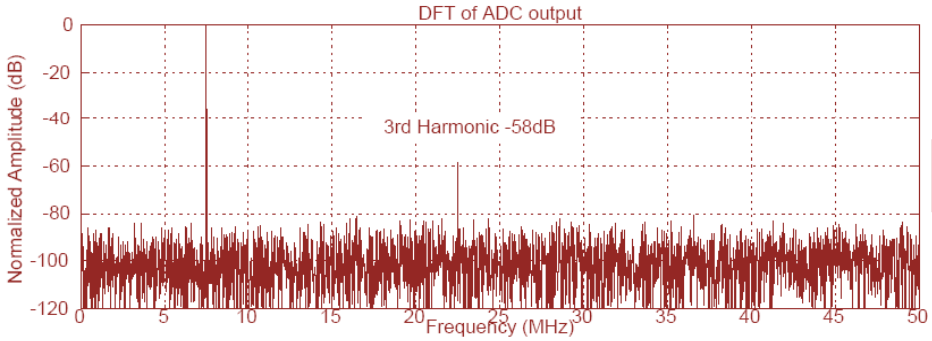
- **2nd-Order Distortion**
  - Produces a 2nd-harmonic + DC offset

Determining Harmonics from INL Profile

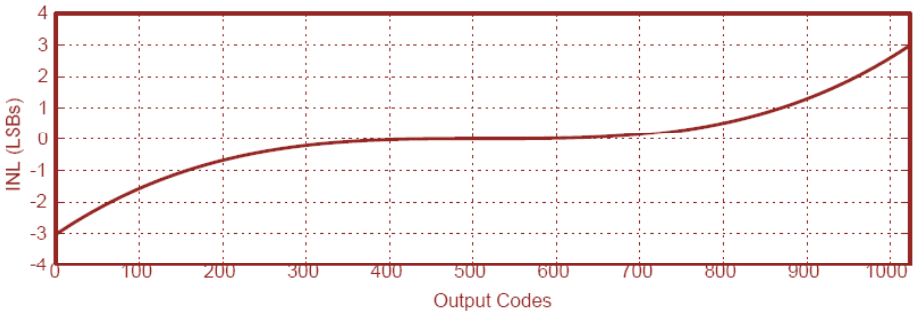


- **To find distortion (THD) from INL profile**
  - Take % loaded section of INL profile and distort though a sinewave mapping
  - Flip it horizontally to produce the error over one complete cycle of the input signal
  - Take DFT of the error. The frequency content is the harmonic distortion

INL with 3rd-Order Distortion

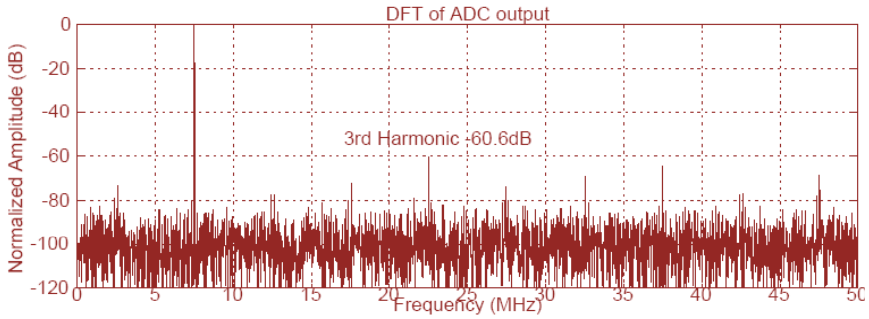


THD = 9.4-bits
90% loading

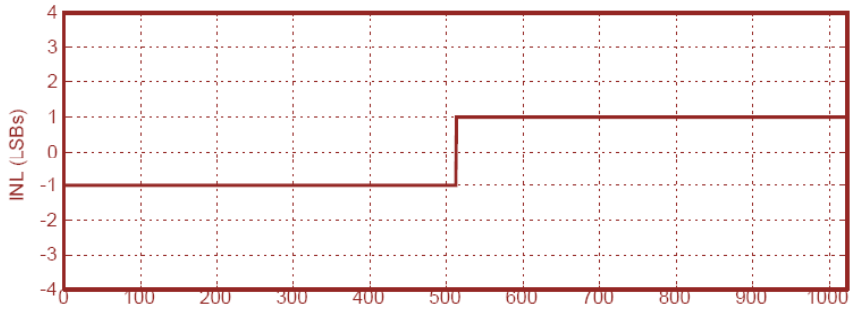


INL ± 3

INL with Abrupt Nonlinearity

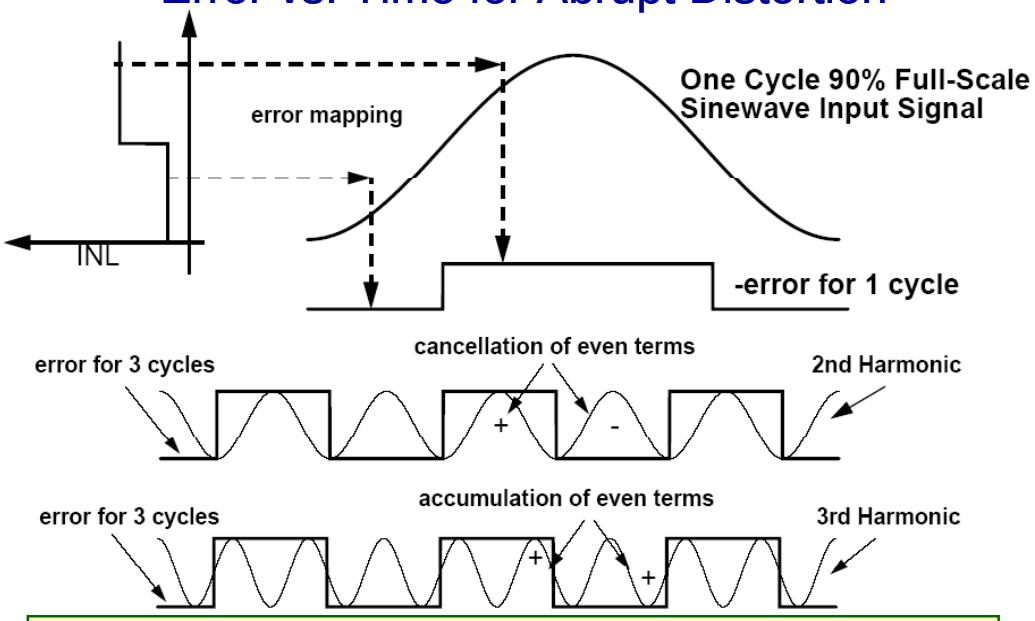


THD = 9.3-bits
90% loading



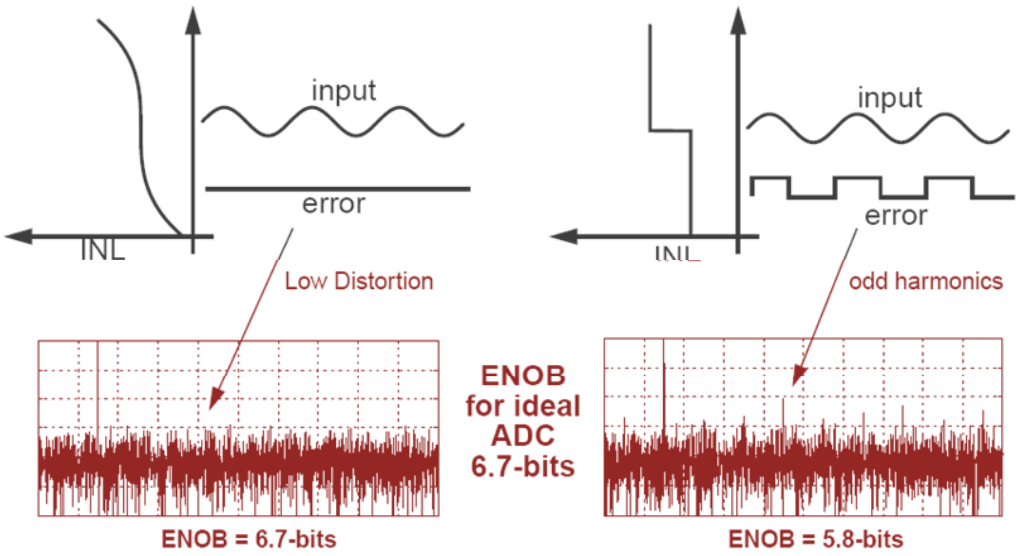
INL ± 1

Error vs. Time for Abrupt Distortion



- **Abrupt Nonlinearity with Odd-Symmetry**
  - Perfect cancelation with respect to even harmonics
  - Accumulation with Odd-Harmonics
  - Non 50% duty-cycle (offset in mid-code) will produce residual even-order

Which ADC is "Better" Abrupt vs. Smooth for Small Signals

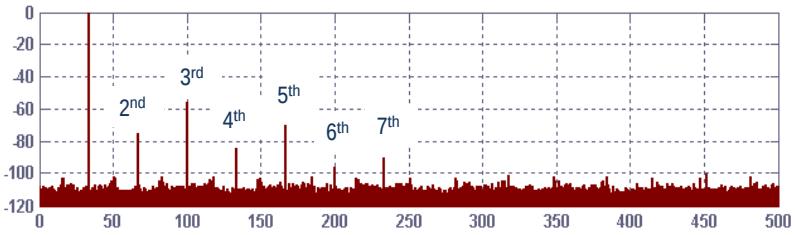


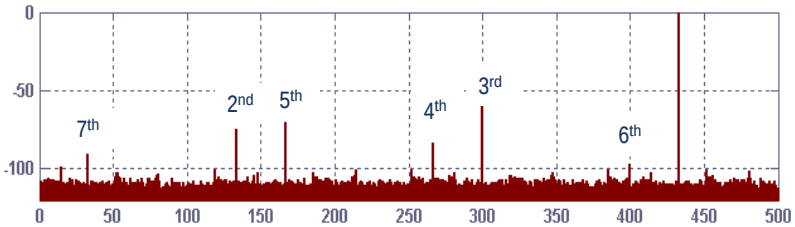
ADCs have ~equal ENOB at 90% loading

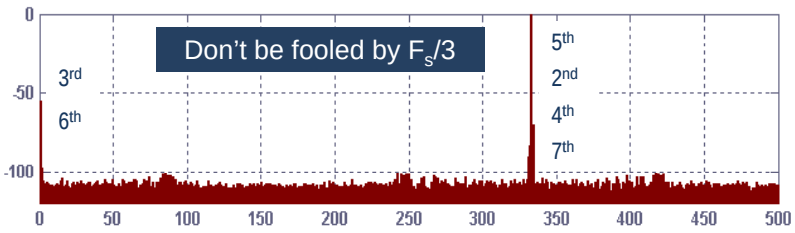
Abrupt nonlinearity is bad for low-level signals
Need dither to "smooth out" errors and reduce spurs

Harmonics and Multi-Tone Testing

Harmonic Folding

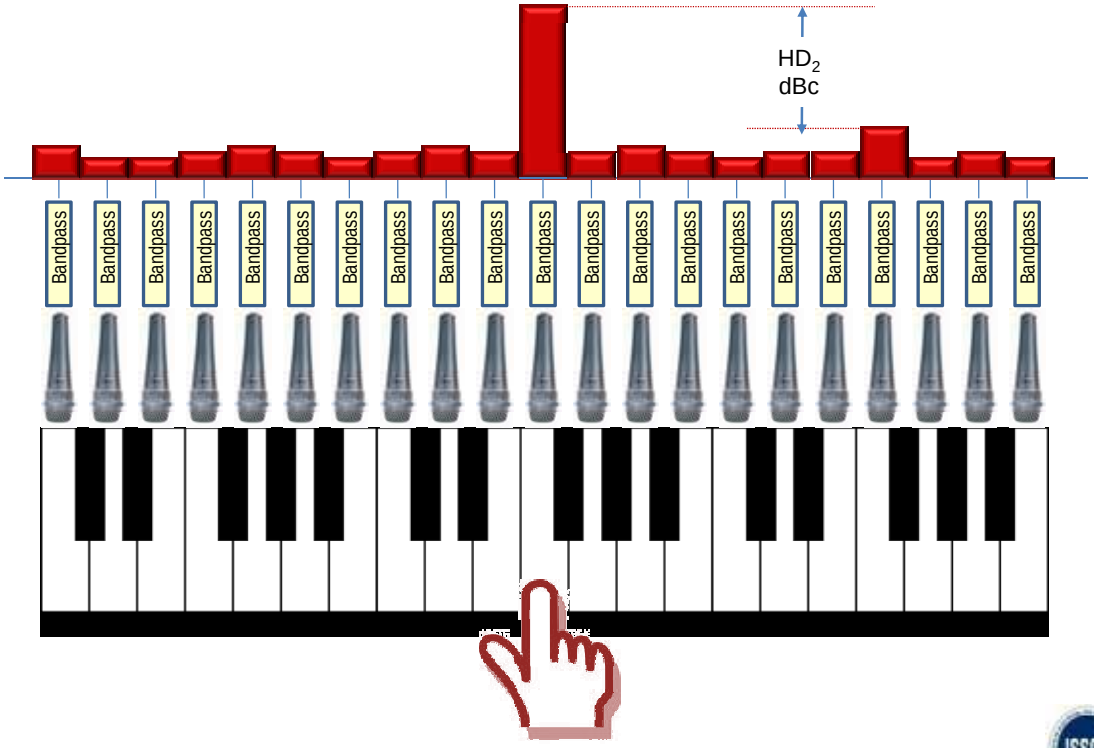




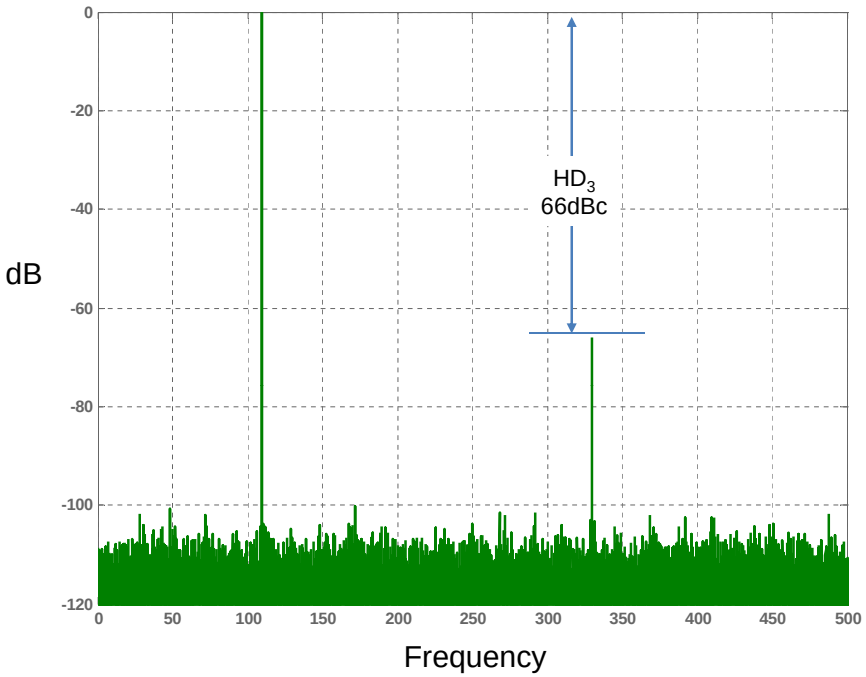


Harmonics bounce back and forth around Nyquist and DC

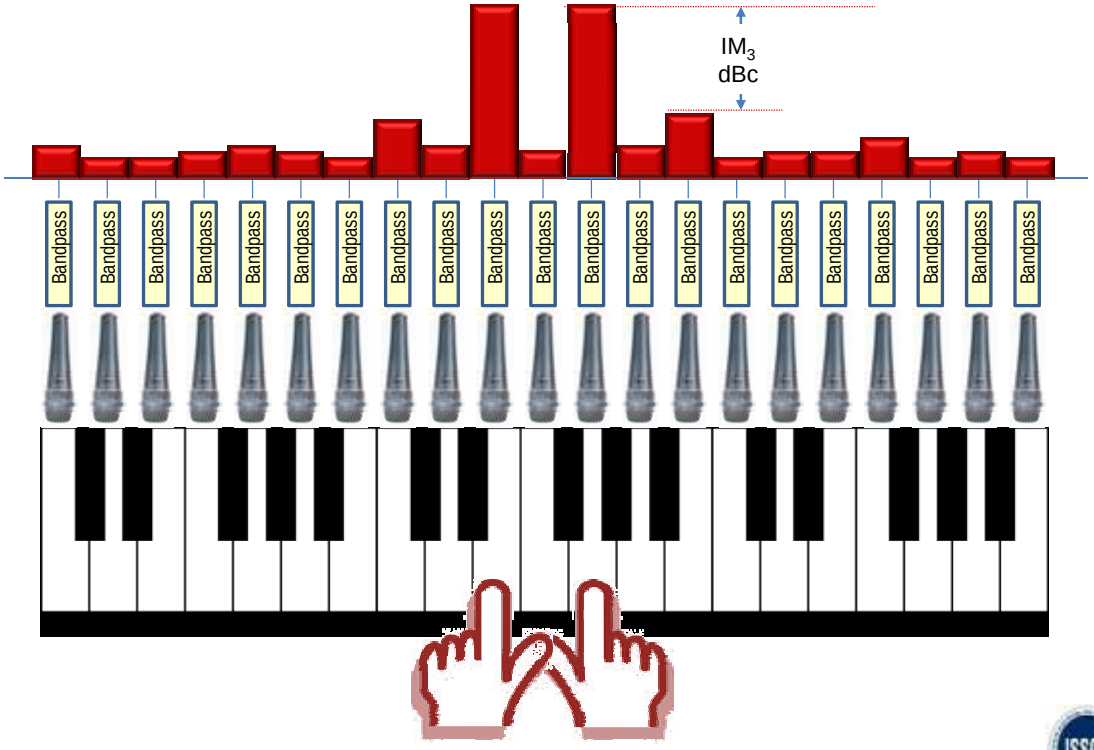
Single Tone Testing



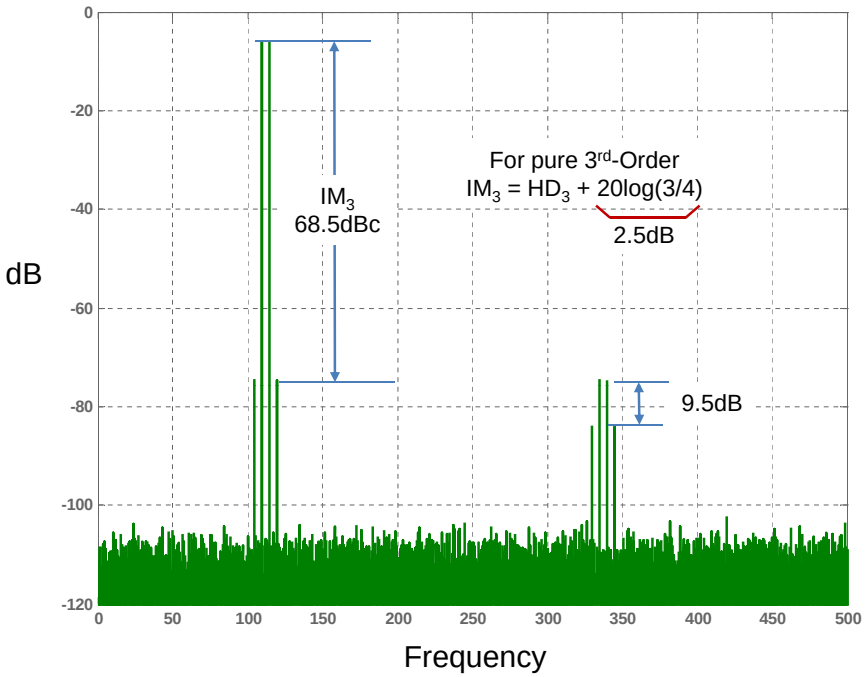
Single Tone Example



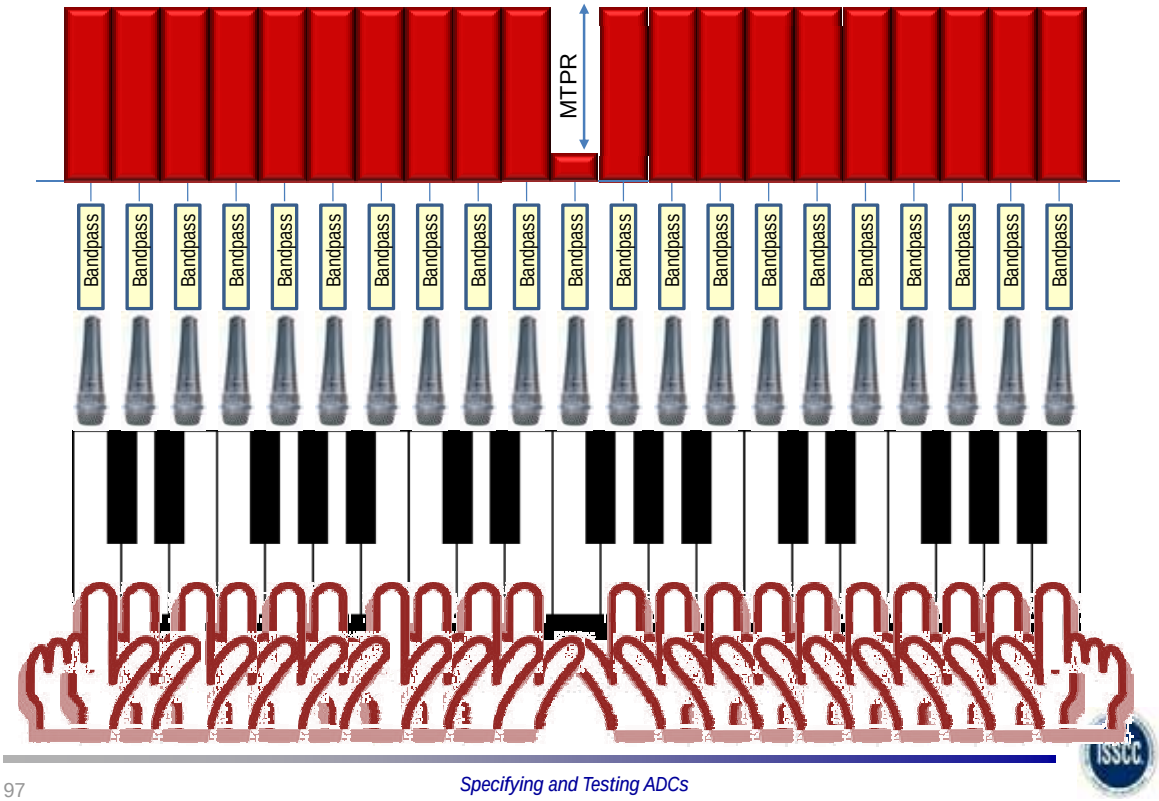
Two-Tone Testing



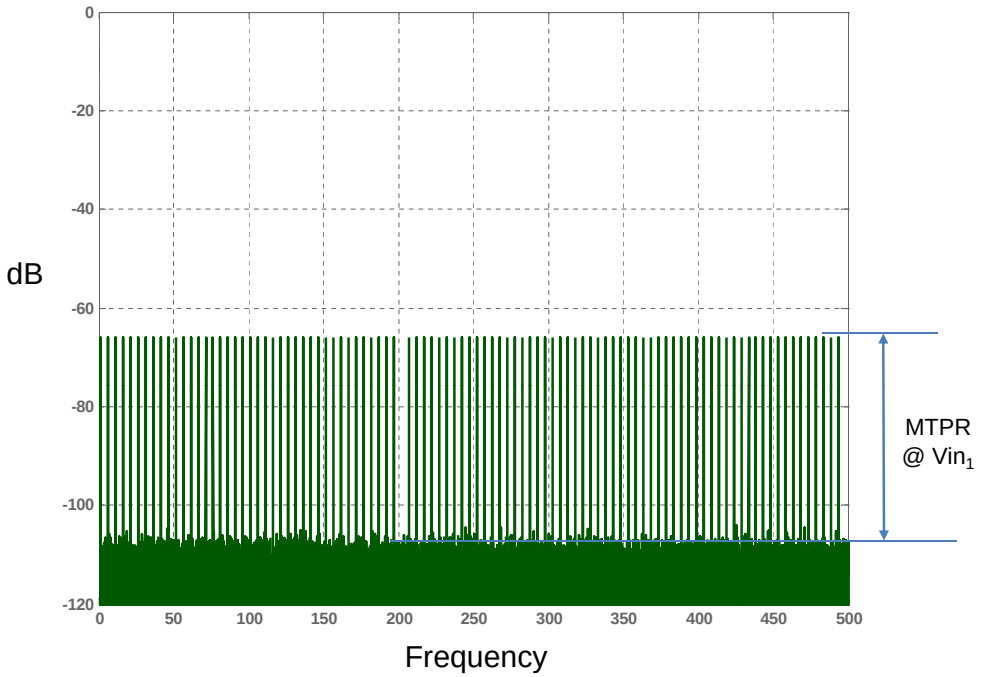
Two-Tone vs. Single Tone



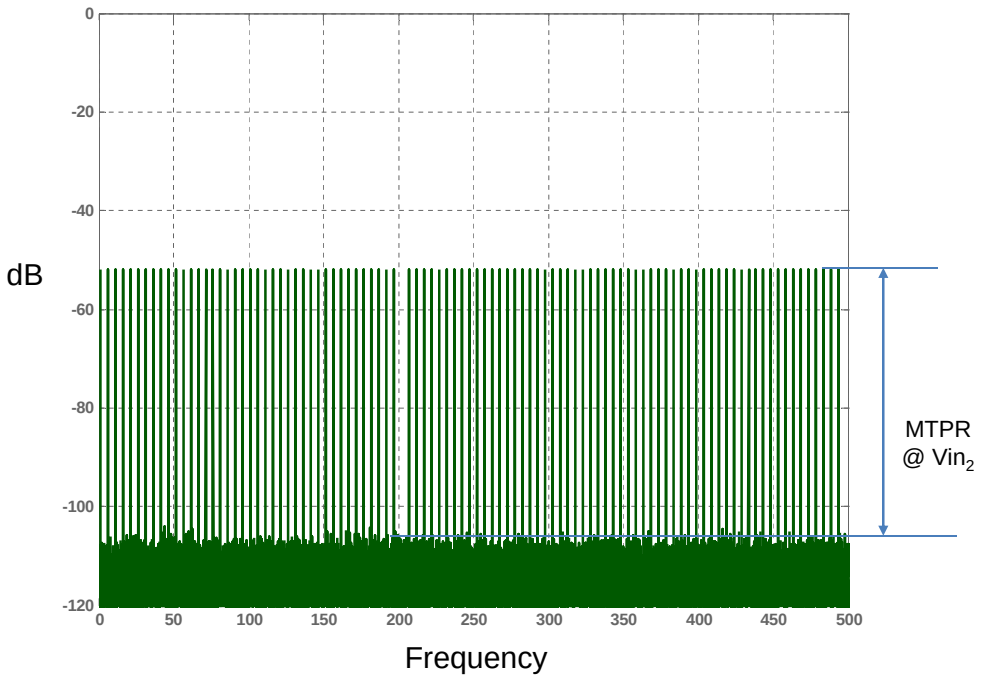
Multi-Tone Testing



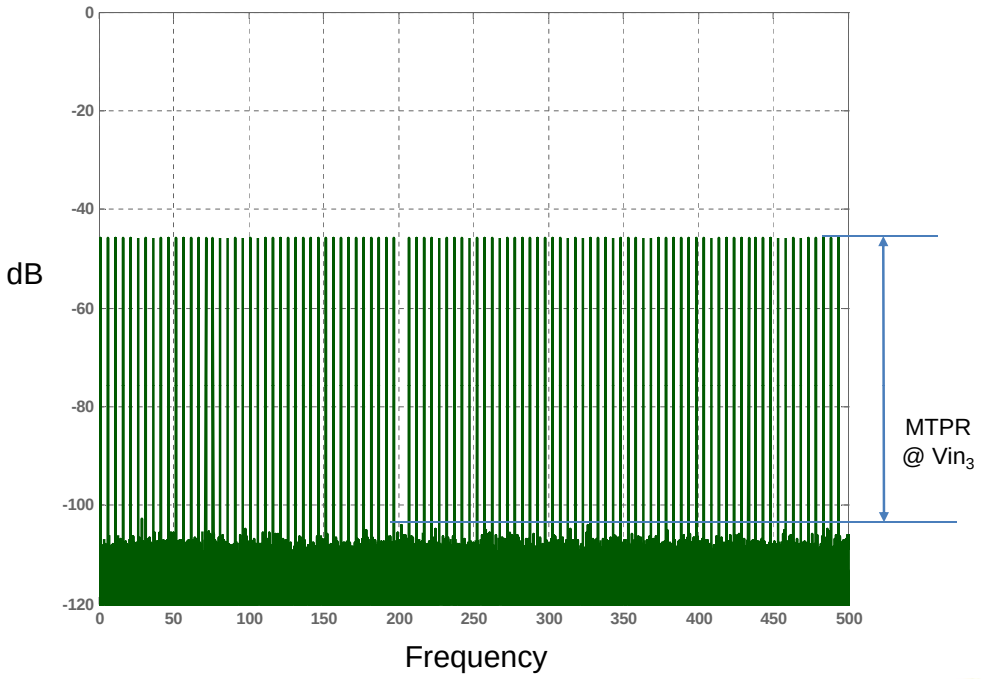
MTPR, NPR, CTB, CSO & More….



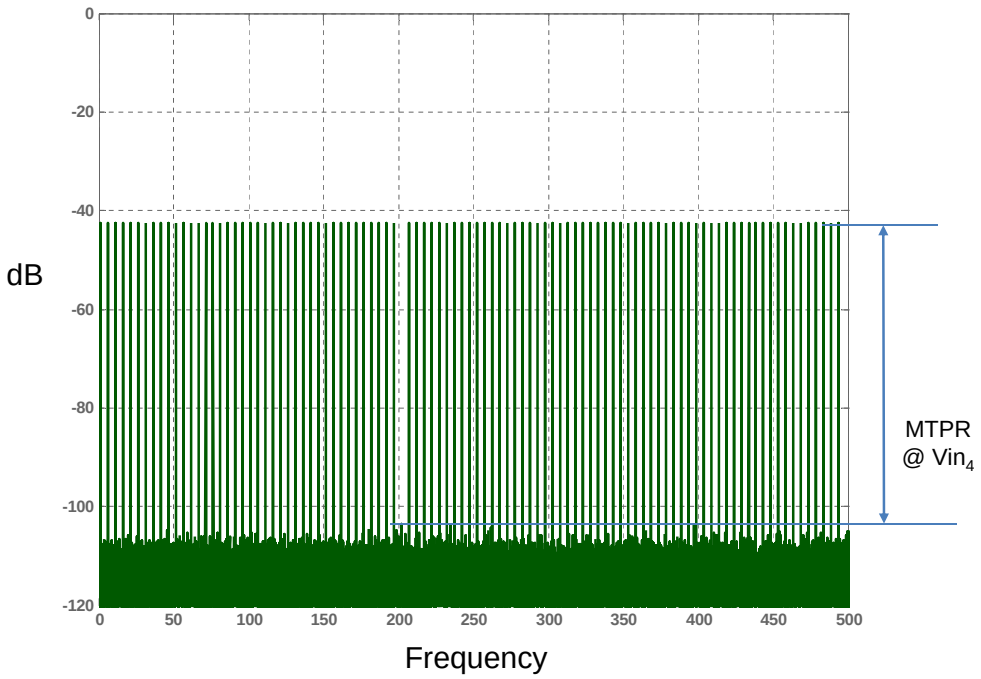
MTPR, NPR, CTB, CSO & More….



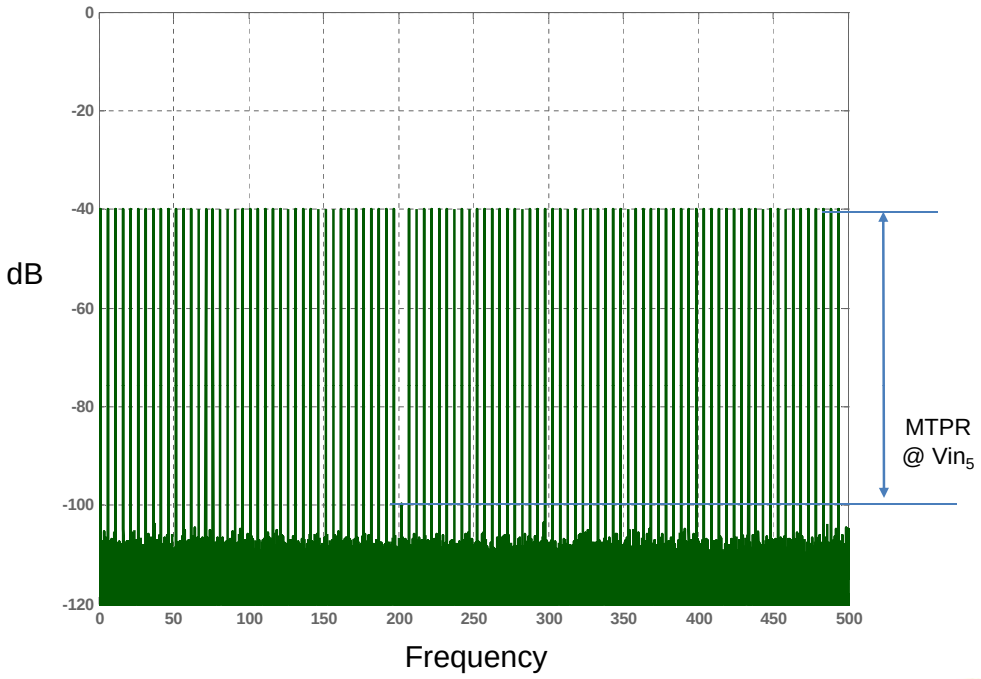
MTPR, NPR, CTB, CSO & More….



MTPR, NPR, CTB, CSO & More….



MTPR, NPR, CTB, CSO & More….



Specs Discussed Thus Far

ADC Specs (some)
~~Offset~~
~~Gain Error~~
~~Missing Codes~~
~~INL~~
~~DNL~~
~~SNR~~
~~SFDR~~
~~THD~~
~~SNDR~~
~~NPR~~
~~MTPR~~
~~IM2~~
~~IM3~~
IP3
ERBW
~~BER~~
~~Aperture uncertainty~~
Aperture delay
Power
FoM

Make sure you characterize your ADC and plot SNR, SFDR, THD, SNDR vs. F_{in} at a given F_s and for various Fs at a fixed ratio of F_{in}/F_s

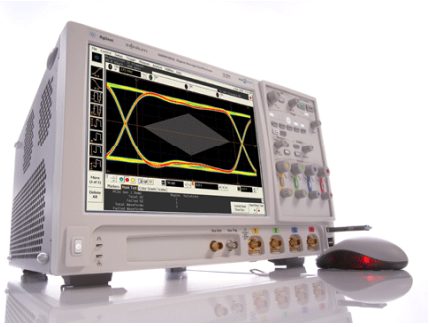
Assorted Analysis & Debugging Techniques

Analysis = Capture + DSP

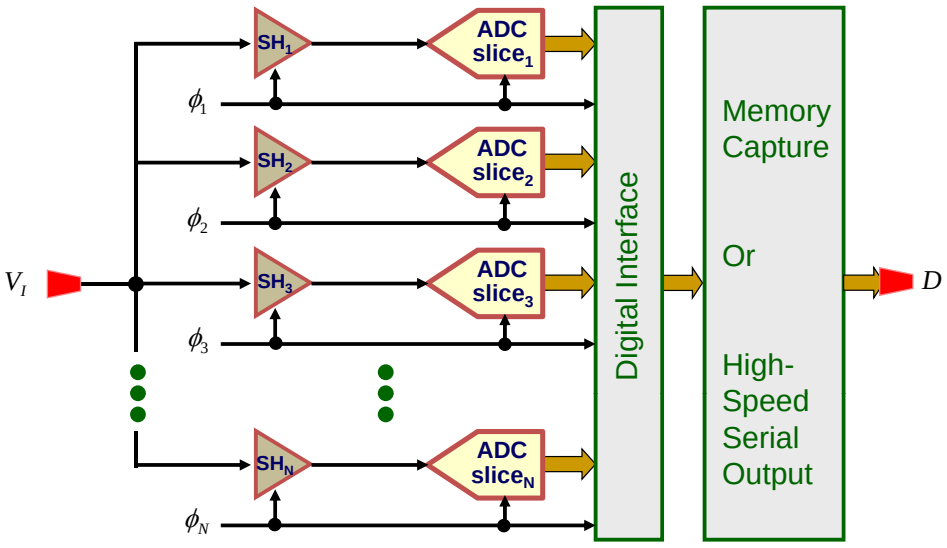
Modern real-time oscilloscopes are sophisticated data capture and analysis systems

All the fancy features on a scope can be recreated in the lab with enough data, accuracy and programming expertise

Data analysis can be targeted specifically for parameter estimation of the ADC architecture under test

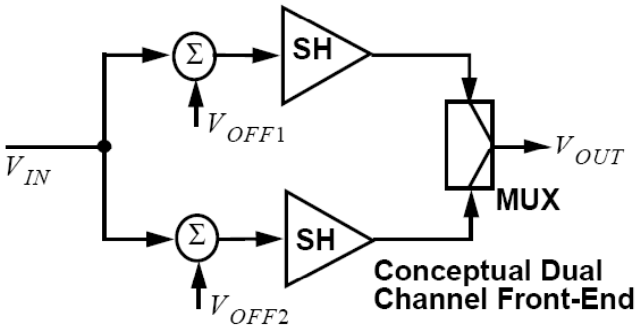


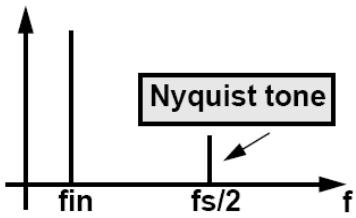
Time Interleaved ADCs

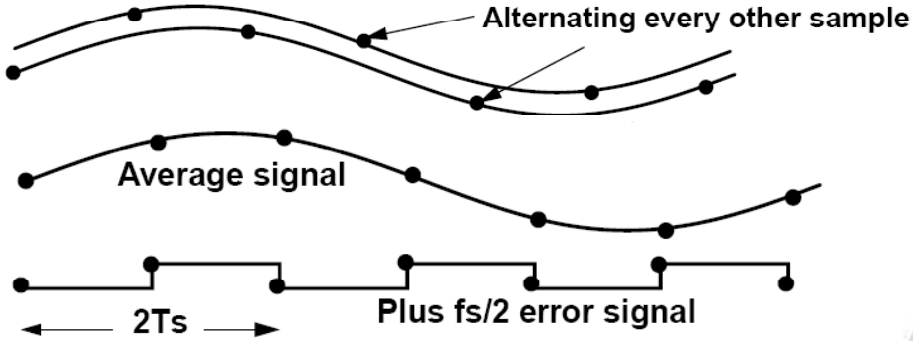


- **Time Interleaved Architecture**
  - Optimal for data capture with large frame size and high speed
  - Optimal for continuous output ADCs
  - Memory added for data capture
  - High-speed Serial I/O added for efficient data output

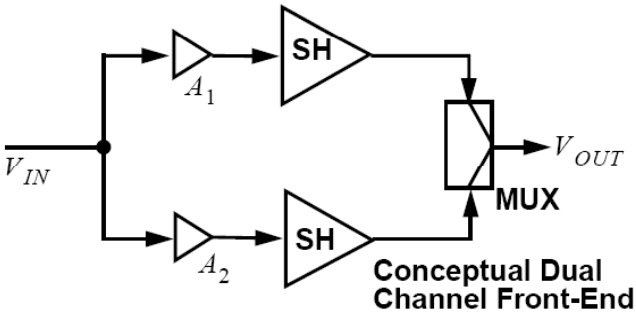
Time Interleaved ADCs, Offsets

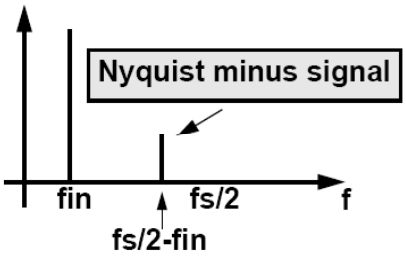


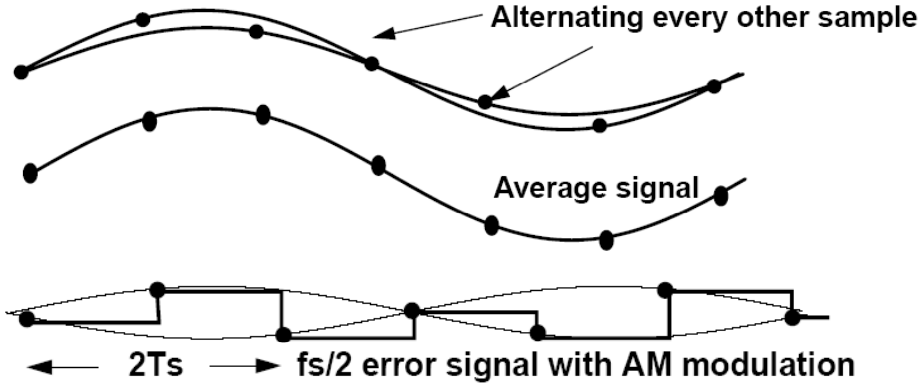




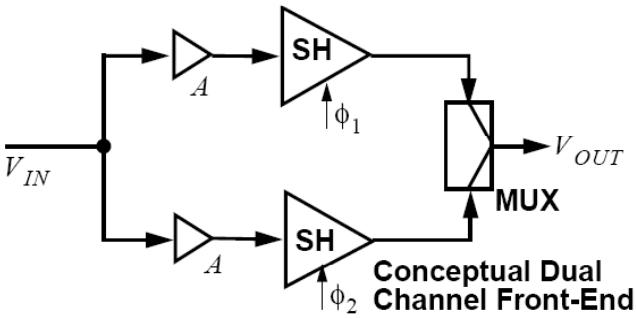
Time Interleaved ADCs, Gain Mistmatch

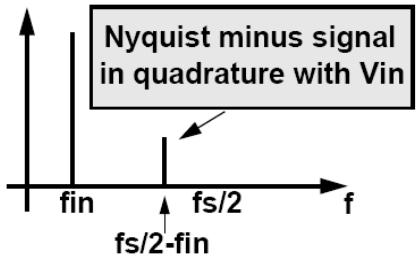


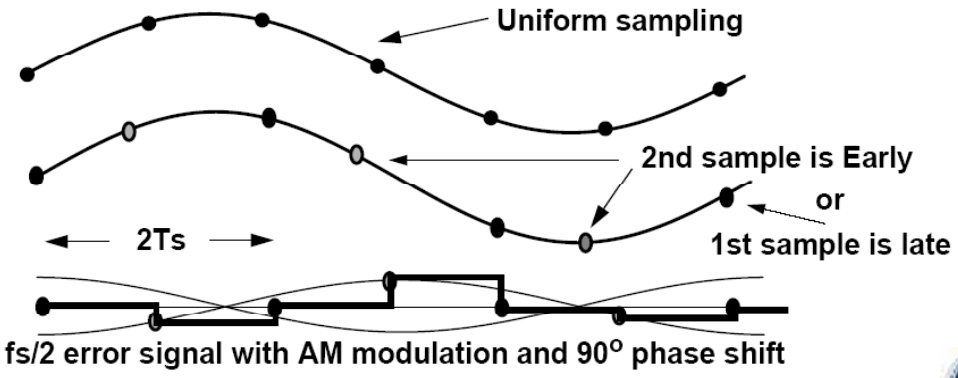




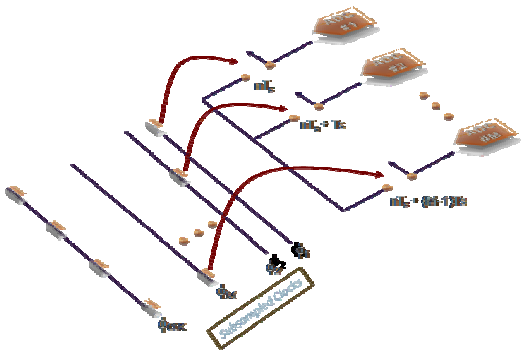
Time Interleaved ADCs, Time Skew

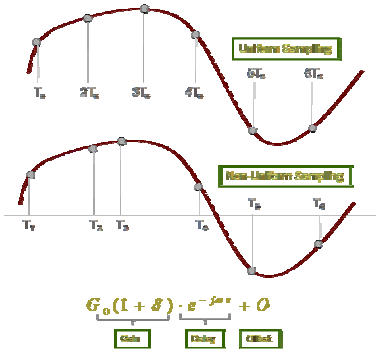




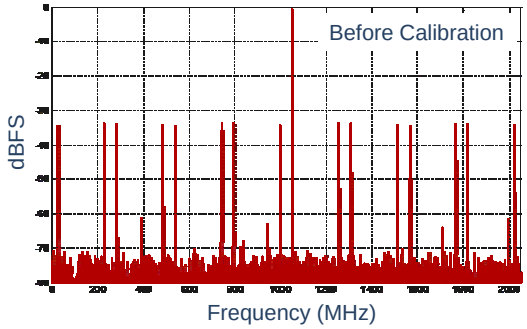


ADC Calibration Techniques: Time Interleaved

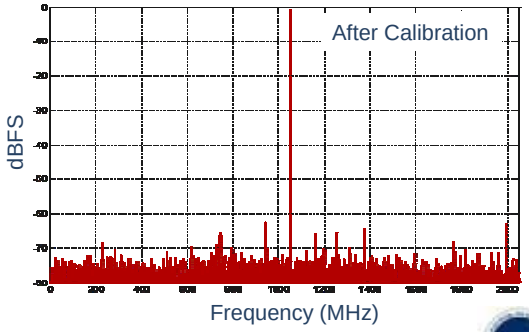




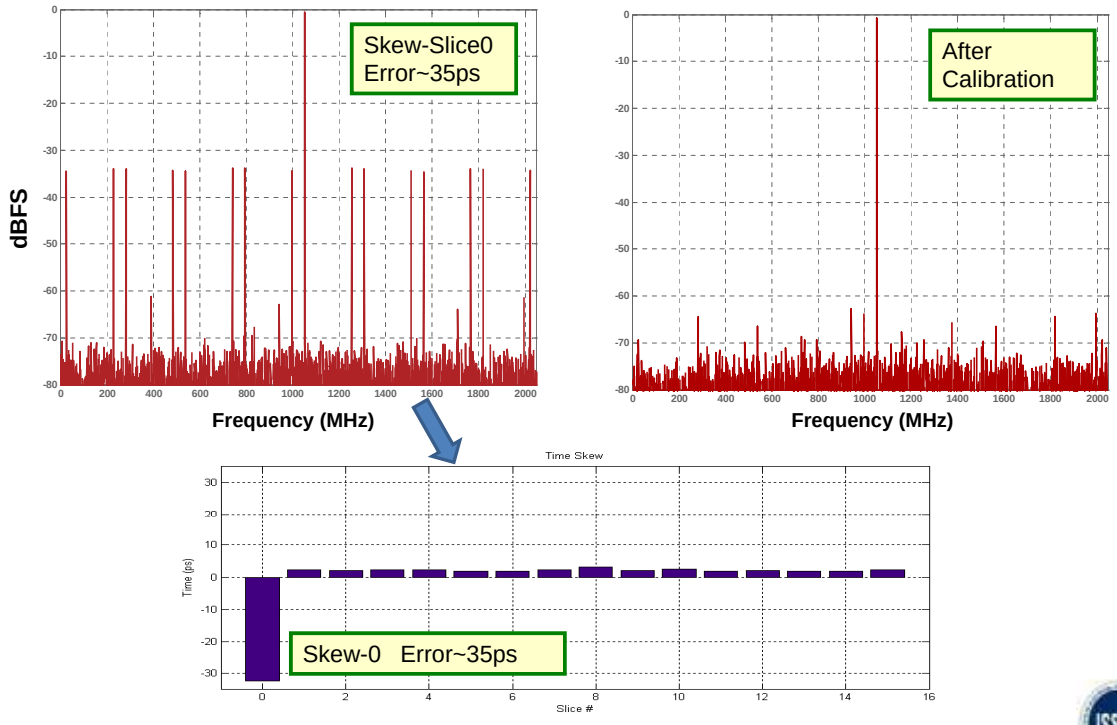
F_{in} = 1.05-GHz, F_s = 4-GS/s



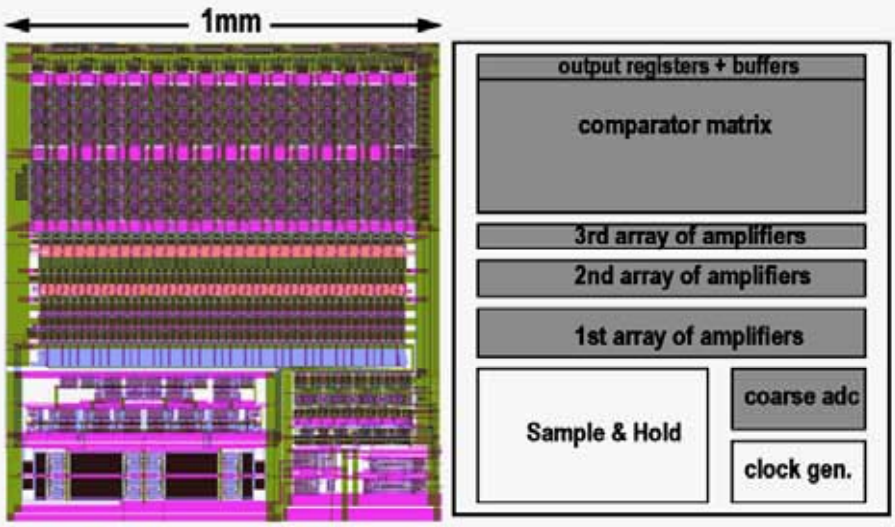
F_{in} = 1.05-GHz, F_s = 4-GS/s



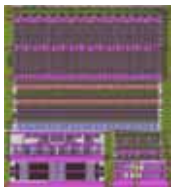
Example 16-channel Time Interleaving



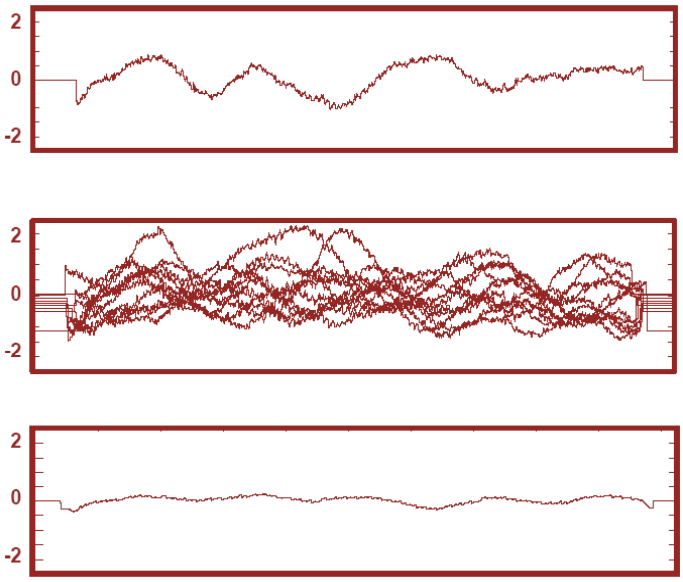
Layout of Folding Averaging ADC



Debug Examples: Ensemble Averaging



10-bit ADC with folding averaging and interpolation

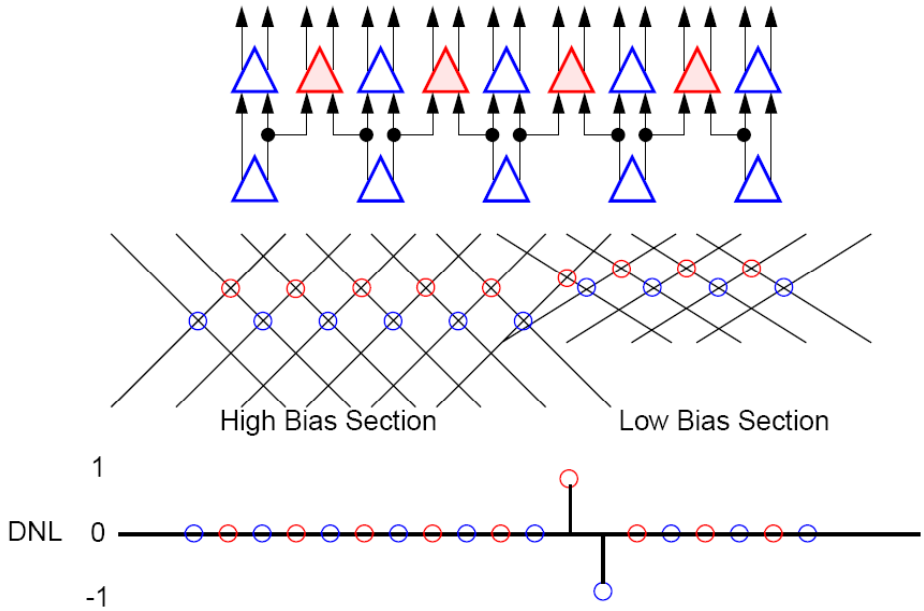


Typical INL Profile
errors are correlated due to averaging

10 INL Profiles

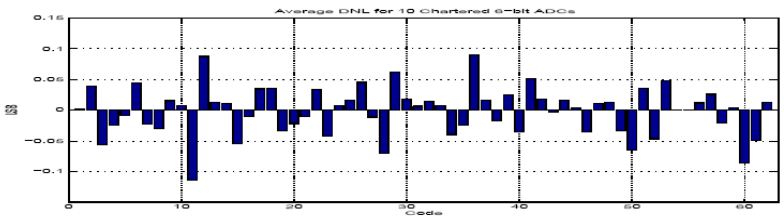
Average of 239 INL Profiles
Mean(INL) shows some residual systematic errors, but much smaller than the random variation

Debug Examples: Bias Mismatch Impact on DNL

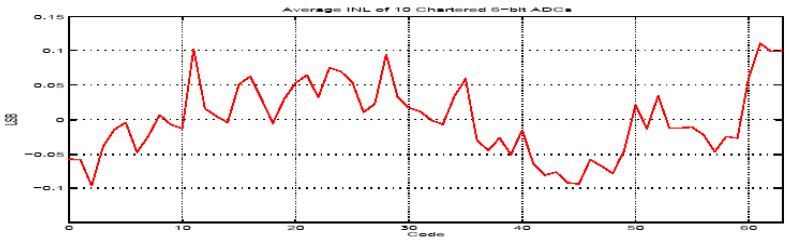


- Pseudo-differential interpolation requires matching of bias currents
- Offsets occur when bias current of adjacent stages are unequal

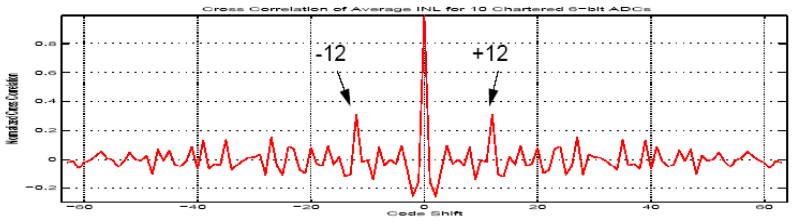
Examples Debug: Bias Mismatch Impact on DNL



Mean DNL (10 Parts)



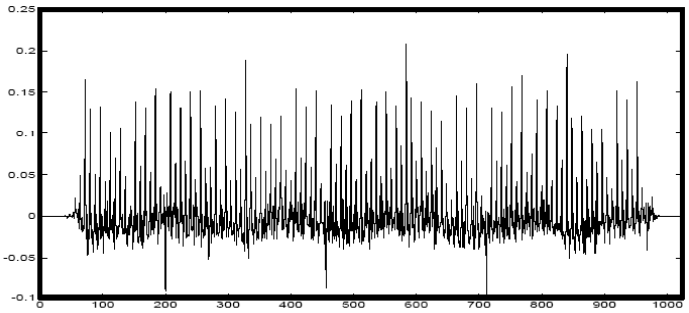
Mean INL (10 Parts)



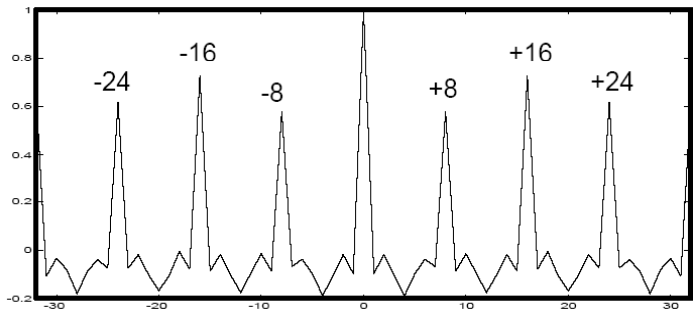
Xcorr(mean(INL))

Correlation of error at 12-code spacing follows the same patterns as the biasing scheme

Systematic Offset: Autocorrelation of Average DNL



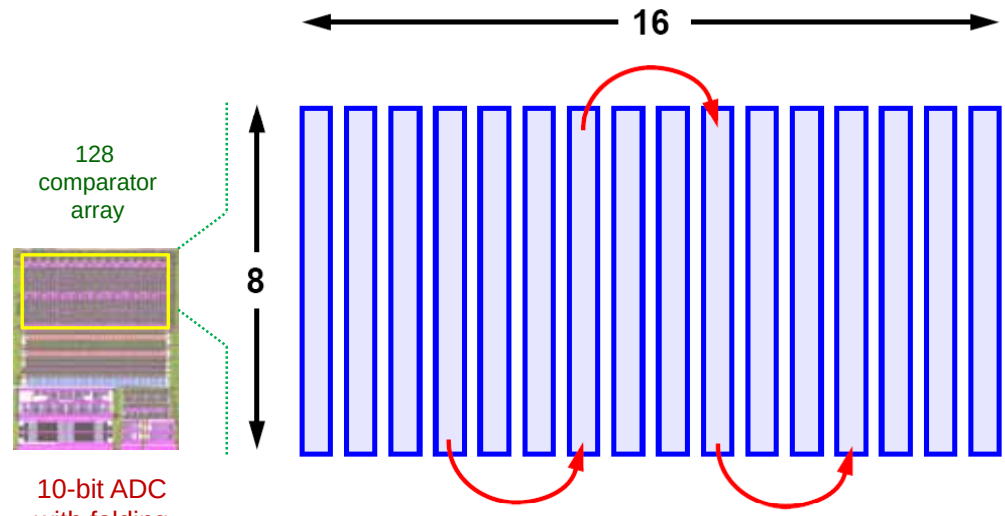
Average DNL of 239 10-bit folding ADCs



Autocorrelation of Average DNL showing high correlation of errors every 8 codes

Averaging and DSP can extract information very accurately

Systematic Comparator Offset due to Layout

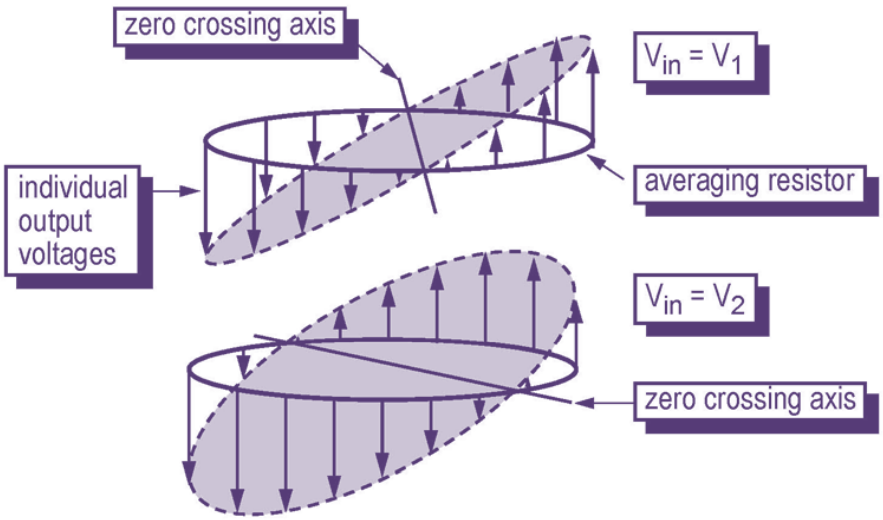


10-bit ADC with folding averaging and interpolation

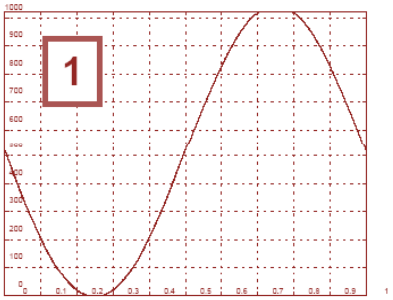
To remove systematic gradients, routing of comparators meanders through the array

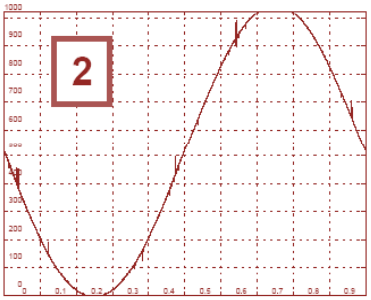
Discontinuity in array causes every 8th comparator to see different routing than the others.

Voltage Distribution on Averaging Resistor



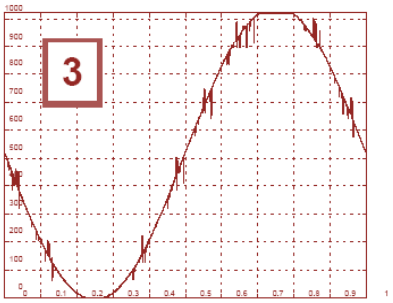
“Movies” in the Shuffle-Plot Domain vs. Cmp VDD

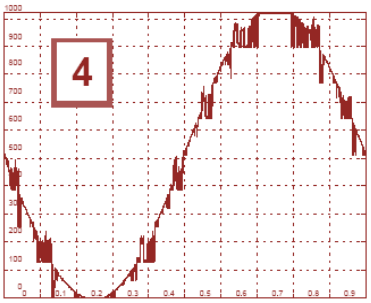




Even sections of 128 codes fail first

Comparator has systematic hysteresis, plus an error due to current clamping in the comparator





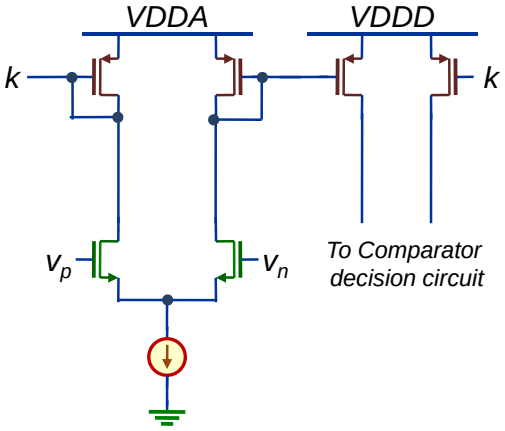
Unable to overcome systematic or hysteresis-induced offsets.

Stupid mistake on my part with a current mirror on 2 supplies

Showing data in sequences vs. any parameter leads to new revelations

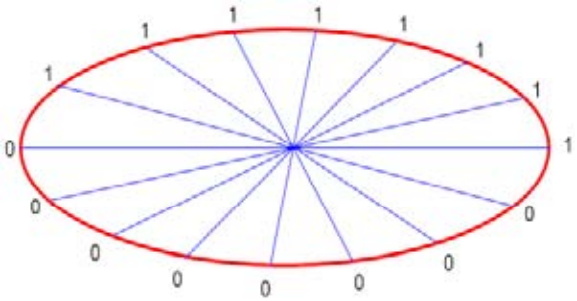
The Problem: Cyclic Thermometer Code in Folding ADC

This is a really bad idea, that I have never repeated, but I did it with good intentions



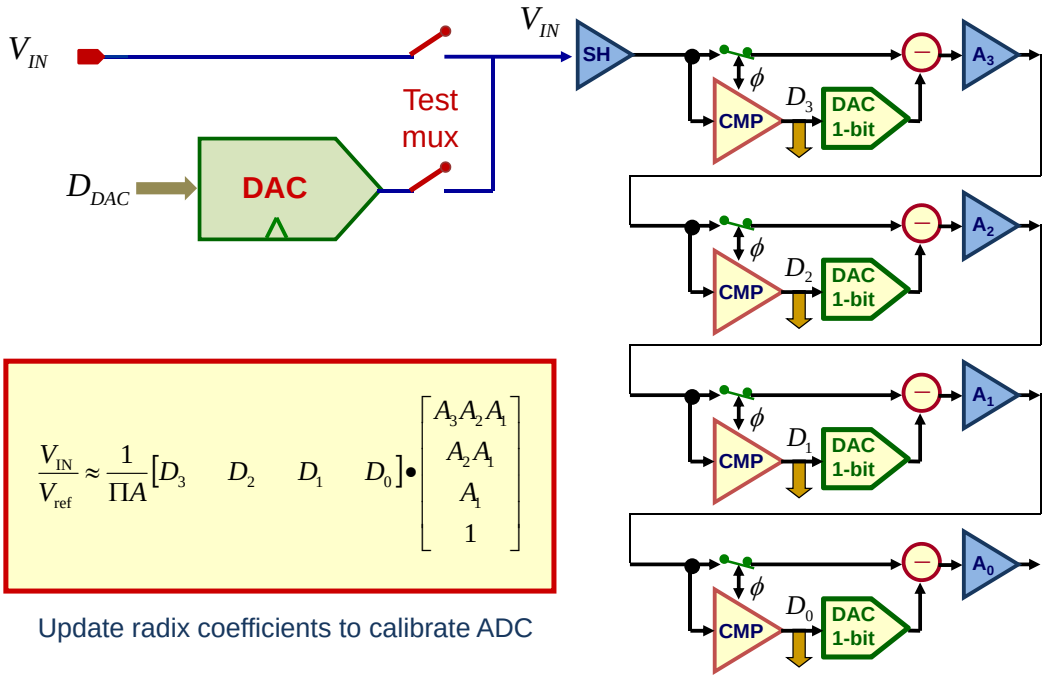
Comparator Preamp

Phantom Thermometer Code:
Off half cycle 0-to-1 transition
Even half cycle 1-to-0 transition



By looking at “movie” was able to realize that comparator strength was asymmetric due to IR drop between VDDA and VDDD

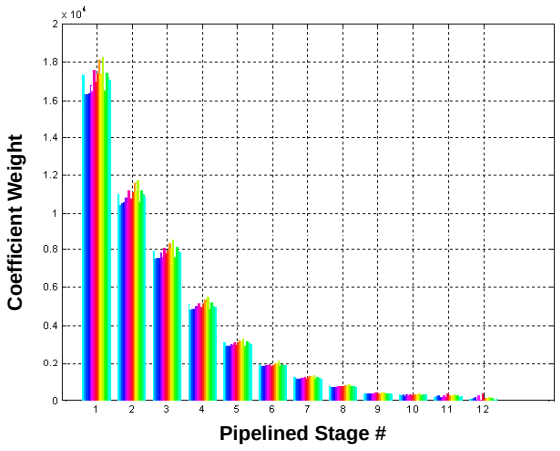
DC Testing: Foreground Calibration

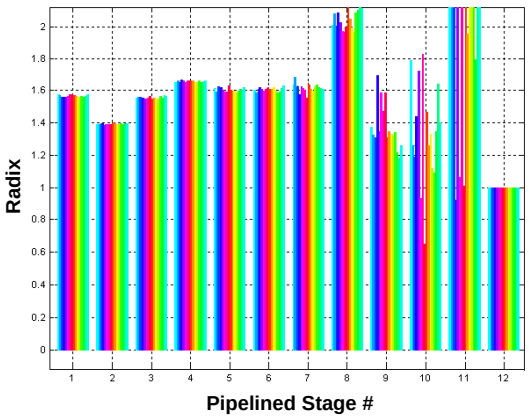


$$\frac{V_{IN}}{V_{ref}} \approx \frac{1}{\Pi A}\begin{bmatrix} D_3 & D_2 & D_1 & D_0 \end{bmatrix} \bullet \begin{bmatrix} A_3A_2A_1 \\ A_2A_1 \\ A_1 \\ 1 \end{bmatrix}$$

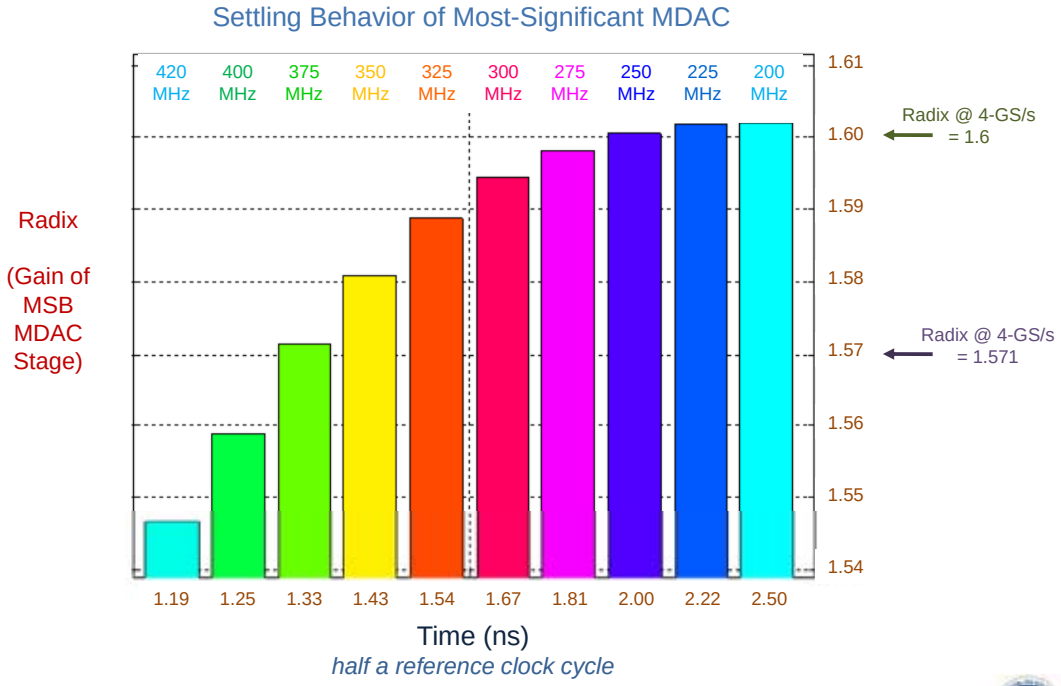
Update radix coefficients to calibrate ADC

Radix Calibration





Radix Evaluation and Settling Behavior



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"High Performance Data Converter Testing"

David Robertson
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Robert Neff
Private Communication: High-speed testing & BER testing

Michael Flynn
Private Communication: High-speed testing & BER testing

Un-Ku Moon & Boris Murmann
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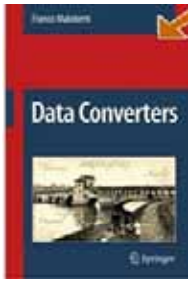
References: 1 of 2

The Data Conversion Handbook
Walt Kester (Editor) *Chapters 2,5*



Data Converters
Franco Maloberti
Chapters 2,9

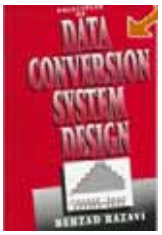
IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters

IEEE Std 1241-2000

References: 2 of 2

CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters
Rudy van de Plassche
Chapters 1-3

CMOS Mixed-Signal Circuit Design
R. Jacob Baker



Data Conversion System Design
Behzad Razavi
Chapter 9

CMOS Data Converters for Communications
Gustavsson, Wikner and Tan
Chapter 1

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