Fractional-*N* PLLs

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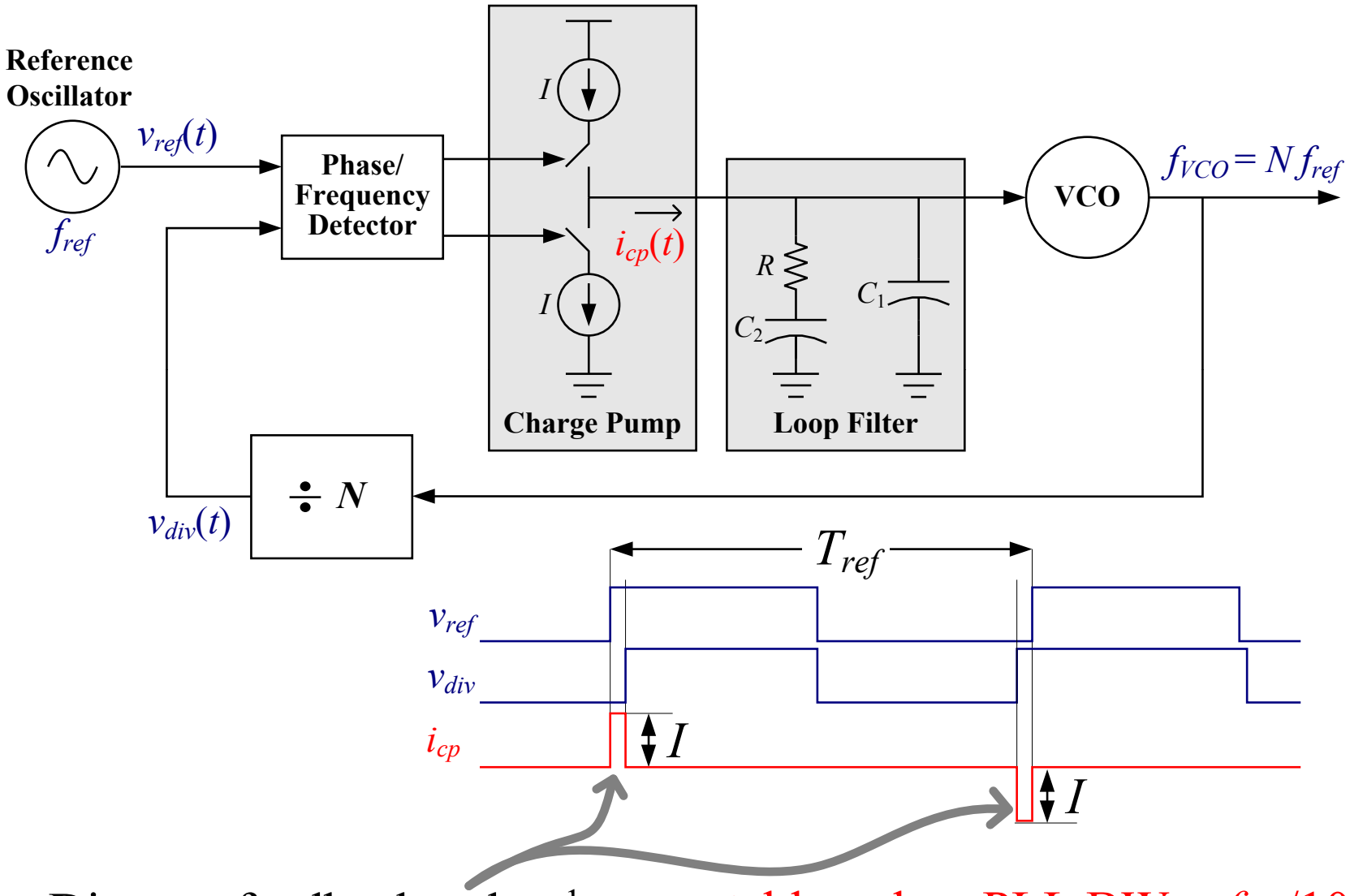
February 11, 2010

Outline

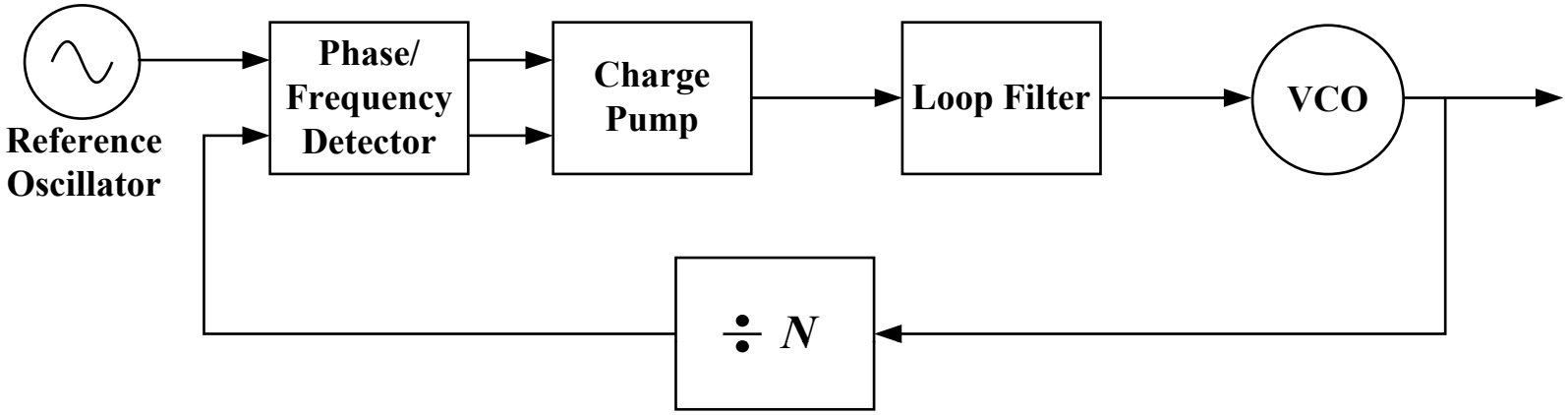
- Summary of Integer-*N* PLL Limitations
- The Idea Behind Fractional-*N* PLLs
- Delta-Sigma Modulation Overview
- Fractional-*N* PLL Dynamics
- Spurious Tones in Fractional-*N* PLLs
- Fractional-*N* PLL Bandwidth Enhancement
- IC Implementation Examples (bonus slides: not presented)

A Typical Integer-*N* PLL



Discrete feedback pulses[1] ⇒ unstable unless PLL BW < $f_{ref}/10$

Integer-*N* PLL Limitations



Have fundamental resolution/bandwidth/noise tradeoff

Lower f_{ref} (larger N) for a given f_{VCO}

$\Rightarrow$ finer tuning resolution

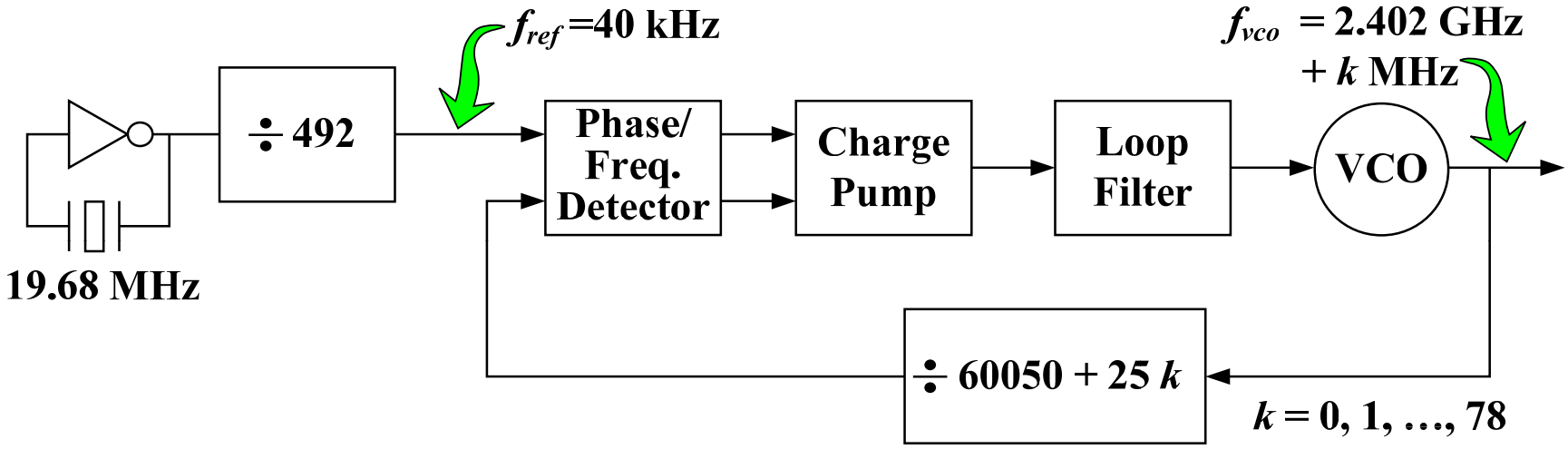
$\Rightarrow$ lower bandwidth (slower settling)

$\Rightarrow$ larger VCO noise contribution

$\Rightarrow$ larger in-band divider, reference, and charge pump noise contributions

Integer-*N* PLL Limitations

Example: Bluetooth channel frequencies from a 19.68 MHz crystal



Problem: Must design loop bandwidth to be less than 4 kHz!

⇒ Can't meet the 200 μs settling requirement

⇒ Can't meet the Bluetooth phase noise requirements

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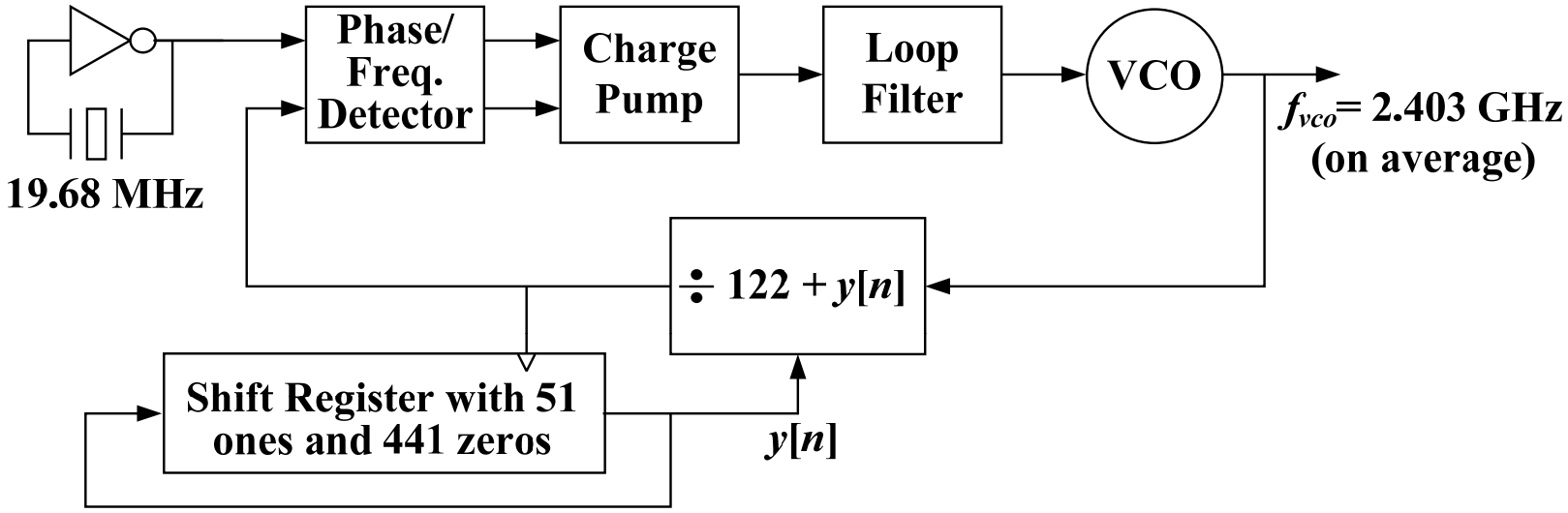
A Bad Fractional-*N* PLL

Example Revisited ($k = 1$ case):



Idea: Periodically switch divider modulus between 122 and 123 so the *average modulus* is 122 + 51/492

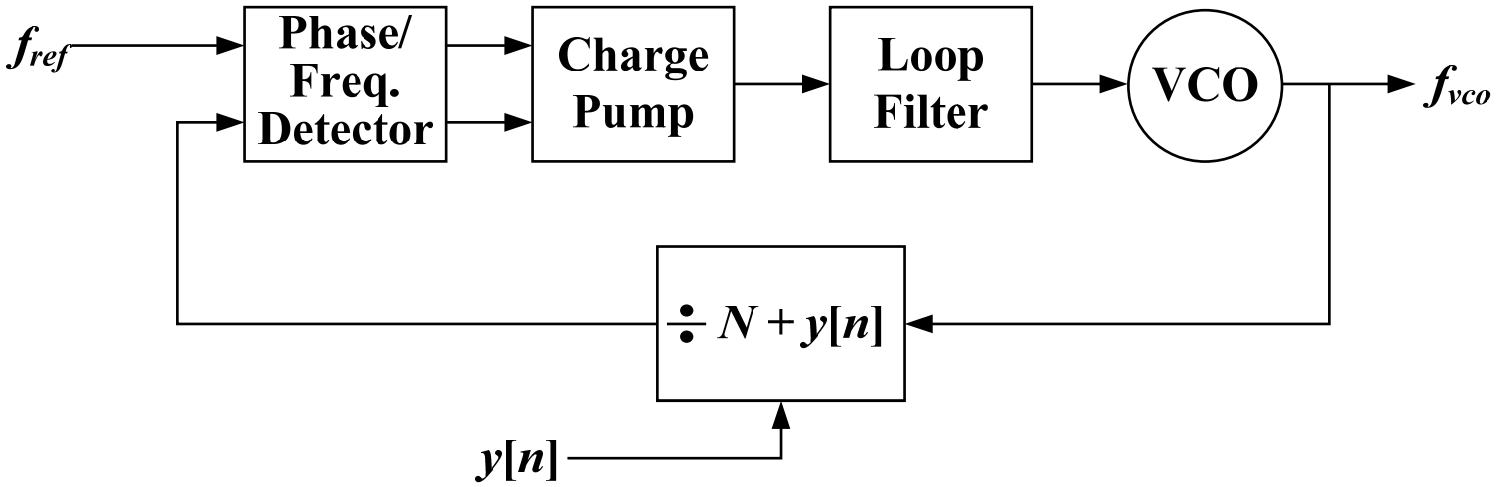
⇒ Have desired VCO frequency (at least on average)

⇒ Loop bandwidth can be up to almost 2 MHz

⇒ Periodic switching causes large spurious tones at multiples of 40 kHz

⇒ At low frequencies the tones see little loop suppression

Observations From These Fractional-*N* PLLs



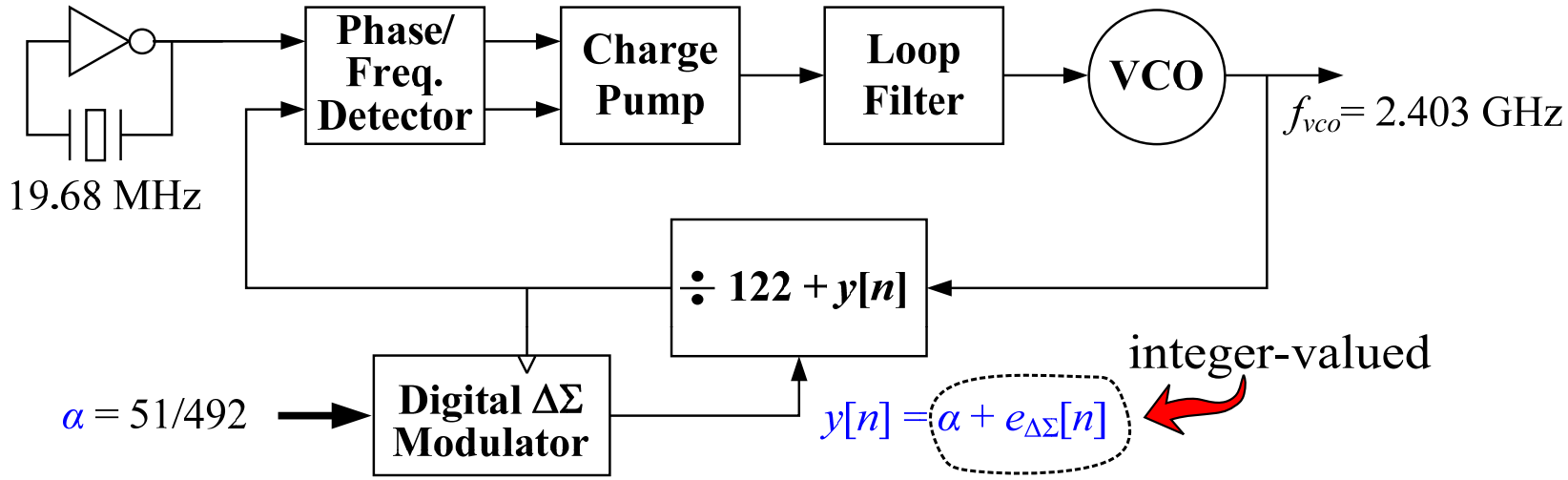
- $y[n]$ must be integer-valued with a sample-rate of f_{ref}
- The PLL lowpass filters $y[n]$ measured at the VCO input, so

$$f_{VCO} = (N + \text{lowpass filtered version of } y[n]) \cdot f_{ref}$$

Conclusion: Would like $(y[n] - 51/492)$ to be zero-mean with most of its power outside the PLL's bandwidth

A Good Fractional-*N* PLL[2-4]

Example Revisited ($k = 1$ case):



Idea: Use a *digital* ΔΣ *modulator* to quantize α such that the *quantization noise* is zero-mean and has most of its power outside the PLL bandwidth. Then

$$f_{VCO} = (122 + \alpha) \cdot f_{ref}$$

⇒ Have precise frequency control without excessive phase noise

⇒ Can also modulate VCO by changing α each reference period

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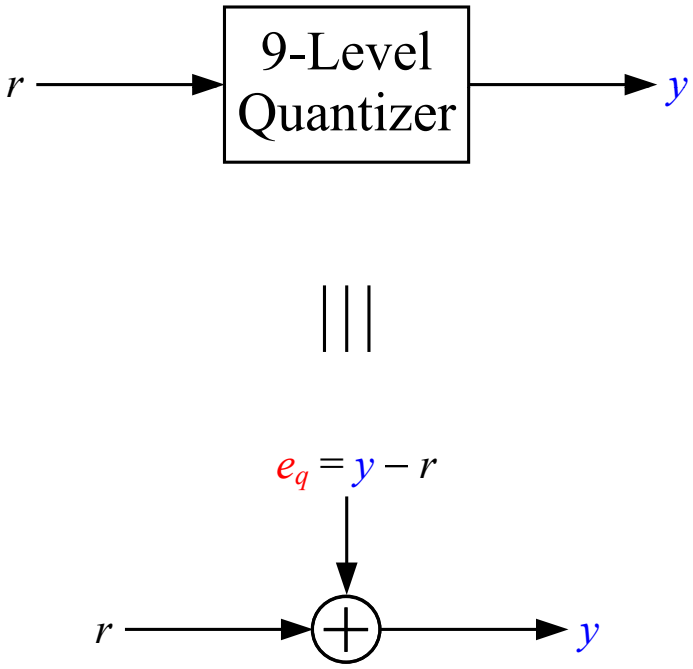
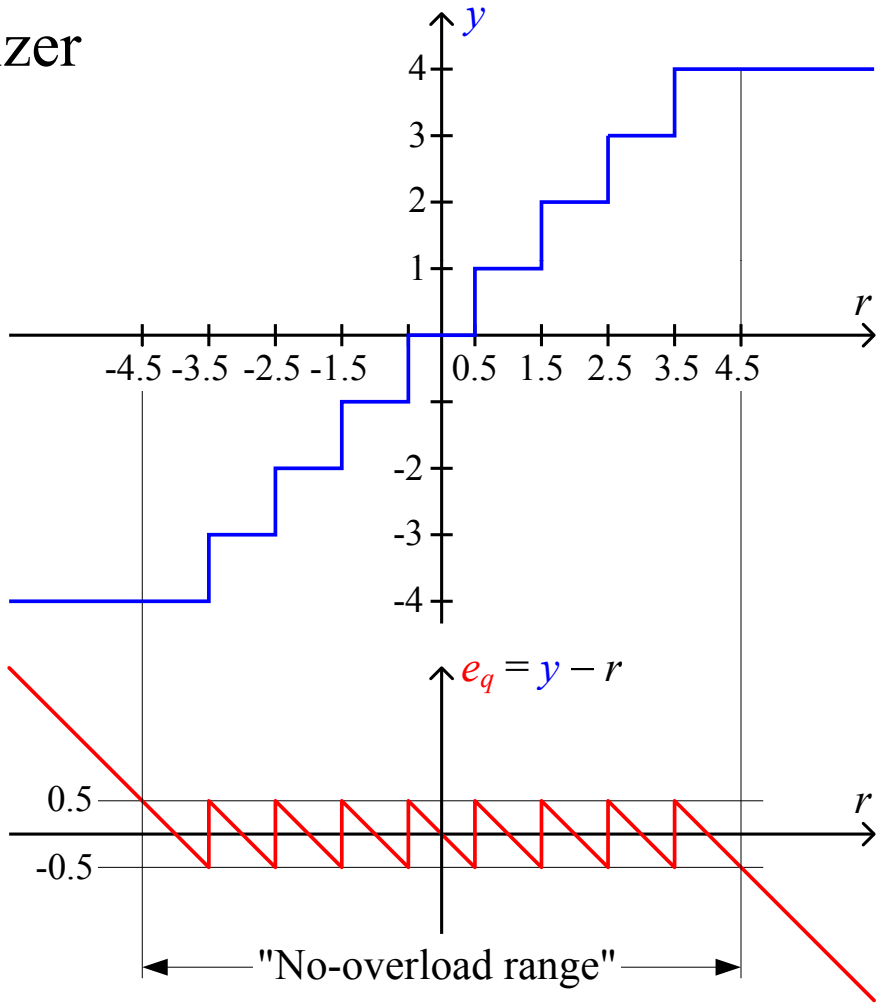
Quantizer Example

There are many types of ΔΣ modulators, but most involve feedback around uniform quantizers.

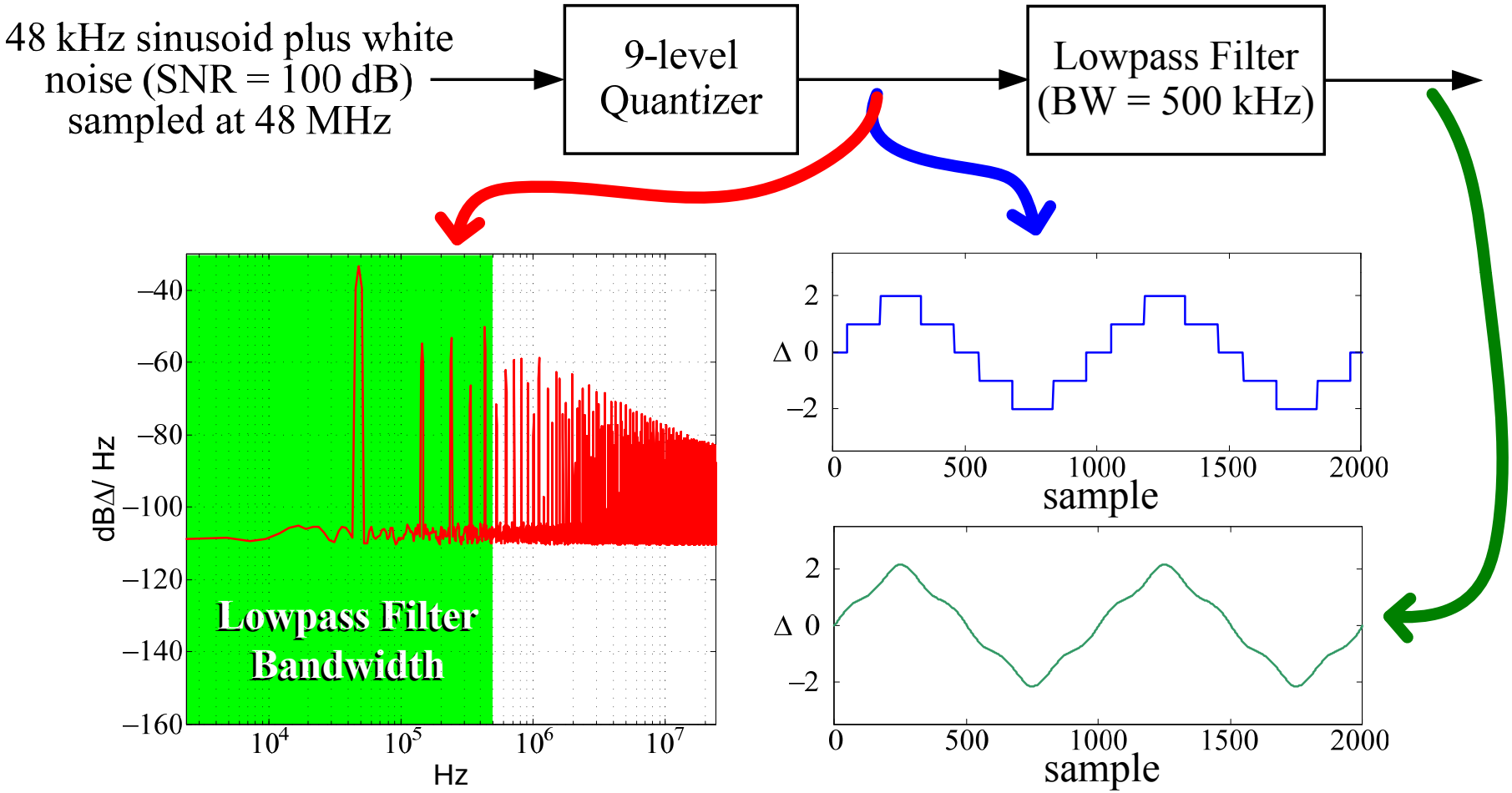
Example: a 9-level uniform quantizer





Quantizer Example

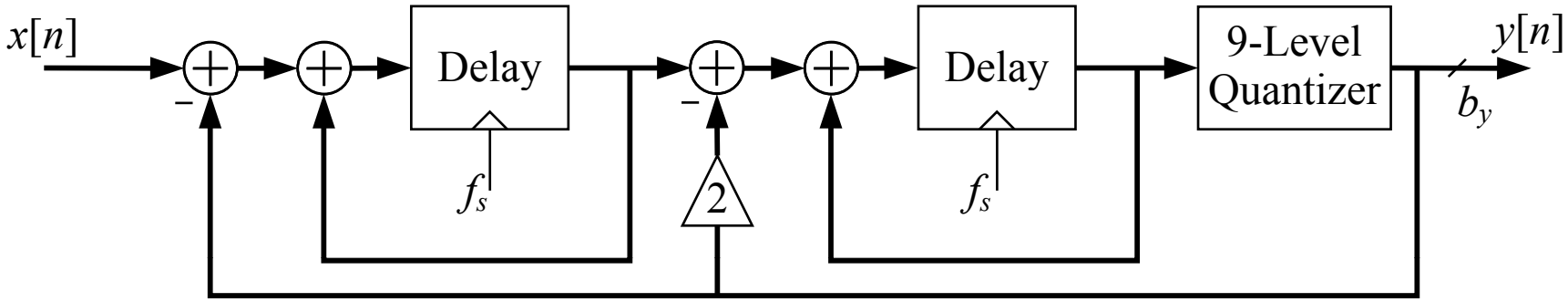
Such quantizers alone do not have well-behaved quantization noise:



In the 0-500 kHz band, the SNDR is only 14 dB

ΔΣ Modulator Example[5]

A *second-order* ΔΣ *modulator* using the same 9-level uniform quantizer:



Can show:

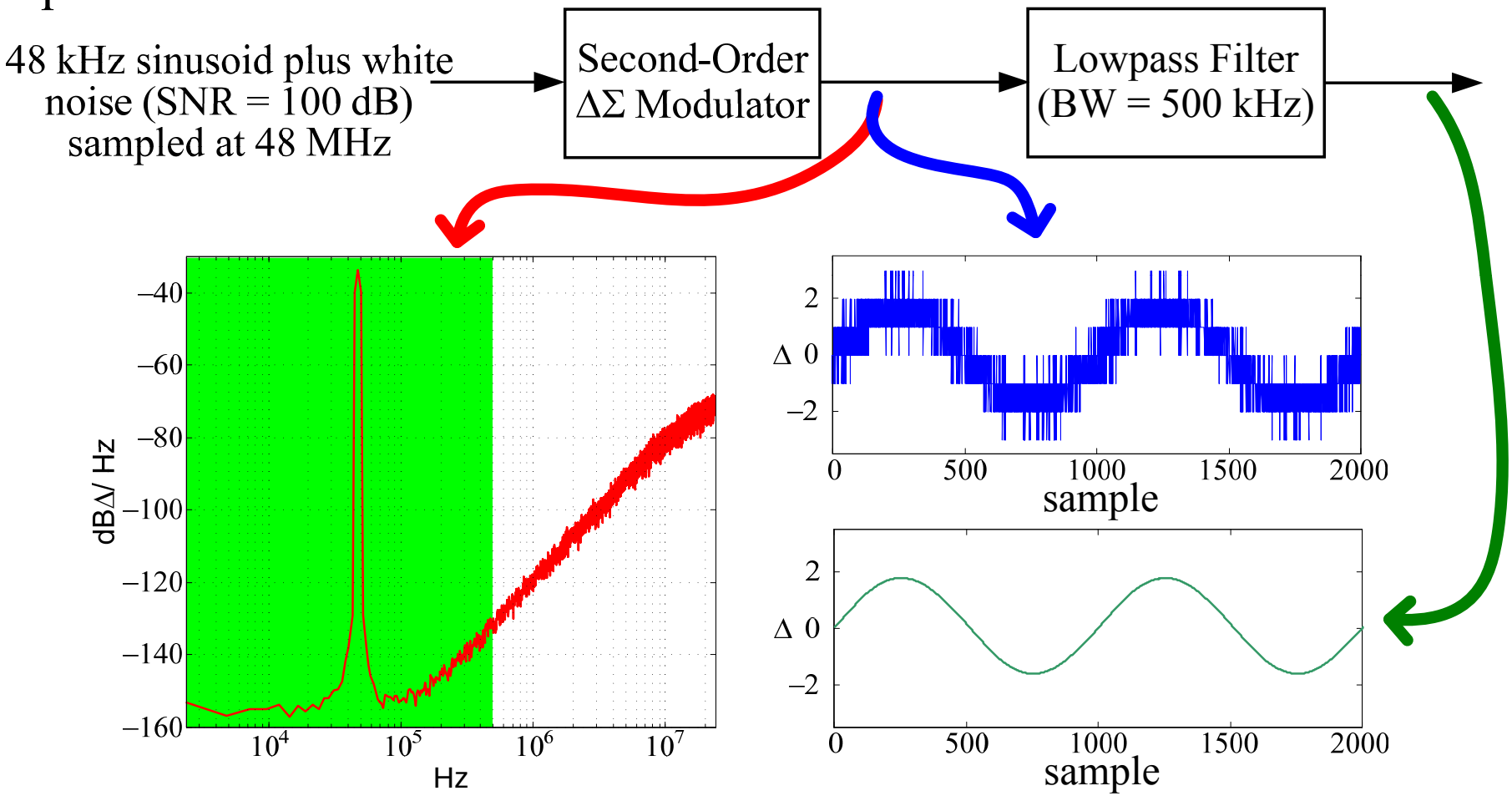
$$y[n] = x[n-2] + \underbrace{e_q[n] - 2e_q[n-1] + e_q[n-2]}_{\Delta\Sigma \text{ Modulator Quantization Noise (call it } e_{\Delta\Sigma}[n])}$$

Idea: The quantization noise, $e_q[n]$, is subjected to two zero-frequency zeros whereas the signal is just delayed

$\Rightarrow$ Quantization noise power is mostly at high frequencies

ΔΣ Modulator Example

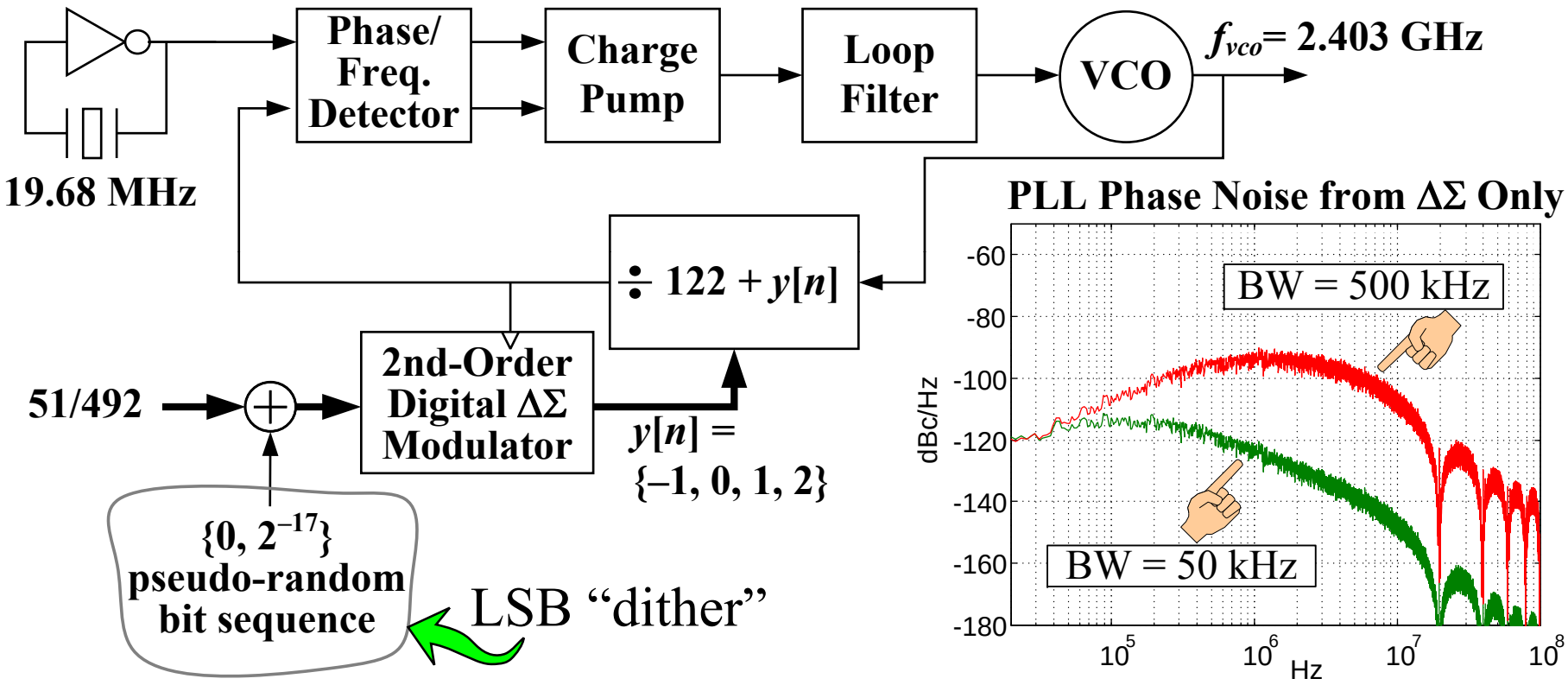
Unlike the quantizer alone, the ΔΣ modulator has well-behaved quantization noise:



In the 0-500 kHz band, the SNDR is 84 dB with no spurious tones!

The ΔΣ Modulator Example in a Fractional-*N* PLL

Example 1 Revisited (*k* = 1 case):



PLL phase noise from the ΔΣ modulator meets the Bluetooth local oscillator requirements for the 50 (but not 500) kHz BW case

ΔΣ Modulator Limitations

- The ΔΣ quantization noise must go somewhere—ideally, above the PLL bandwidth (up to $f_{ref}/2$)

  $\Rightarrow$ Phase noise spec places limit on PLL bandwidth

- Increasing the ΔΣ modulator order[6] puts more of the quantization noise above the PLL bandwidth, but the PLL has limited filtering capabilities

  $\Rightarrow$ Higher than 3rd-order ΔΣ modulation rarely used

- Must use dither, e.g., 1-bit pseudo-random LSB dither[7-8], to eliminate spurious tones in $y[n]$

- ΔΣ modulators with 1-bit quantization are rarely used because they require $\max\{x[n]\} - \min\{x[n]\} < 1$ which limits the achievable output frequencies, and dithering does not eliminate spurious tones

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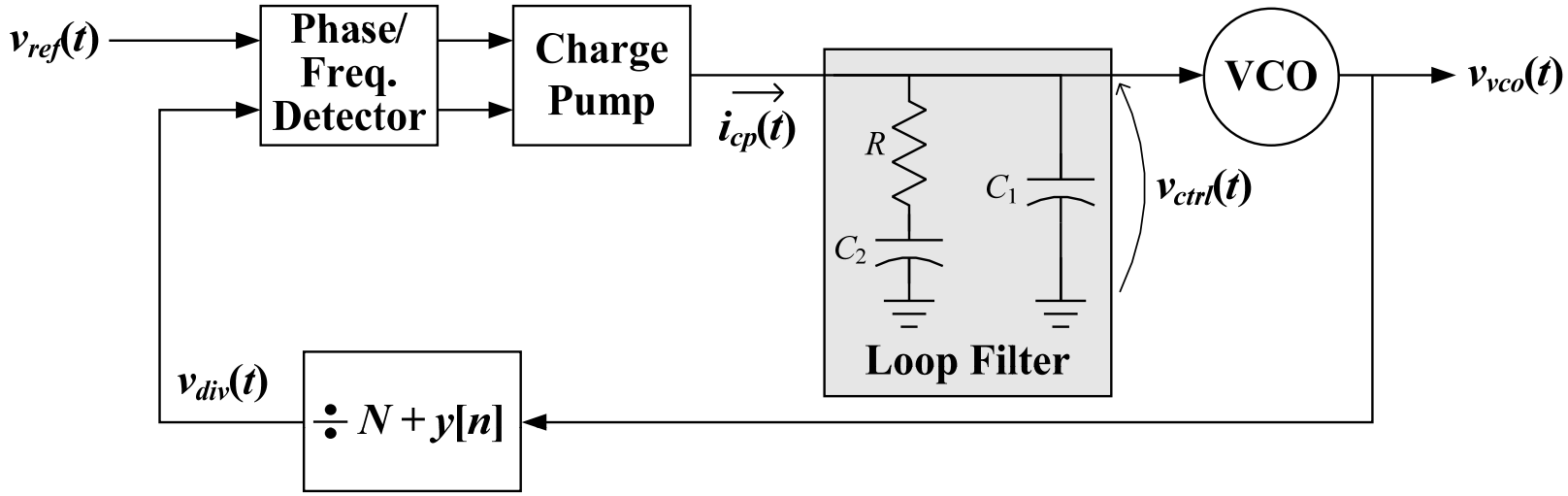
Contributors to the PLL's Phase Noise



The PLL's phase noise, $\theta_{PLL}(t)$, depends on:

$\theta_{ref}(t)$ = reference oscillator phase noise,

$\theta_{VCO}(t)$ = VCO phase noise,

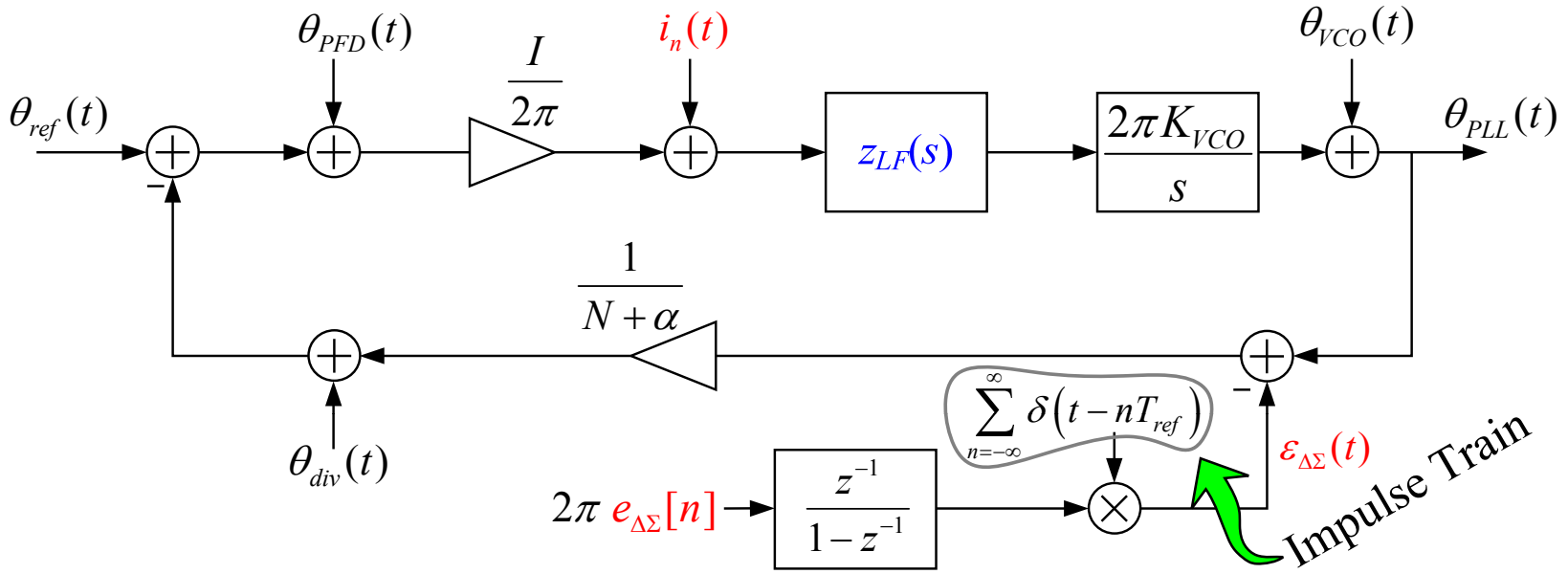
$\theta_{div}(t)$ = divider phase noise,

$\theta_{PFD}(t)$ = PFD phase noise,

$i_n(t)$ = charge pump and loop filter noise (referred to the loop filter input), and

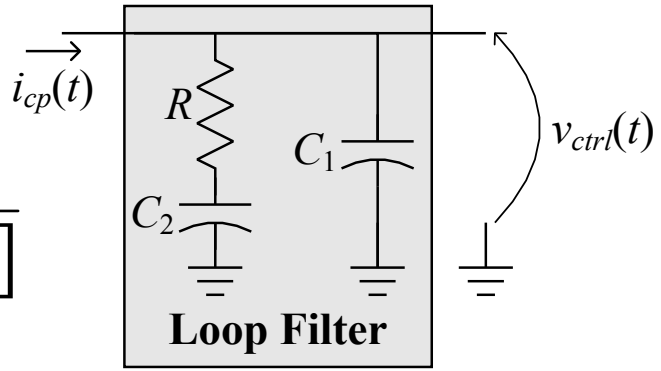
$e_{\Delta\Sigma}[n]$ = $\Delta\Sigma$ modulator quantization noise (Slide 12)

"Linearized" Fractional-*N* PLL Model[9]



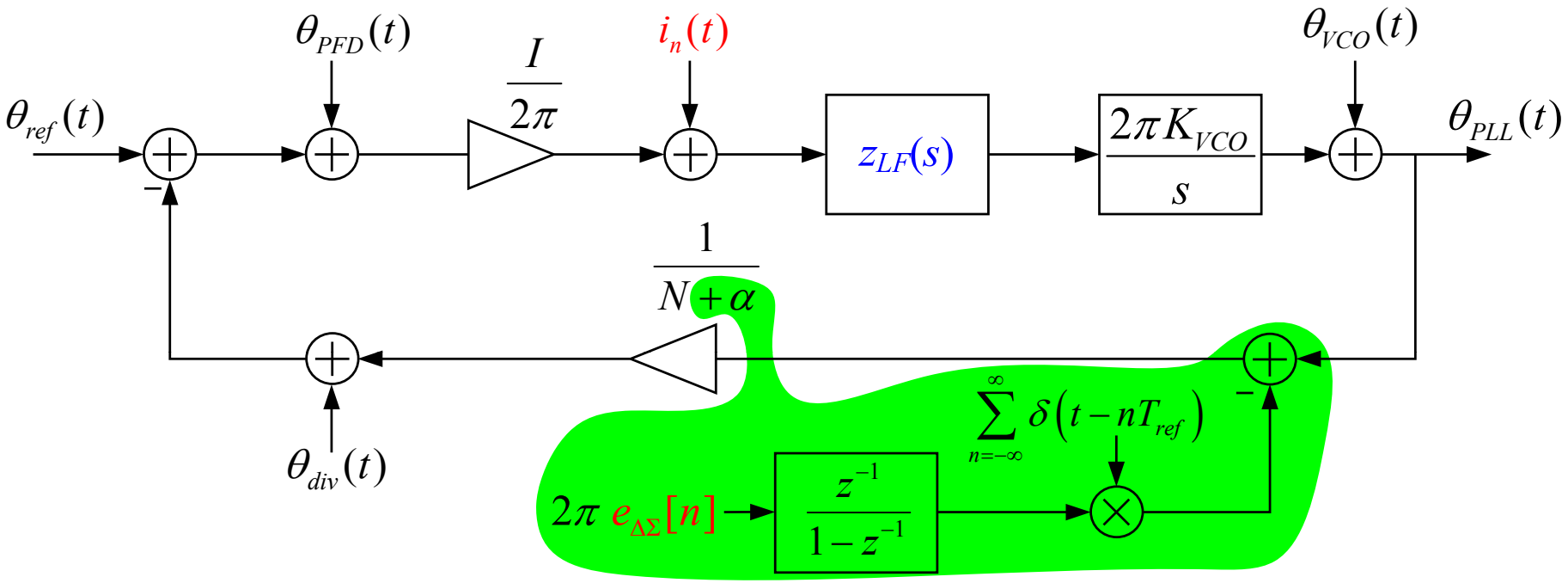
where $z_{LF}(s) \equiv \dfrac{v_{ctrl}(s)}{i_{cp}(s)}$

$$= \frac{1}{C_1 + C_2} \frac{1 + sRC_2}{s\left[1 + sRC_1C_2/(C_1 + C_2)\right]}$$



and K_{VCO} = VCO gain (Hz/V)

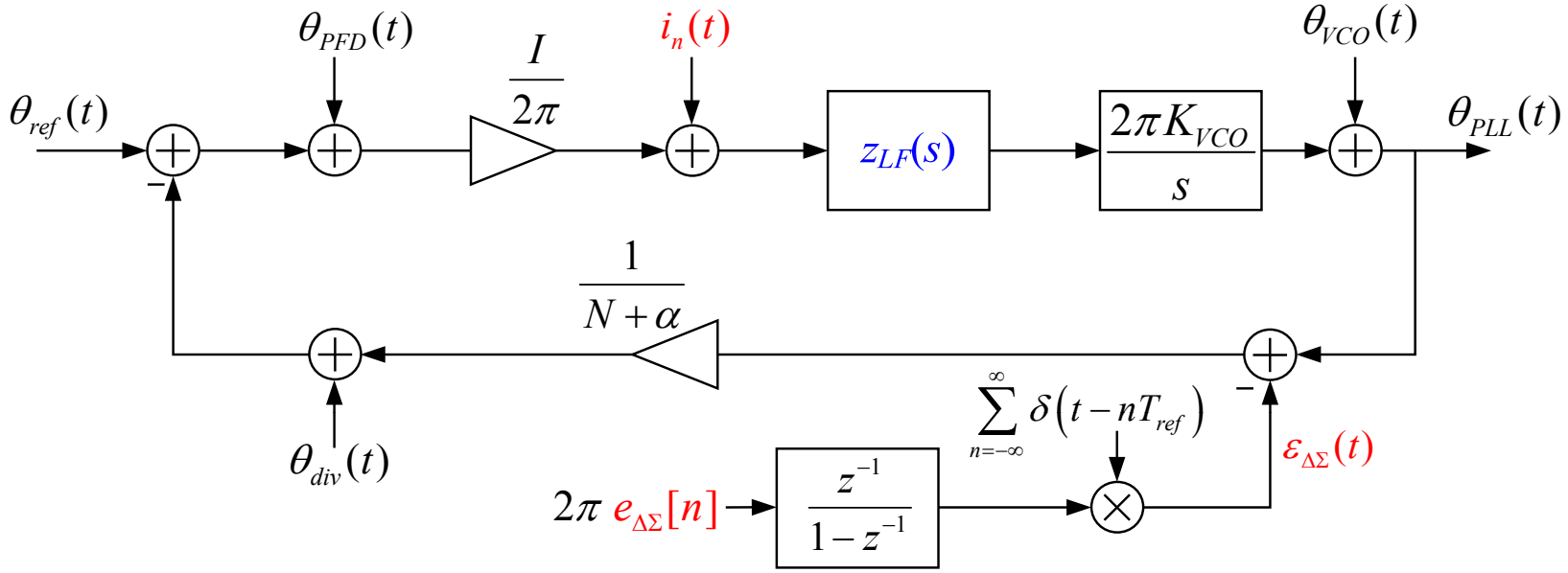
Fractional-*N* and Integer-*N* PLL Model Differences



Shaded region is the only difference between fractional-*N* and integer-*N* PLL linearized models

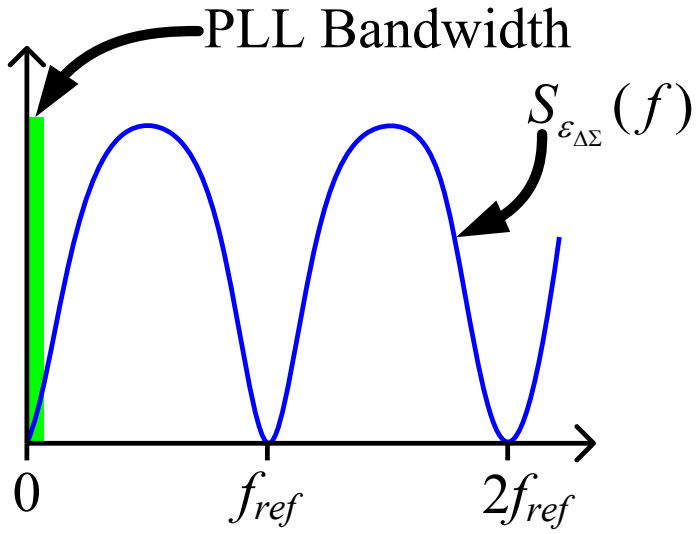
Usually, $N >> \alpha$, so fractional-*N* PLLs have the same loop equations and noise transfer functions (except for ΔΣ quantization noise) as integer-*N* PLLs

ΔΣ Modulator Quantization Noise Path

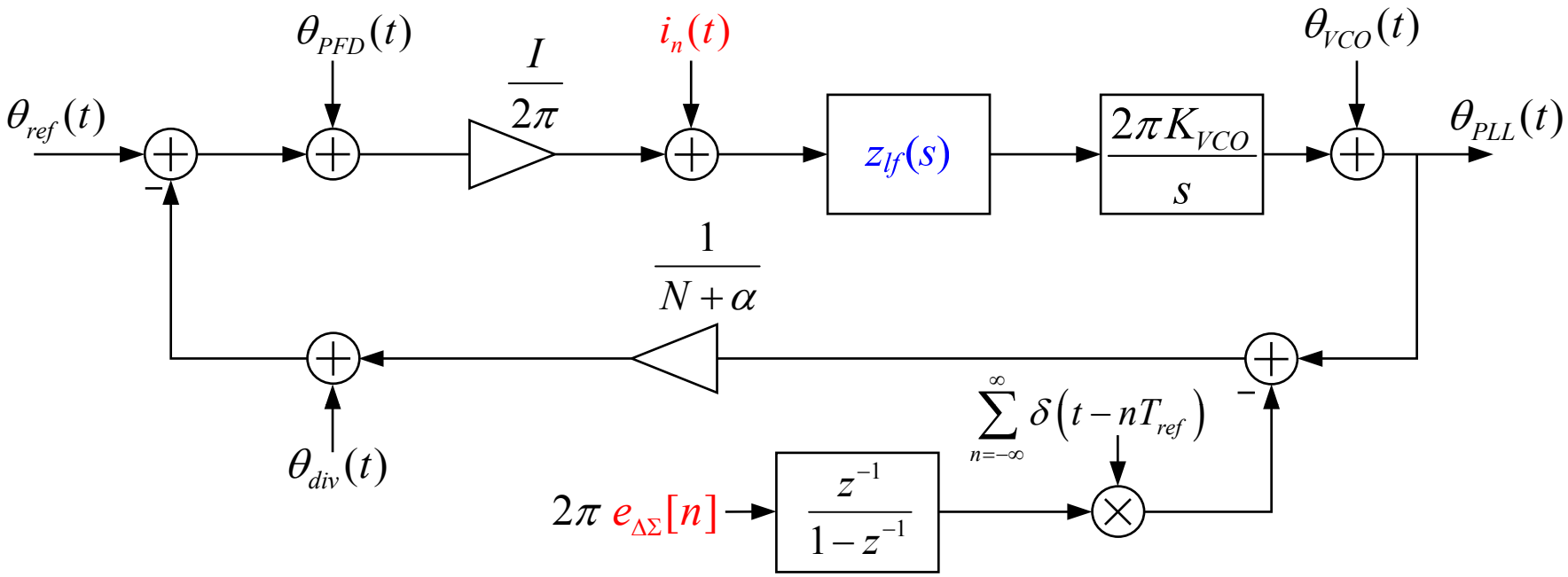


The PSD of $\varepsilon_{\Delta\Sigma}(t)$ for an L^{th}-order ΔΣ modulator:

$$S_{\varepsilon_{\Delta\Sigma}}(f)=\frac{\pi^2}{12 f_{ref}}\left[2\cdot\sin\left(\frac{\pi f}{f_{ref}}\right)\right]^{2(L-1)}$$



A Secondary Effect of the ΔΣ Modulator



Fractional-N PLL charge pump pulses are wider than integer-N charge pump pulses by $\left|\frac{1}{f_{VCO}}\sum_{k=0}^{n-1} e_{\Delta\Sigma}[k]\right|$

which has a variance of $1/(6f_{VCO}^2)$ or $1/(2f_{VCO}^2)$ for a ΔΣ modulator order of 2 or 3, respectively

$\Rightarrow$ This increases the effect of charge pump noise on $\theta_{PLL}(t)$

Fractional-N PLL Design Example

Local oscillator PLL for a direct conversion Bluetooth receiver:

Requirements:

- Crystal frequency: 19.68 MHz (other crystals are easier)
- PLL output frequencies: $f_{VCO} = 2.402\ \text{GHz} + k\ \text{MHz}$, $k = 0, \ldots, 78$
- Loop bandwidth: $f_{BW} > 40\ \text{kHz}$
- Phase margin: $\text{PM} > 60°$
- Total PLL phase noise: $\leq -120\ \text{dBc/Hz}$ at $\geq 3\ \text{MHz}$ from f_{VCO}

Assume:

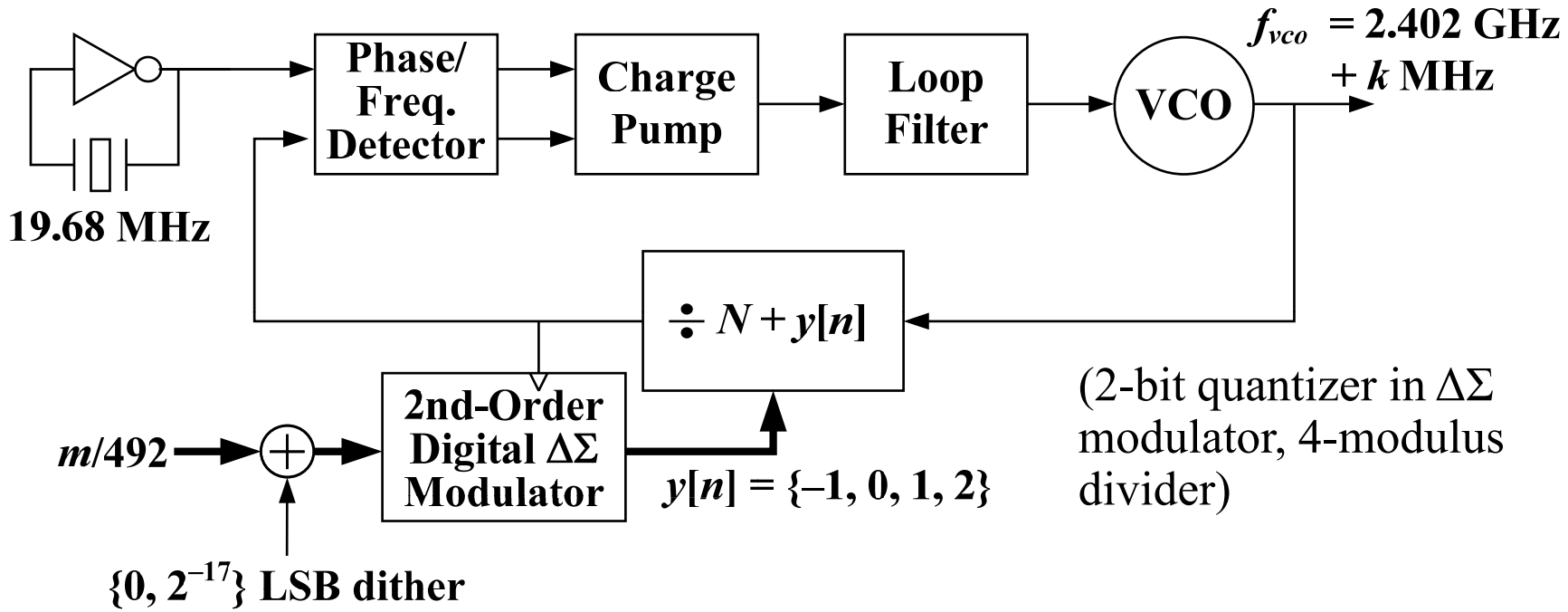
Reference source, VCO, divider, PFD and charge pump have been designed and meet noise specifications provided the ΔΣ modulator and loop filter each contribute $\leq -130\ \text{dBc/Hz}$ at 3 MHz from f_{VCO}

Design Tasks:

- Choose ΔΣ modulator and frequency plan
- Choose loop filter component values

Fractional-*N* PLL Design Example

Assume a 2nd-order ΔΣ modulator is sufficient (will verify later):



Frequency Plan:

- To get $k = 0, 1, \ldots,$ or 18: set $N = 122$, $m = k \cdot 25 + 26$
- To get $k = 19, 21, \ldots,$ or 38: set $N = 123$, $m = (k - 19) \cdot 25 + 9$
- To get $k = 39, 41, \ldots,$ or 57: set $N = 124$, $m = (k - 39) \cdot 25 + 17$
- To get $k = 58, 60, \ldots,$ or 78: set $N = 125$, $m = (k - 58) \cdot 25$

Fractional-*N* PLL Design Example

Relevant loop equations: (derived from linearized model[16])

$$PM = \tan^{-1}\left(\frac{b-1}{2\sqrt{b}}\right), \qquad \text{where } b = \frac{C_2}{C_1} + 1$$

$$f_{BW} = \frac{IK_{VCO}R}{2\pi N} \cdot \frac{b-1}{b}$$

$$RC_2 = \frac{\sqrt{b}}{2\pi f_{BW}}$$

$$S_{\theta_{PLL}}(f)\Big|_{\Delta\Sigma \text{ only}} \cong 10 \cdot \log\left\{\frac{4\pi^2 b}{3f_{ref}}\left[\sin^2\left(\frac{\pi f}{f_{ref}}\right)\right]\left(\frac{f_{BW}}{f}\right)^4\right\} \quad \text{dBc/Hz,}$$

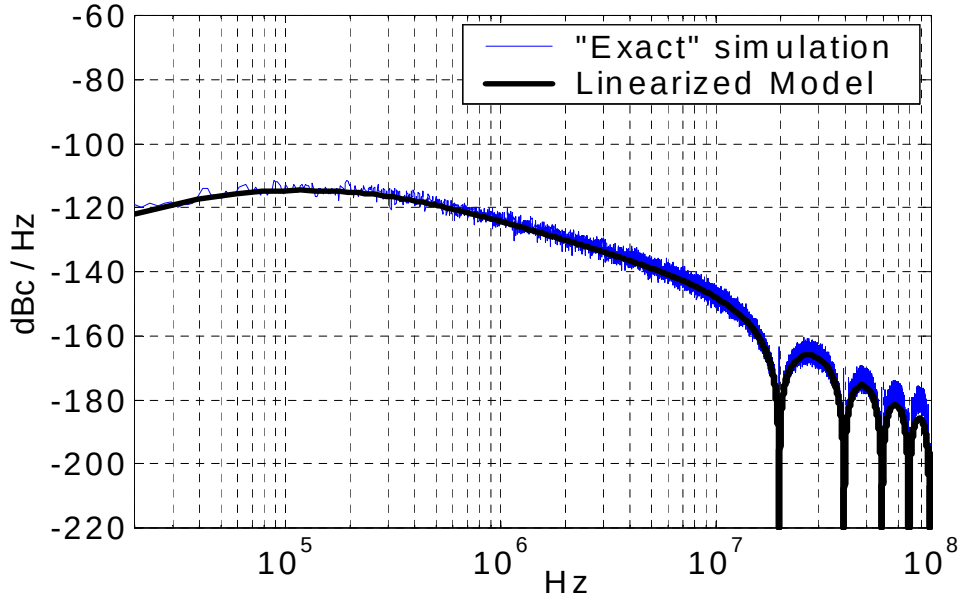
$$\left(\text{valid for } f > \frac{C_1 + C_2}{2\pi R C_1 C_2}\right)$$

Fractional-*N* PLL Design Example

Calculations: (for $K_{VCO} = 200$ MHz/V, $I = 200$ μA)

1) Choose $b = 15$ in PM equation to get $PM = 62^0$
2) Solve $S_{\theta_{PLL}}(3 \cdot 10^6 \text{ Hz})\big|_{\Delta\Sigma \text{ only}} = -130$ dBc/Hz to get $f_{BW} = 44$ kHz
3) Use the f_{BW} equation to get $R = 915\ \Omega$
4) Use the RC_2 and b equations to get $C_2 = 15.3$ nF and $C_1 = 1.1$ nF

Phase Noise:



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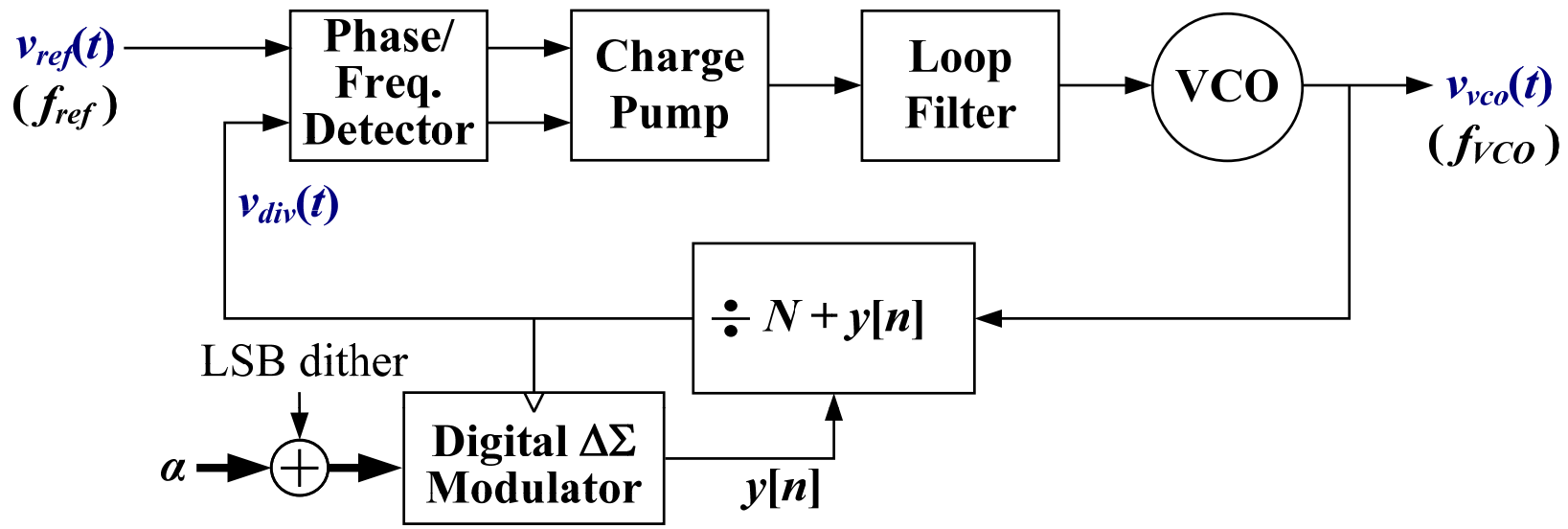
Reference Spurs and Fractional Spurs

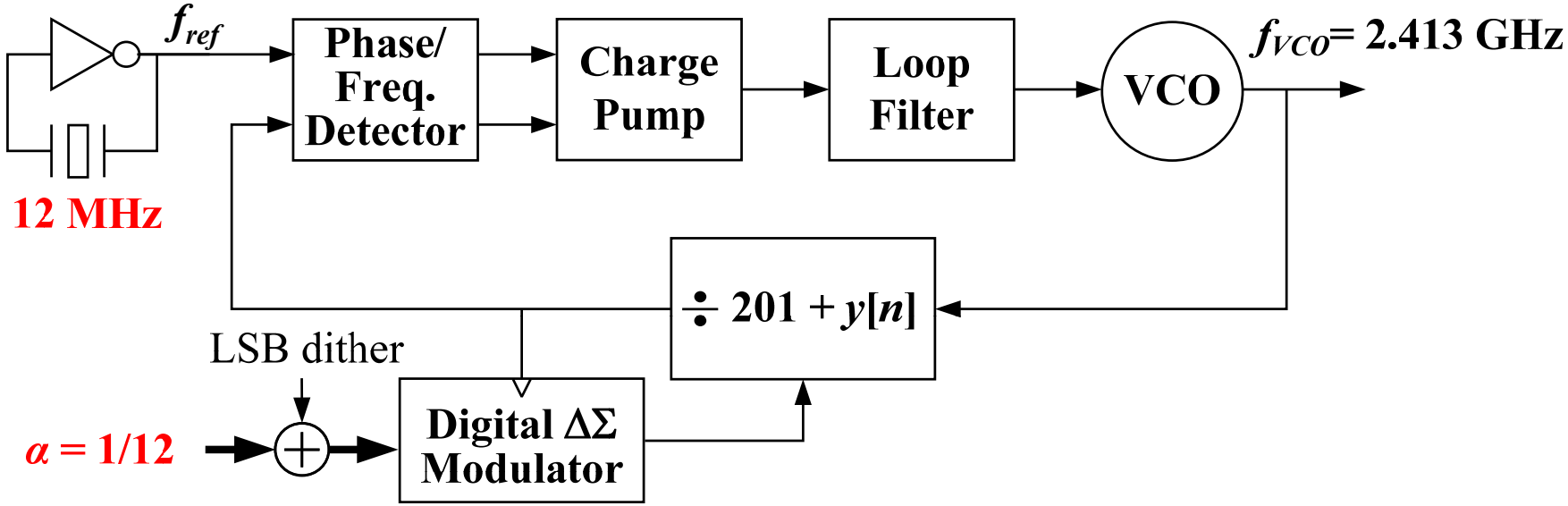


PLL phase noise always contains spurious tones ("spurs"):

- Have reference spurs at multiples of f_{ref} (like integer-N PLLs)
- Have fractional spurs at multiples of αf_{ref} modulo f_{ref}

Fractional Spur Overview

Example



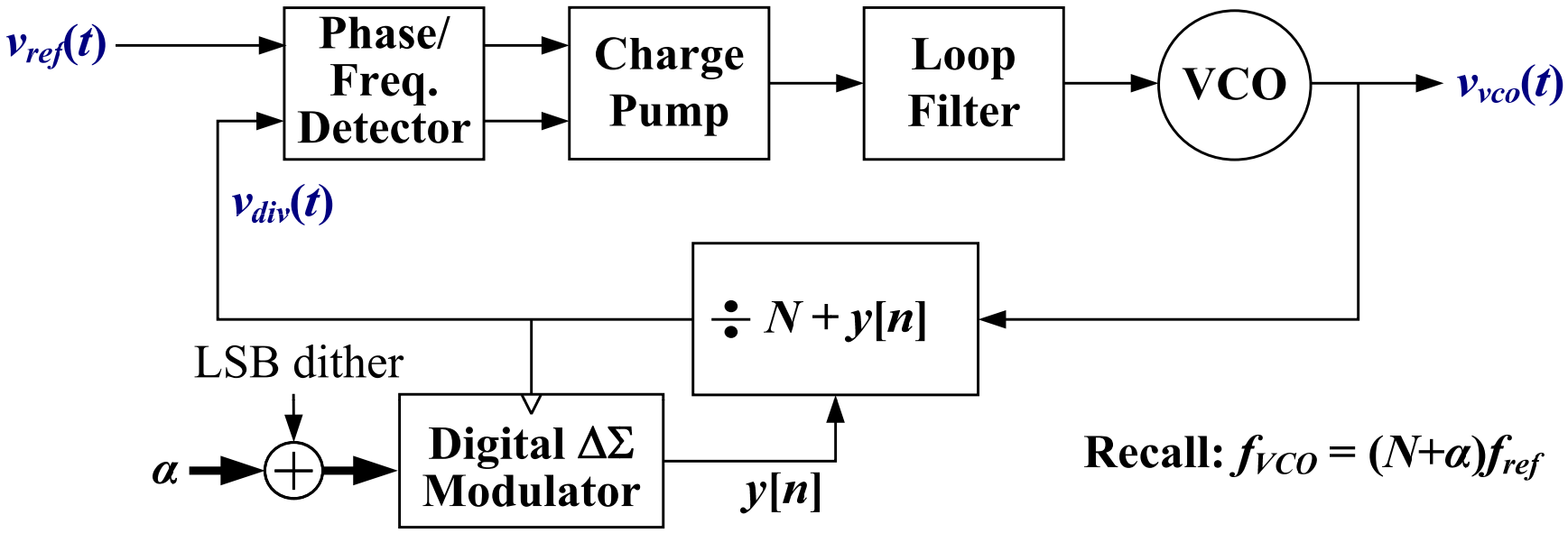
$\Rightarrow$ fractional spurs at multiples of αf_{ref} = 1 MHz

In general, a PLL lowpass filters most fractional spurs

- Effective only for spurs above PLL bandwidth
- Spurs within PLL bandwidth are unfiltered (typ. > −60dBc)

$\Rightarrow$ design restrictions on α, f_{ref}, and the PLL bandwidth

Overview of Fractional Spur Mechanisms



Mechanism 1:

Nonlinear coupling of $v_{ref}(t)$ and $v_{vco}(t)$ (or $v_{div}(t)$)
e.g., [Nth harmonic in $v_{ref}(t)$]×$v_{vco}(t) \Rightarrow \alpha f_{ref}$ spur

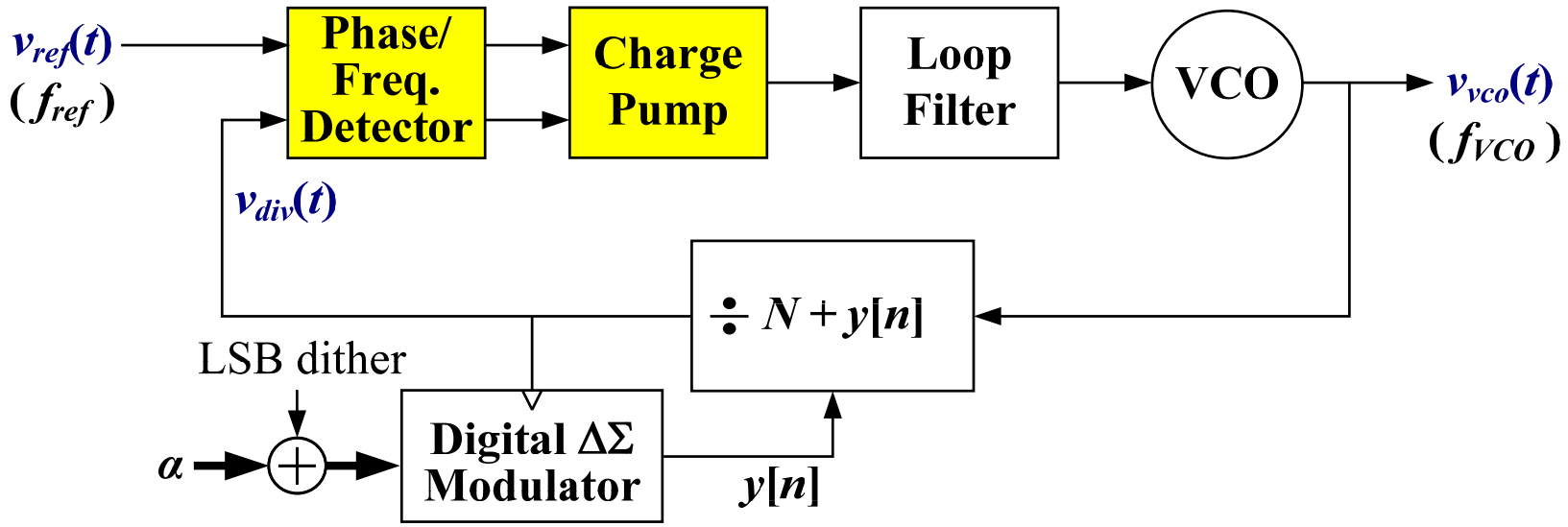
Mechanism 2:

Nonlinear distortion of ΔΣ quantization noise by non-ideal analog circuits (little known because same spur frequencies as Mechanism 1)

Fractional Spur Mechanism 1

- Parasitic coupling of $v_{ref}(t)$ and $v_{vco}(t)$ (or $v_{div}(t)$) cause *fractional spurs*

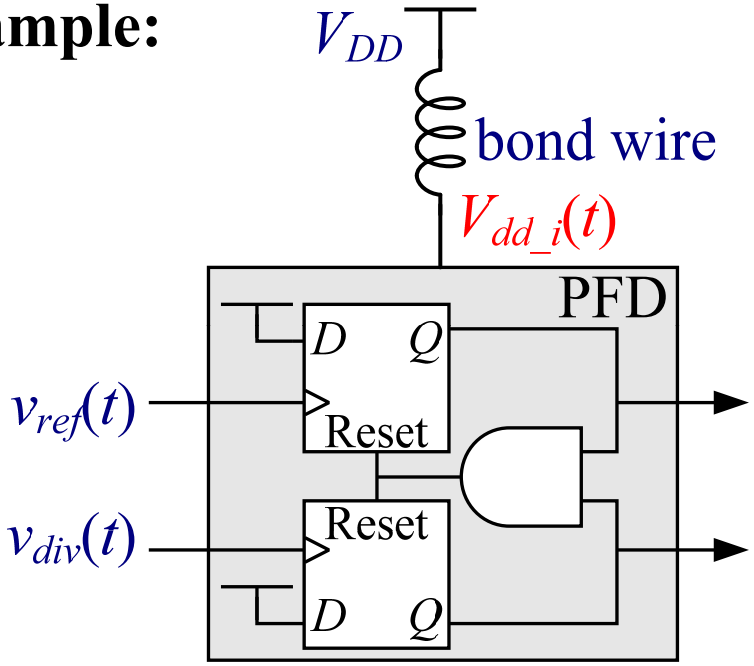
- The greatest opportunities for such coupling occur in the PFD and CP because they process signals aligned to $v_{ref}(t)$ and $v_{div}(t)$:

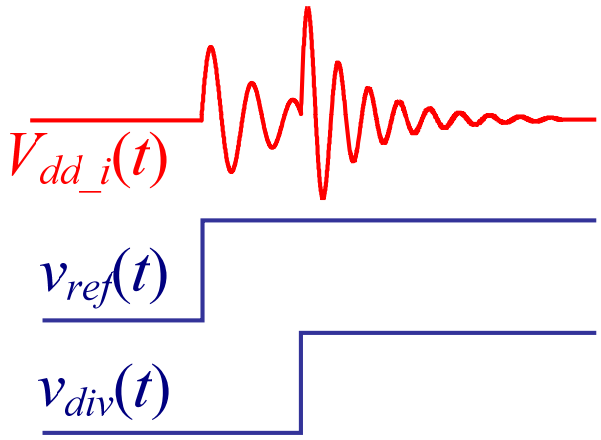


Fractional Spur Mechanism 1

Power supplies to the PFD and CP are the main coupling paths

Example:

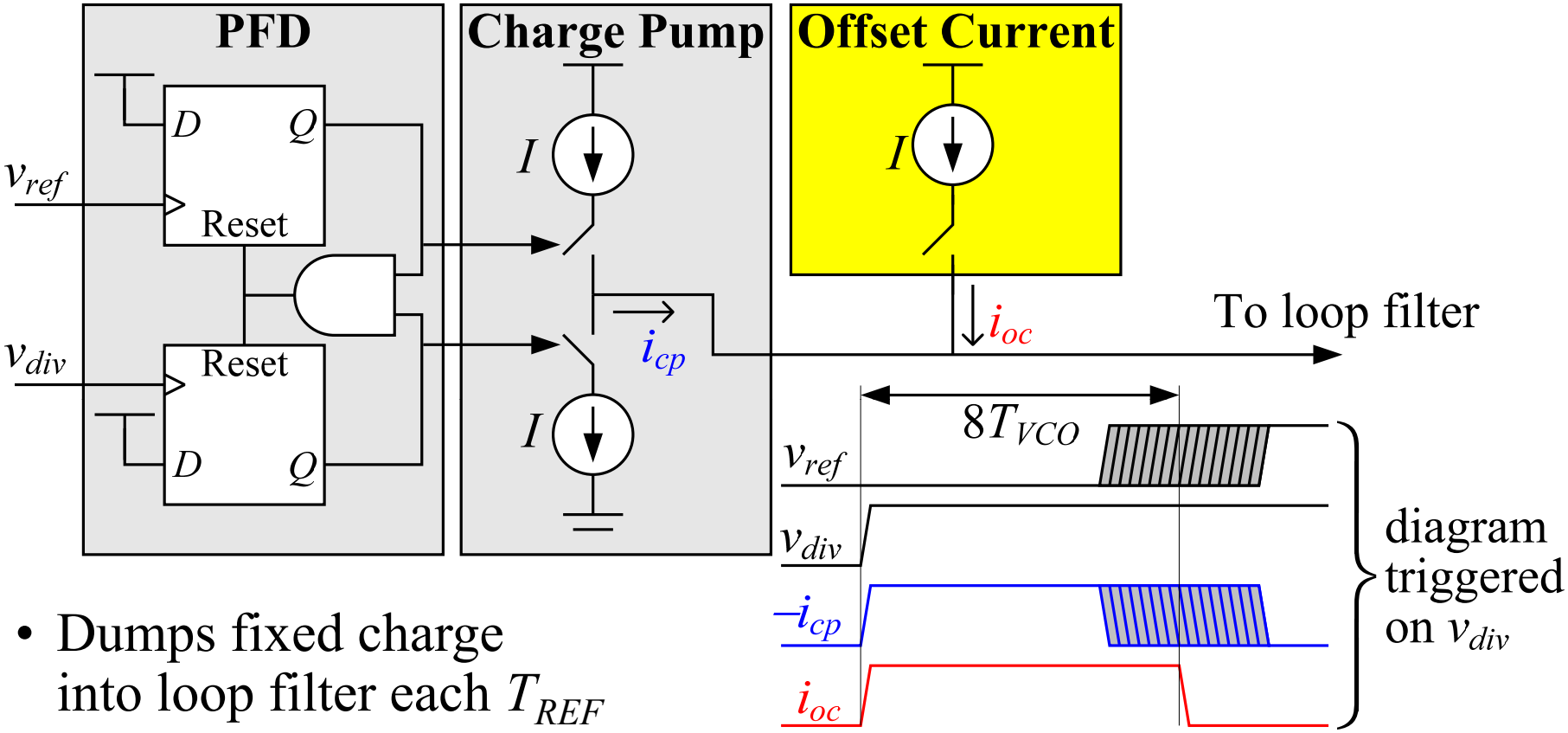




- The $v_{ref}(t)$ edge causes ringing through the V_{DD} bond wire
- If ringing persists to the next $v_{div}(t)$ edge, the bottom flip-flop output is affected by $v_{ref}(t)$ as well as $v_{div}(t)$

  $\Rightarrow$ nonlinear coupling of $v_{ref}(t)$ and $v_{div}(t)$

Solution: Offset Current to Separate PFD Edges[13]

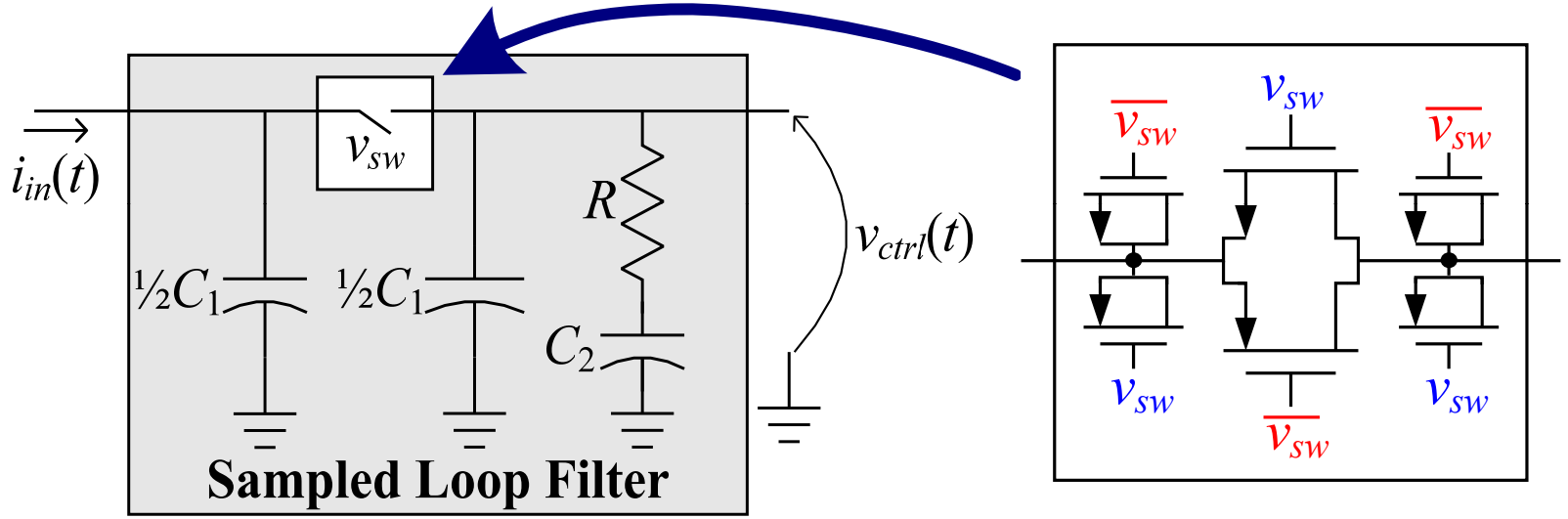


- Dumps fixed charge into loop filter each T_{REF}
- This separates edges of v_{ref} and v_{div}
  $\Rightarrow V_{DD}$ ringing has time to die out
- Similar to method presented in [10]
- But current source mismatches cause big reference spur!

A Simple Method to Reduce the Reference Spur

Can use a sampled loop filter to reduce the reference spur (and improve ΔΣ noise cancellation – details later)[11-14]

Example:[13]



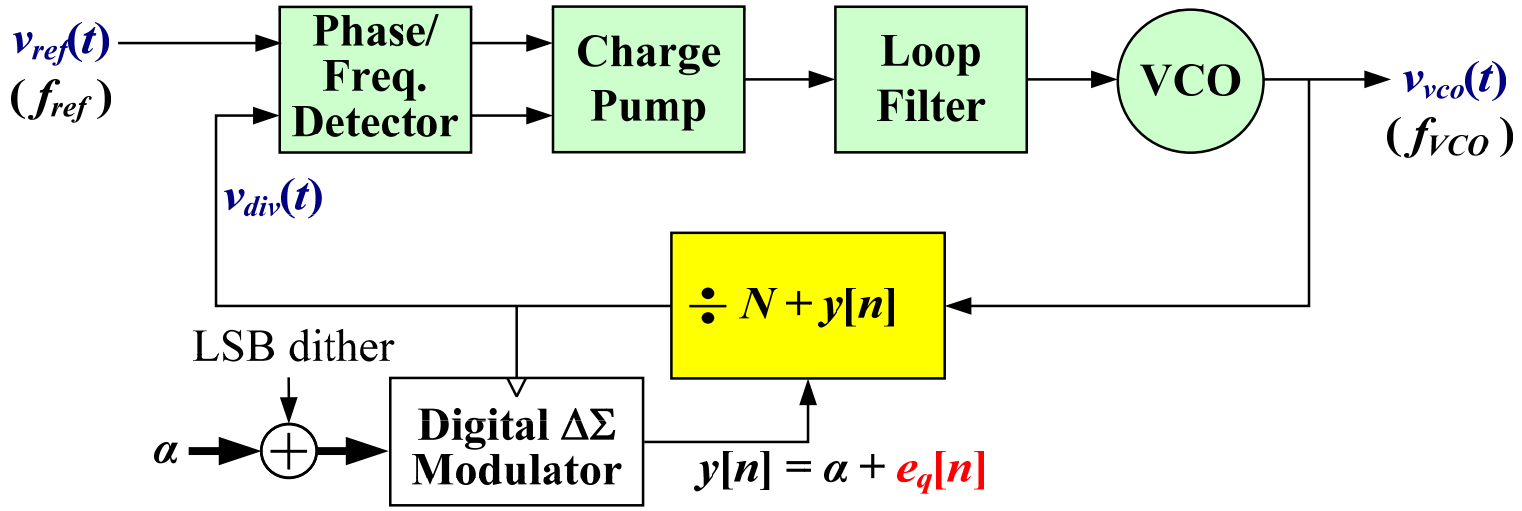
- Switch is open only when $i_{in} \neq 0$ (e.g., 25 ns per reference period)
  $\Rightarrow$ no reference spur from current source mismatches
- Charge injection is impulsive so it sees $R \approx$ open circuit and is well-cancelled by the half-size dummy switches

Fractional Spur Mechanism 2

Nonlinearities come from the analog circuits:

- Nonlinearities in the divider operate on $e_q[n]$
- Nonlinearities from other blocks operate on $\sum_{k=0}^{n} e_q[k]$

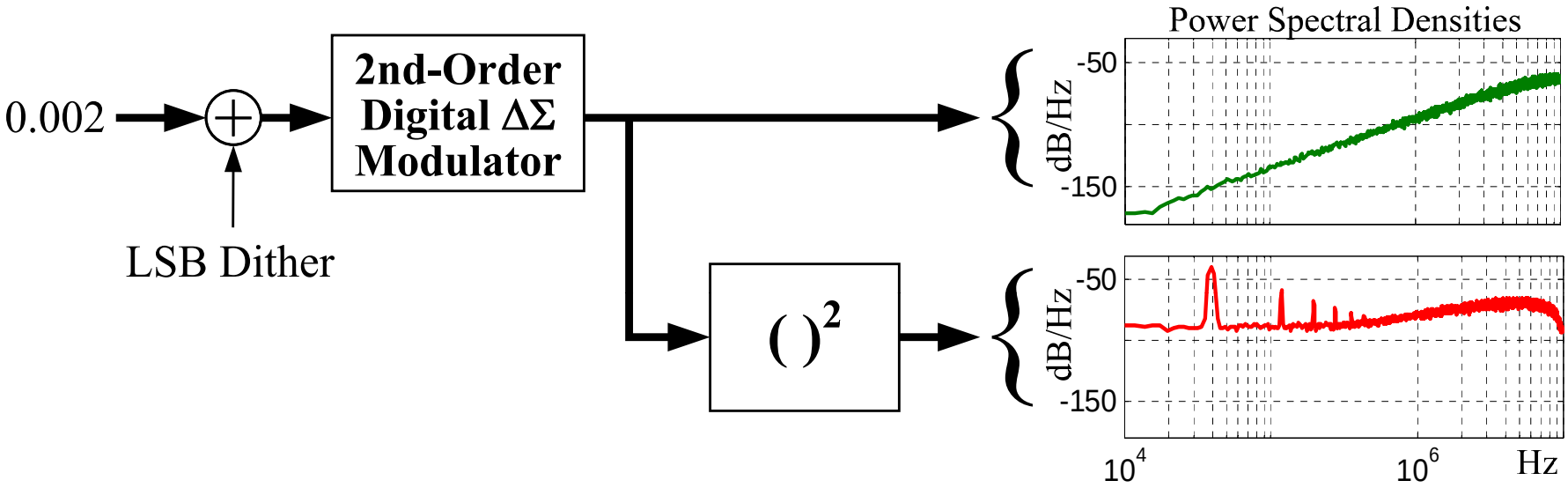
"running sum of $e_q[n]$"



If the nonlinearity applied to $e_q[n]$ or its running sum causes spurs, then the PLL's output signal contains spurs

Fractional Spur Mechanism 2

Example: Effect of second-order distortion:



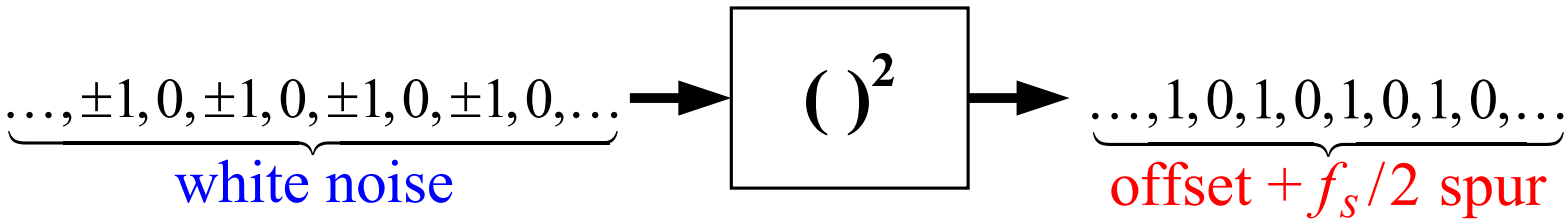
- Similar results occur with other types of non-linear distortion
- Similar results occur regardless of the type of ΔΣ modulator and dither used

⇒ The ΔΣ modulator is the root cause of the problem!

Plausibility Demonstration of Mechanism 2

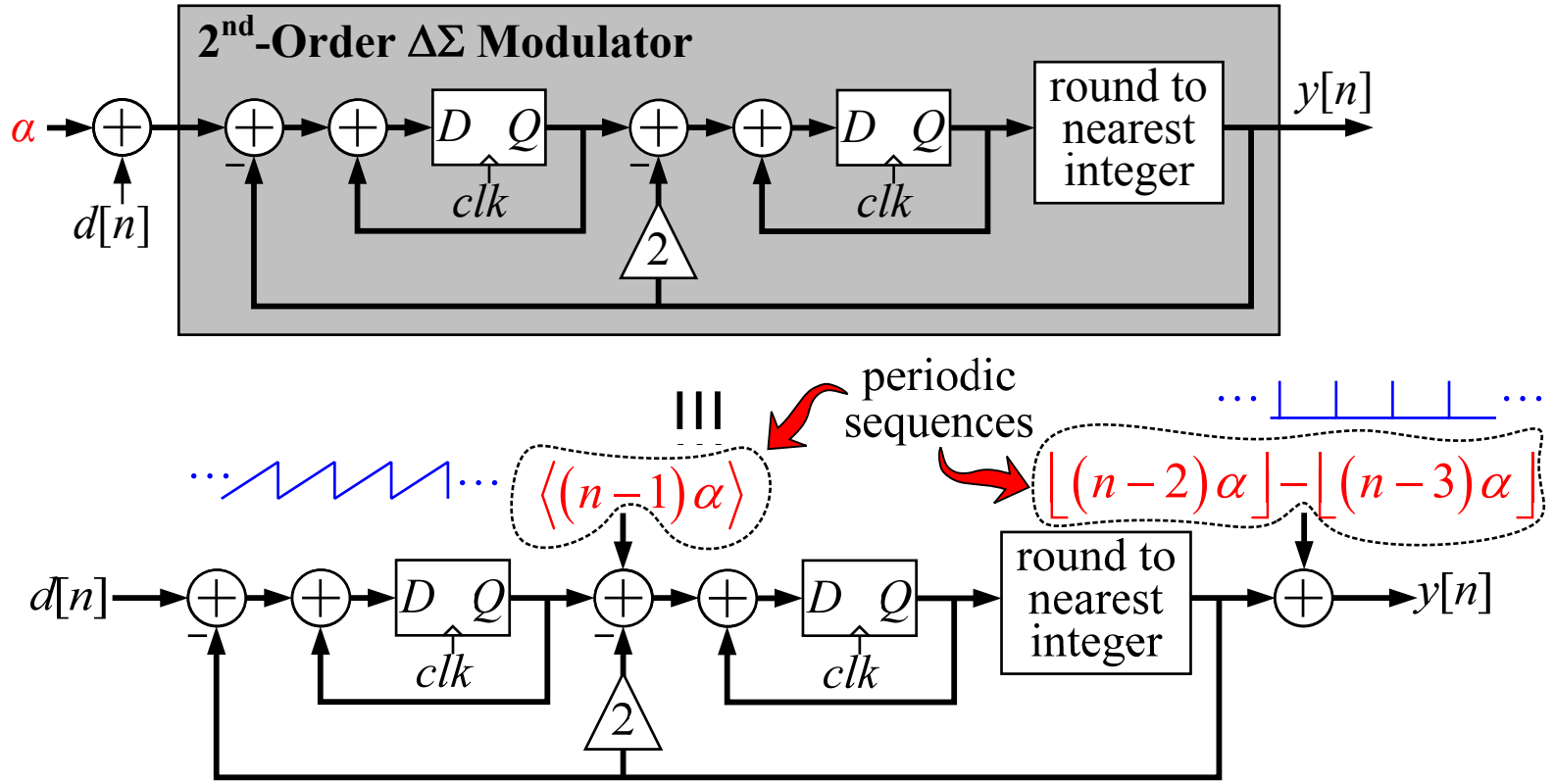
Q: How can nonlinear distortion create spurs from a "spur-free" sequence?

A: The following example gives a simple plausibility demonstration



The randomness is *sufficient* to ensure that the input is spur-free, but it is *insufficient* to ensure that its square is spur-free.

Details of Mechanism 2

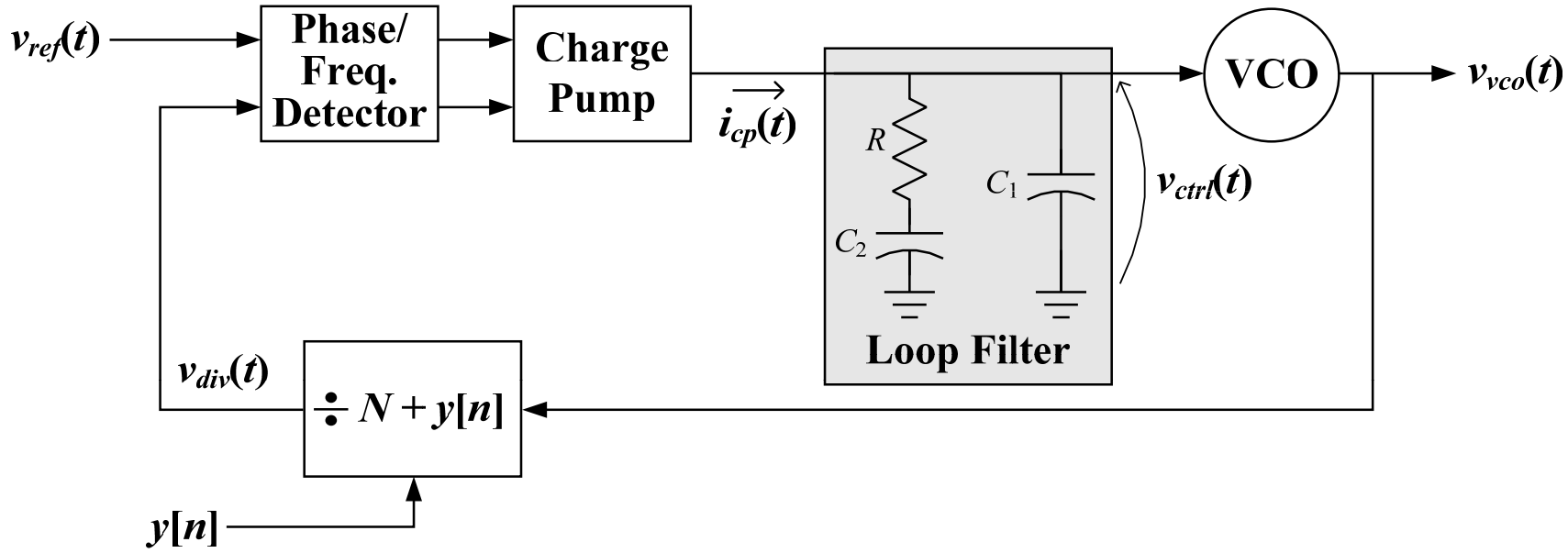


where $\langle x \rangle$ = fractional part of x, and $\lfloor x \rfloor = x - \langle x \rangle$

Each periodic sequence has spurs. Randomness from the dither prevents spurs in $y[n]$, but not in $y^k[n]$ for $k > 1$

$\Rightarrow$ must minimize analog circuit nonlinearity

Nonlinearity: Modulus-Dependent Divider Delays

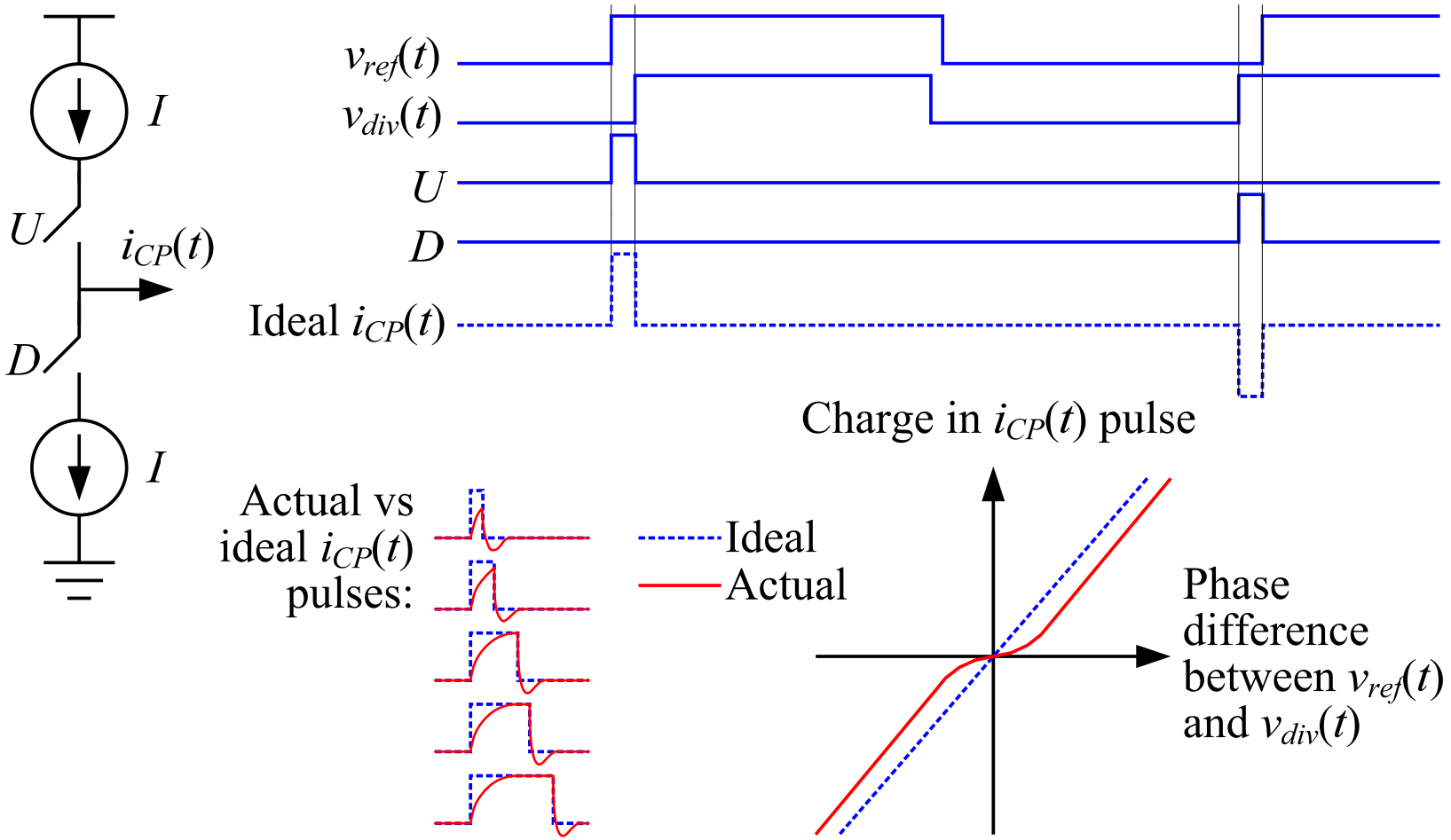


Problem: *Modulus-dependent divider delays*, i.e., error in $v_{div}(t)$ that depends upon $y[n]$, can be a major source of nonlinearity

Solution: Resynchronize divider output to nearest VCO edge or at least a higher-frequency edge within divider [15]

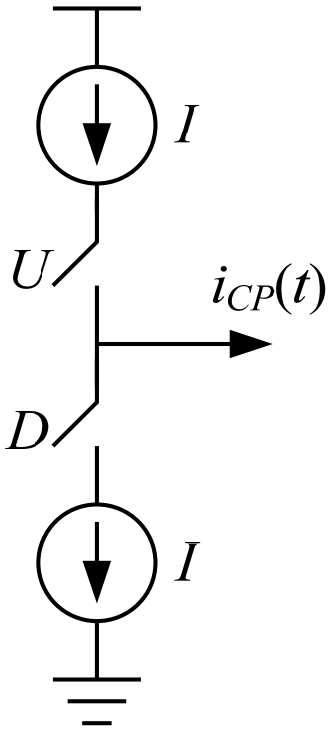
Nonlinearity: Charge Pump Dead Zone

The “obvious” way to control the charge pump leads to a “dead zone” which causes nonlinearity:

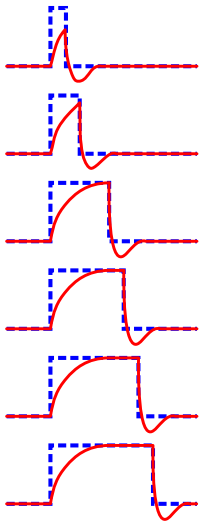


Nonlinearity: Charge Pump Dead Zone

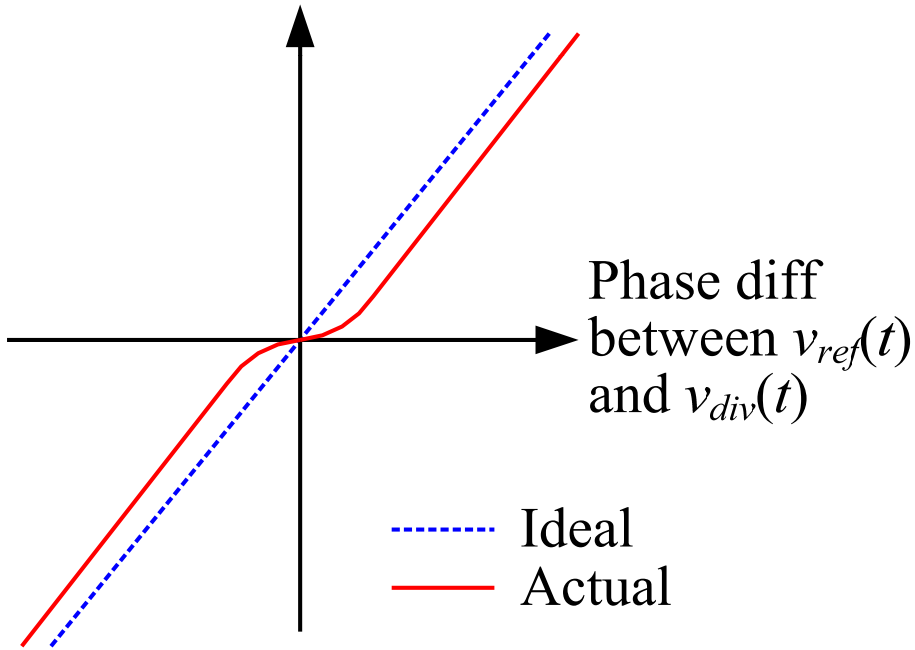
Observation: The charge in the $i_{CP}(t)$ pulse changes linearly with the phase difference between $v_{ref}(t)$ and $v_{div}(t)$ provided the current sources are on long enough to fully settle



Example $i_{CP}(t)$ pulses when $D = 0$

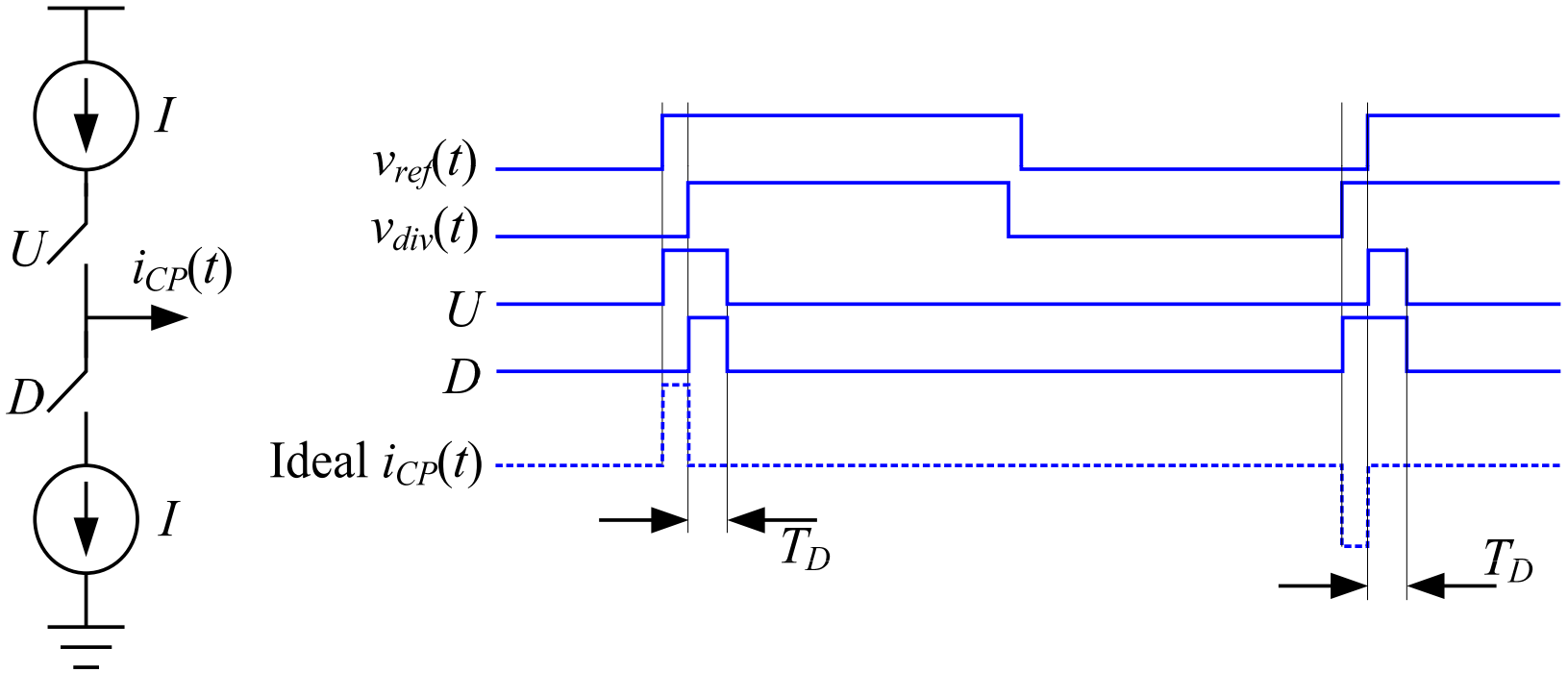


Charge in $i_{CP}(t)$ pulse



Charge Pump Dead Zone Nonlinearity Solution[16]

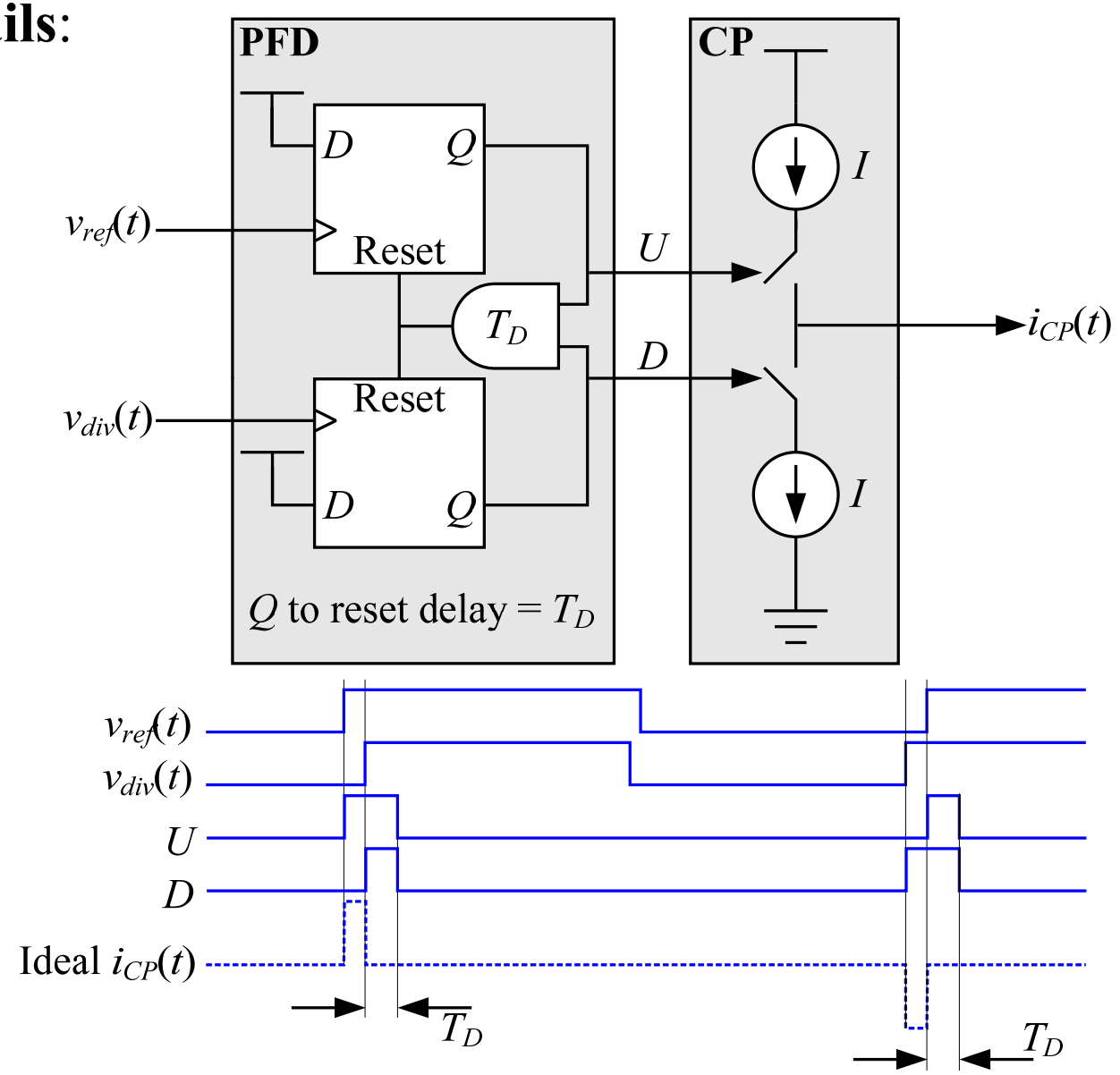
Ideally, $i_{CP}(t) = 0$ when both CP current sources are on, so for each $i_{CP}(t)$ pulse, turn both on long enough to settle (at least T_D), with the $i_{CP}(t)$ pulse formed by their difference:



This eliminates the dead zone, but increases CP noise and mismatches cause a periodic ripple which adds to the reference spur

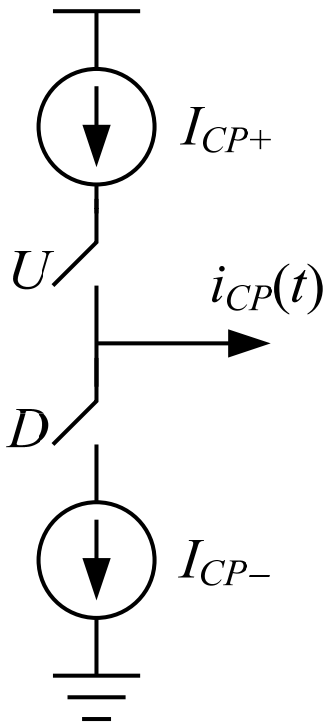
Charge Pump Dead Zone Nonlinearity Solution[16]

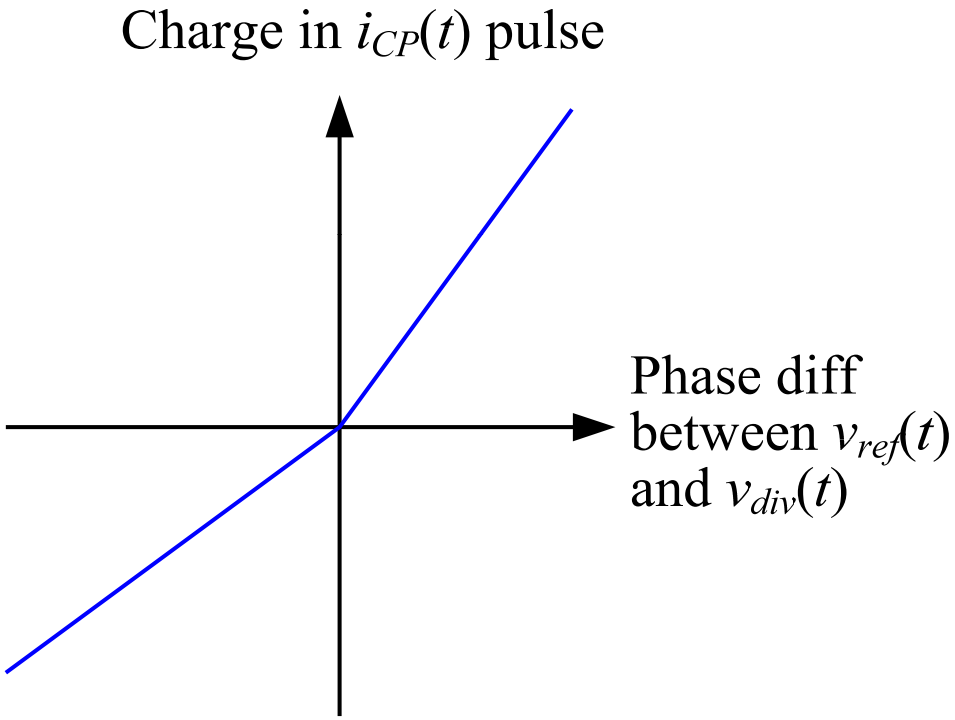
PFD Details:



Nonlinearity: Positive-Negative CP Mismatch

Nonlinearity arises from mismatched positive and negative currents:



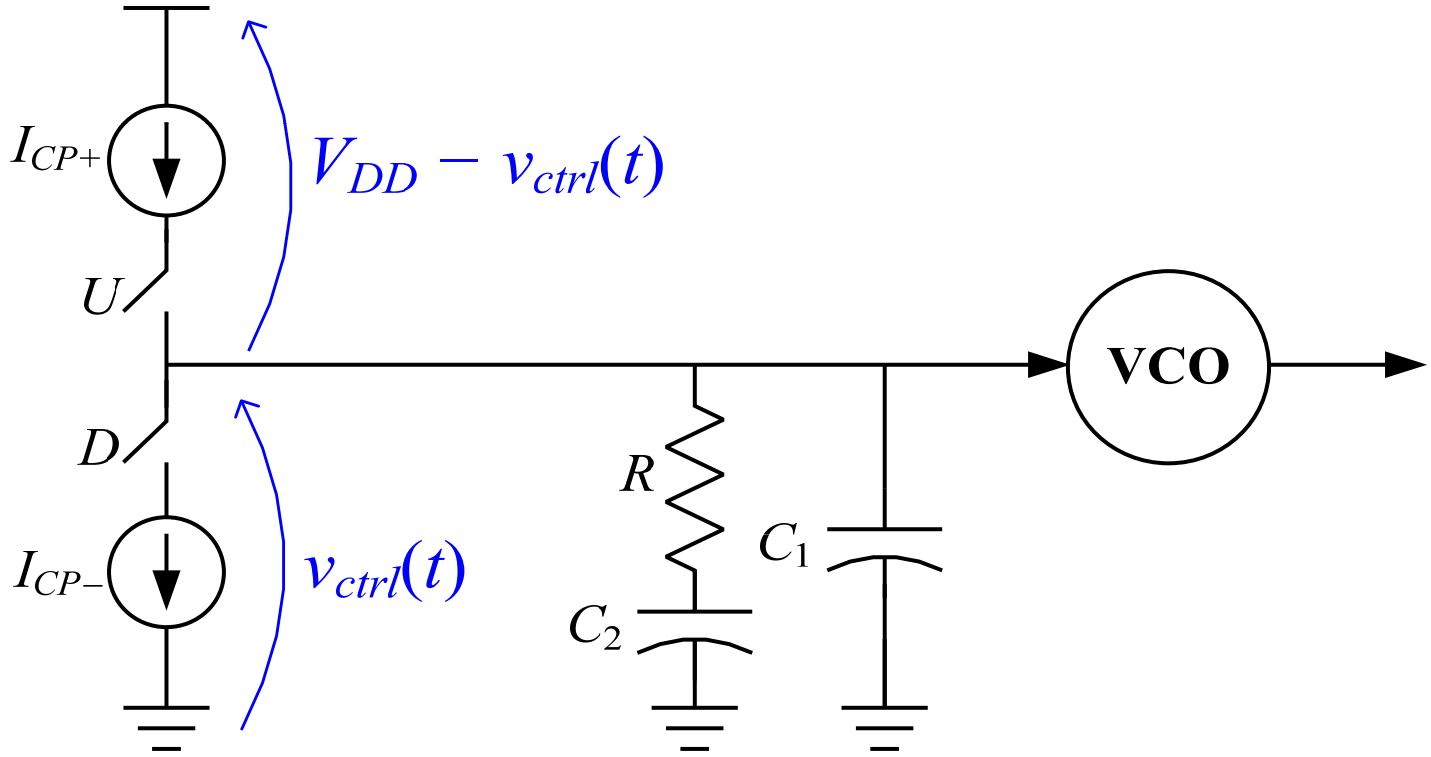


The slope discontinuity implies nonlinear behavior

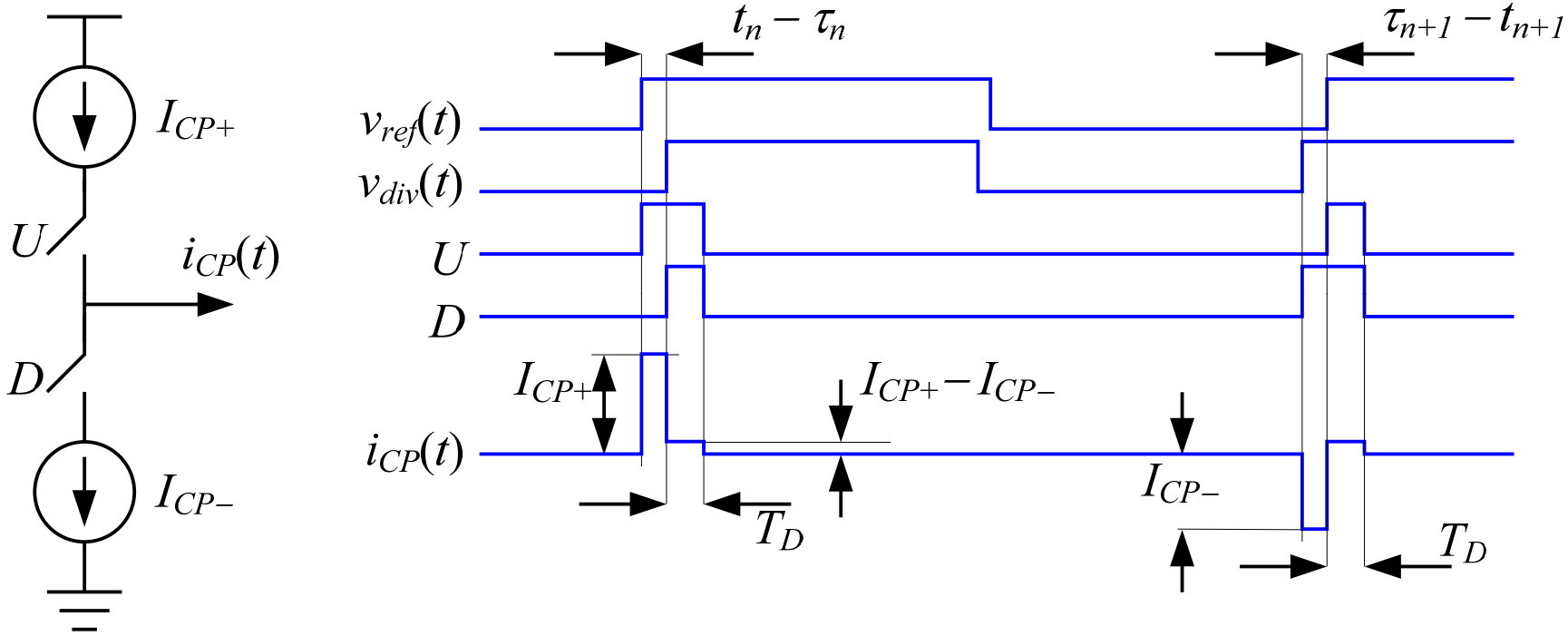
Nonlinearity: Positive-Negative CP Mismatch

Q: What's so hard about matching current sources?

A: The voltages across the *p* and *n* current sources do not track and they span a wide range depending on the PLL frequency



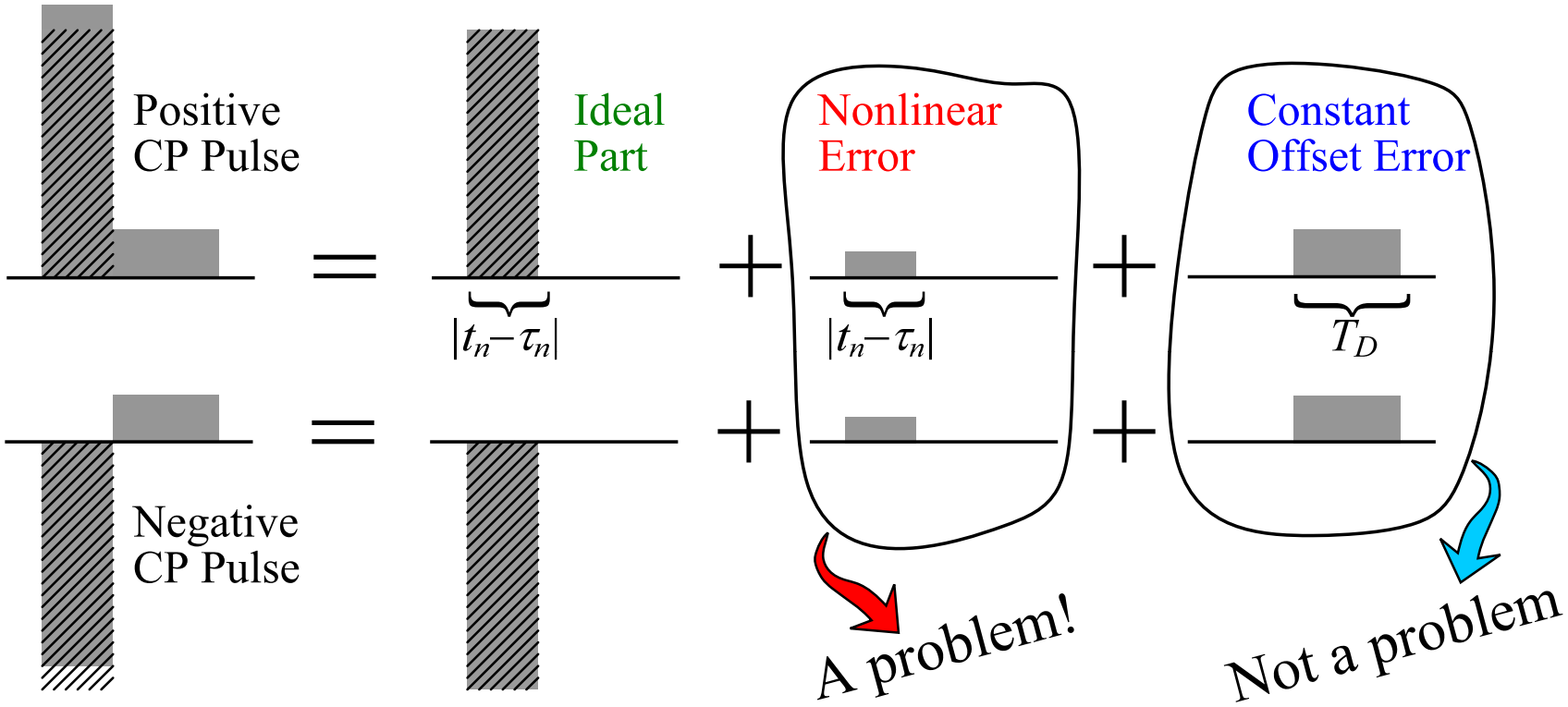
Nonlinearity: Positive-Negative CP Mismatch



(The T_D delay is to eliminate the dead zone as described previously)

Nonlinearity: Positive-Negative CP Mismatch

A closer look at typical charge pump pulses:



Total Charge:

$$\frac{1}{2}\underbrace{(t_n-\tau_n)(I_{CP+}+I_{CP-})}_{\text{Desired Term}}+\underbrace{\frac{1}{2}|t_n-\tau_n|\overbrace{(I_{CP+}-I_{CP-})}^{\text{Tends to be Large}}}_{\text{Nonlinear Term}}+\text{const}$$

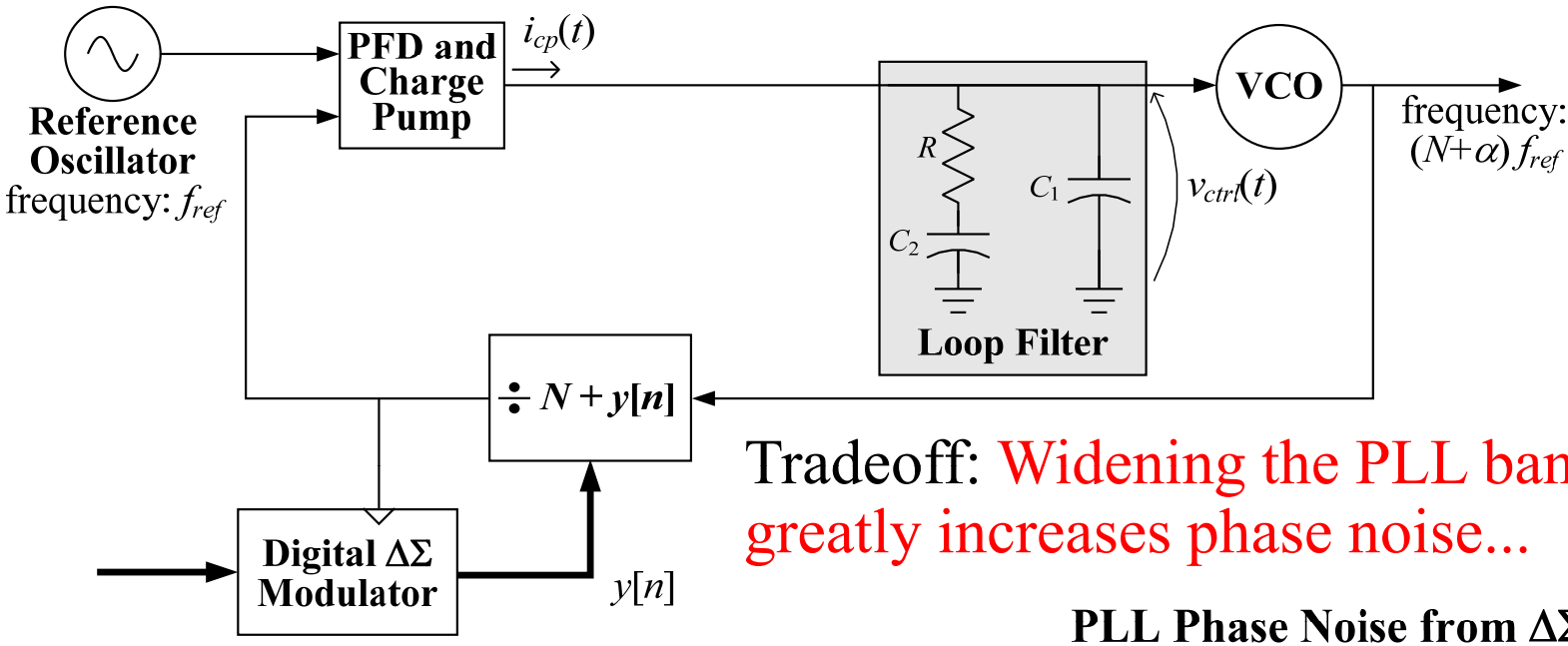
Positive-Negative CP Mismatch Solutions

- ✓ **Solution 1:** Increase output impedance of charge pump current sources (but this requires headroom)
- ✓ **Solution 2:** Actively balance the charge pump current sources using replica bias and an op-amp feedback circuits[17] (works well for narrow-band PLLs, but increases settling time)
- ✓ **Solution 3:** Modify PFD and charge pump so good matching is only required between like current sources[18]
- ✓ **Solution 4:** Use a charge pump offset (Slide 32) so only one charge pump current source carries phase information, and use a sampled loop filter (Slide 33) to avoid a large reference spur[13]

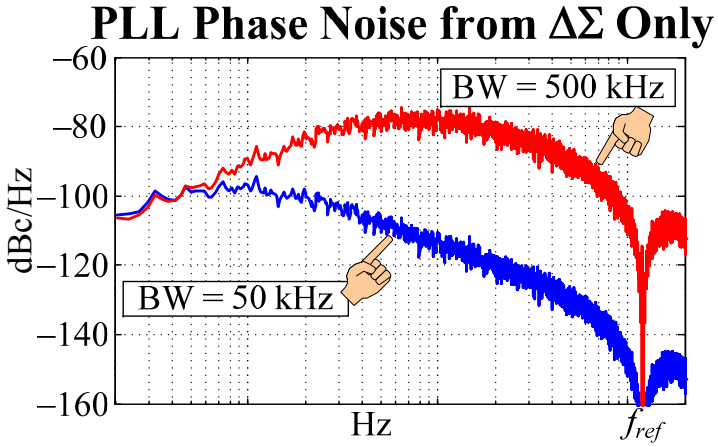
Outline

- Summary of Integer-*N* PLL Limitations
- The Idea Behind Fractional-*N* PLLs
- Delta-Sigma Modulation Overview
- Fractional-*N* PLL Dynamics
- Spurious Tones in Fractional-*N* PLLs
- **Fractional-*N* PLL Bandwidth Enhancement**
- IC Implementation Examples (bonus slides: not presented)

A Fundamental Fractional-*N* PLL Tradeoff



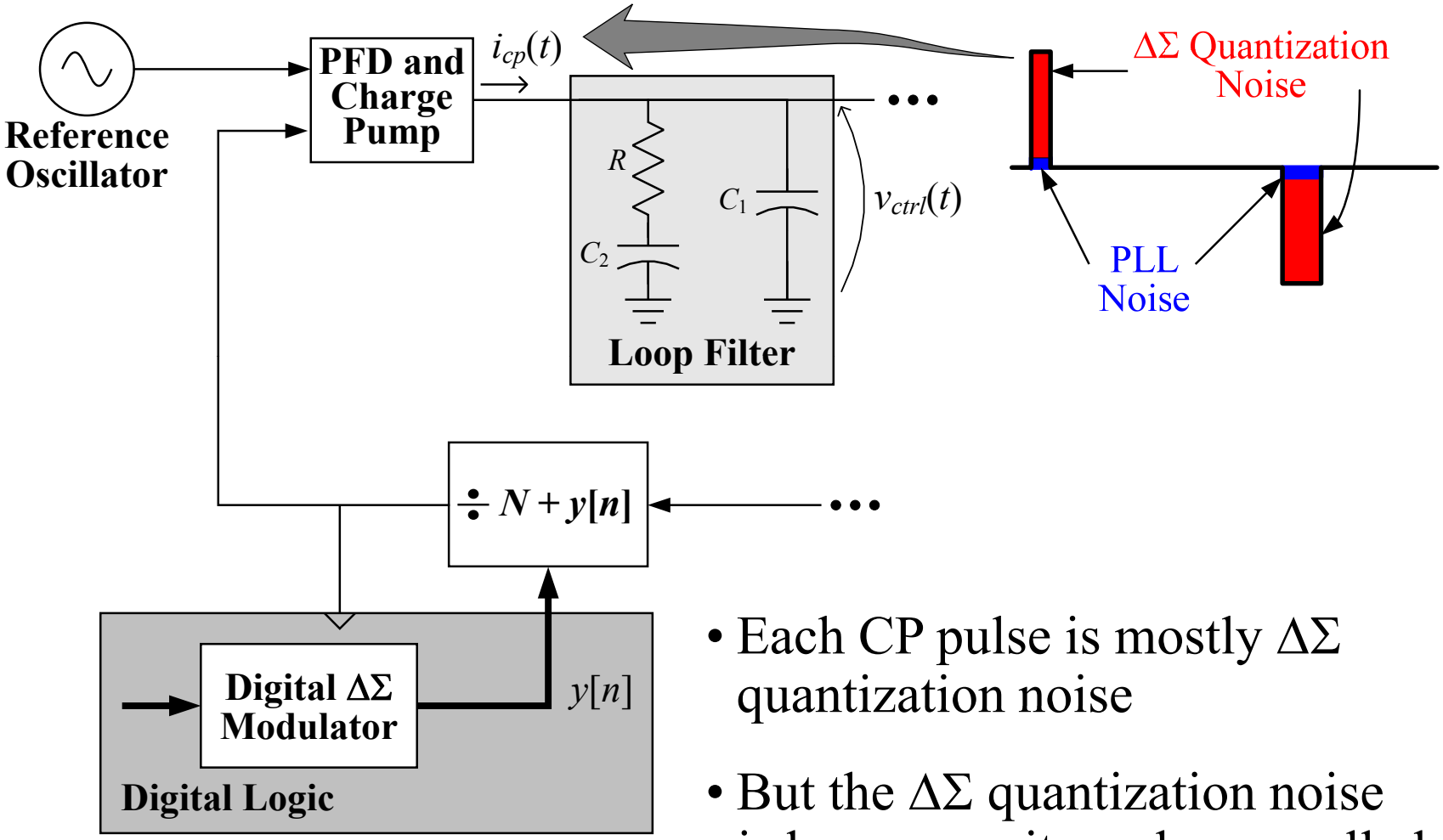
Tradeoff: Widening the PLL bandwidth greatly increases phase noise...



... but it also:

- reduces PLL settling time
- reduces sensitivity to VCO pulling
- enables an on-chip loop filter
- enables in-loop transmit modulation

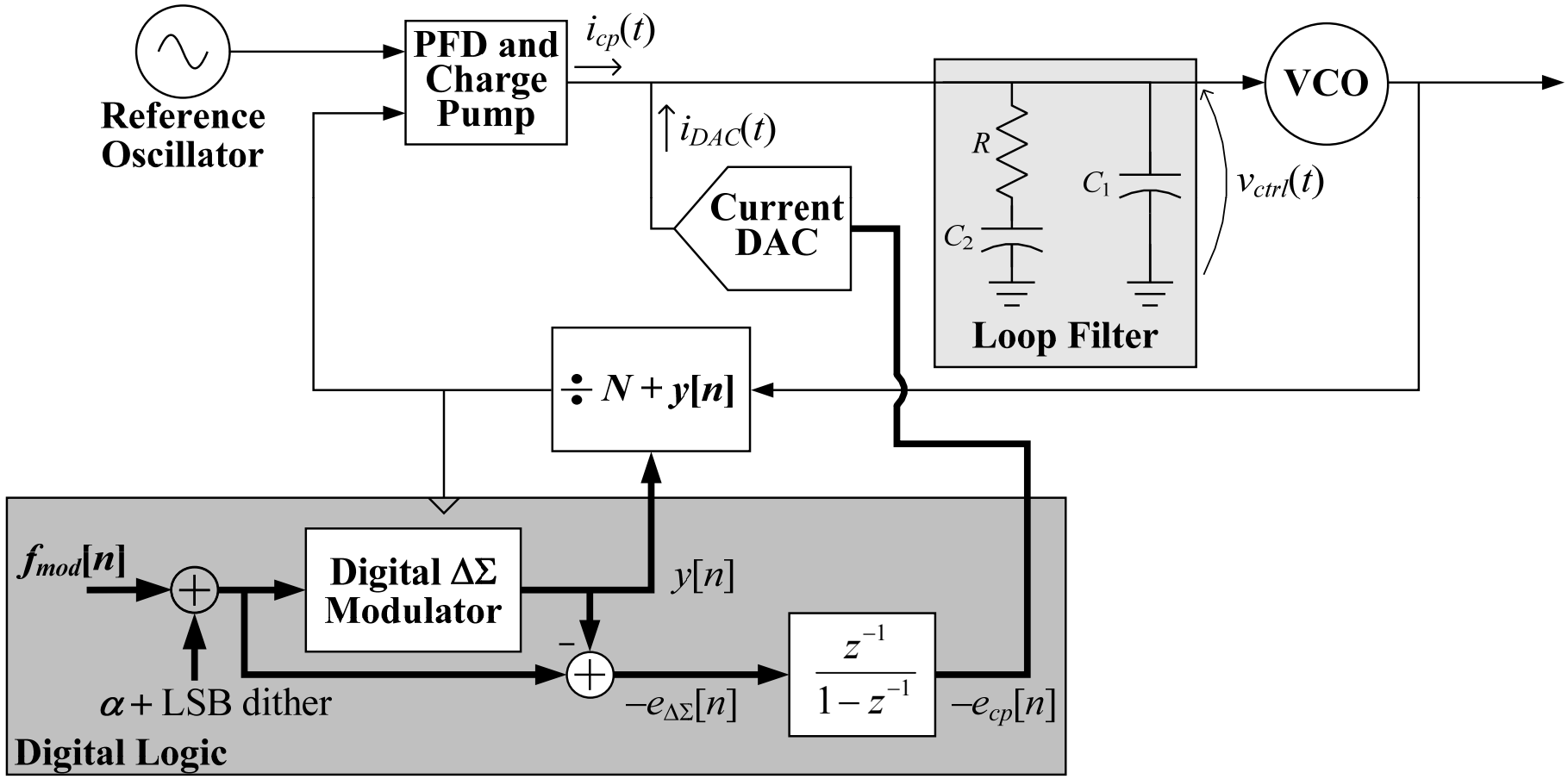
Idea Behind ΔΣ Phase Noise Cancellation



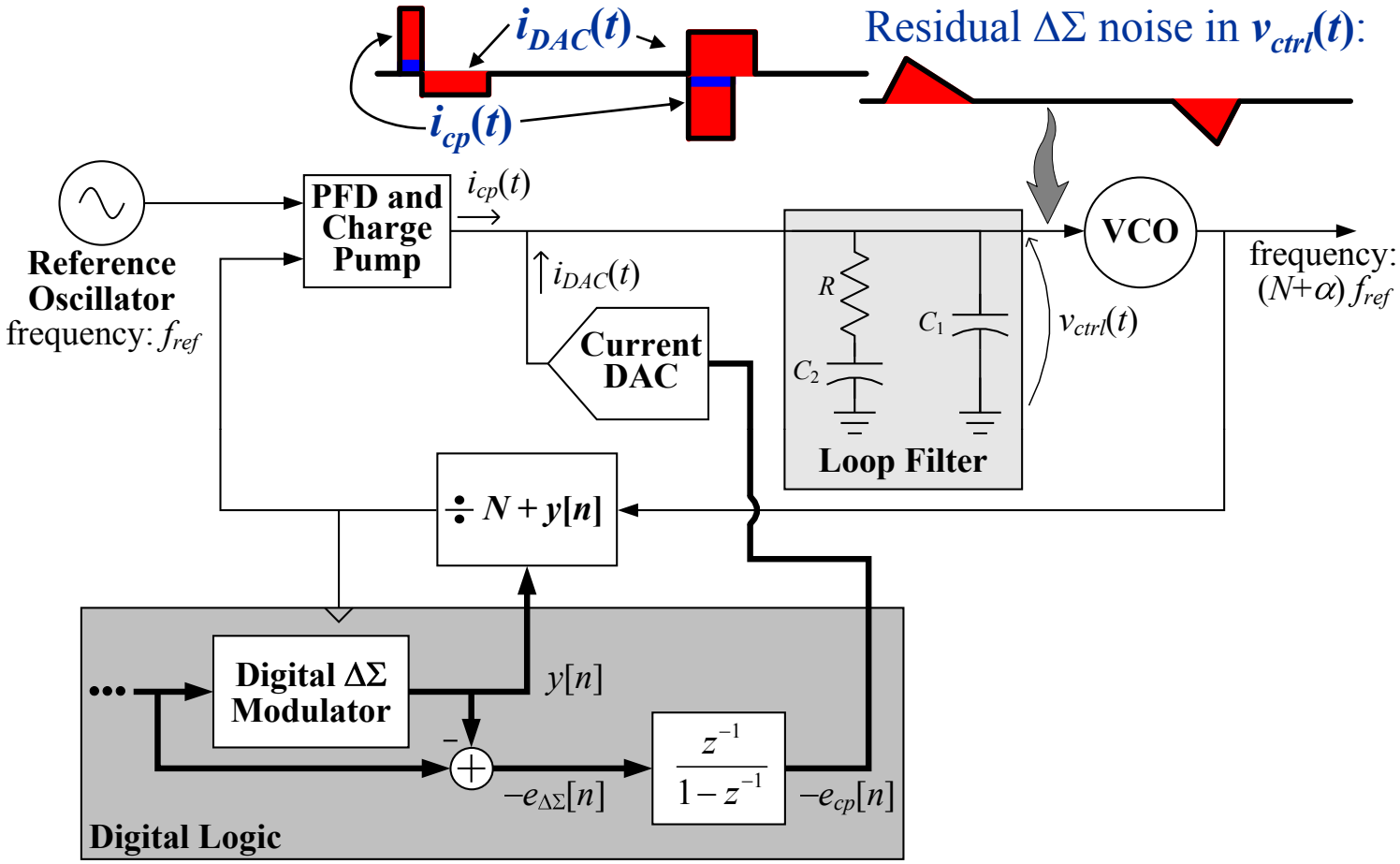
- Each CP pulse is mostly ΔΣ quantization noise
- But the ΔΣ quantization noise is known, so it can be cancelled with a DAC

A ΔΣ Phase Noise Canceling Fractional-*N* PLL

Use a wide PLL bandwidth but cancel the ΔΣ quantization noise prior to the loop filter [10, 12-14, 18-19]

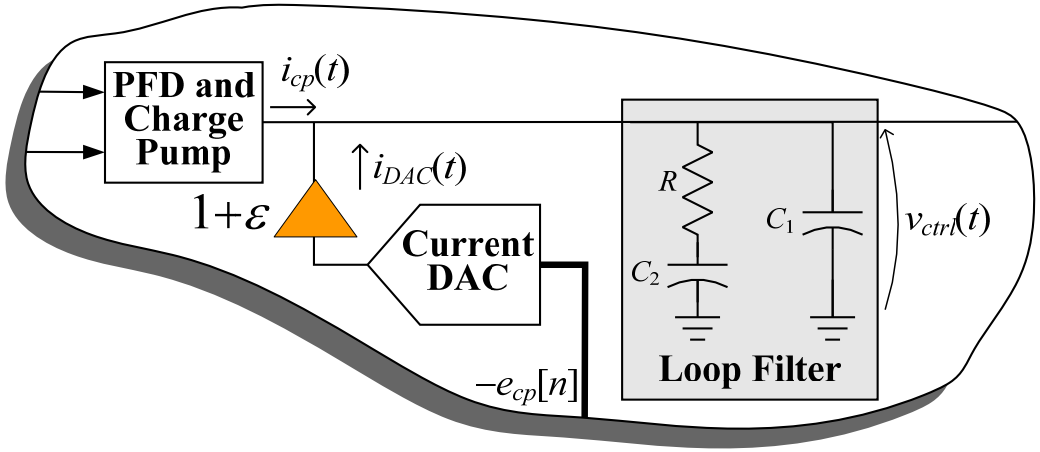


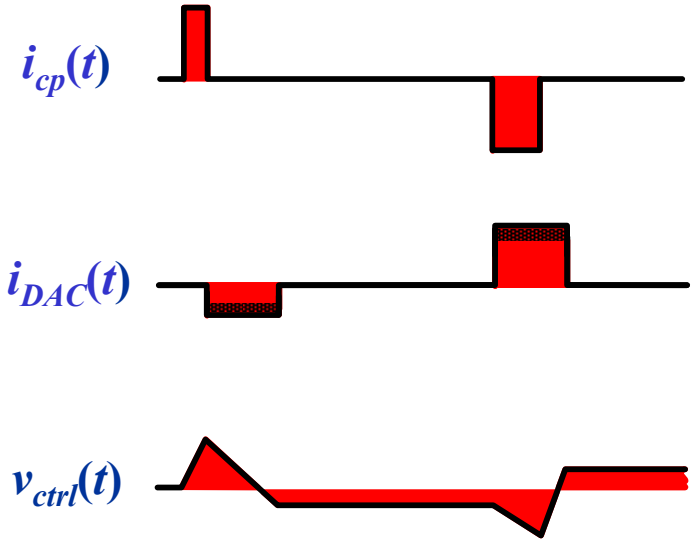
ΔΣ Phase Noise Cancellation



The DAC cancels most of the ΔΣ quantization noise prior to loop filter so PLL bandwidth need not be small

Effect of DAC Gain Error





- DAC gain error degrades the phase noise cancellation
- Passive matching is sufficient in many cases when f_{ref} is large enough (e.g., ≥ 35 MHz)
- Each halving of f_{ref} increases the phase noise from DAC gain error by $6(L–½)$ dB (L = ΔΣ order)[19]
- Adaptive gain calibration can be used for low f_{ref} cases[19]

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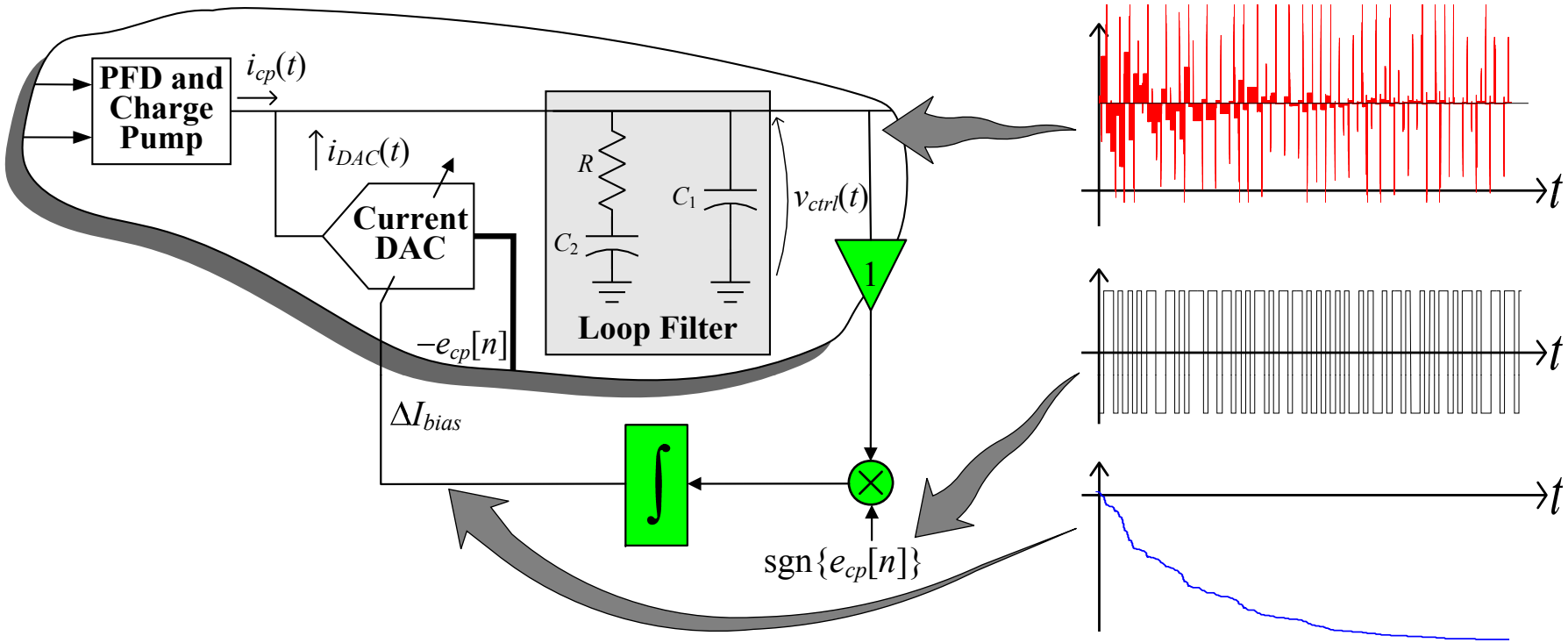
- **IC Implementation Examples** (bonus slides: not presented)

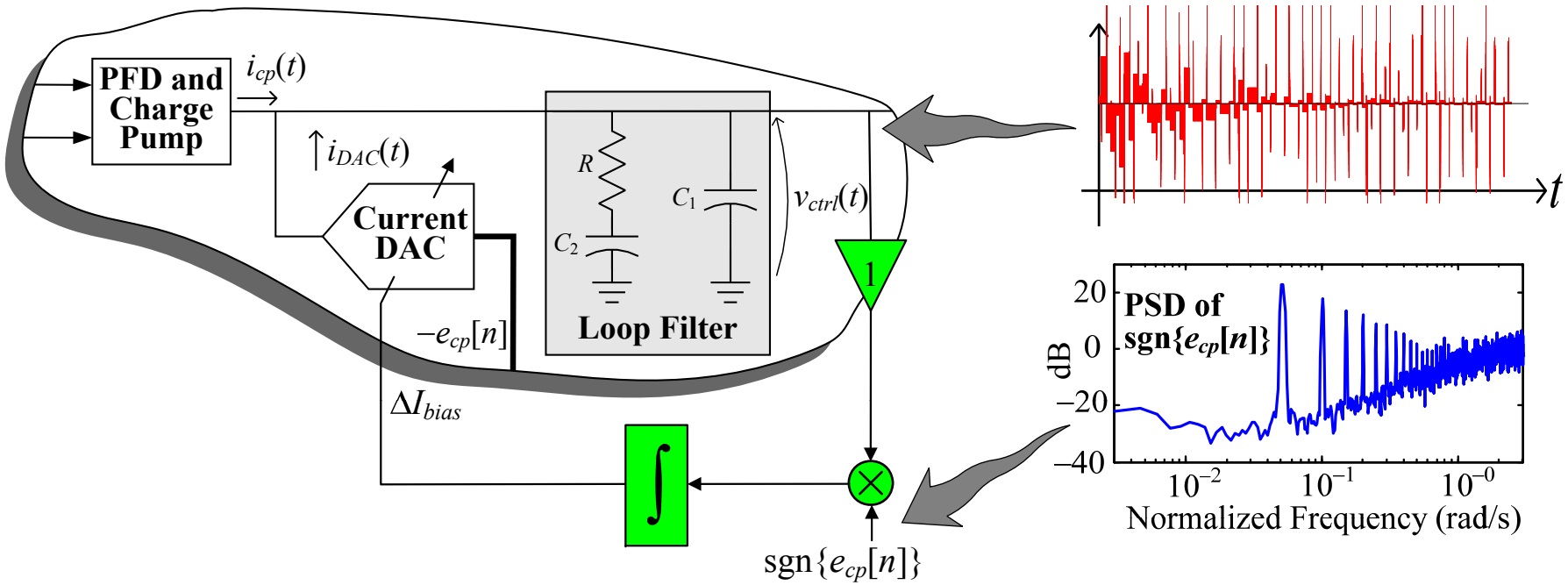
A Direct Method of Adaptive Calibration[20]



A Sign-LMS algorithm adjusts ΔI_{bias} until DAC gain is correct

- Term proportional to $e_{cp}[n]$ remains in v_{ctrl} if DAC cancellation is not perfect
- Since $\mathrm{sgn}\{e_{cp}[n]\} \times e_{cp}[n] = |e_{cp}[n]|$, integrator ramps up or down until ΔI_{bias} is adjusted properly

What's the Catch?

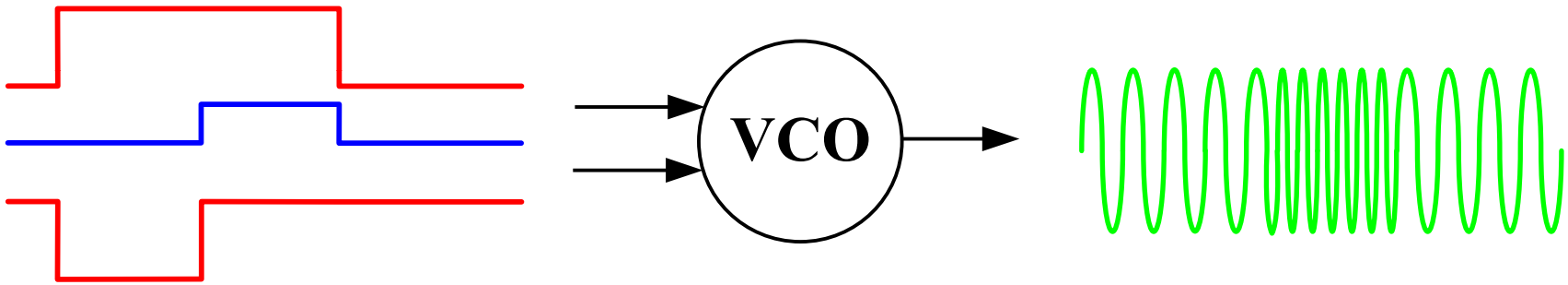


- v_{ctrl} can have a large DC component (it sets the VCO freq)
- Hence, the LMS loop contains a large $\mathrm{sgn}\{e_{cp}[n]\}$ term
- But $\mathrm{sgn}\{e_{cp}[n]\}$ contains large spurious tones
- To suppress the tones, the LMS loop BW must be *very* low

$\Rightarrow$ Very slow calibration settling, e.g., 1s in prior art

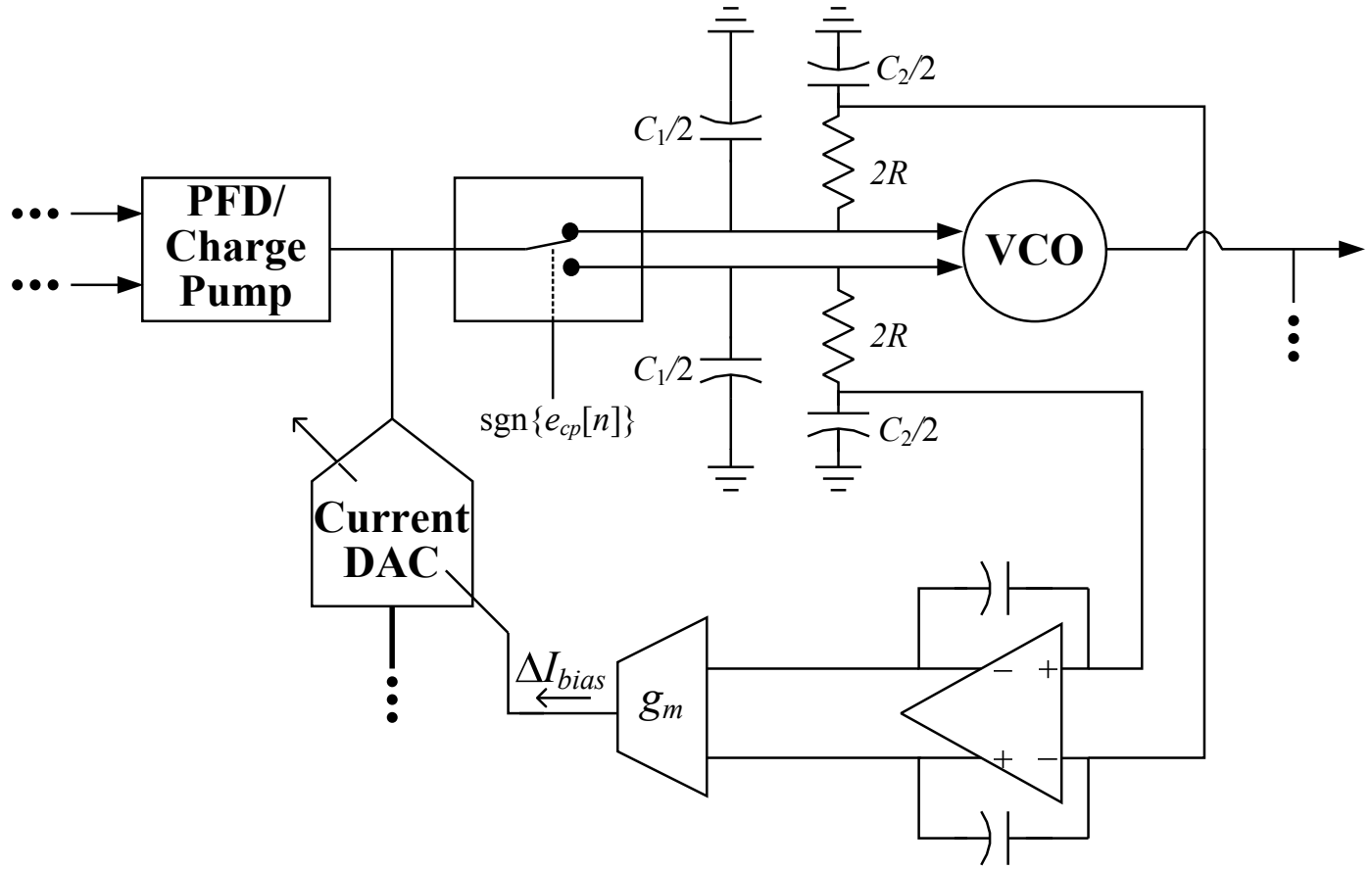
A Fast-Settling Adaptive Calibration Technique[19]

Idea: Split the VCO's varactor into 2 parallel halves; use the common-mode voltage to control the VCO and the differential-mode voltage to control the calibration loop



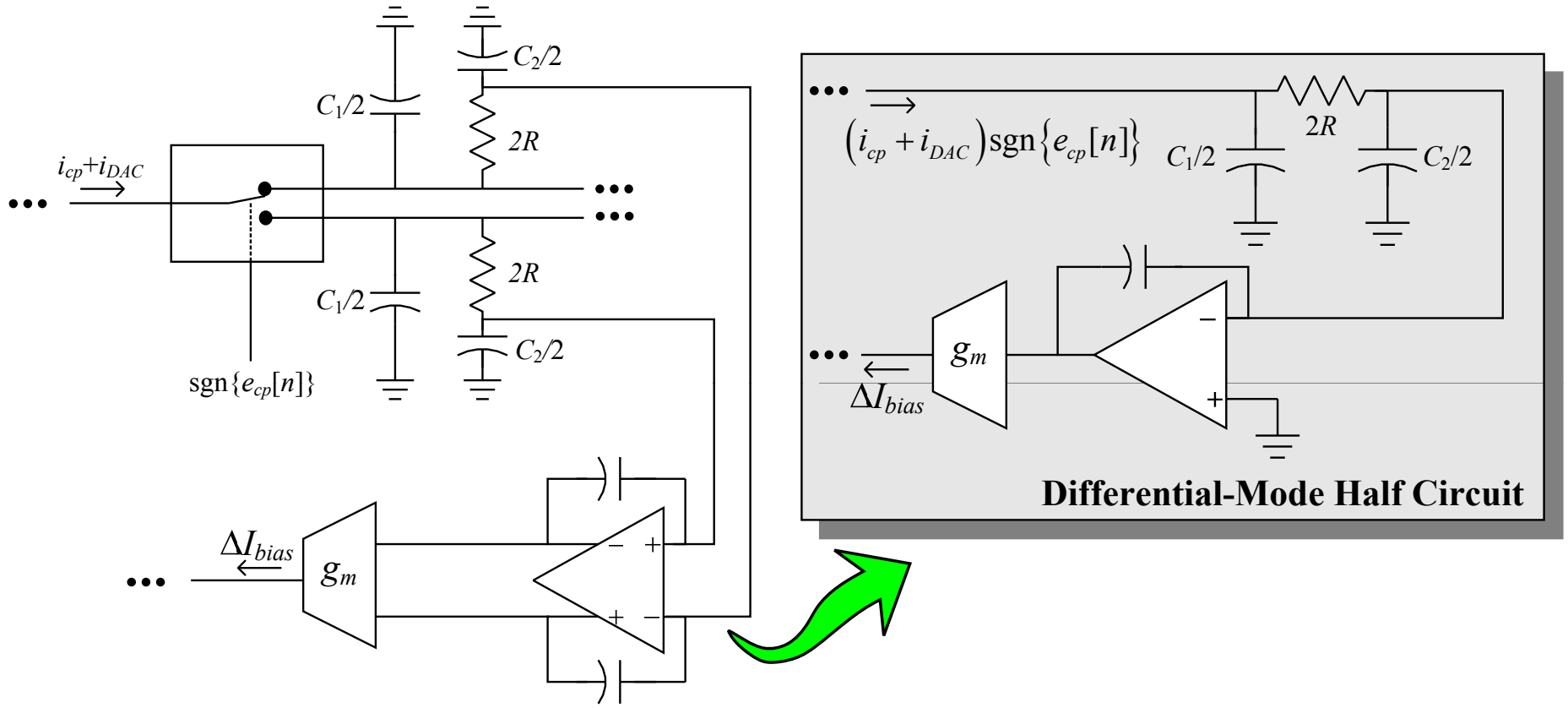
- VCO is controlled by its common-mode input voltage, but is insensitive to differential-mode voltage
- The differential-mode voltage is now available to independently control calibration loop

A Fast-Settling Adaptive Calibration Technique



- Two parallel half-sized loop filters and varactors create differential signal path for calibration loop
- Multiplication by ±1 performed by current steering
- Calibration feedback loop is DC-free

The Calibration Loop Signal Path

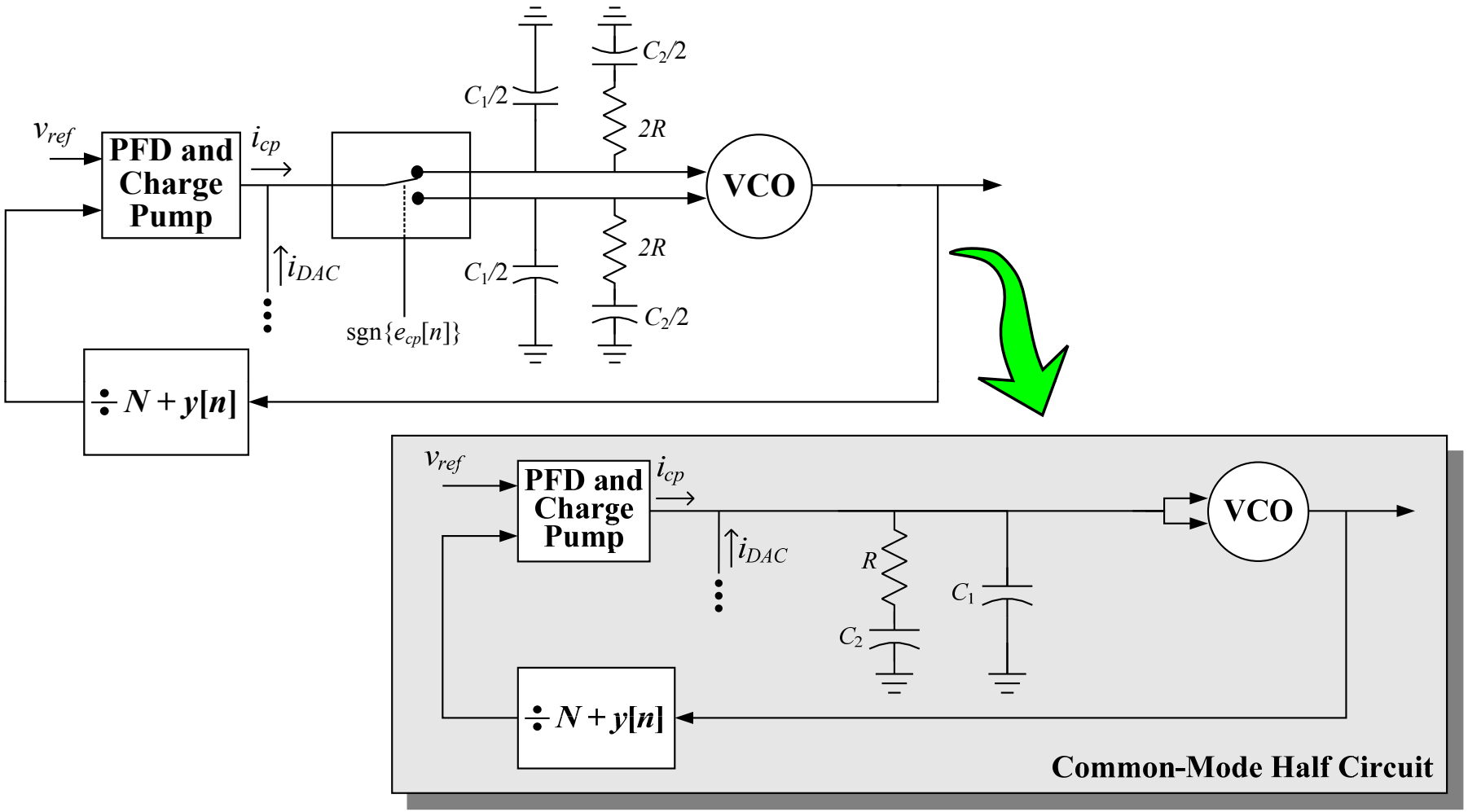


The calibration loop is controlled by a differential-mode signal that has no DC component

⇒ Calibration signal does not have to be filtered out by the calibration loop

⇒ Can have a wide calibration loop BW!

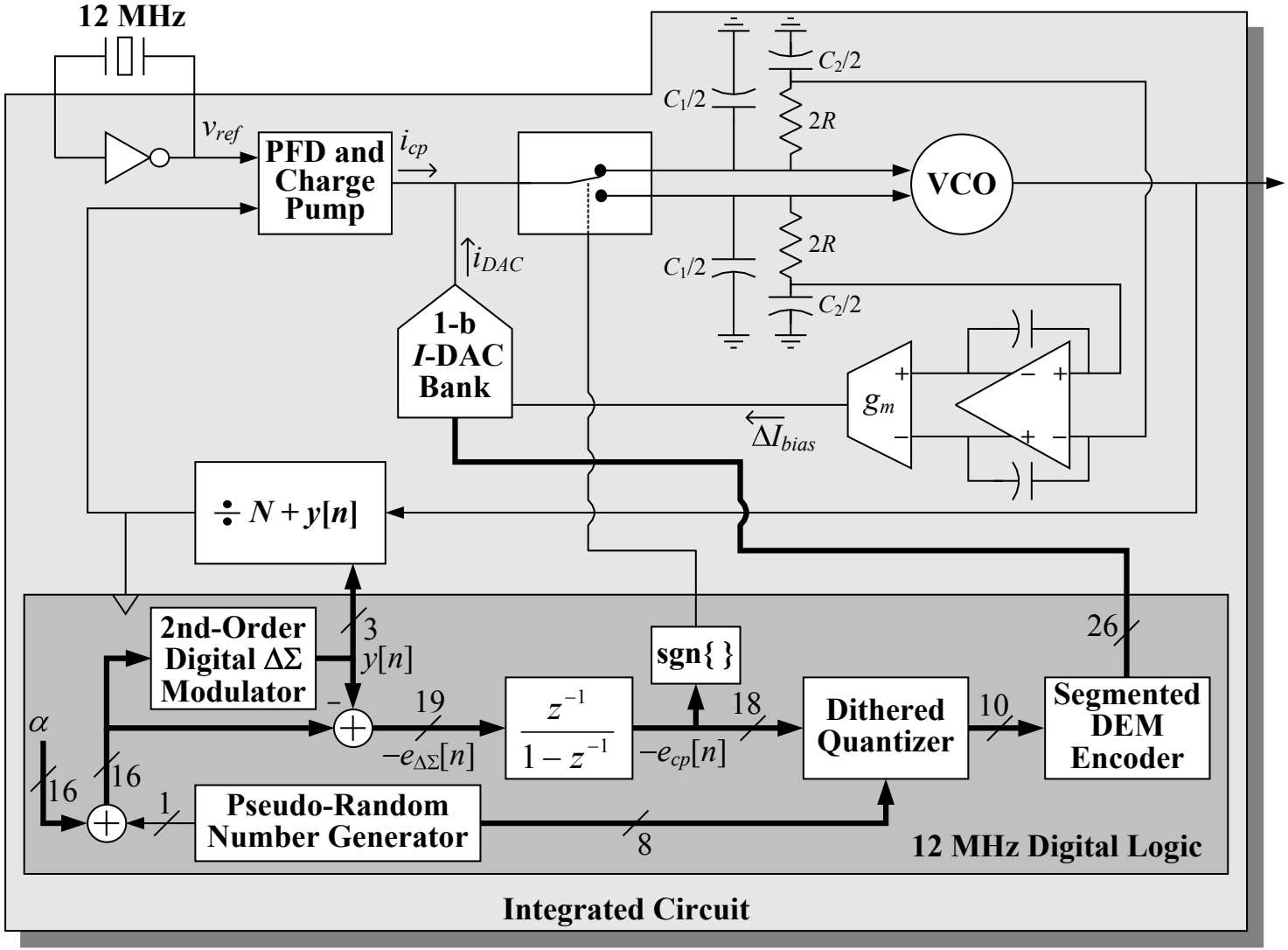
The PLL Signal Path



The VCO output is insensitive to calibration signal

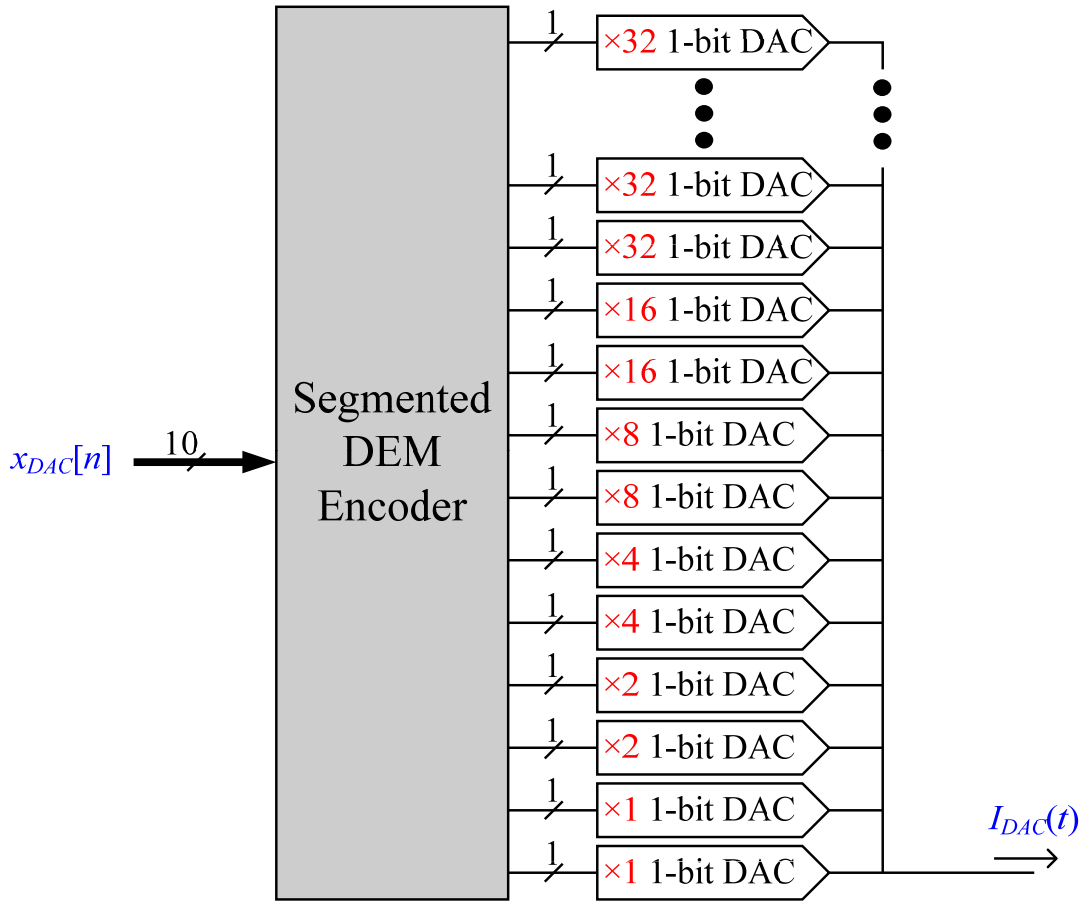
⇒ Calibration does not affect operation of PLL!

Example PLL IC 1: Block Diagram[19]



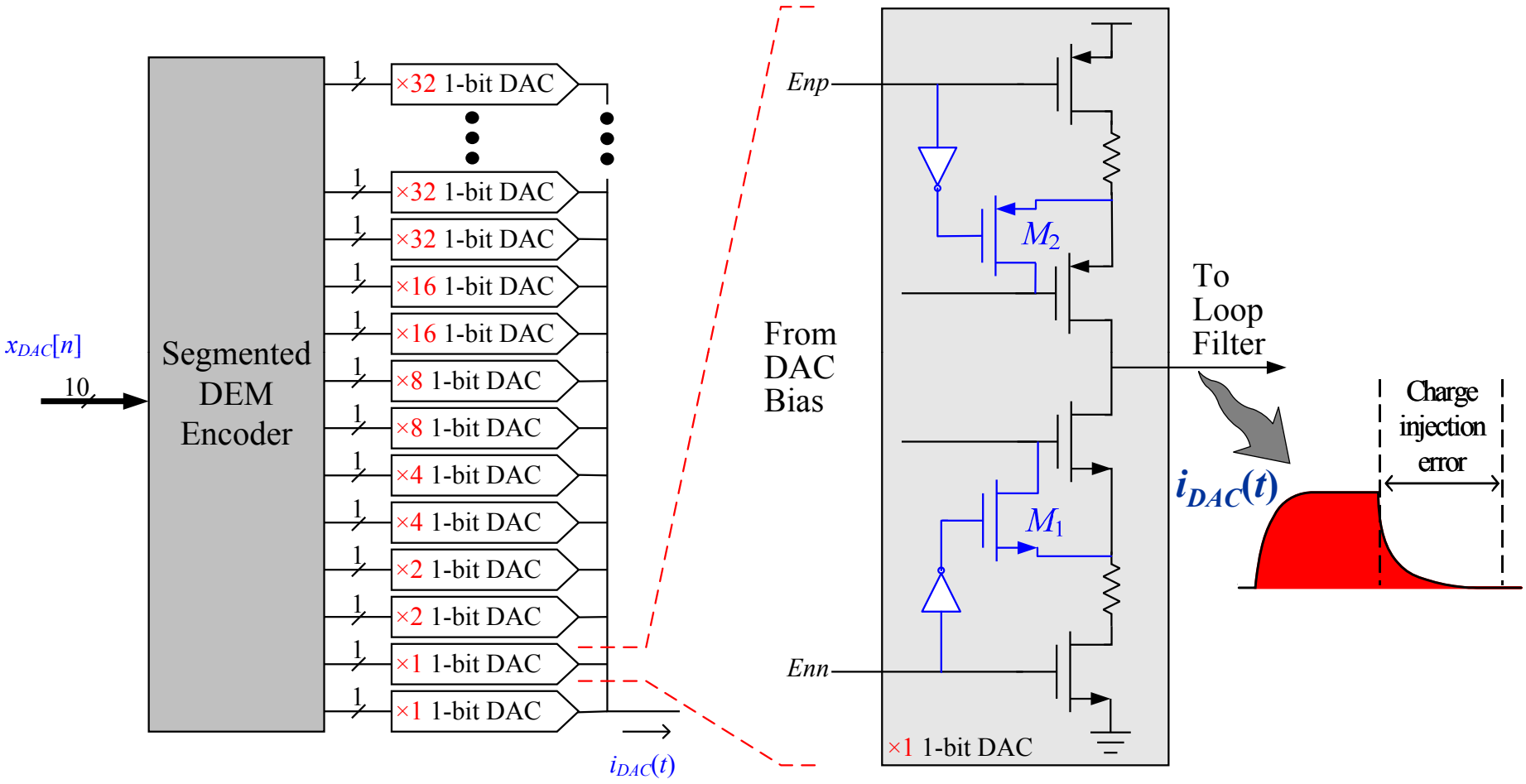
Output frequency: 2.4-2.5GHz; bandwidth: 730kHz
Technology: 0.18μm CMOS; Supply Voltage: 1.8V

Example PLL IC 1: DAC Topology



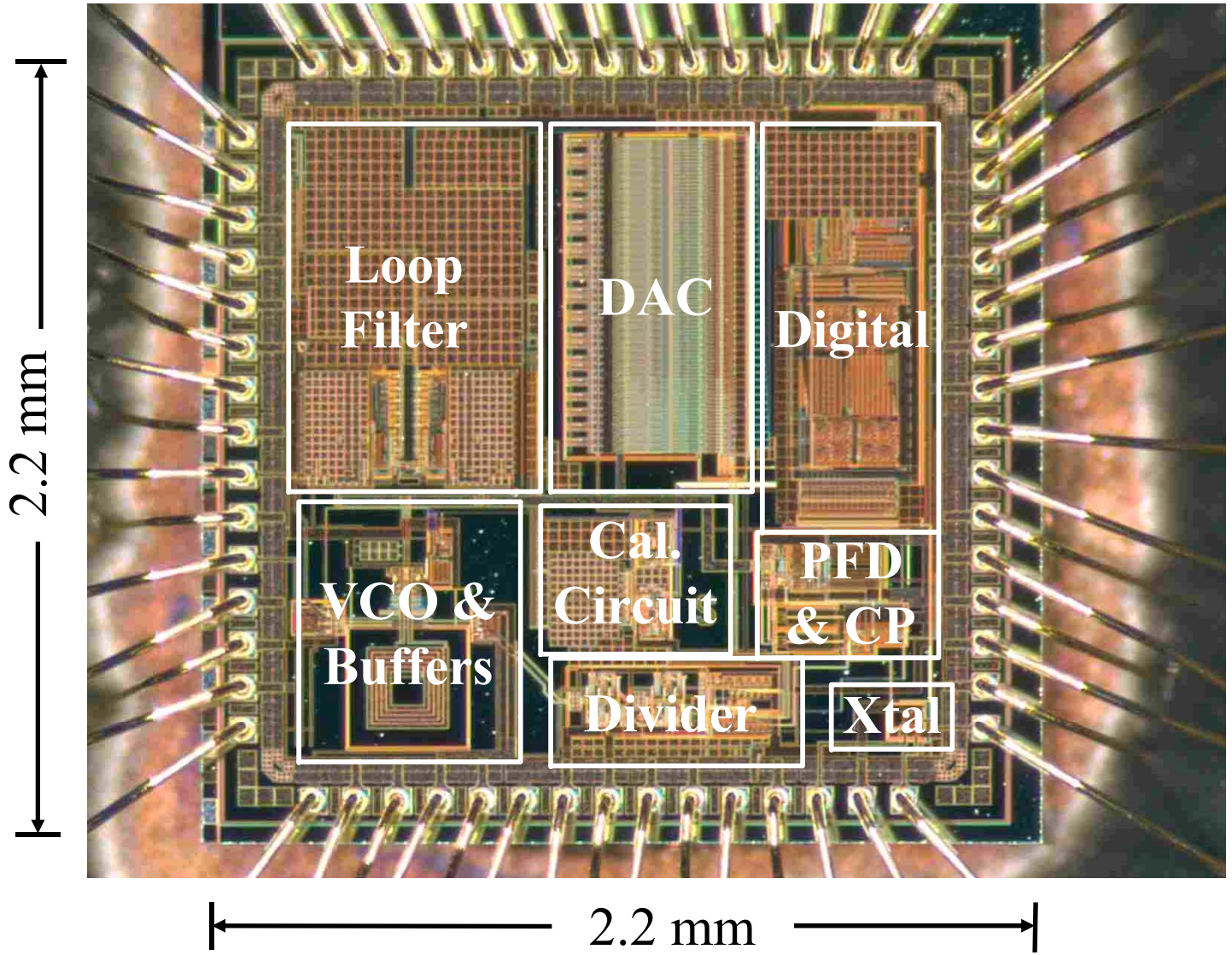
Segmented dynamic element matching used to eliminate harmonic distortion from non-ideal DAC weights and pulse shapes [21]

Example PLL IC 1: 1-bit DAC Circuit Details

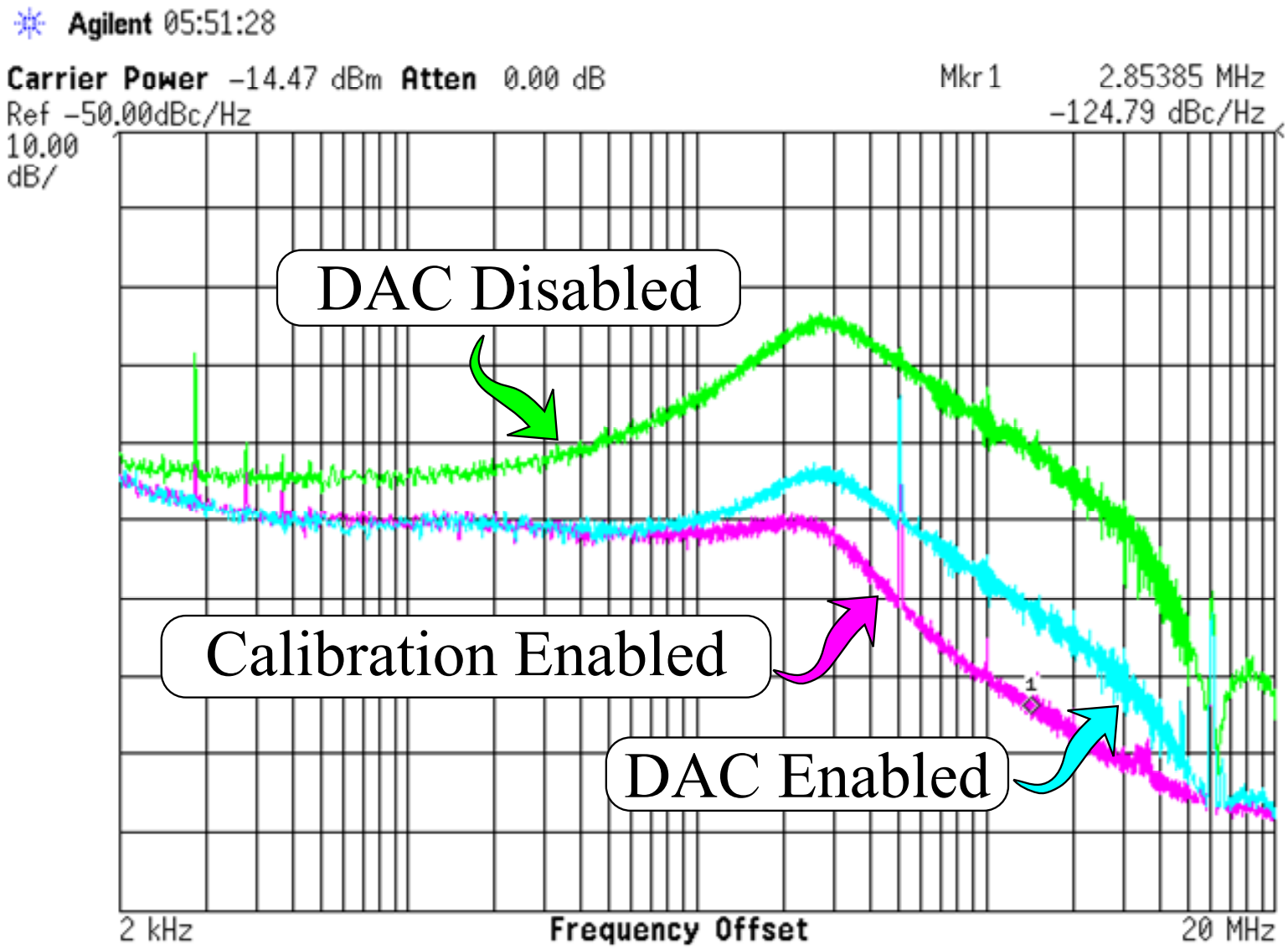


M_1 and M_2 used to minimize injection of channel charge into loop filter

Example PLL IC 1: Die Photograph



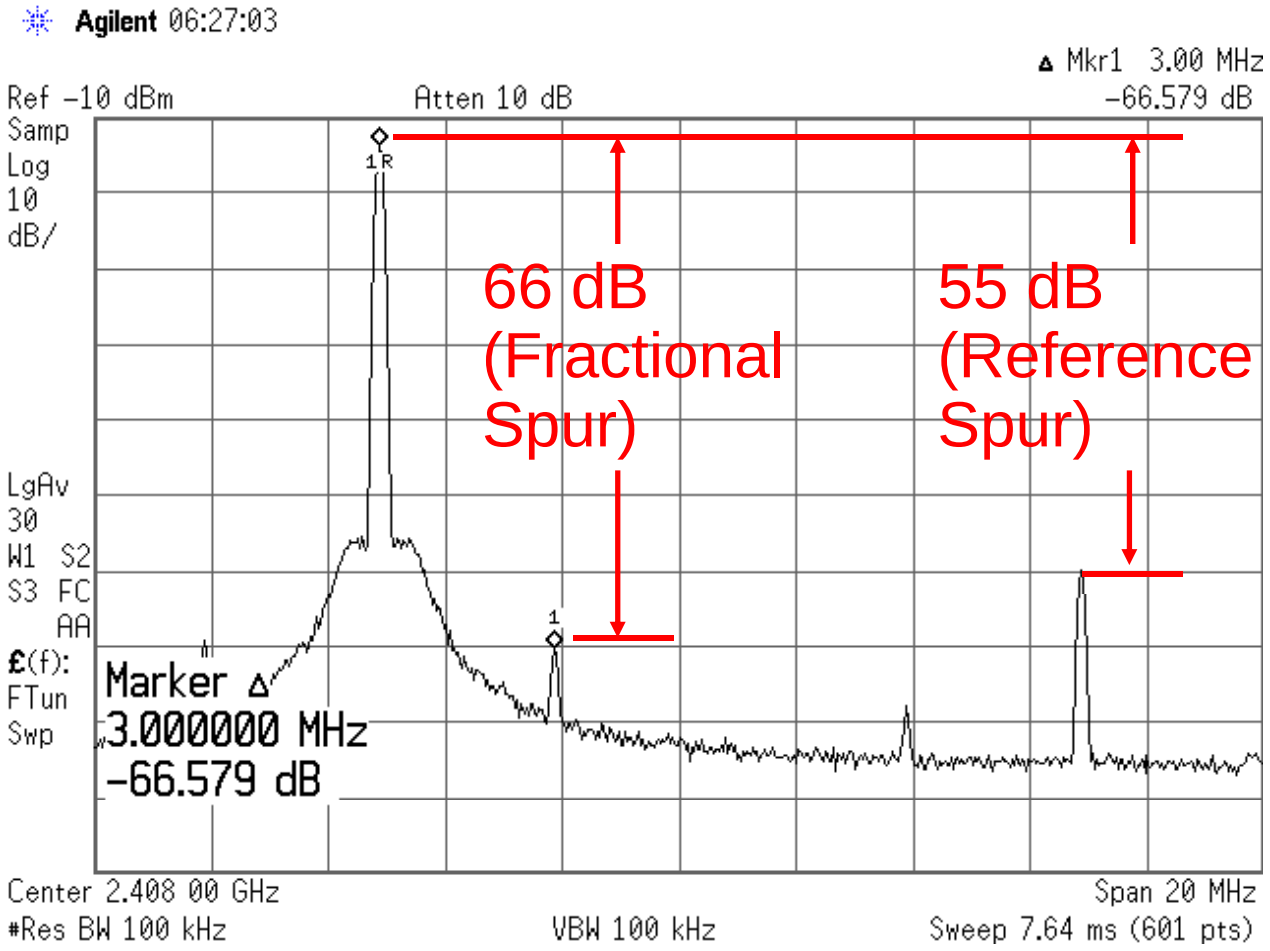
Example PLL IC 1: Measured Phase Noise



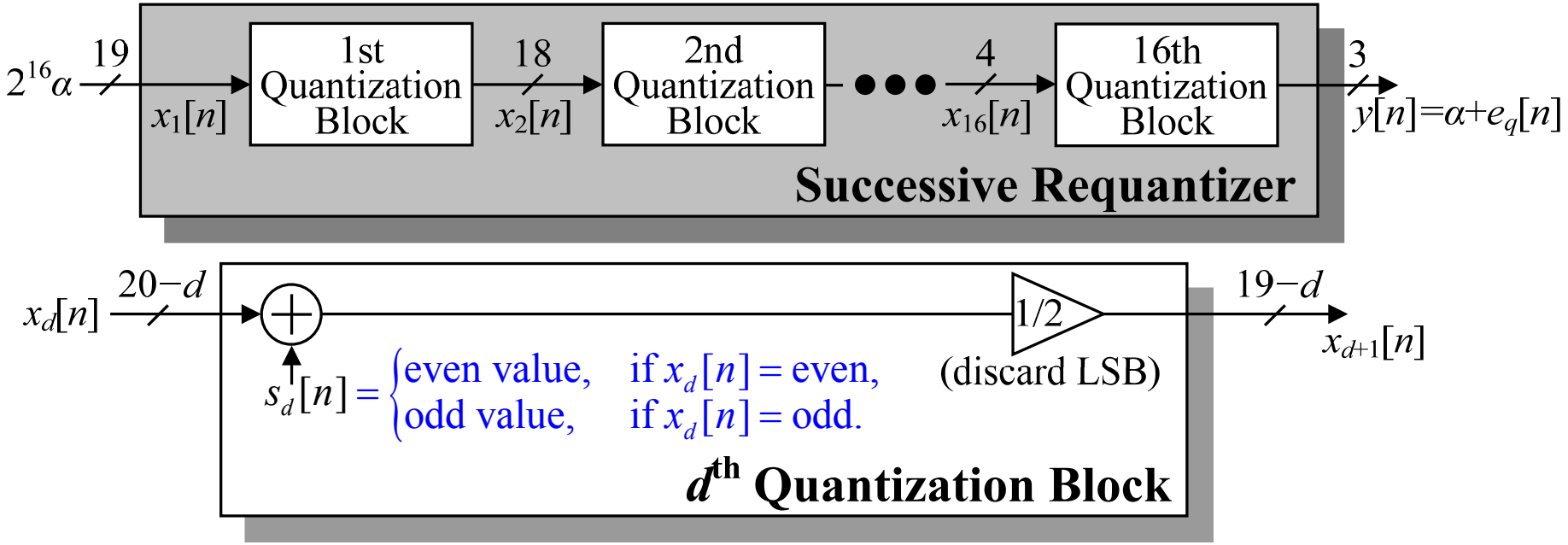
Example PLL IC 1: Performance Details

Design Details		
Technology	TSMC 0.18 μm 1P6M CMOS	
Package and Die Area	32 pin TQFN, 2.2 × 2.2 mm^2	
Reference Frequency	12 MHz	
Output Frequency	2.4 – 2.5 GHz	
Loop Bandwidth	> 730 kHz	
Measured Core Current Consumption (at 1.8V)		
VCO and Divider Buffer	6.9 mA	20.9 mA
Divider	5.8 mA	
CP (dynamic biasing enabled)	2.7 mA	
Digital	0.5 mA	
DAC	3.6 mA	
Calibration	1.4 mA	
Measured Worst Case Integer-*N* Performance		
Phase Noise @ 100 kHz	–104 dBc/Hz	
Phase Noise @ 3 MHz	−126 dBc/Hz	
Reference Spur	−55 dBc	
Measured Worst Case Performance with DAC and Calibration Disabled		
Phase Noise @ 100 kHz	−88 dBc/Hz	
Phase Noise @ 3 MHz	−91 dBc/Hz	
Fractional Spur @ ≥3 MHz	−45 dBc	
Reference Spur	−52 dBc	
Measured Worst Case Performance with DAC and Calibration Enabled		
Phase Noise @ 100 kHz	−101 dBc/Hz	
Phase Noise @ 3 MHz	−124 dBc/Hz	
Fractional Spur @ ≥3 MHz	−62 dBc	
Reference Spur	−53 dBc	

Example PLL IC 1: Measured Spur Performance



A ΔΣ Modulator Replacement[22]



- $2^{16}\alpha$ = integer (resolution of α is 2^{-16})
- Each quantization block divides by two and quantizes by one bit
- LSB of $s_d[n] + x_d[n]$ is zero so discarding it implements ÷2
- $e_q[n]$ is a linear combination of the $s_d[n]$ sequences
- $s_d[n]$ sequences must have properties desired of $e_q[n]$

Must Design Good $s_d[n]$ Sequences

Quantization block operation: $x_{d+1}[n] = \frac{1}{2}\left(x_d[n] + s_d[n]\right)$

In this work, have designed $s_d[n]$ to:

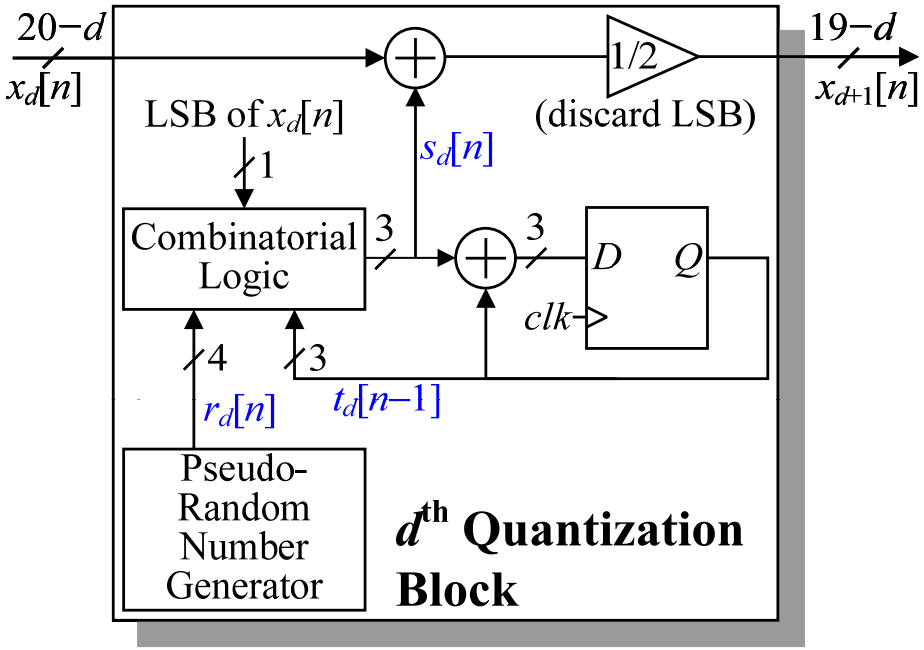
1. Ensure that the bit-width of $x_{d+1}[n]$ is that of $x_d[n]$ minus one
   $\Rightarrow$ parity of $s_d[n]$ must equal parity of $x_d[n]$
   $\Rightarrow$ magnitude of $s_d[n]$ must not be too large
2. Keep $t_d[n]$ bounded ($\Rightarrow$ 1st-order shaped PSD)
3. Prevent spurs in $(s_d[n])^p$, $p = 1, \ldots, 5$, and $(t_d[n])^q$, $q = 1, 2, 3$
   (this requires $s_d[n] \in \{0, \pm 1, \pm 2, \pm 3\}$)

where $t_d[n]$ is the running sum of $s_d[n]$

Tradeoff: Achieving item 3 increases power of $s_d[n]$

Phase noise cancellation circumvents this problem

The Quantization Block Details

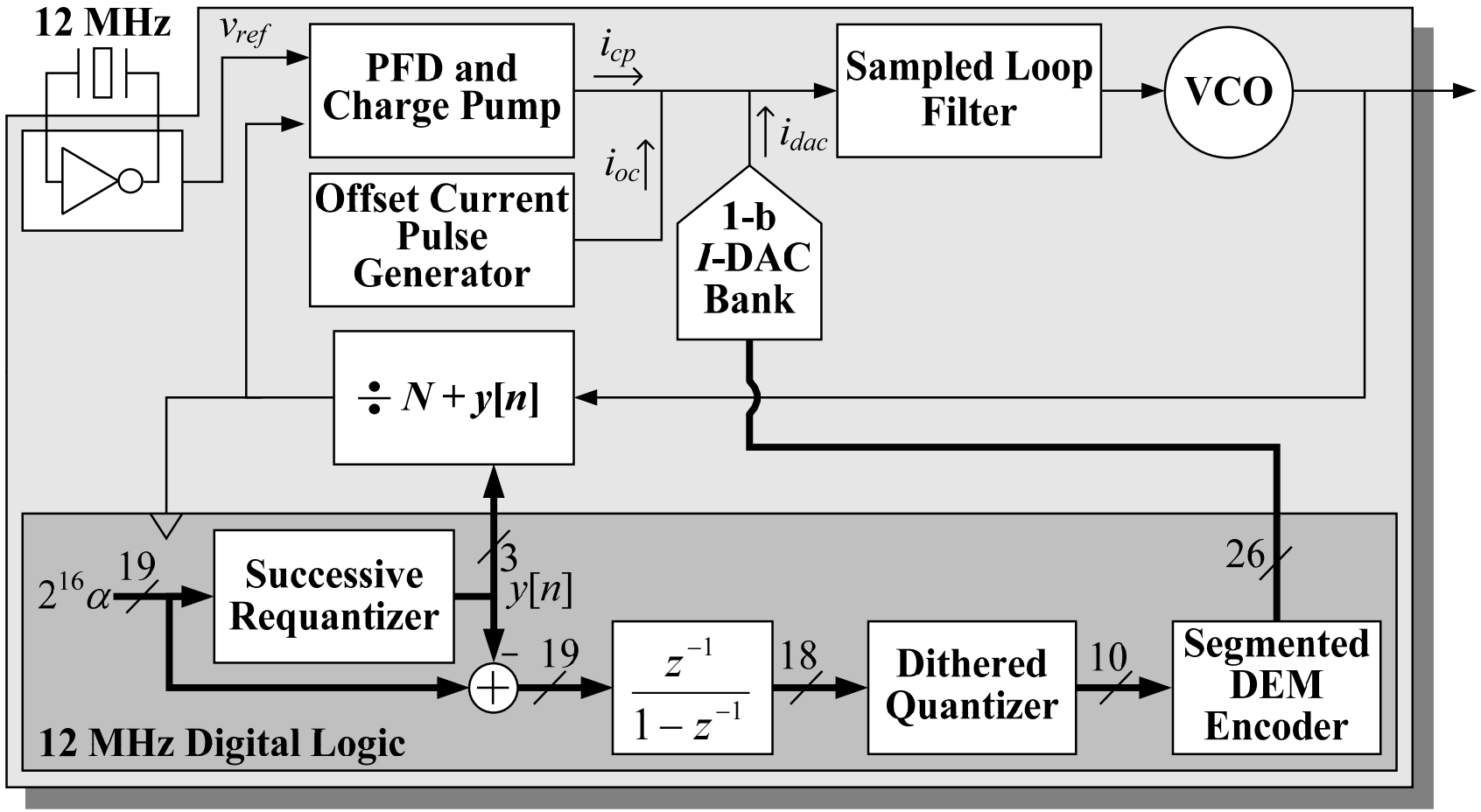


Combinatorial Logic Truth Table:

LSB of $x_d[n] = 0$			LSB of $x_d[n] = 1$		
$t_d[n-1]$	$r_d[n]$	$s_d[n]$	$t_d[n-1]$	$r_d[n]$	$s_d[n]$
2	≥ 0 and ≤ 3	0	2	≤ -1 or ≥ 4	−1
2	≤ -1 or ≥ 4	−2	2	≥ 0 and ≤ 3	−3
1	≤ -1 or ≥ 6	0	1	≥ 1 and ≤ 3	1
1	≥ 0 and ≤ 5	−2	1	≤ -1 or ≥ 4	−1
0	0 or 1	2	1	0	−3
0	≤ -1 or ≥ 4	0	0	≥ 0	1
0	2 or 3	−2	0	≤ -1	−1
−1	≤ -1 or ≥ 6	0	−1	≥ 1 and ≤ 3	−1
−1	≥ 0 and ≤ 5	2	−1	≤ -1 or ≥ 4	1
−2	≥ 0 and ≤ 3	0	−1	0	3
−2	≤ -1 or ≥ 4	2	−2	≤ -1 or ≥ 4	1
			−2	≥ 0 and ≤ 3	3

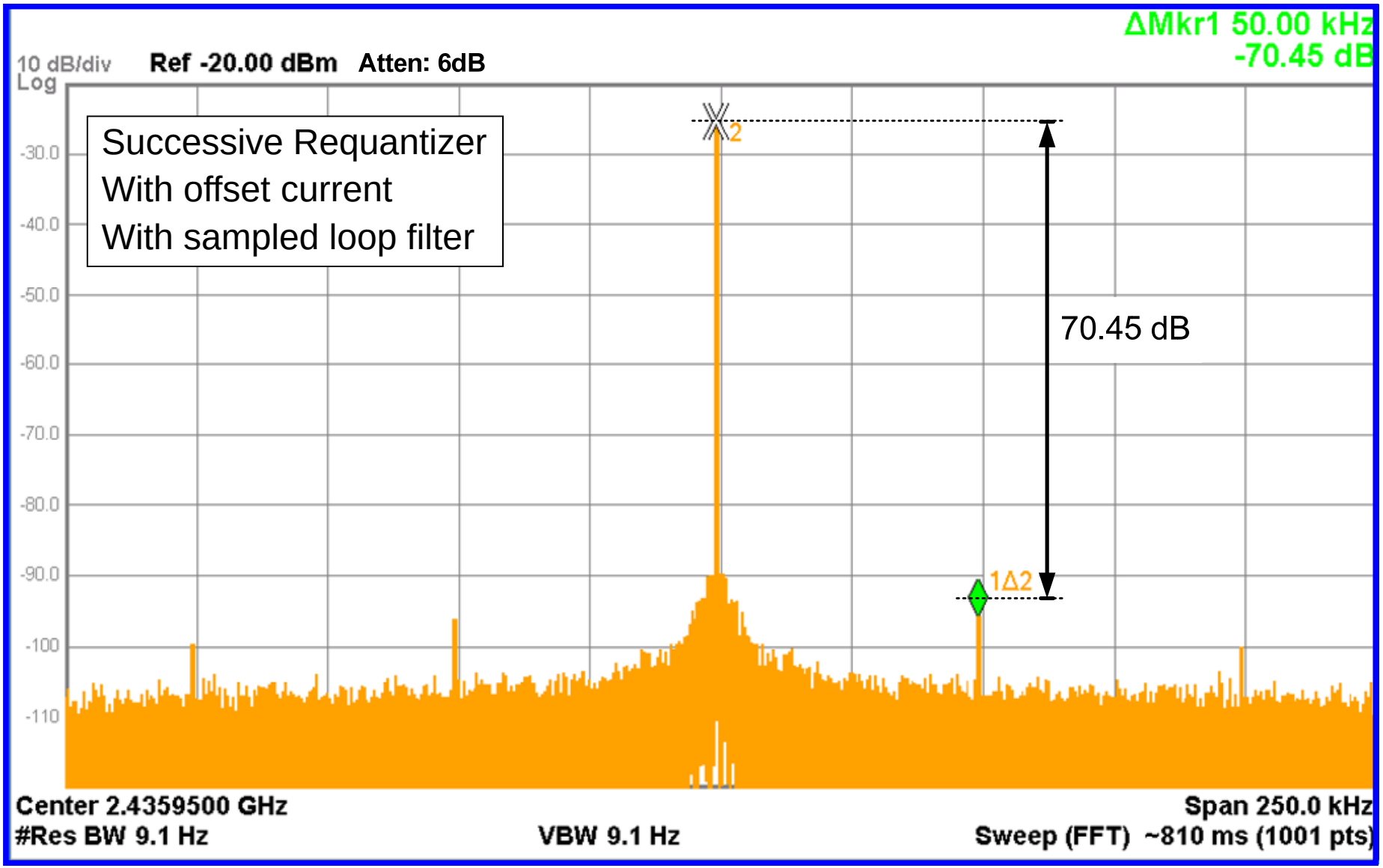
- $t_d[n]$ = running sum of $s_d[n]$
- $t_d[n]$ kept bounded $\Rightarrow$ 1st-order PSD shape
- No spurs in $(s_d[n])^p$, $p = 1, 2, \ldots, 5$, and $(t_d[n])^q$, $q = 1, 2, 3$
- See [22] for the math

Example PLL IC 2: Block Diagram[13]



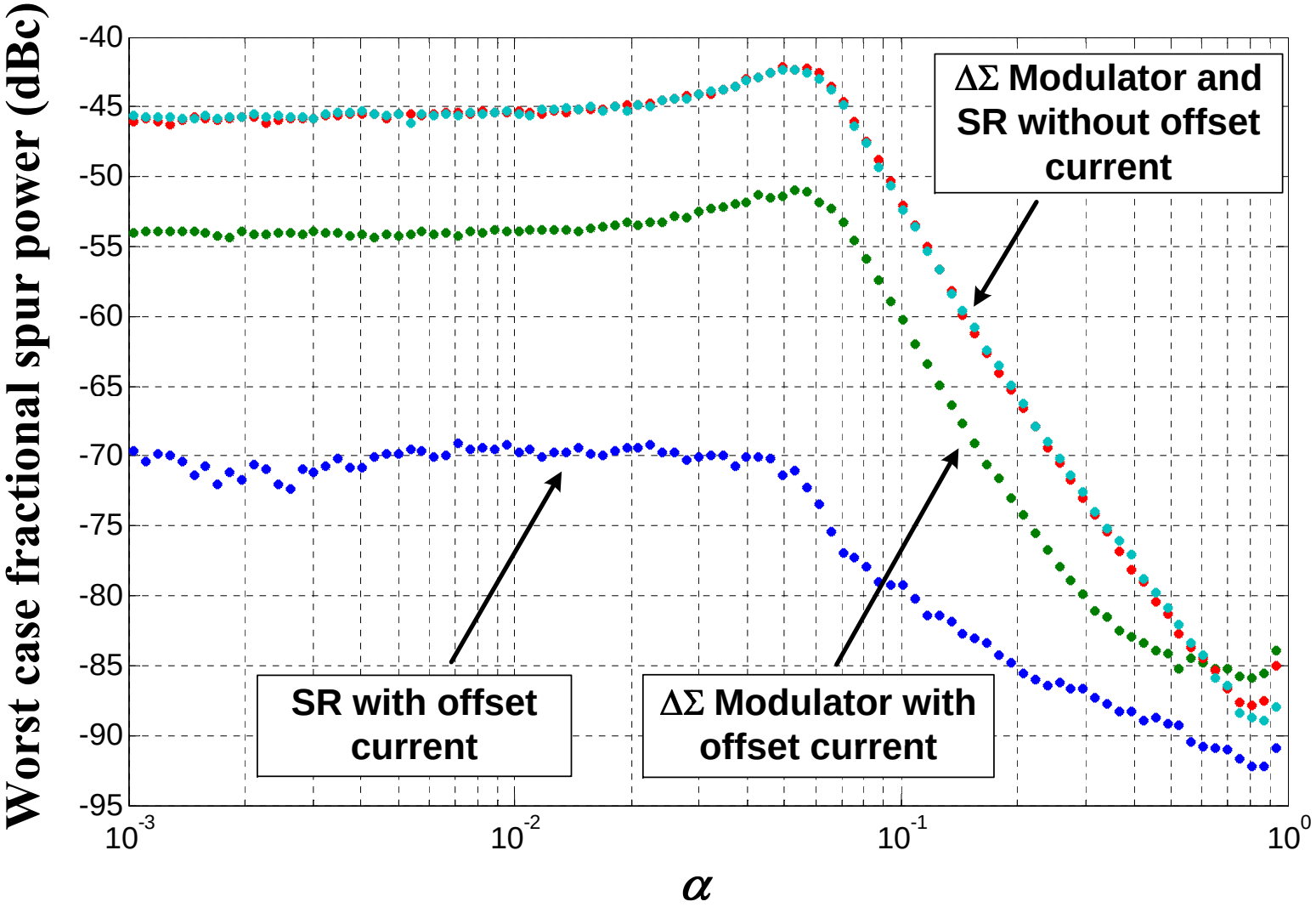
- $f_{VCO} \in$ 2.4 GHz ISM band; f_{ref} = 12 MHz; PLL BW = 975 kHz
- Phase noise cancellation with calibration (not shown) as in [19]
- Also contains a ΔΣ modulator for comparison

Example PLL IC 2: Meas. Close-In Fractional Spur

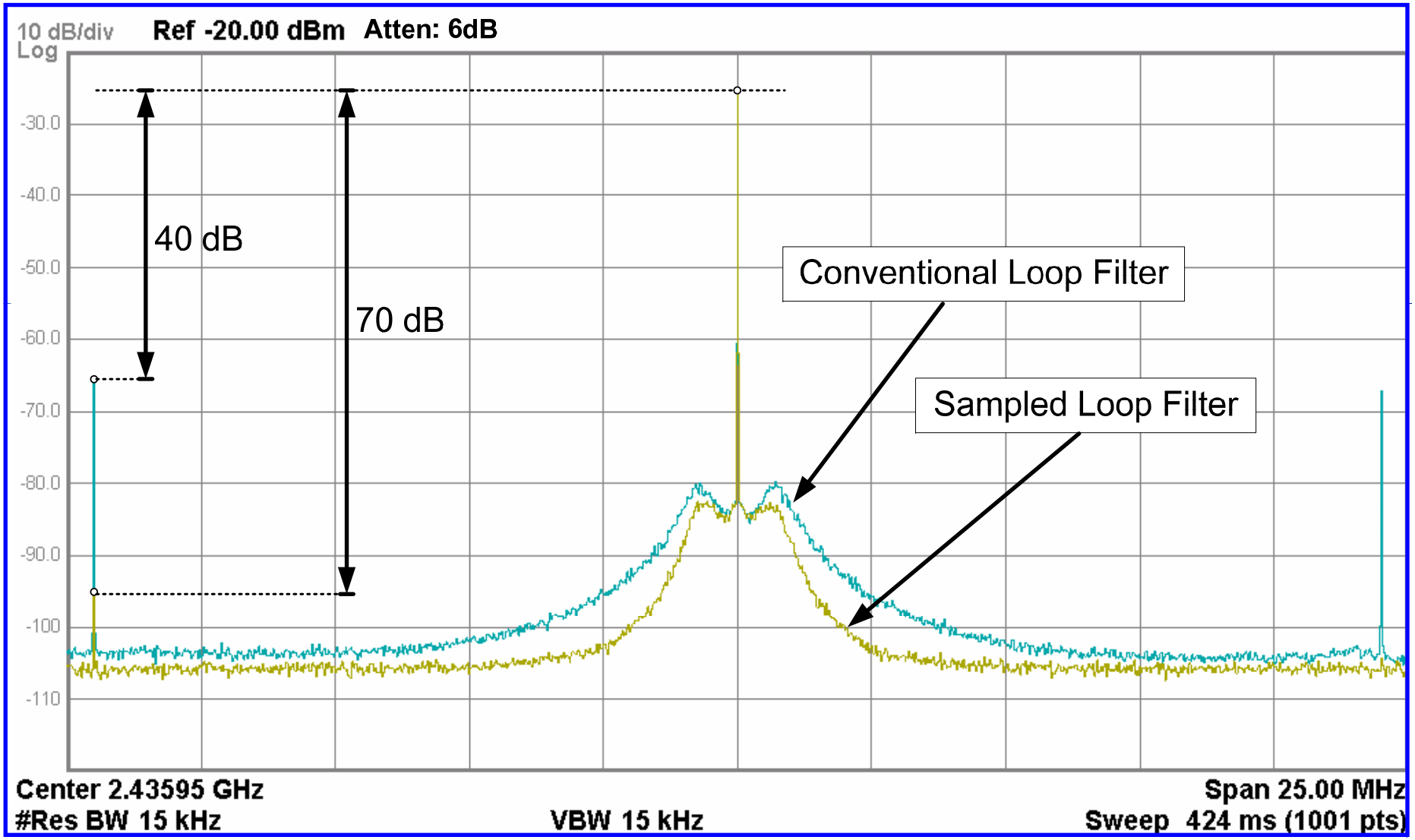


Example PLL IC 2: Measured Fractional Spur Levels

Comparison between ΔΣ Modulator and SR with and without offset current:



Example PLL IC 2: Measured Output Spectra

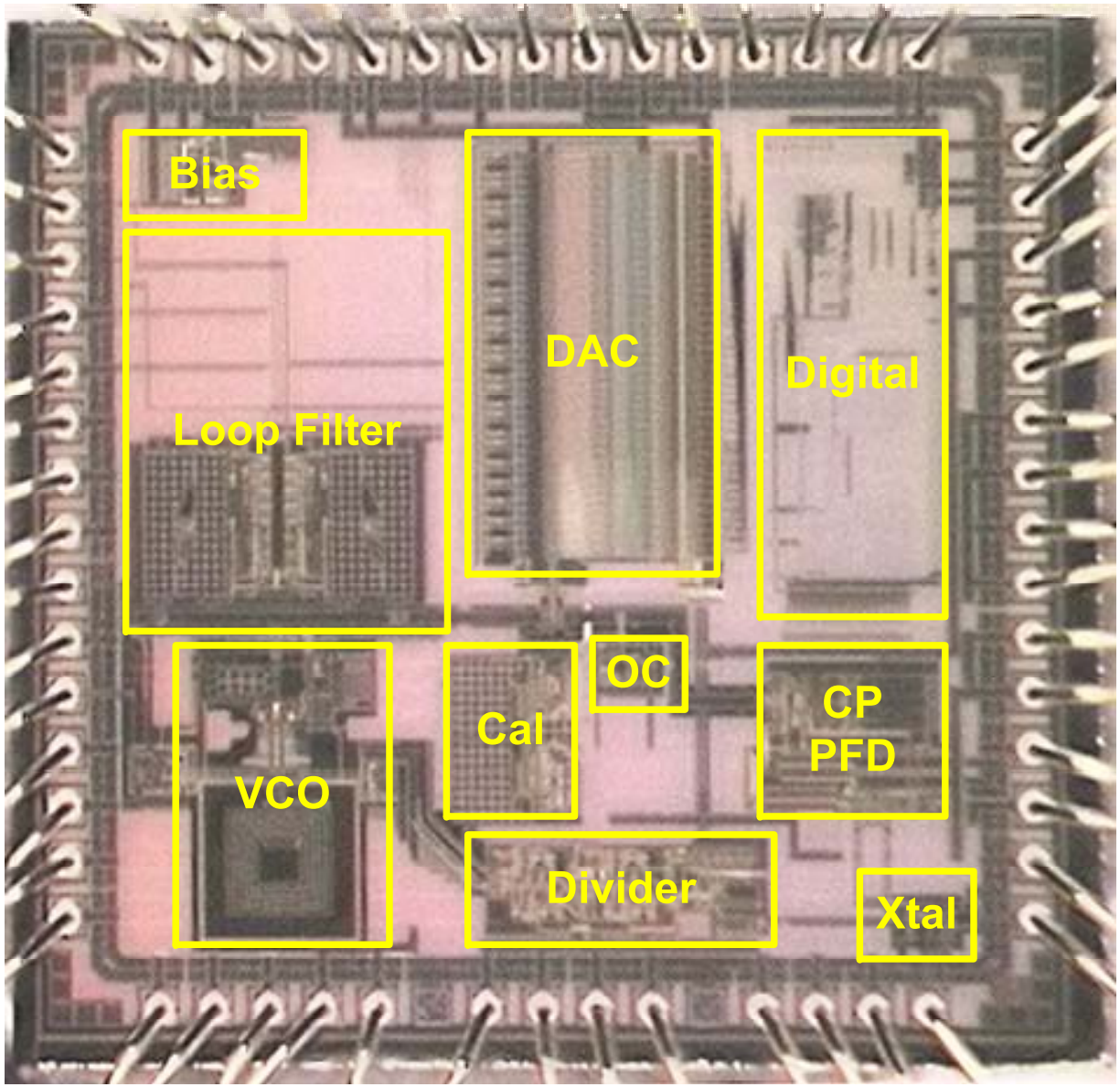


Example PLL IC 2: Performance Table

Design Details		
Technology	0.18 um 1P6M CMOS	
Package and die area	32 pin TQFN, 2.2 × 2.2 mm^2	
Reference frequency, output frequency band	12 MHz, 2.4 – 2.5 GHz	
Measured loop bandwidth	975 kHz	
Measured Current Consumption (V_{DD} = 1.8V)		
VCO and divider buffer	5.9 mA	Core 27.1 mA
Divider	7.3 mA	
Charge pump, PFD, and buffers	8.6 mA	
Offset current pulse generator	0.6 mA	
Digital	1.9 mA	
DAC	2.8 mA	
Bandgap ref, crystal buffer, external buffer	9.8 mA	
Measured Fractional-N Performance		
Phase noise at 100 kHz	-98 dBc/Hz	
Phase noise at 3 MHz	-121 dBc/Hz	
Worst case inband fractional spur†	-64 dBc	
Worst case reference spur	-70 dBc	

†Over 4 IC copies each measured with 100 values of $0 < \alpha < 1$

Example PLL IC 2:Die Photograph



Conclusion

Have Discussed:

- Integer-*N* PLL Limitations
- The Idea Behind Fractional-*N* PLLs
- Delta-Sigma Modulation Overview
- Fractional-*N* PLL Dynamics
- Spurious Tones in Fractional-*N* PLLs
- Fractional-*N* PLL Bandwidth Enhancement

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