T2
Pipelined A/D Converters: The Basics

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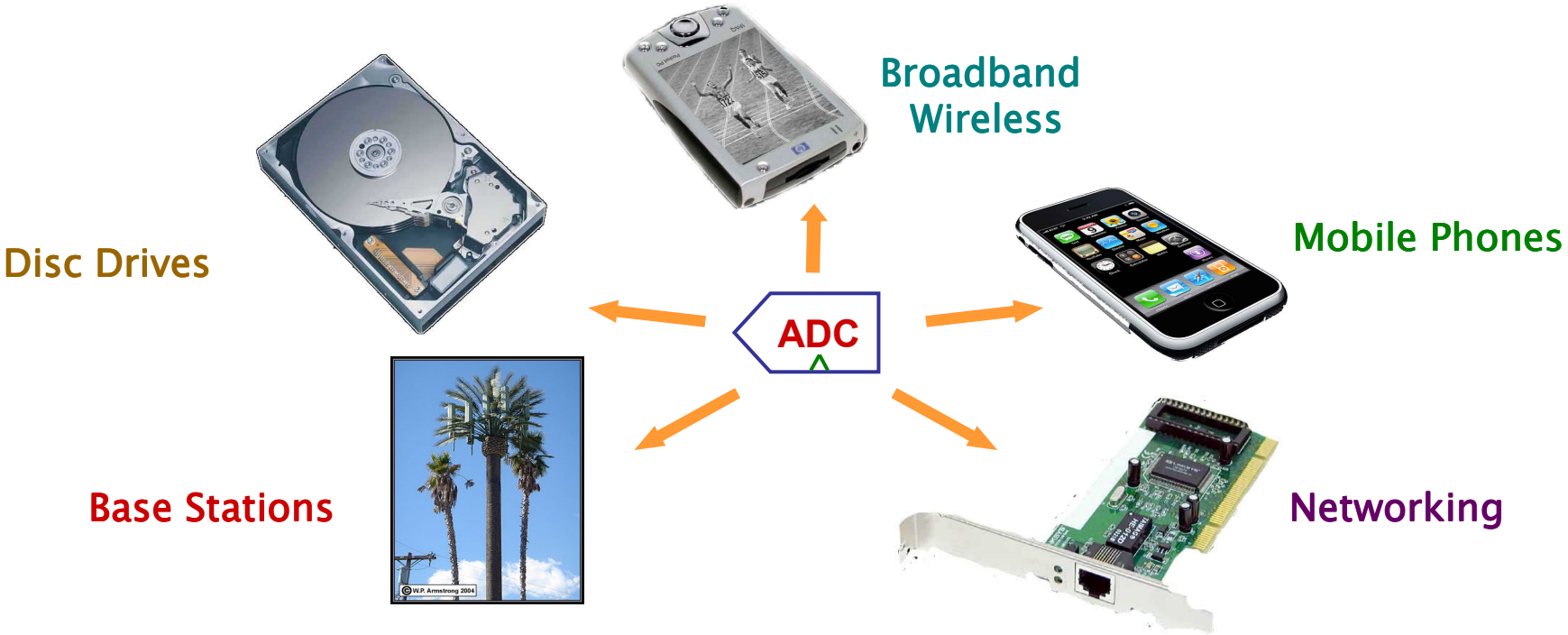
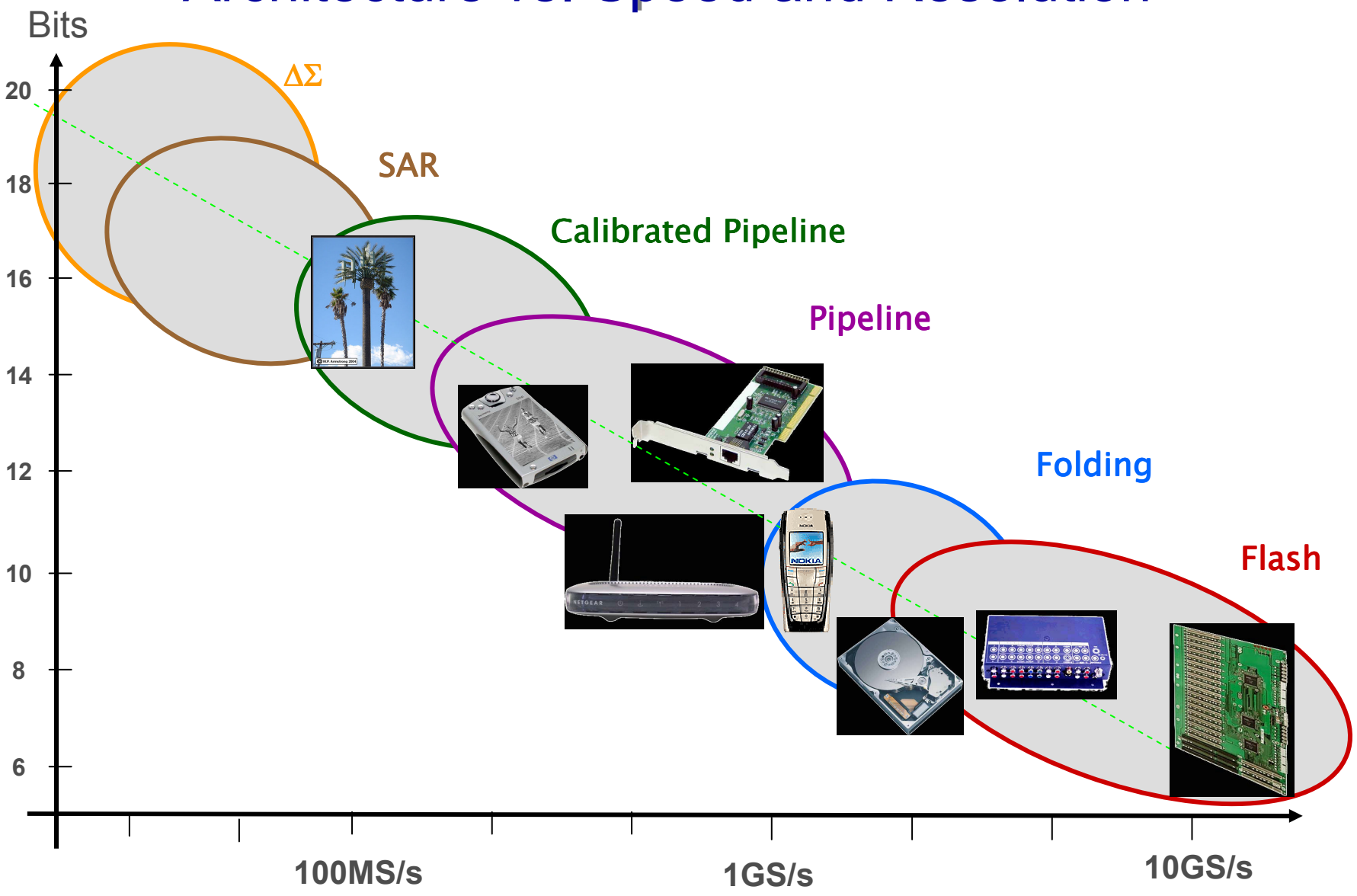
Sunday 03 Feb 2008

Applications: ADC Performance is Critical

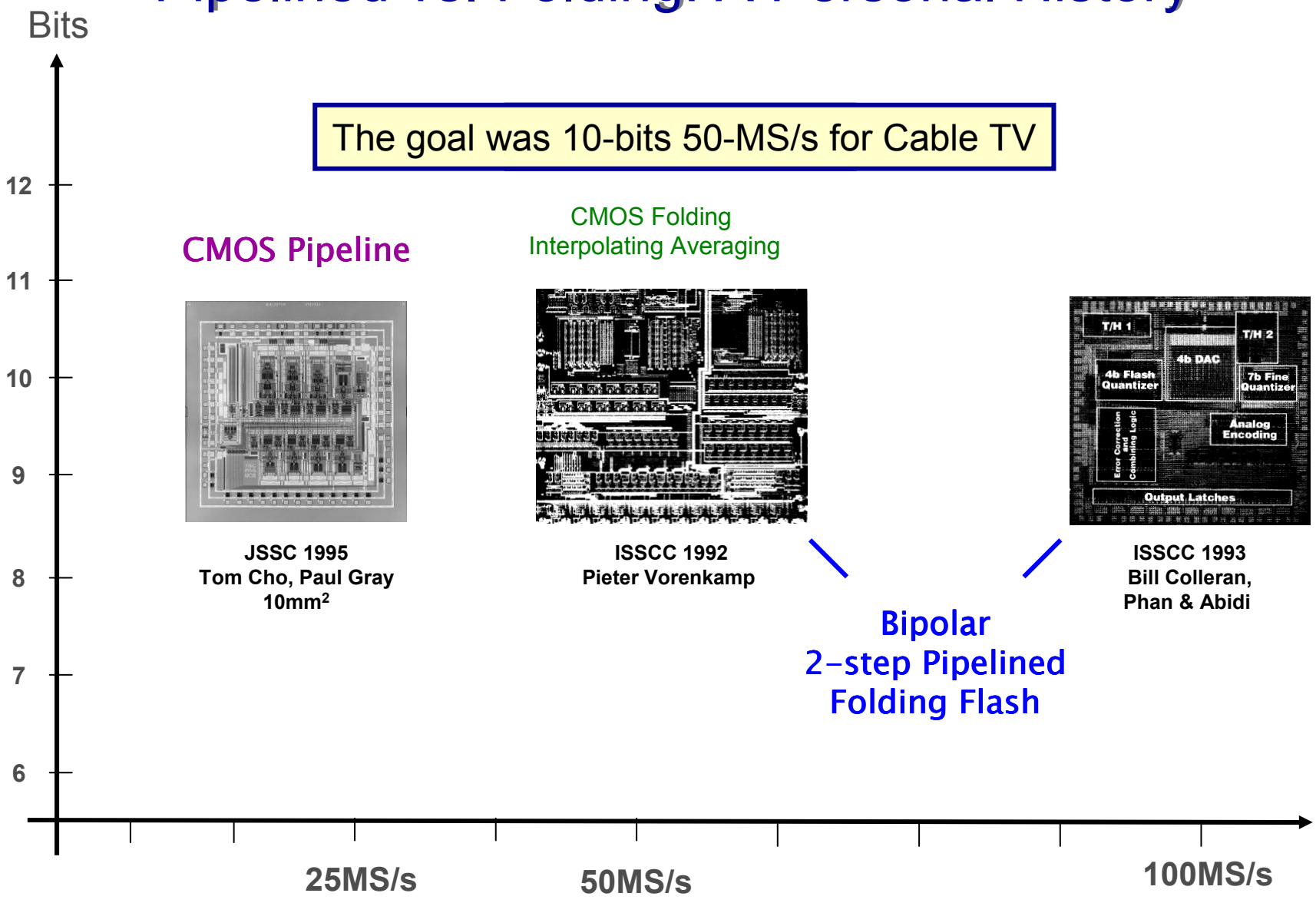
- Dramatic improvement in converter performance is required for emerging IEEE communication standards
- Data converters will be a key enabling technology to realize ICs at the appropriate power



Architecture vs. Speed and Resolution



Pipelined vs. Folding: A Personal History



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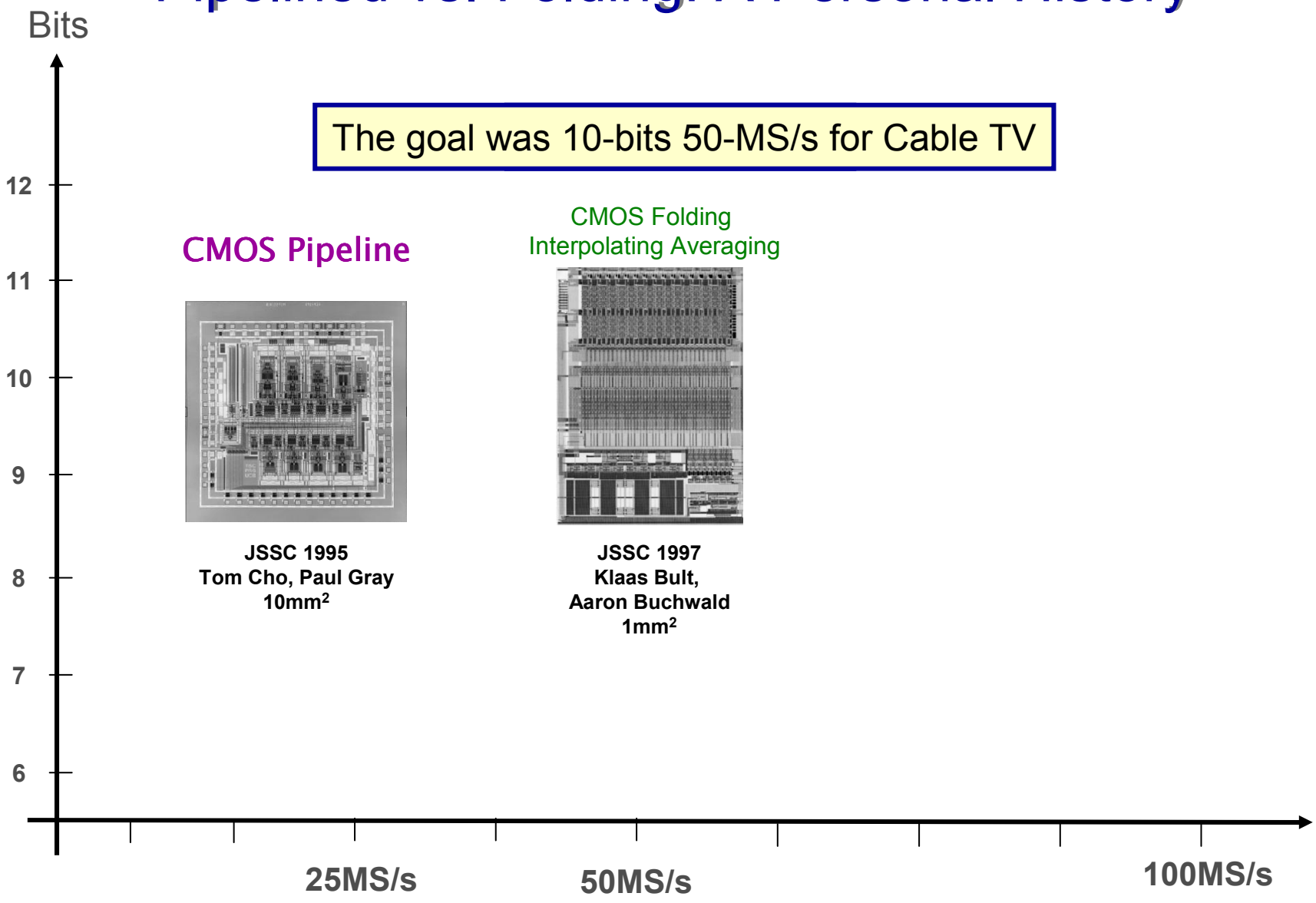
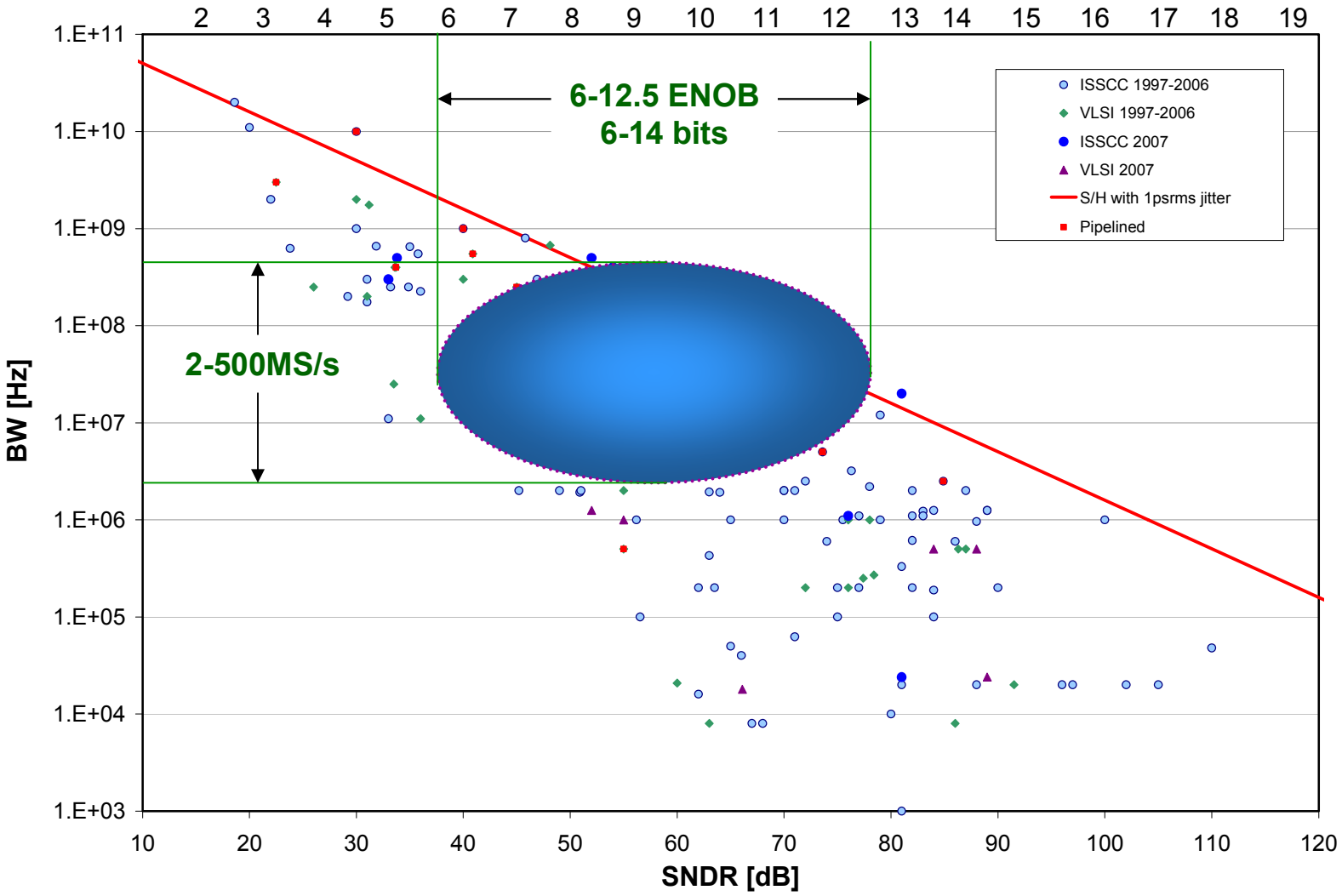
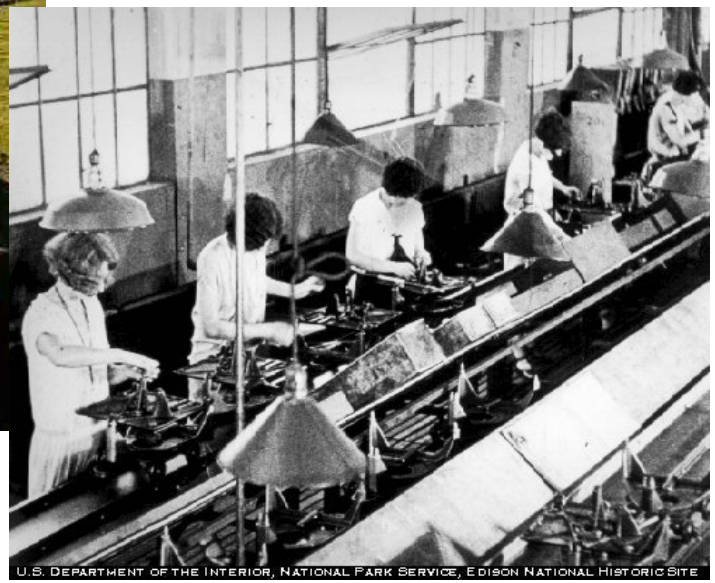


Pipelined ADCs Speed and Resolution



B. Murmann, "ADC Performance Survey 1997-2007," [Online]. Available: http://www.stanford.edu/~murmann/adcsurvey.html.

What is a "Pipelined" ADC



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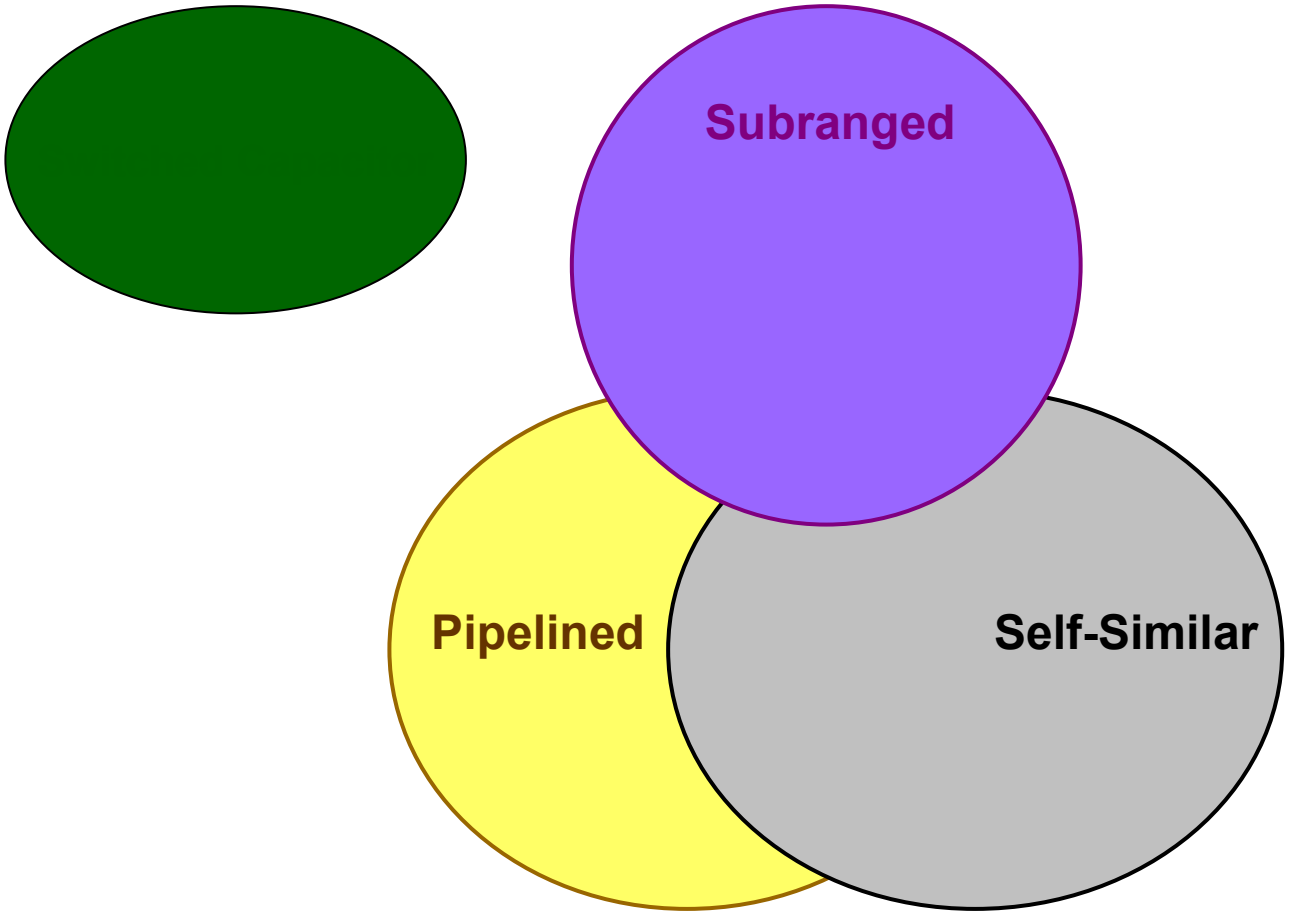
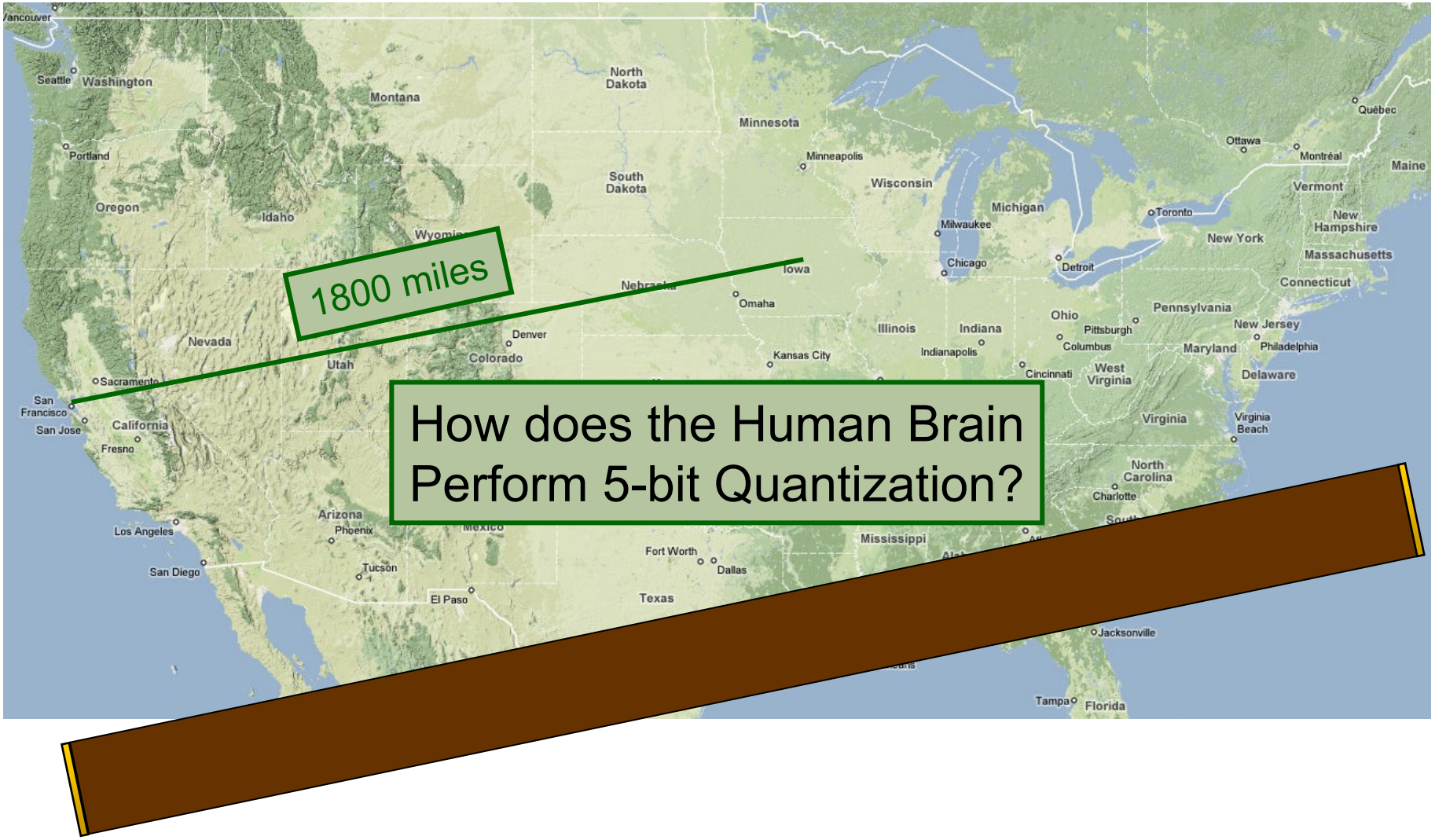


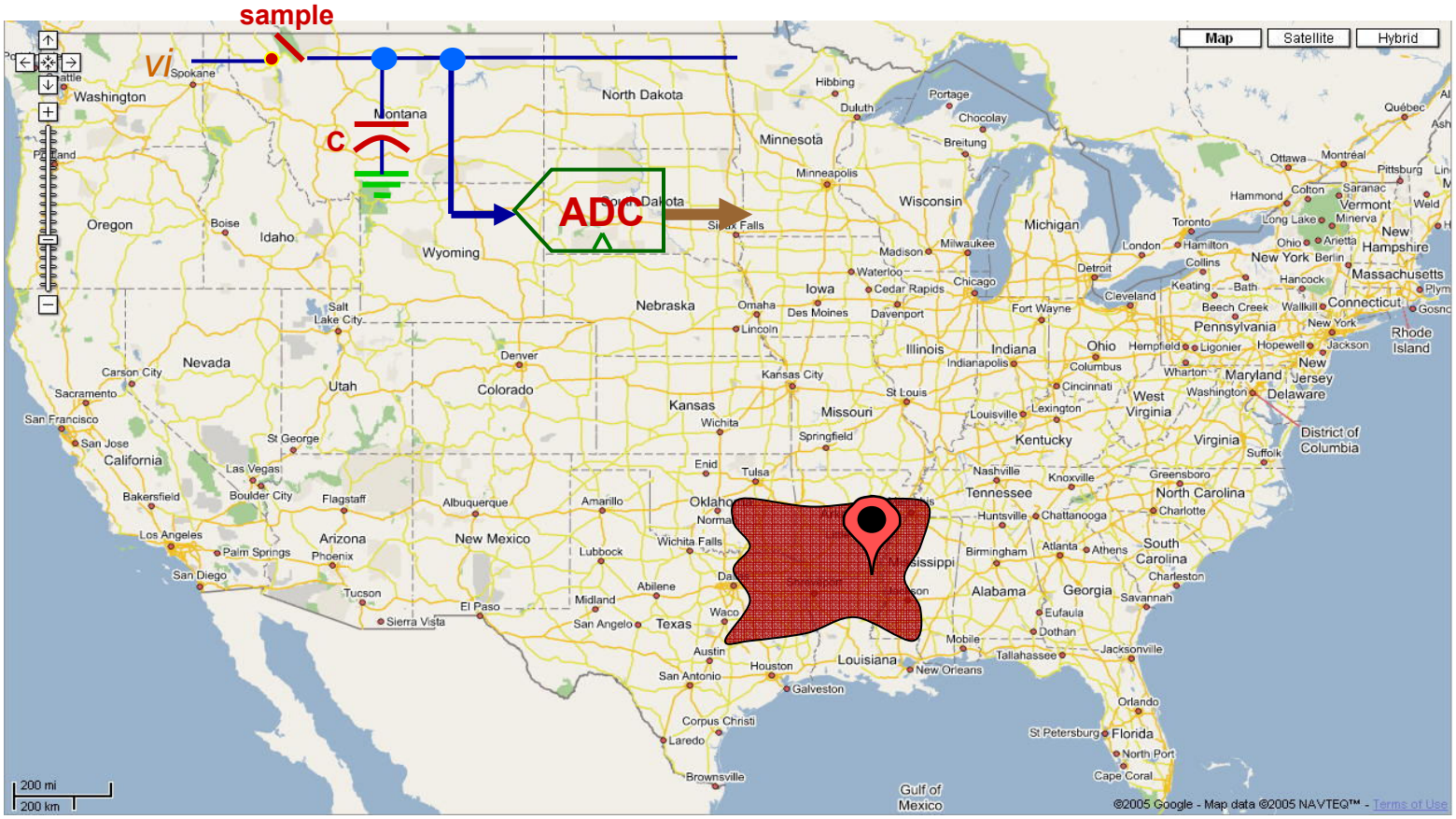
Usually
but not
necessarily

Efficient Calculation Machine Similar to Systolic Arrays – FFT Butterfly Calculation

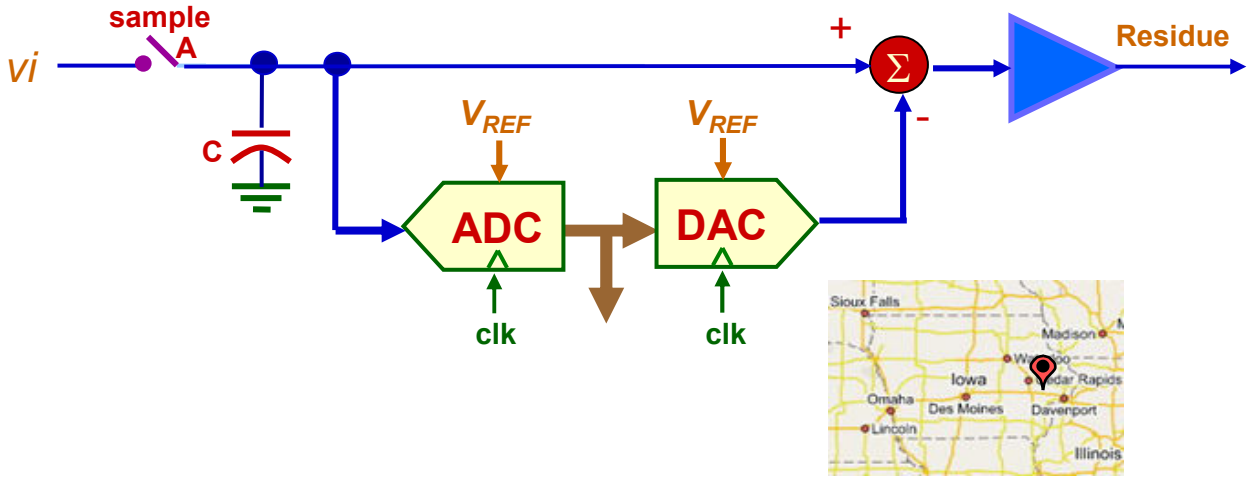
5-bit Flash: Ruler Analogy



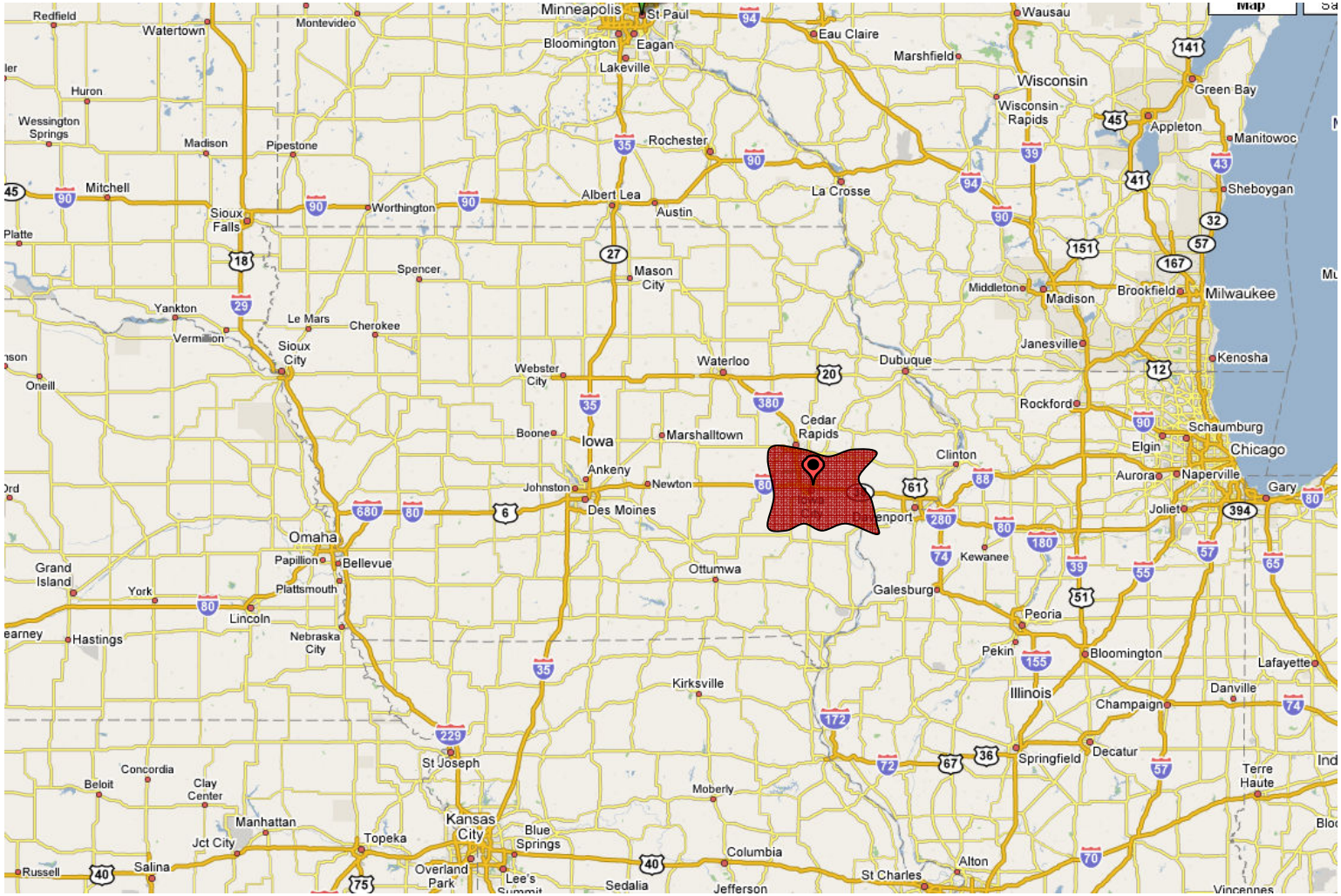
15-bit Spatial Sub-Ranging ADC



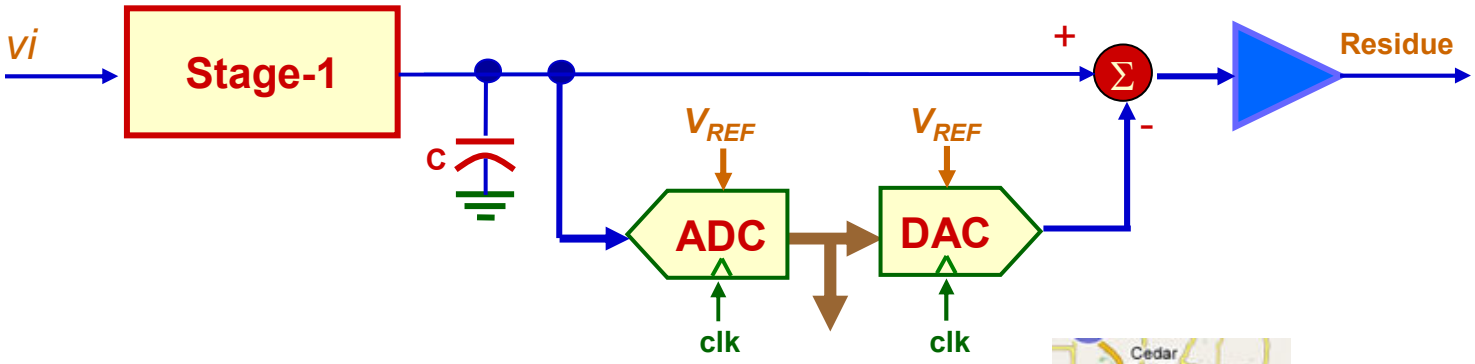
Coarse Estimate – Center - Amplify



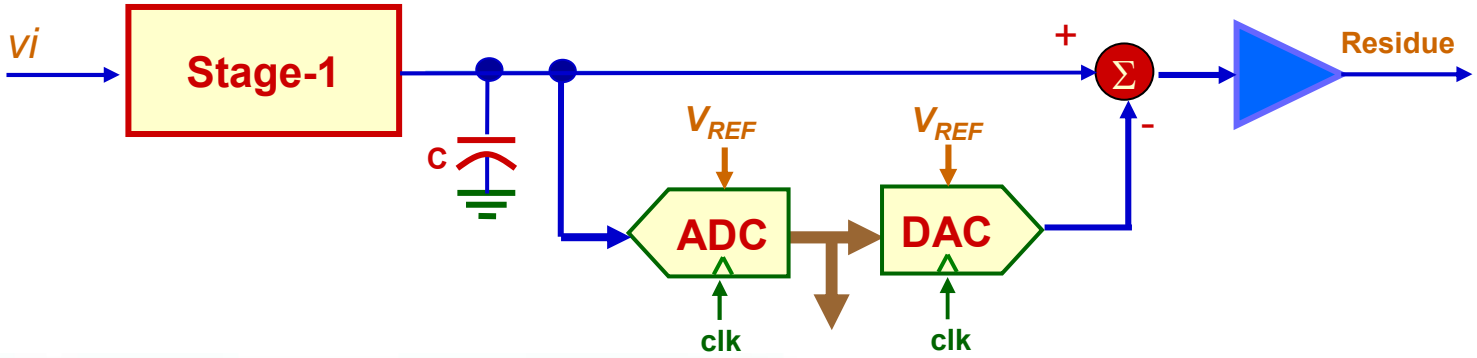
2nd-Stage Sub-range



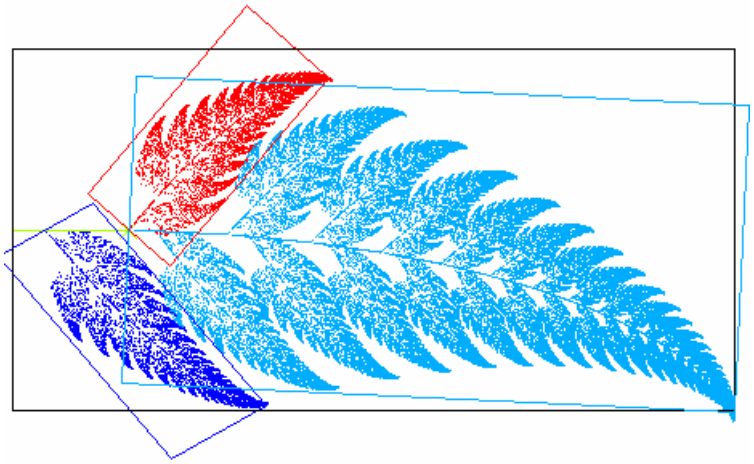
Repeat Centering and Residue Amplification



Self Similarity

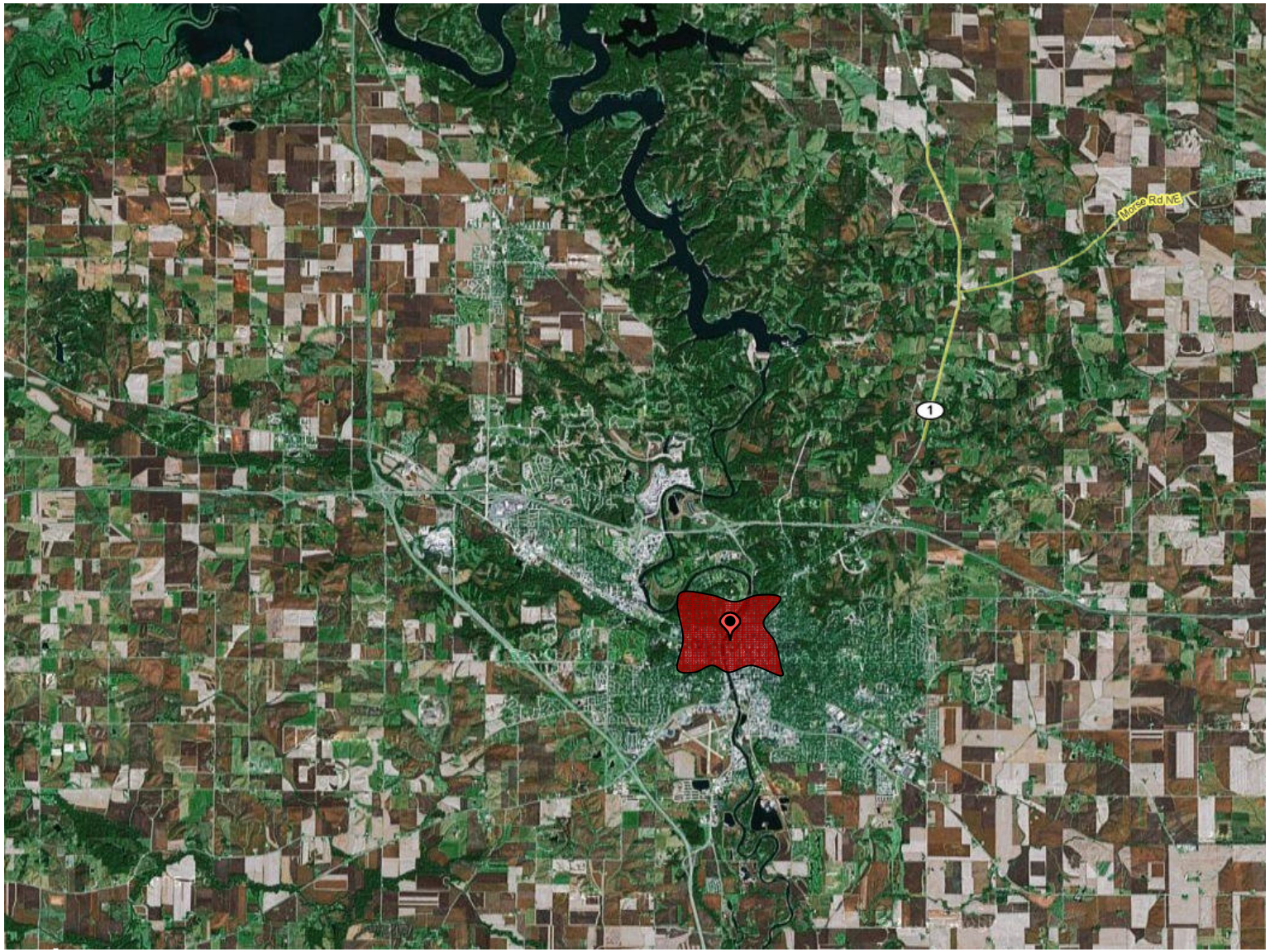


Matryoshka / Russian Nesting Dolls



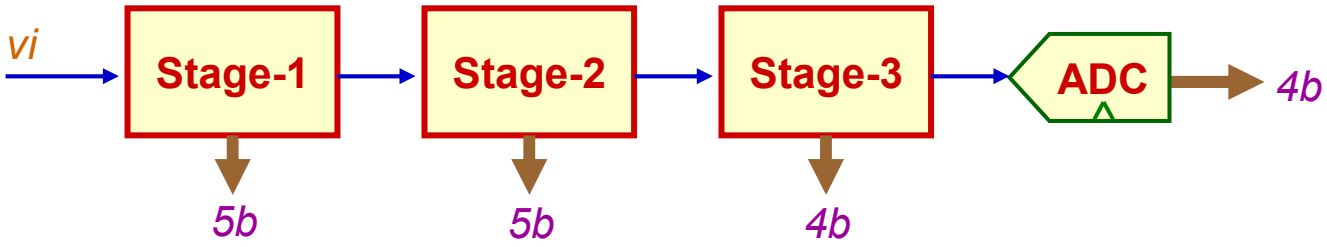
Fractal Geometry of Nature

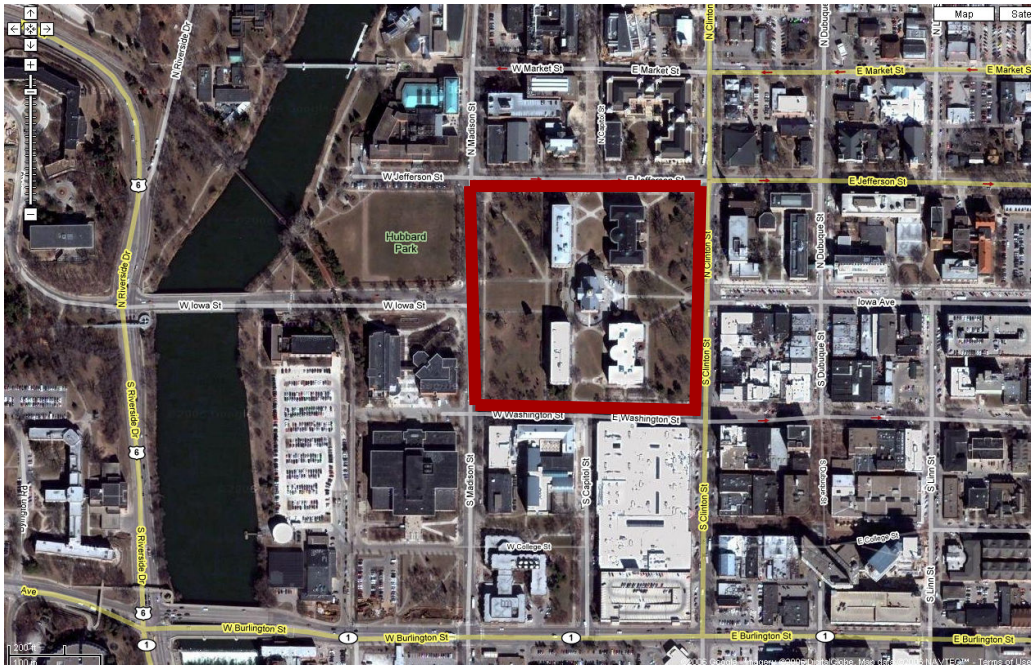
3rd-Stage Sub-range



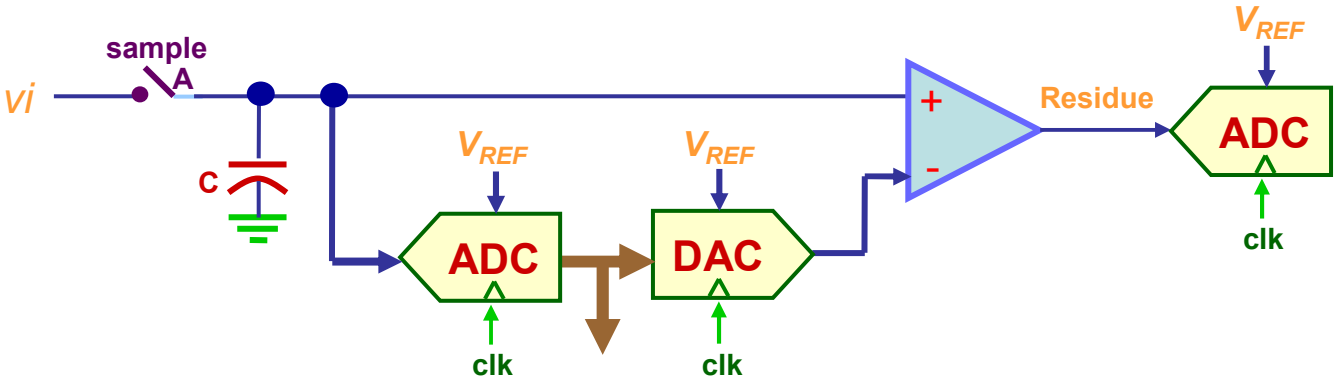
4th Stage - Features Large Enough to Quantize

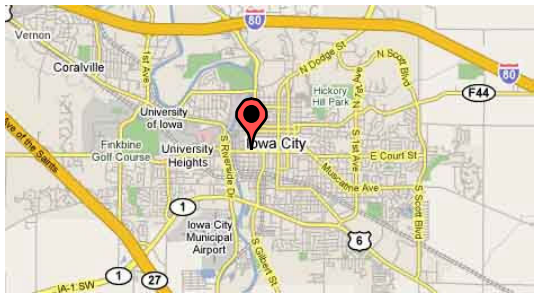
4-Stage 15-bit Pipeline ADC

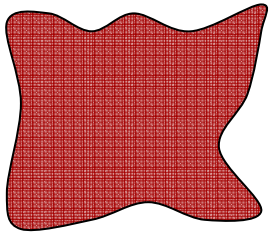




Challenges in Pipeline ADCs: Offsets & DAC

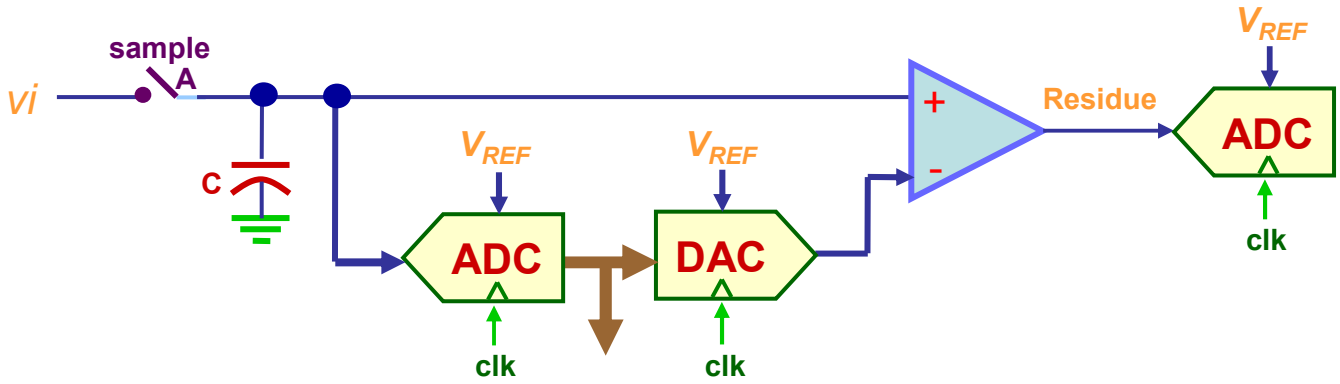


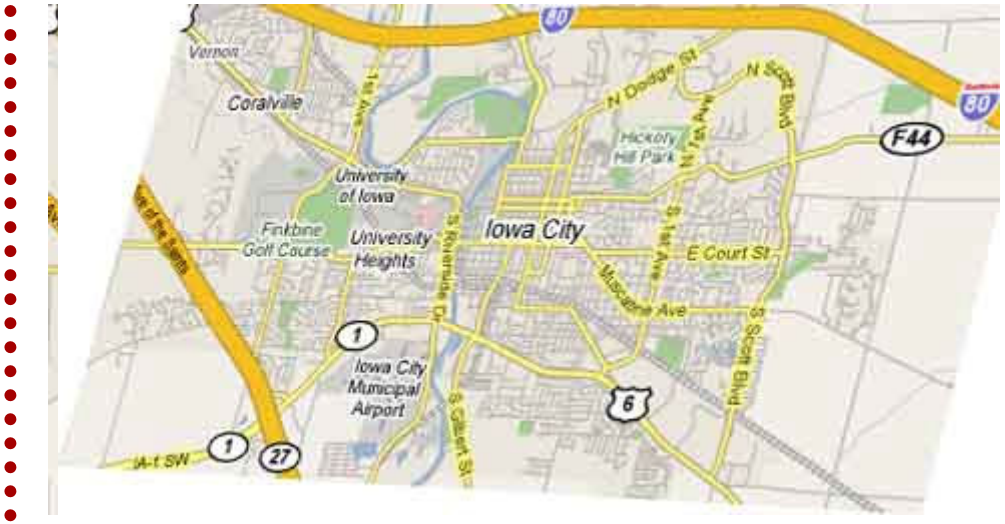




Limitations in accuracy due to
Comparator Offsets & Non-Linearity in DAC

Challenges in Pipeline ADCs: Gain and Non-linearity



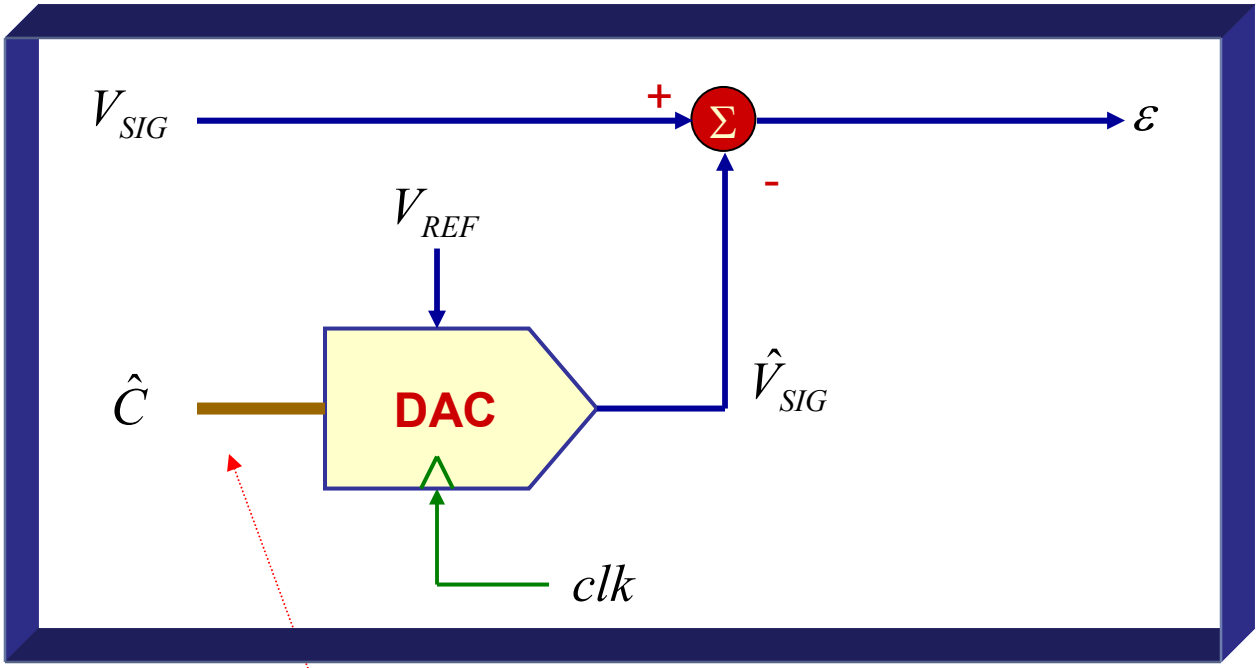


Limitations in accuracy due to gain errors and amplifier non-linearity

ADC = DAC + Comparison

Successive Approximation & Relationship to Pipelined ADCs

Signal vs. DAC Comparison: Inverse Transfer Function



Approximation Error

$$\varepsilon = V_{SIG} - \hat{C}V_{REF}$$

Digital Output Code

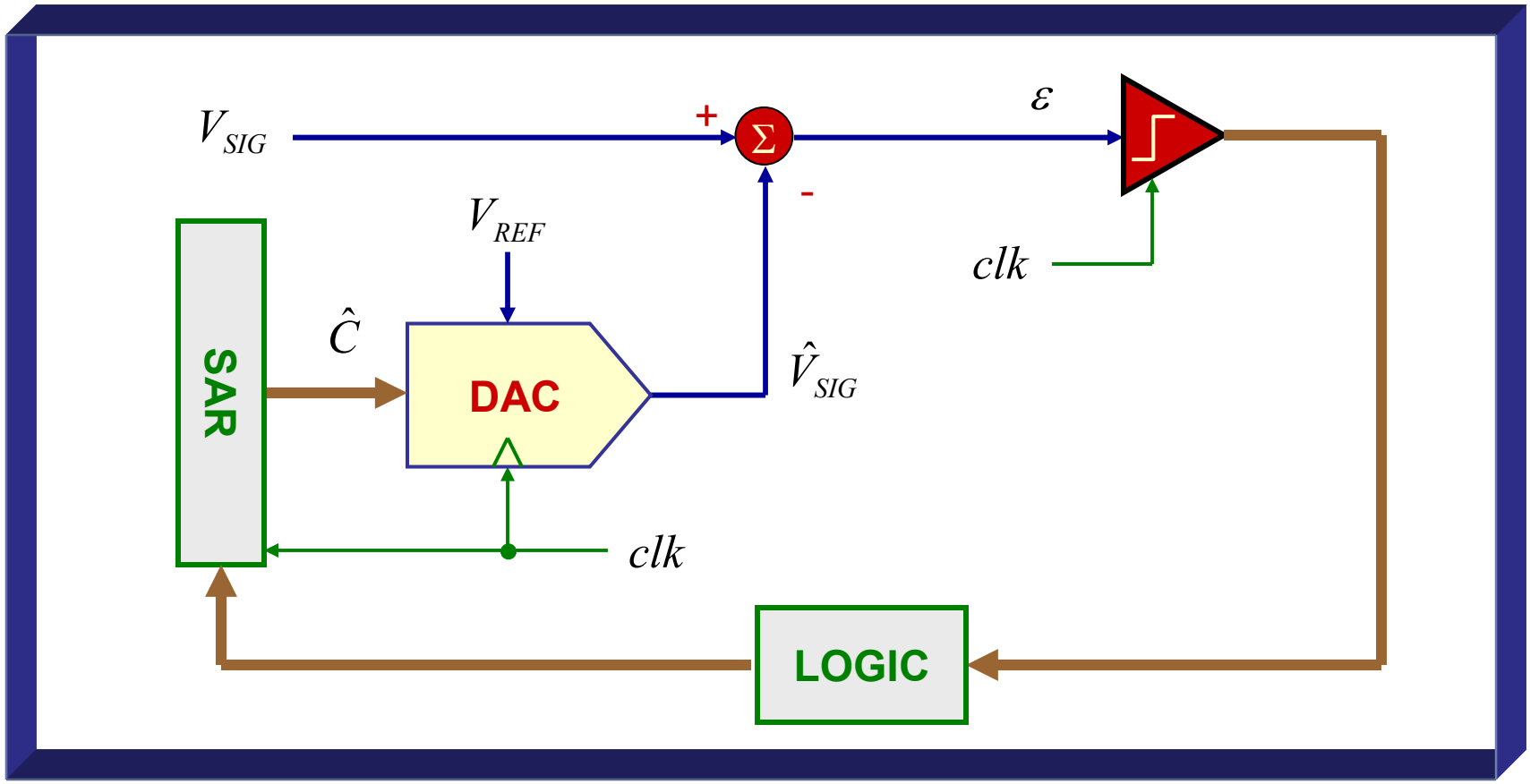
$$\text{for } \varepsilon \cong 0$$

$$\hat{C} = \text{Digital Code}$$

DAC Limits Accuracy

- Drive DAC to minimize error
- ADC accuracy depends on DAC

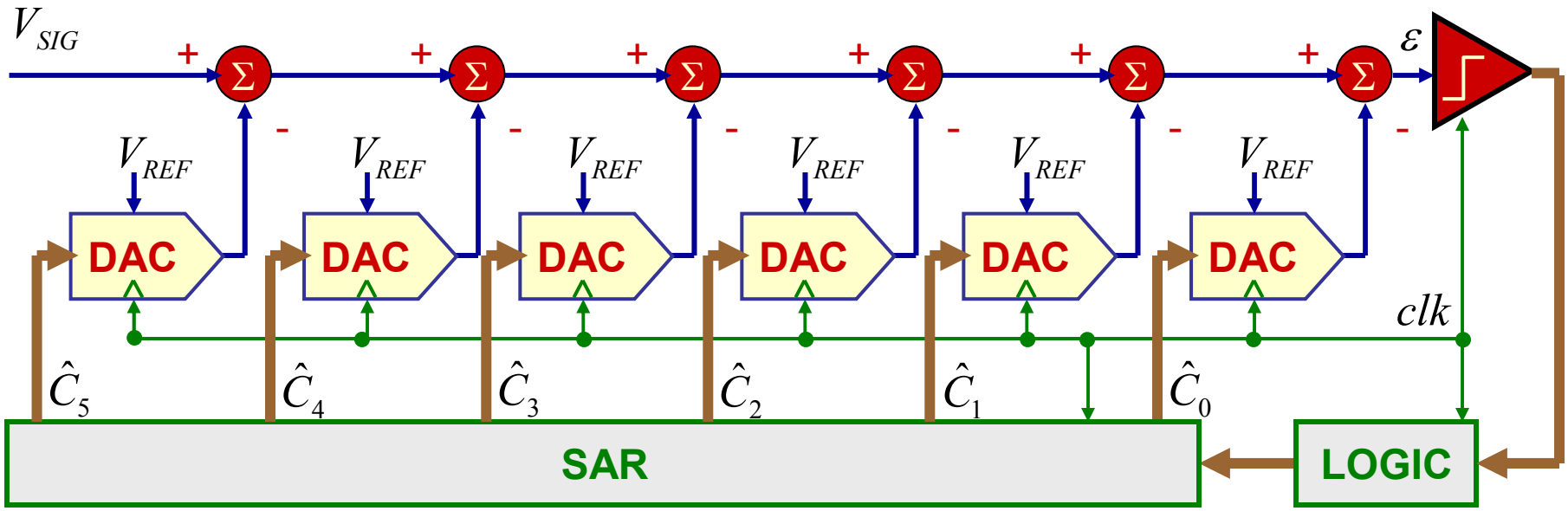
Successive Approximation ADC (SAR)



Use Feedback to Drive Error to Zero

- Successive Approximation
- Iteratively change DAC code until error is minimized

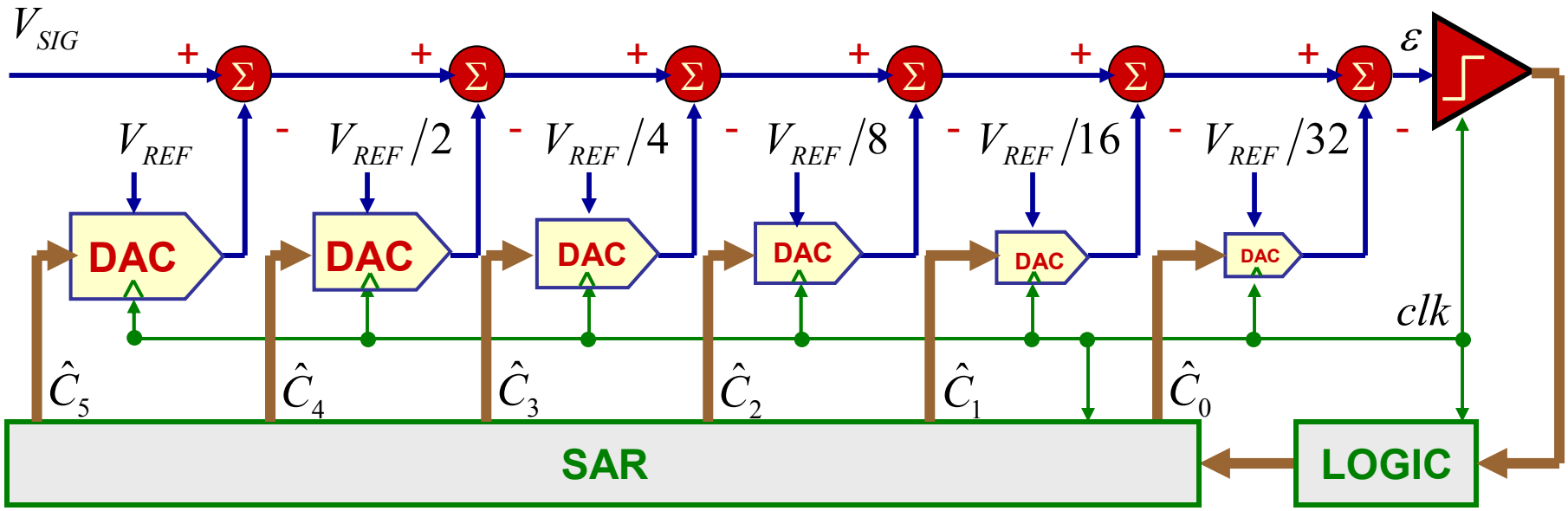
ADC Basics: DAC Successive Approximation



DACs are identical

- Error contribution from each DAC affects performance equally
- Full precision required at each node

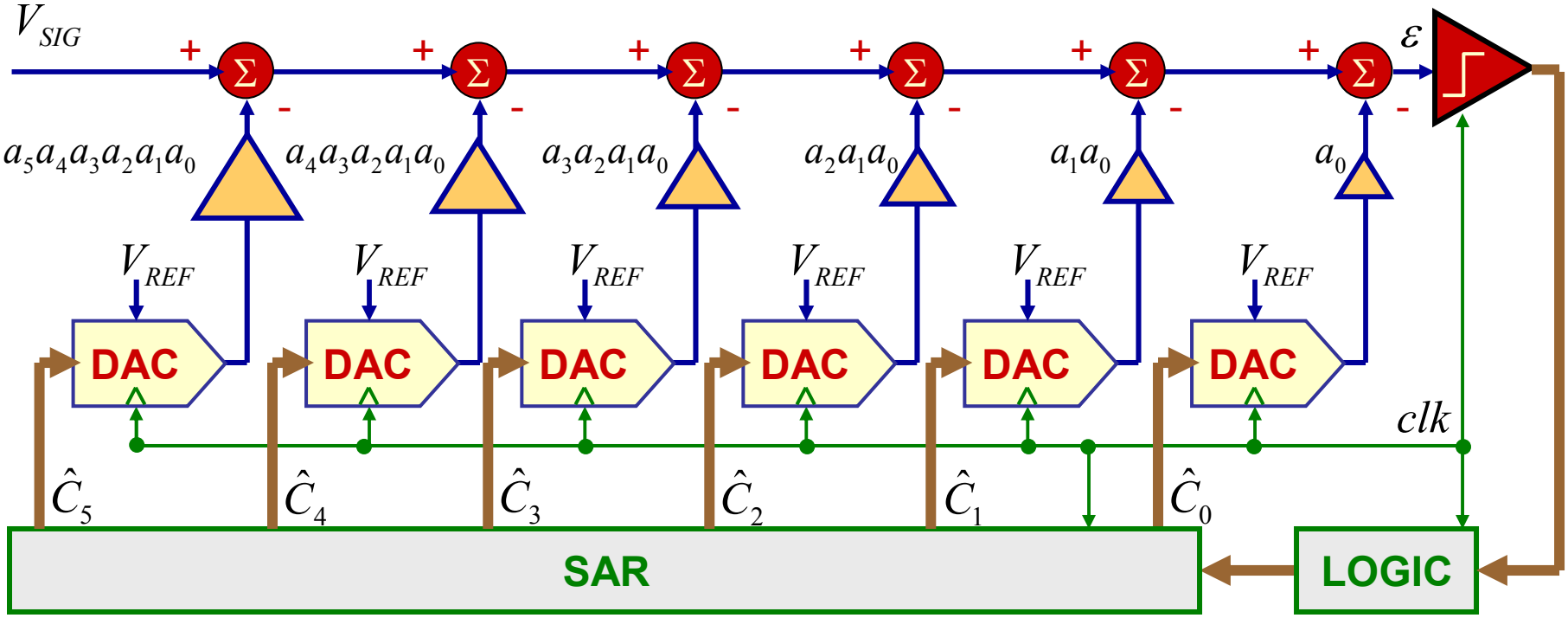
ADC Basics: DAC Binary Weighting



DACs are Binary Weighted

- Error contribution from DAC mismatch is scaled by reference
- MSB DACs must have better matching than LSB DACs

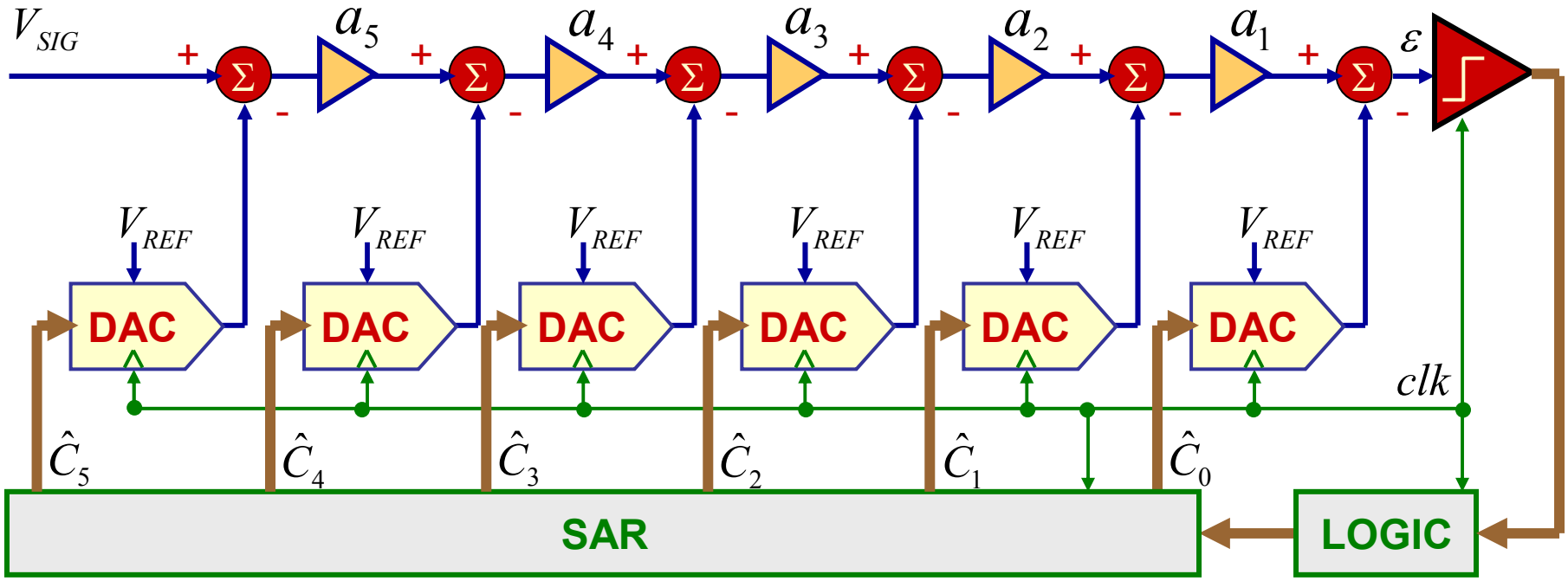
Binary Weighting Using Gain Blocks



DACs are identical, but see different gain to output

- Error contribution from each DAC is proportional to gain in signal path
- MSB DAC is most critical

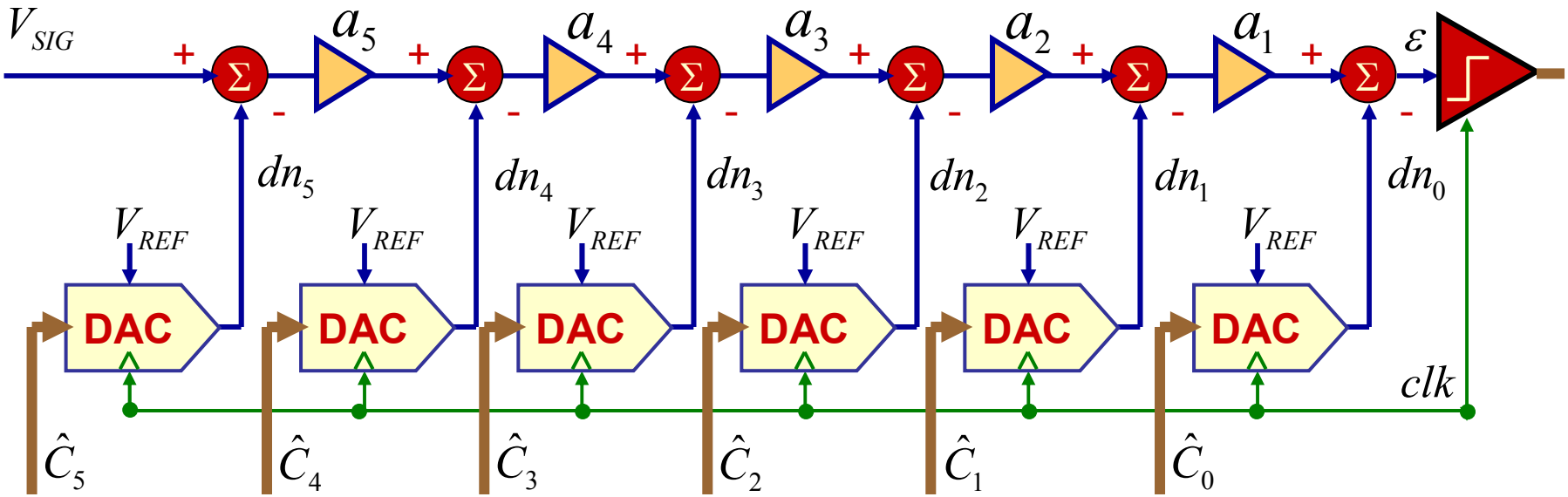
Binary Weighting with Distributed Gain (a_0=1)



DACs are identical: Gain is Distributed

- MSB DAC most critical because it sees largest gain
- Feed-forward path is now modular. All sections are identical

Dominant Error Sources

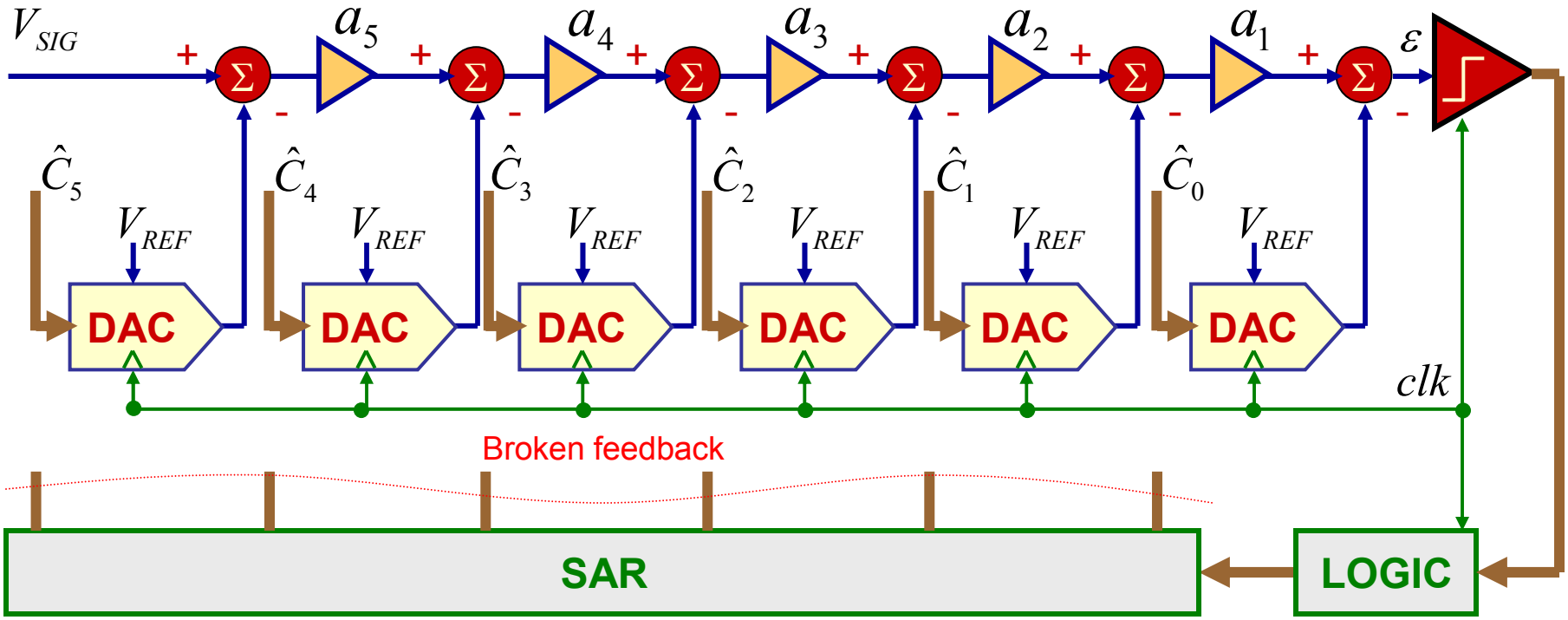


$$d_{IN} = dn_5 + \frac{dn_4}{a_5} + \frac{dn_3}{a_5 a_4} + \frac{dn_2}{a_5 a_4 a_3} + \frac{dn_1}{a_5 a_4 a_3 a_2} + \frac{dn_0}{a_5 a_4 a_3 a_2 a_1}$$

Noise Summary

- The larger the gain at the input less the impact of noise in distortion from subsequent stages
- Dominant Noise Term is from input stage

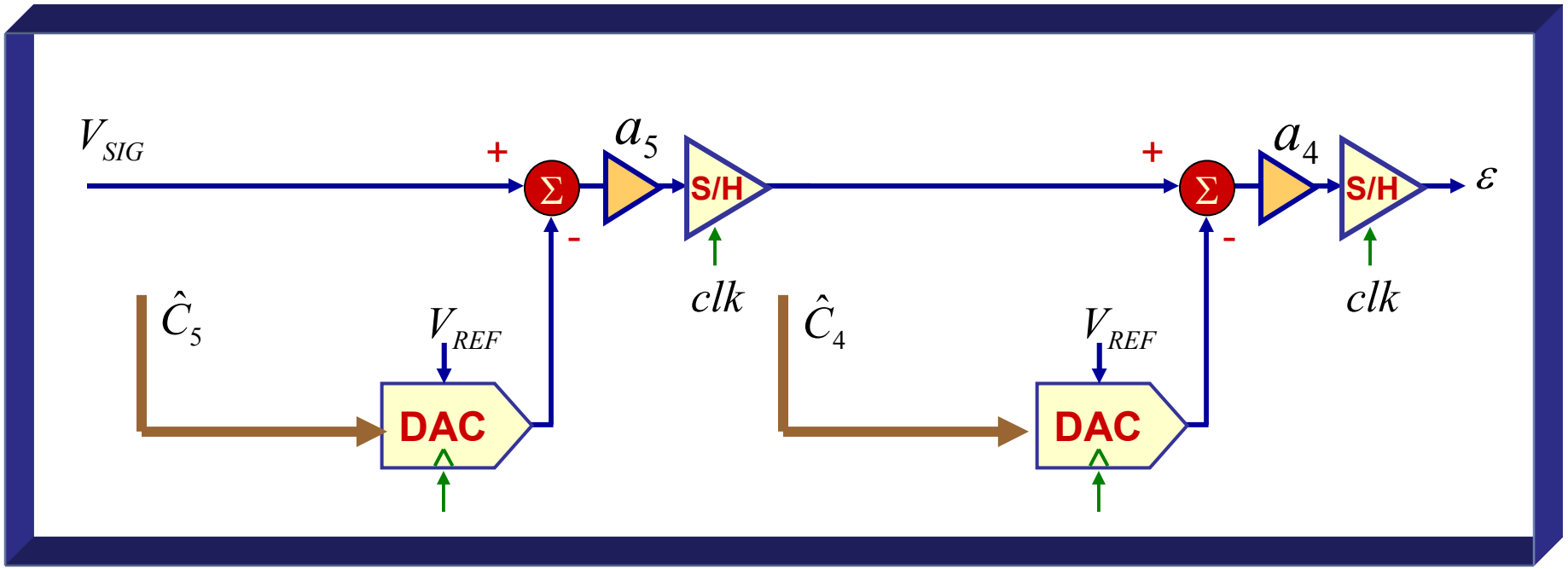
Transition from Feedback-Based to Pipeline



Feedback not allowed for pipeline design

- Can not afford to wait for signal to propagate down the chain
- Coefficients must be set by Feed-forward path
- Error Sources and Expression of Analog Output of DACs do not change
- Problem is now is to set Coefficients without overflow of internal nodes

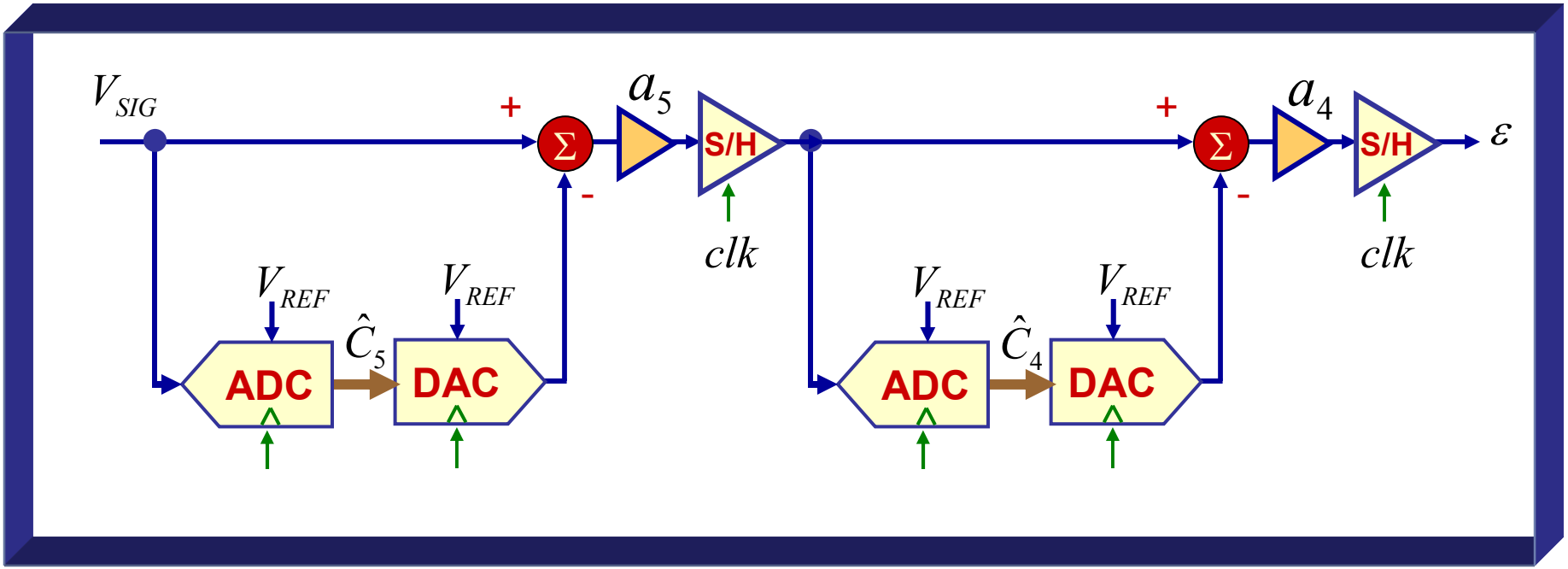
Adding Analog Delay Allows Pipeline



Sample and Hold as an Analog Delay

- With analog memory each section works on a single residue
- Latency increases, but throughput is high with one complete conversion per clock cycle

ADCs in Feed-Forward Path Replace Feedback

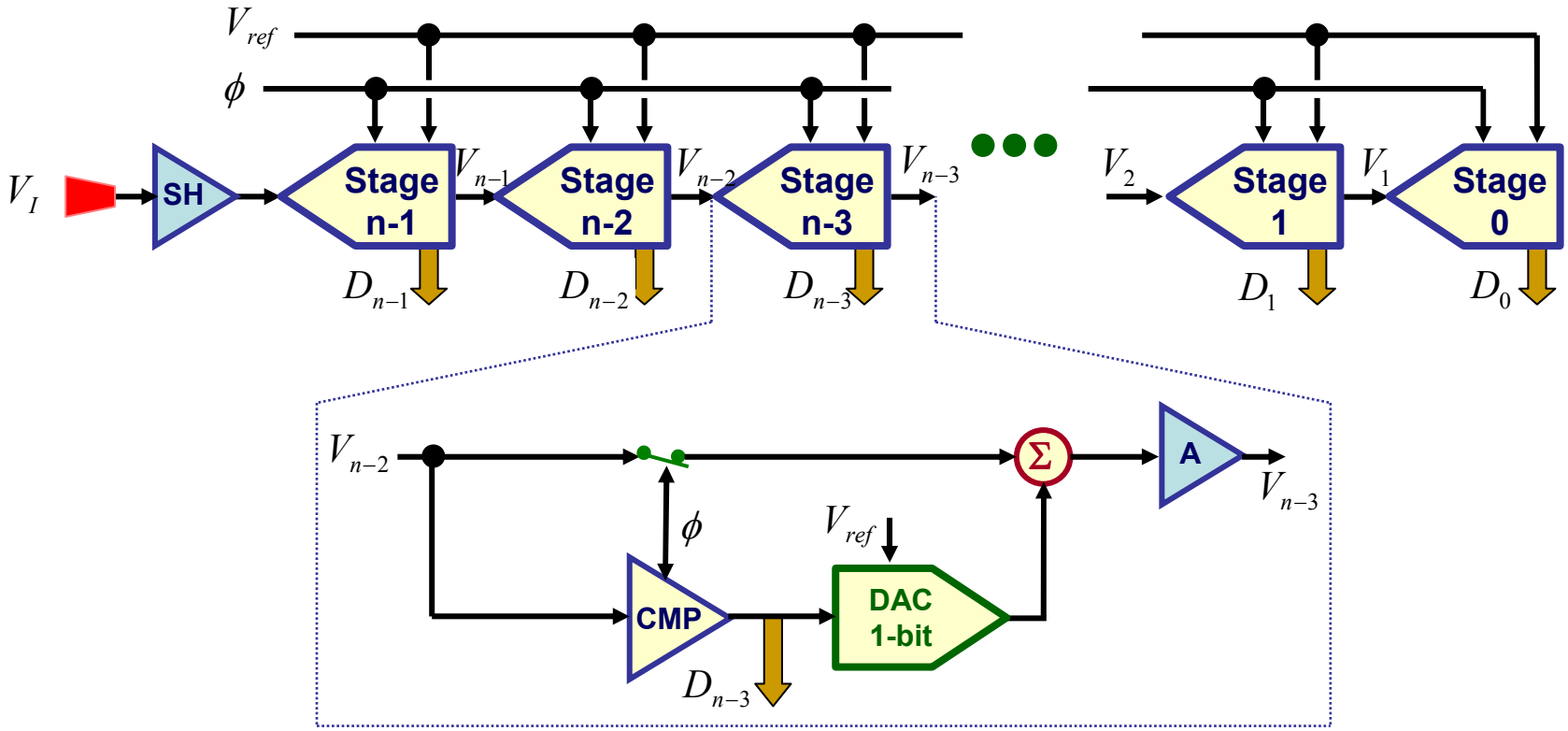


Final result does NOT depend on feed-forward ADCs

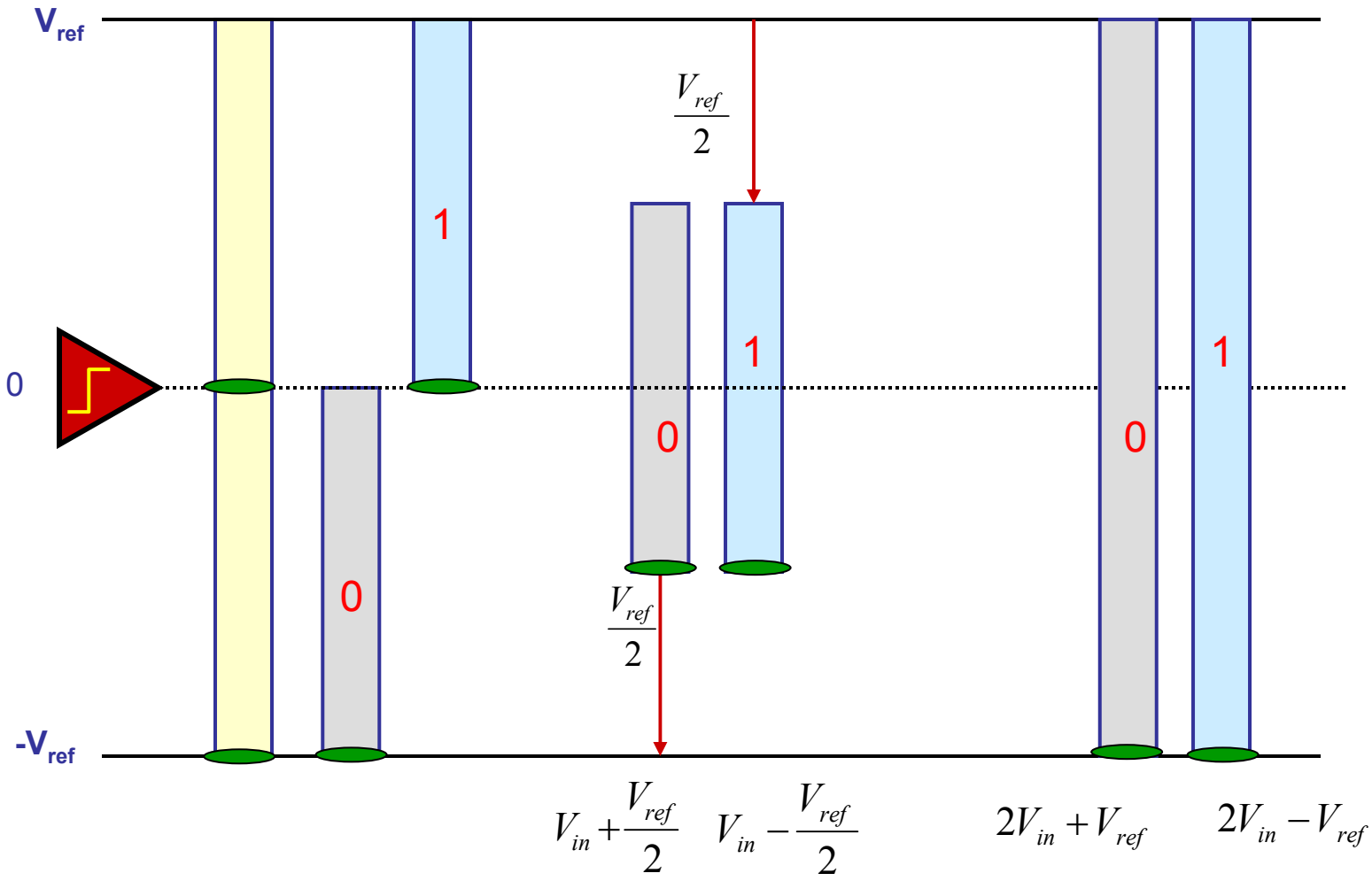
- Provided error "e" is minimized, accuracy is identical to SAR-based ADC
- Coarse ADC job is to get "close" and avoid overflow at intermediate nodes

Simple 1-bit-per-stage Pipelined ADC

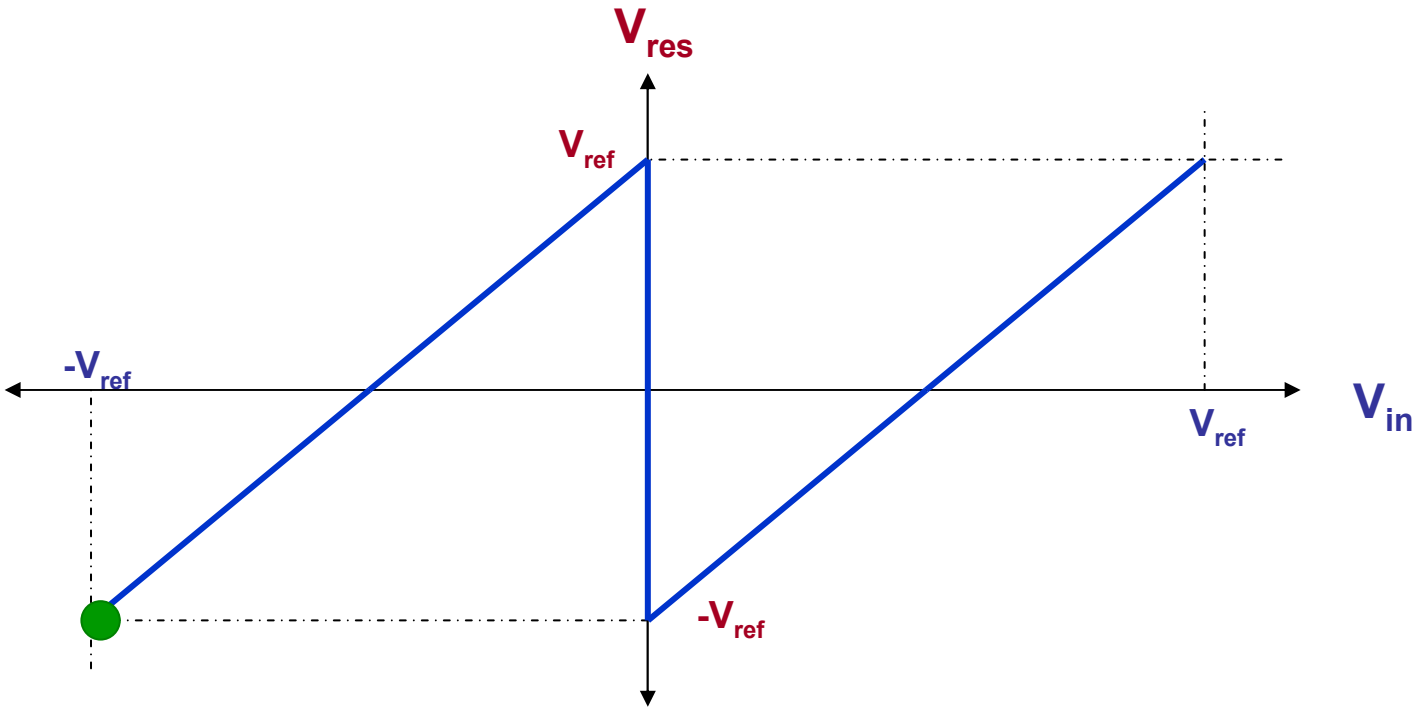
Simple Radix-2 Pipelined ADC



Voltage Sub-Ranges: No Overlap



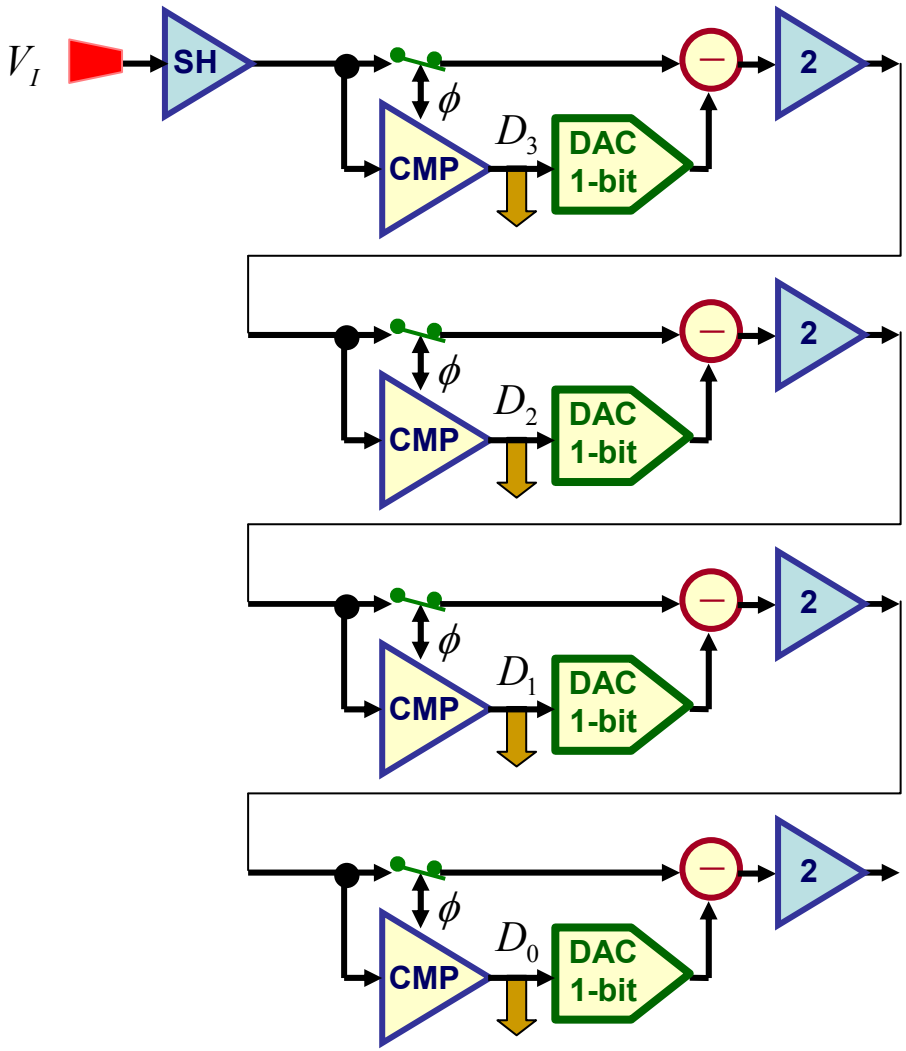
Residue Plot: Input to Residue Transfer Function



No margin in Coarse ADC

- Offset of coarse ADC must be at full accuracy
- No over-range margin in amplitude

Radix-2 Pipelined ADC: Residue Voltages



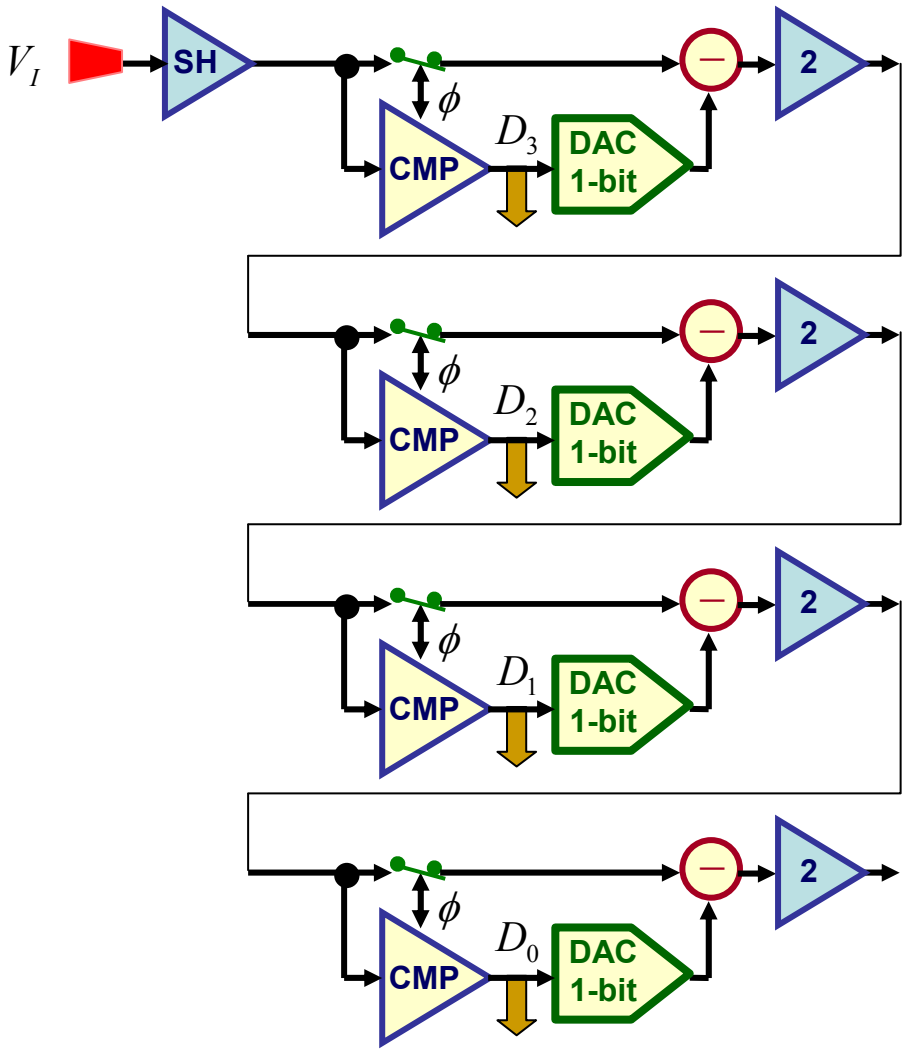
$$V_3 = 2\left[V_{IN} - D_3 V_{ref}\right]$$

$$V_2 = 2\left[2\left[V_{IN} - D_3 V_{ref}\right] - D_2 V_{ref}\right]$$

$$V_1 = 2\left[2\left[2\left[V_{IN} - D_3 V_{ref}\right] - D_2 V_{ref}\right] - D_1 V_{ref}\right]$$

$$V_0 = 2\left[2\left[2\left[2\left[V_{IN} - D_3 V_{ref}\right] - D_2 V_{ref}\right] - D_1 V_{ref}\right] - D_0 V_{ref}\right]$$

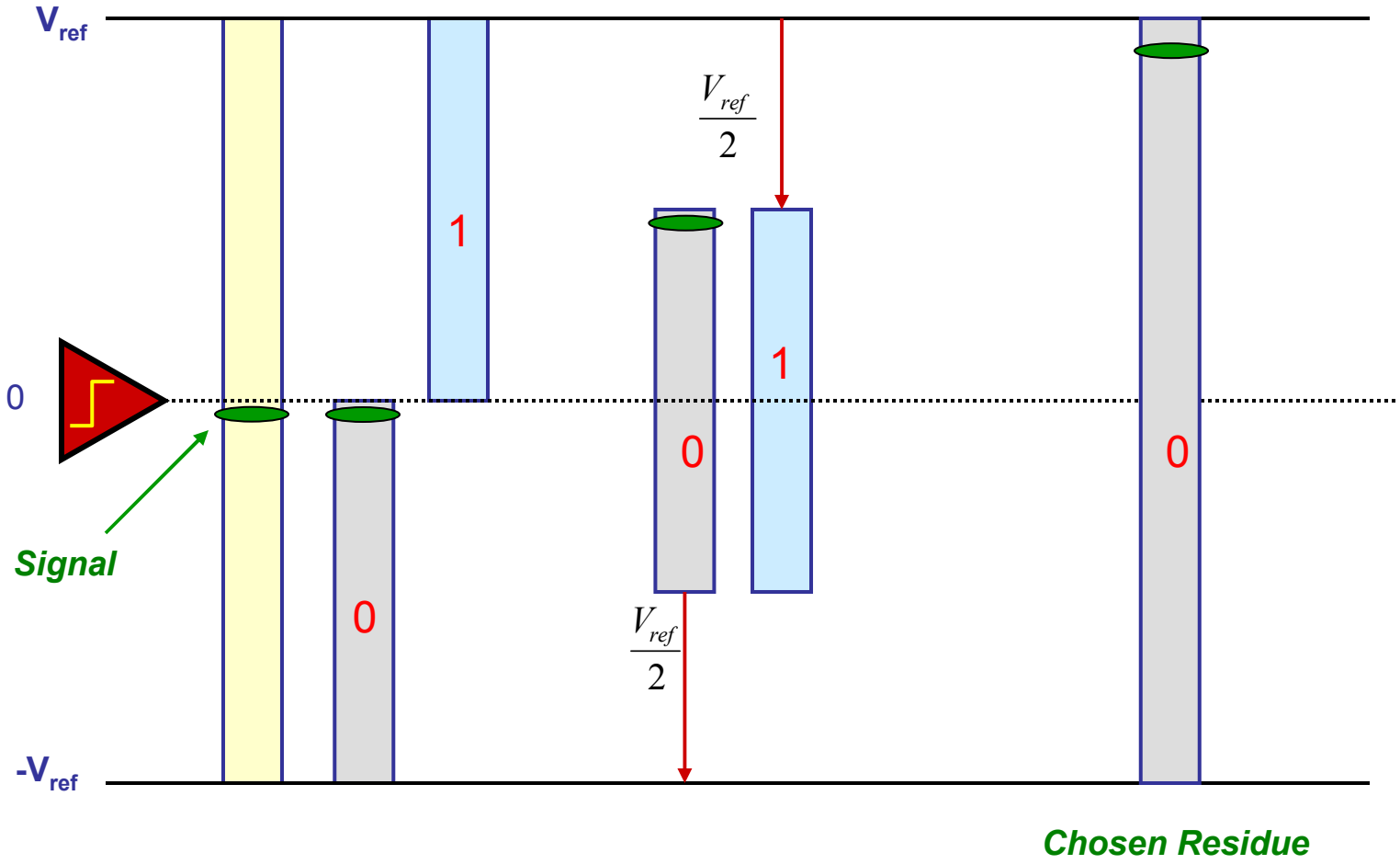
Slice Architecture: Pipelined ADC



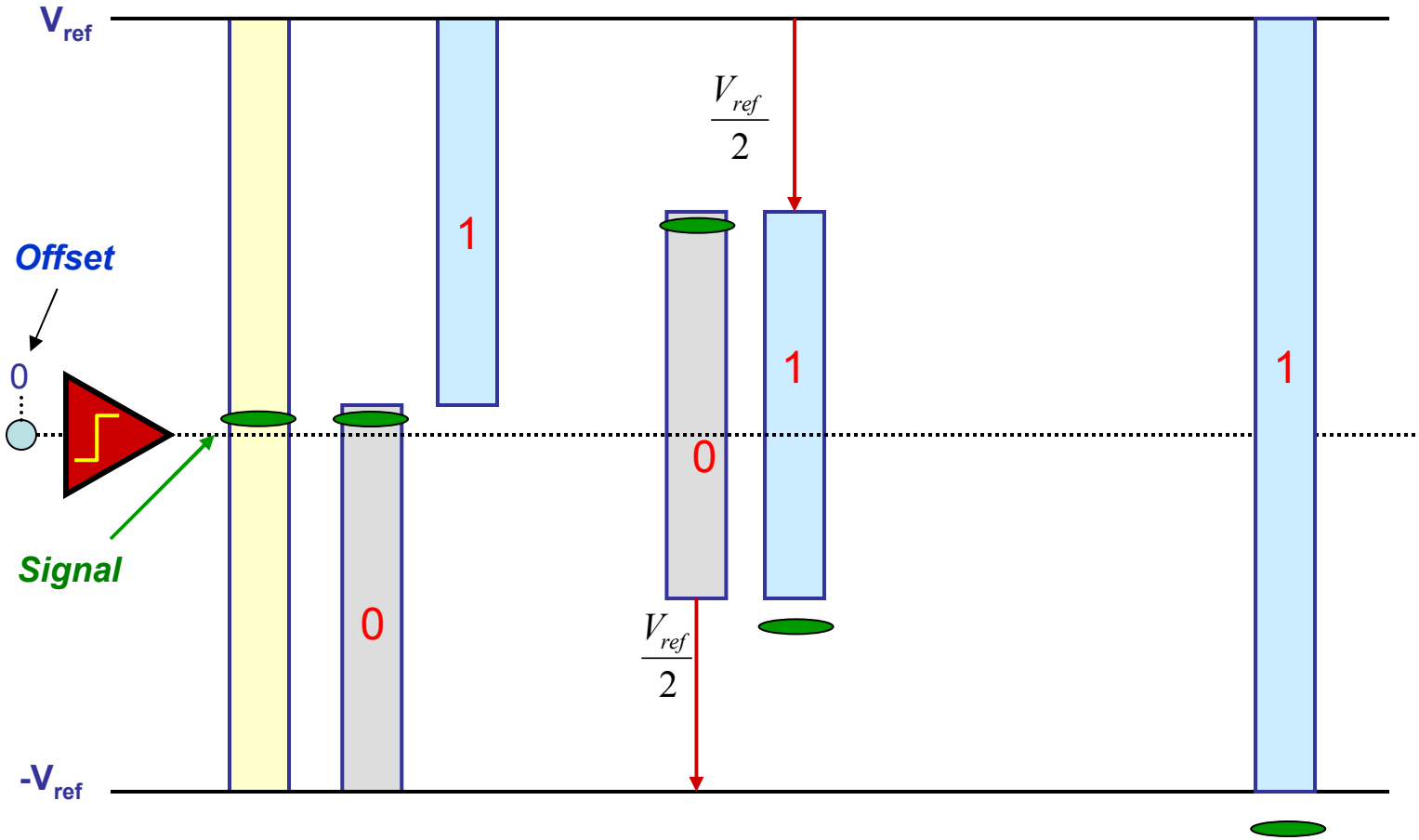
$$\frac{V_0}{2} = 8V_{\text{IN}} - V_{\text{ref}}\left[8D_3 + 4D_2 + 2D_1 + D_0\right]$$

$$\frac{V_{\text{IN}}}{V_{\text{ref}}} \approx \frac{1}{8}\begin{bmatrix} D_3 & D_2 & D_1 & D_0 \end{bmatrix} \bullet \begin{bmatrix} 8 \\ 4 \\ 2 \\ 1 \end{bmatrix}$$

1-bit-per-Stage ADC with Input Near Zero



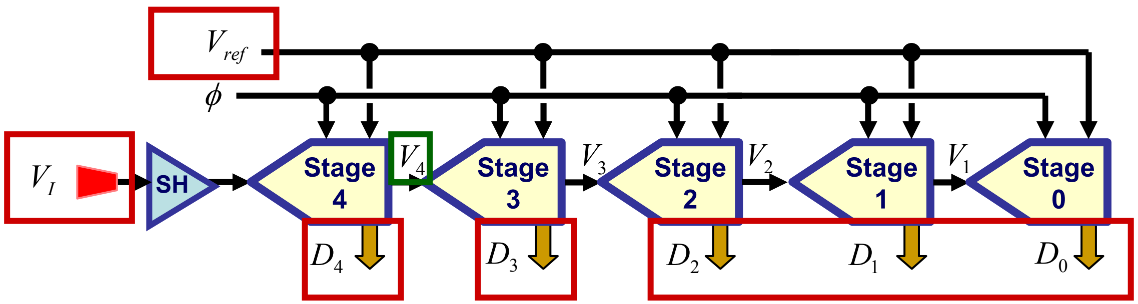
Voltage Sub-Ranges: Comparator Offset



Chosen Residue
Clipping: Major Error

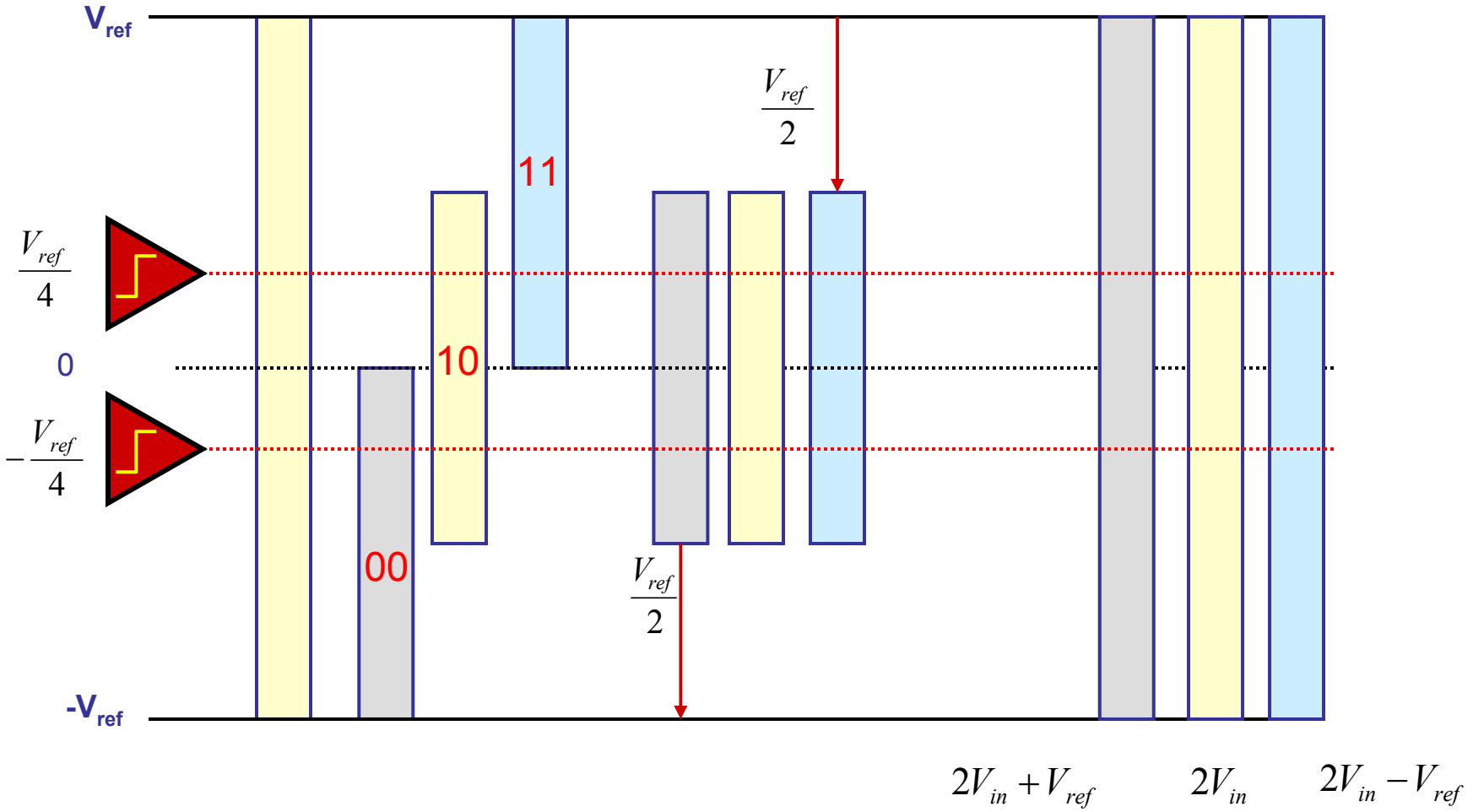
Redundancy

Long Division: Natalya's 6th Grade Homework

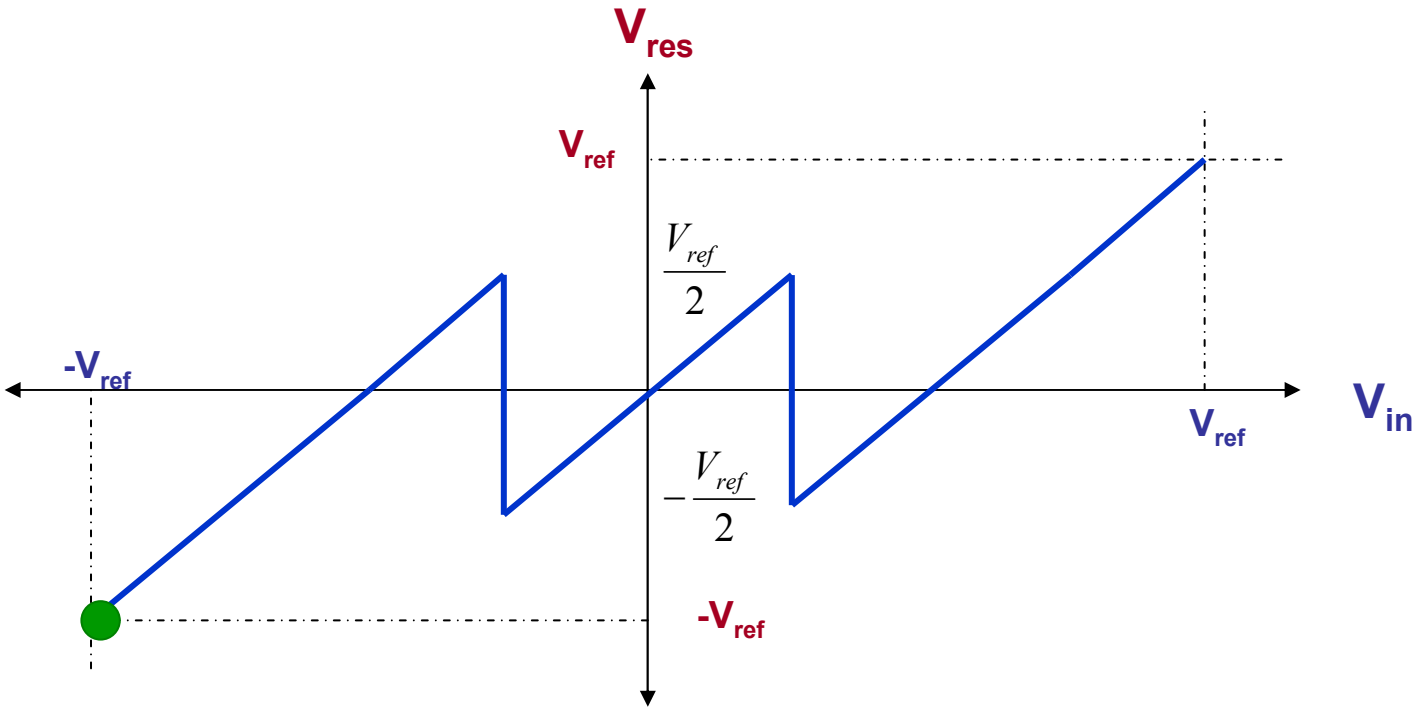



```
          1 0        <- Redundancy / Overlap
          3   . 1 5 6
1 0 2  | 4 0 9 6 . 0 0 0        = 4 0 . 1 5 6
         3 0 6
         -------
         1 0 3 6      <- residue
         1 0 2 0
         -------
             1 6 0
             1 0 2
             -------
               5 8 0
               5 1 0
               -------
                 7 0 0
                 6 1 2
                 -------
                   8 2
```

Voltage Sub-Ranges: With Overlap



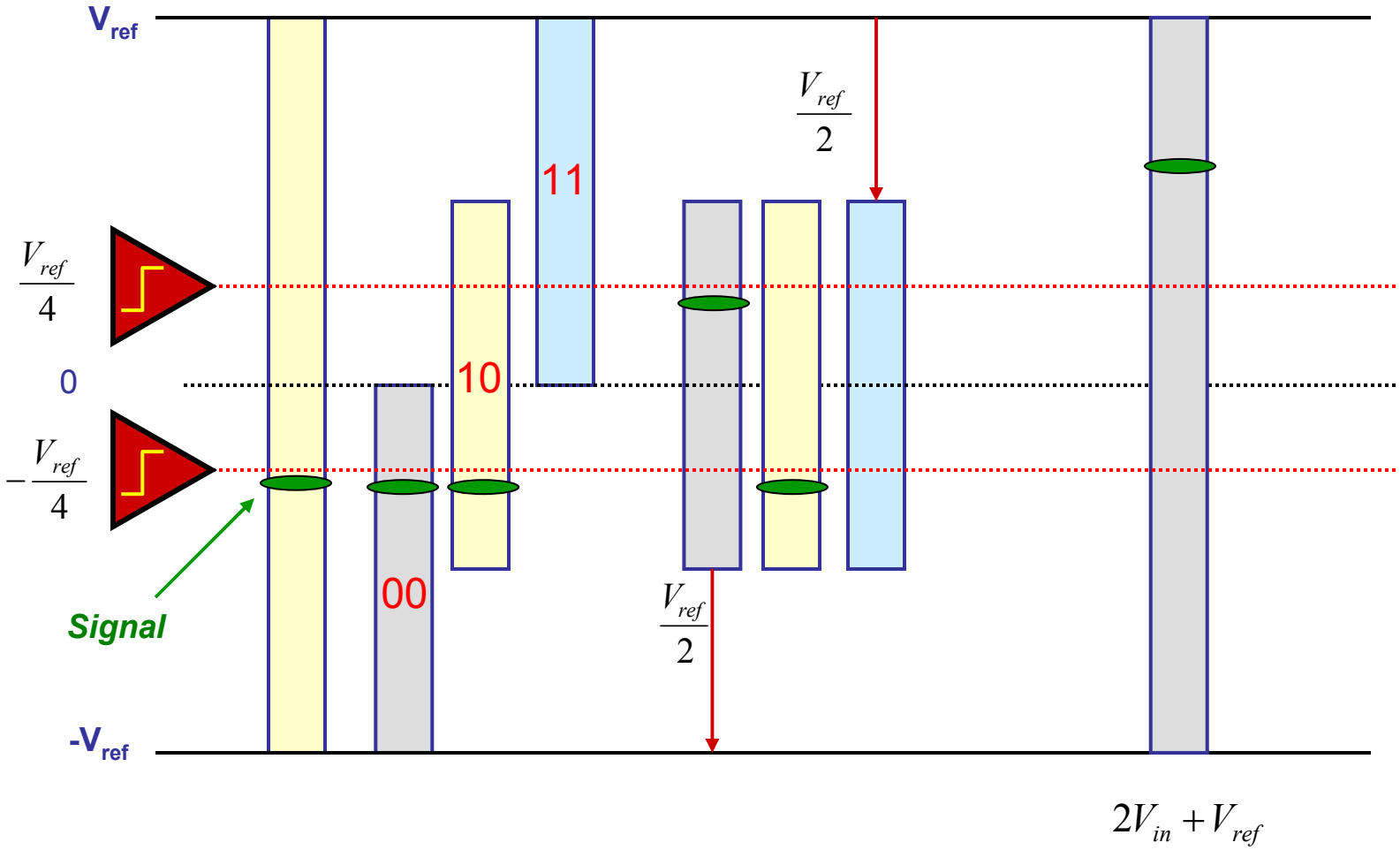
Residue Plot: with Redundancy



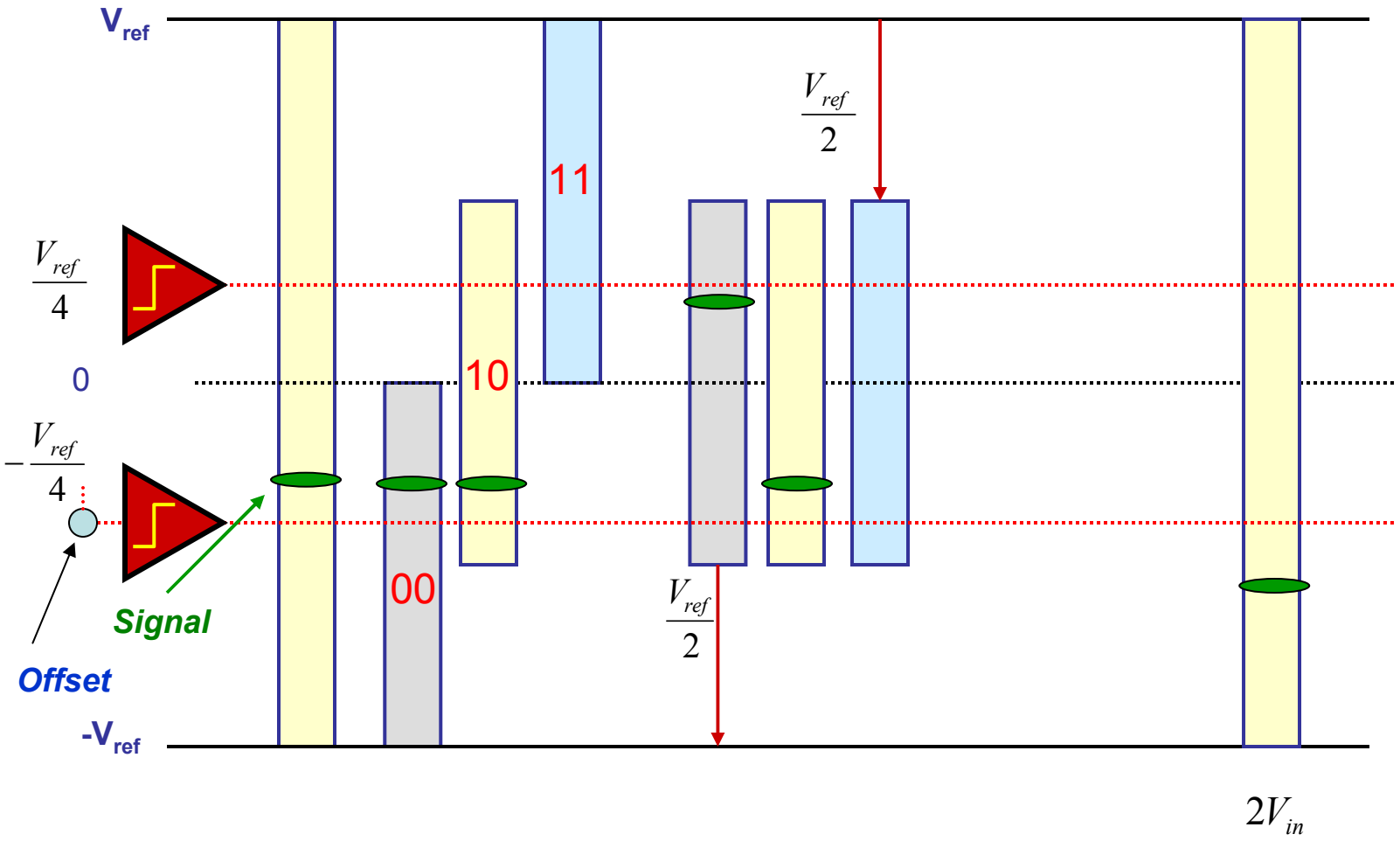
Redundancy Relaxes Coarse ADC Requirements

- Offset of coarse ADC need only be accurate to Vref/4
- Half of the voltage swing is used for over-range

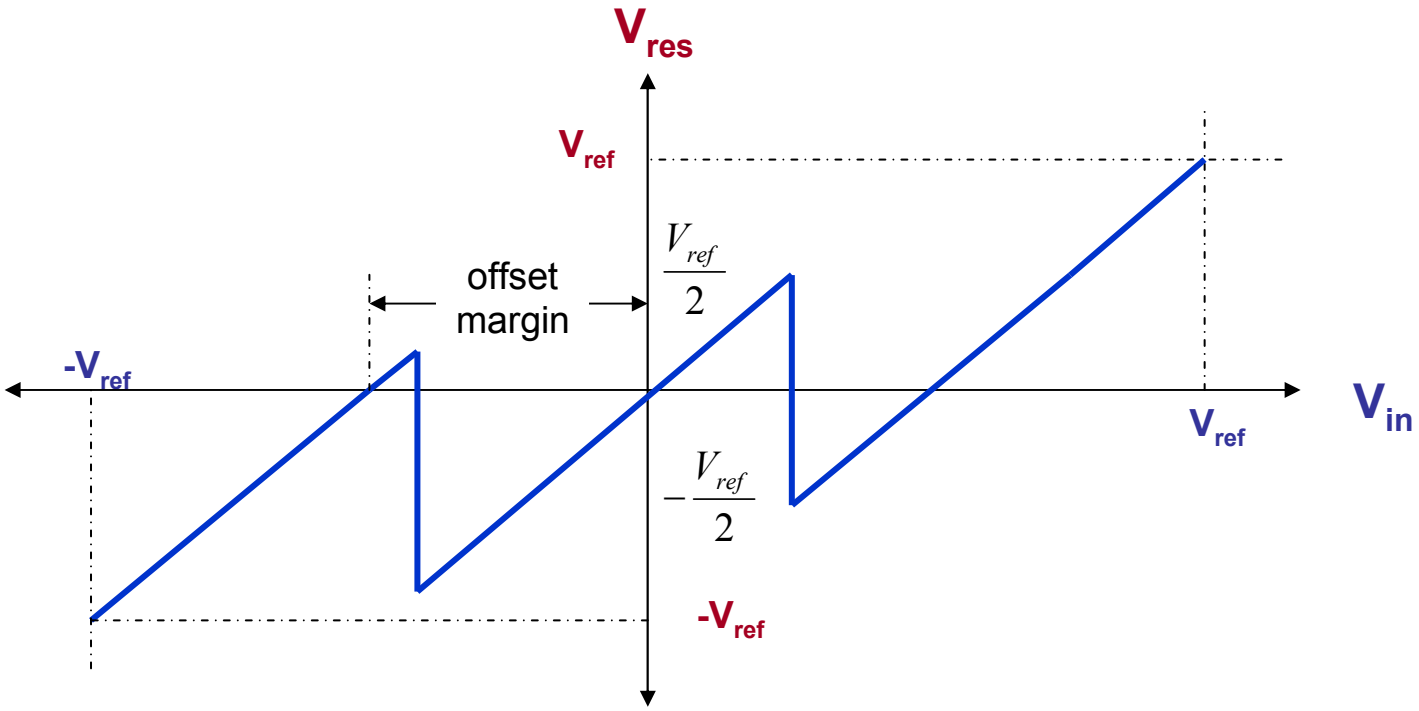
Voltage Sub-Ranges: With Overlap



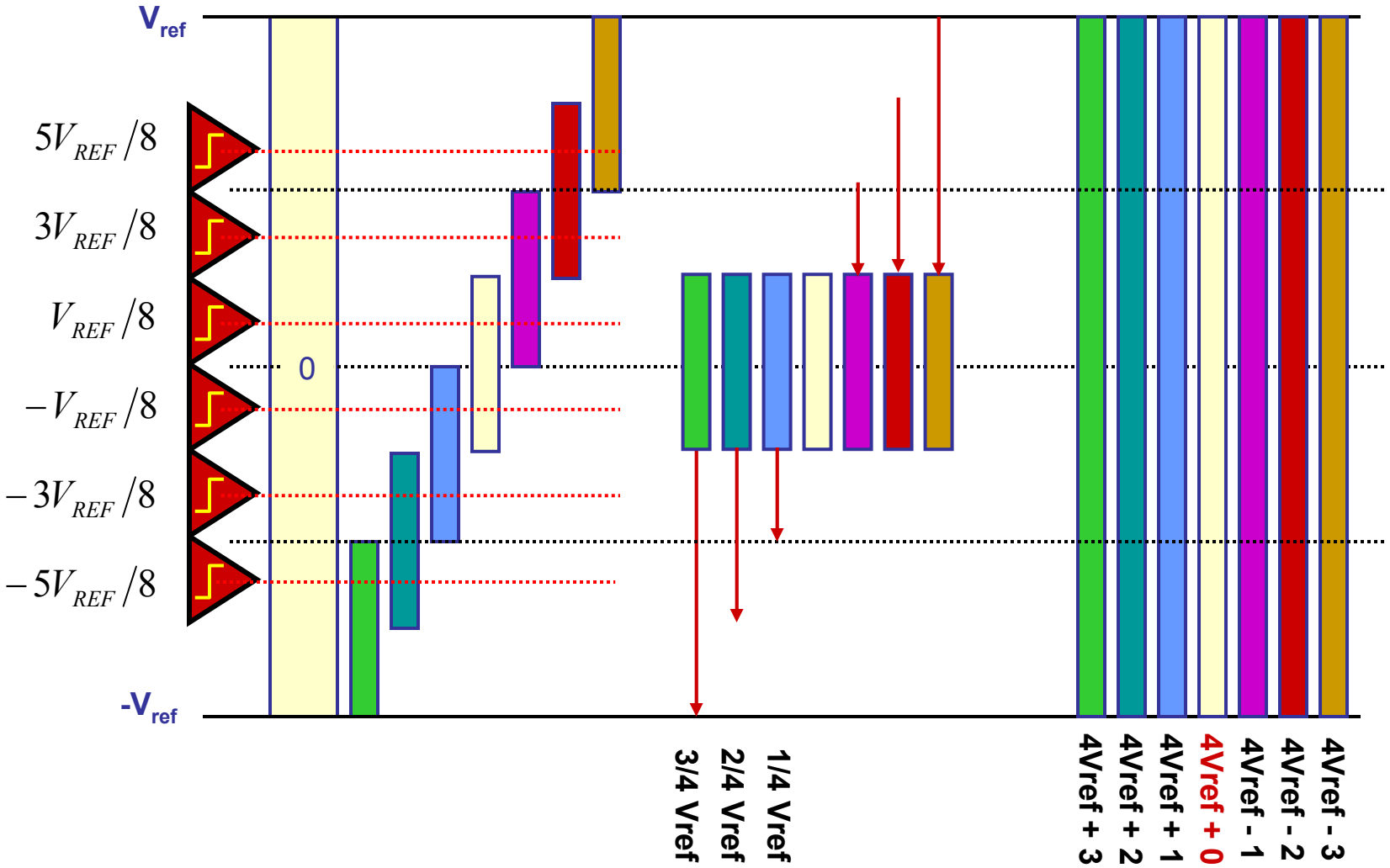
Voltage Sub-Ranges: Offset Margin +/-Vref/4



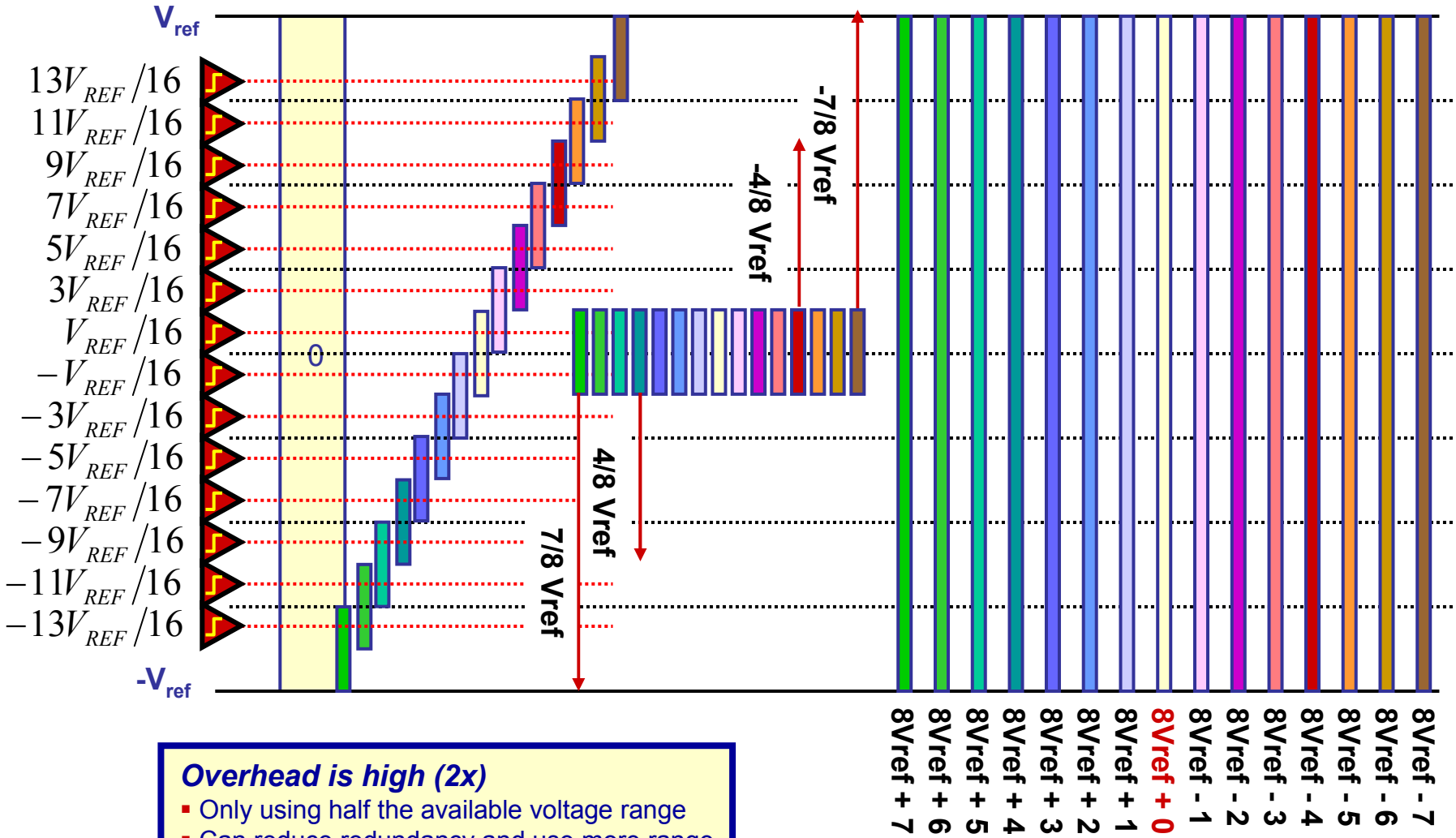
Residue Plot: with Redundancy



Voltage Sub-Ranges: 2-bit (4x Gain)



Voltage Sub-Ranges: 3-bit (8x Gain)

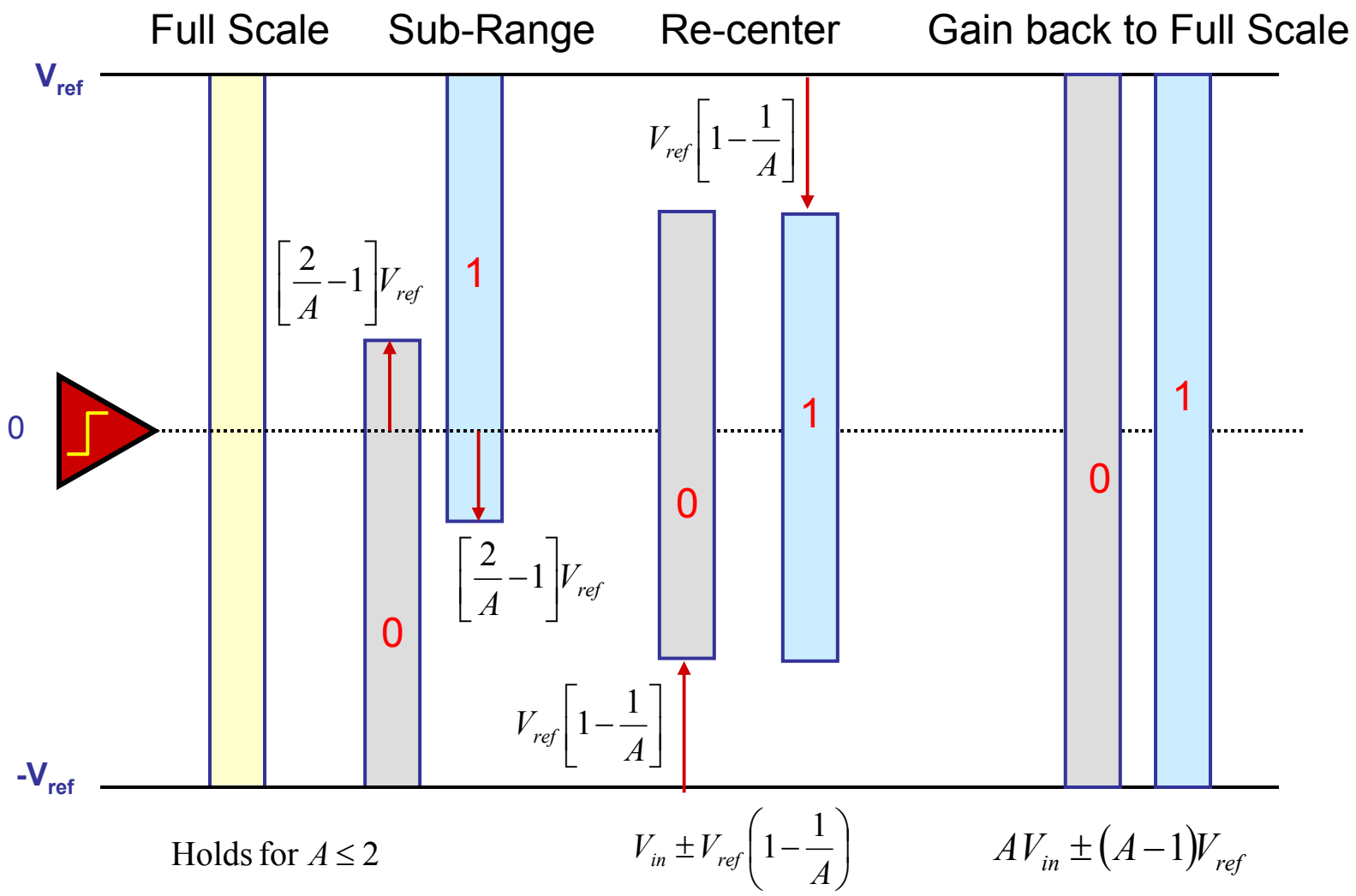


Overhead is high (2x)

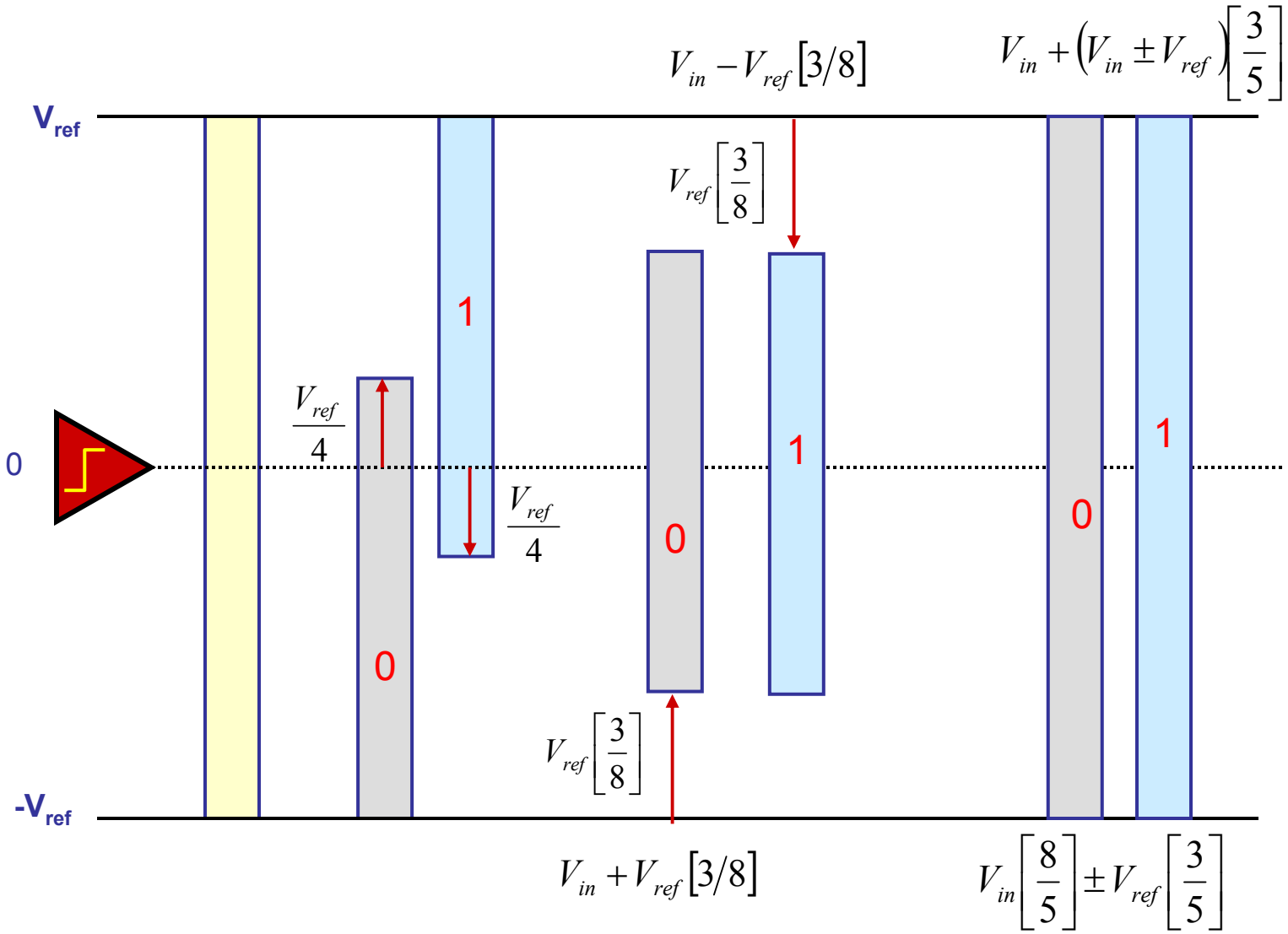
- Only using half the available voltage range
- Can reduce redundancy and use more range at expense of potential over-range

Less than 1-bit-per-stage Pipelined ADC

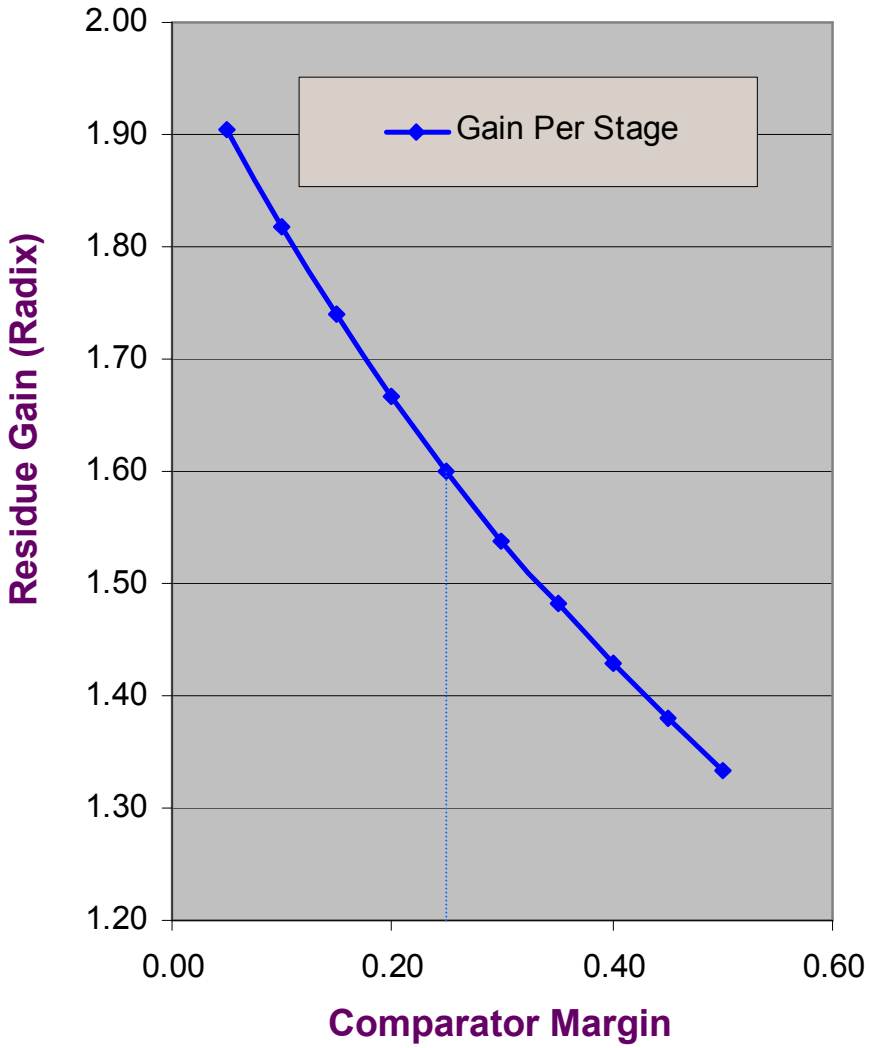
Voltage Sub-Ranges: Single Comparator



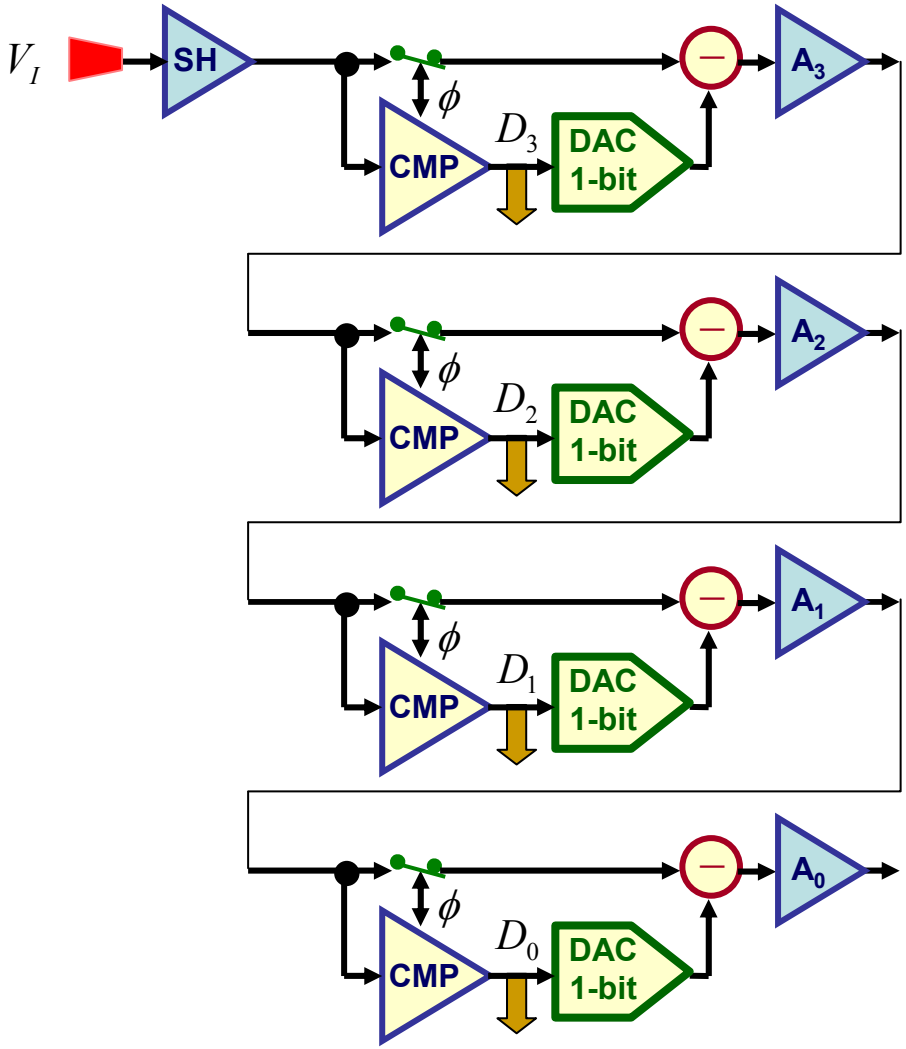
Voltage Sub-Ranges: Example A=1.6



Radix vs. Margin



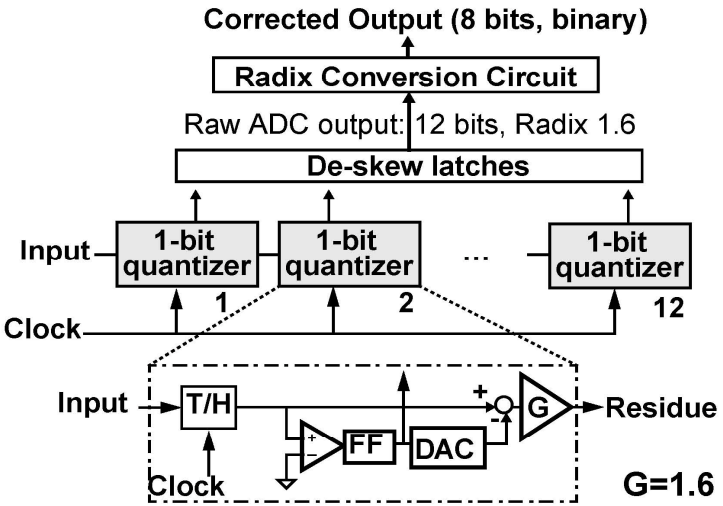
Pipelined ADC: Radix Less Than Two



$$\frac{V_{\text{IN}}}{V_{\text{ref}}} \approx \frac{1}{A_3 A_2 A_1}\begin{bmatrix} D_3 & D_2 & D_1 & D_0 \end{bmatrix} \bullet \begin{bmatrix} A_3 A_2 A_1 \\ A_2 A_1 \\ A_1 \\ 1 \end{bmatrix}$$

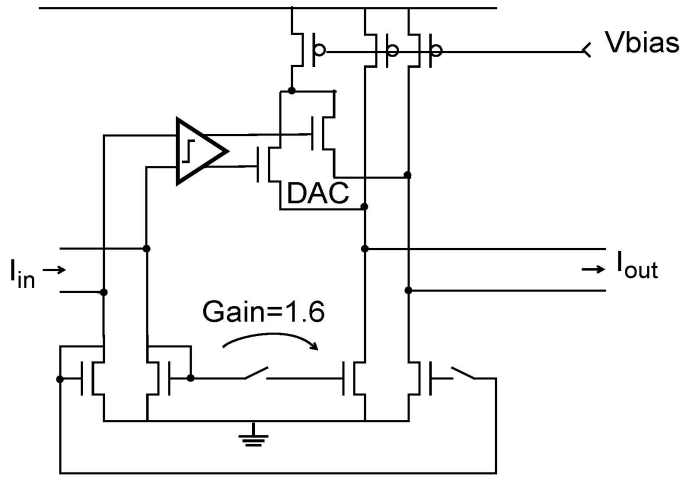
Doesn't Need to Be Switched Cap

Pipeline ADC Block Diagram



- Only 1 comparator per stage

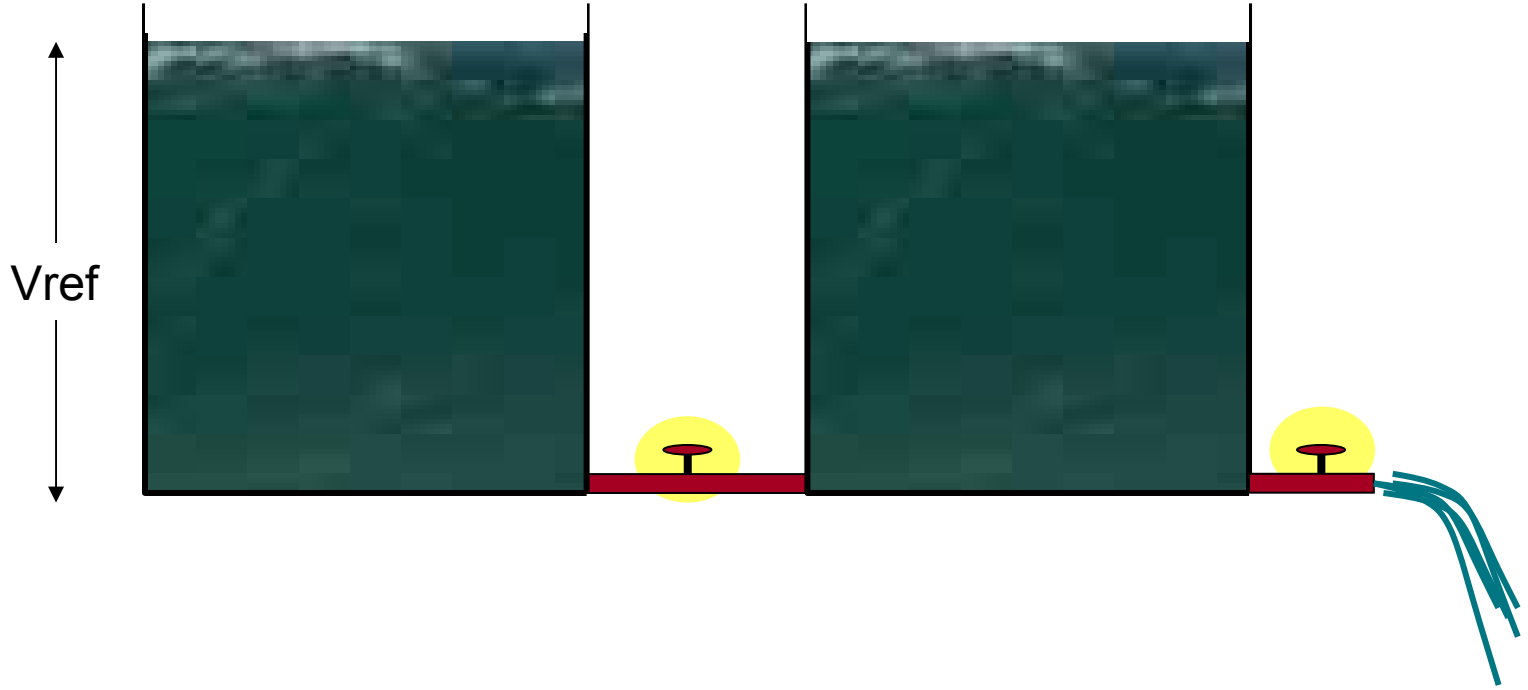
Current-Mode ADC Stage



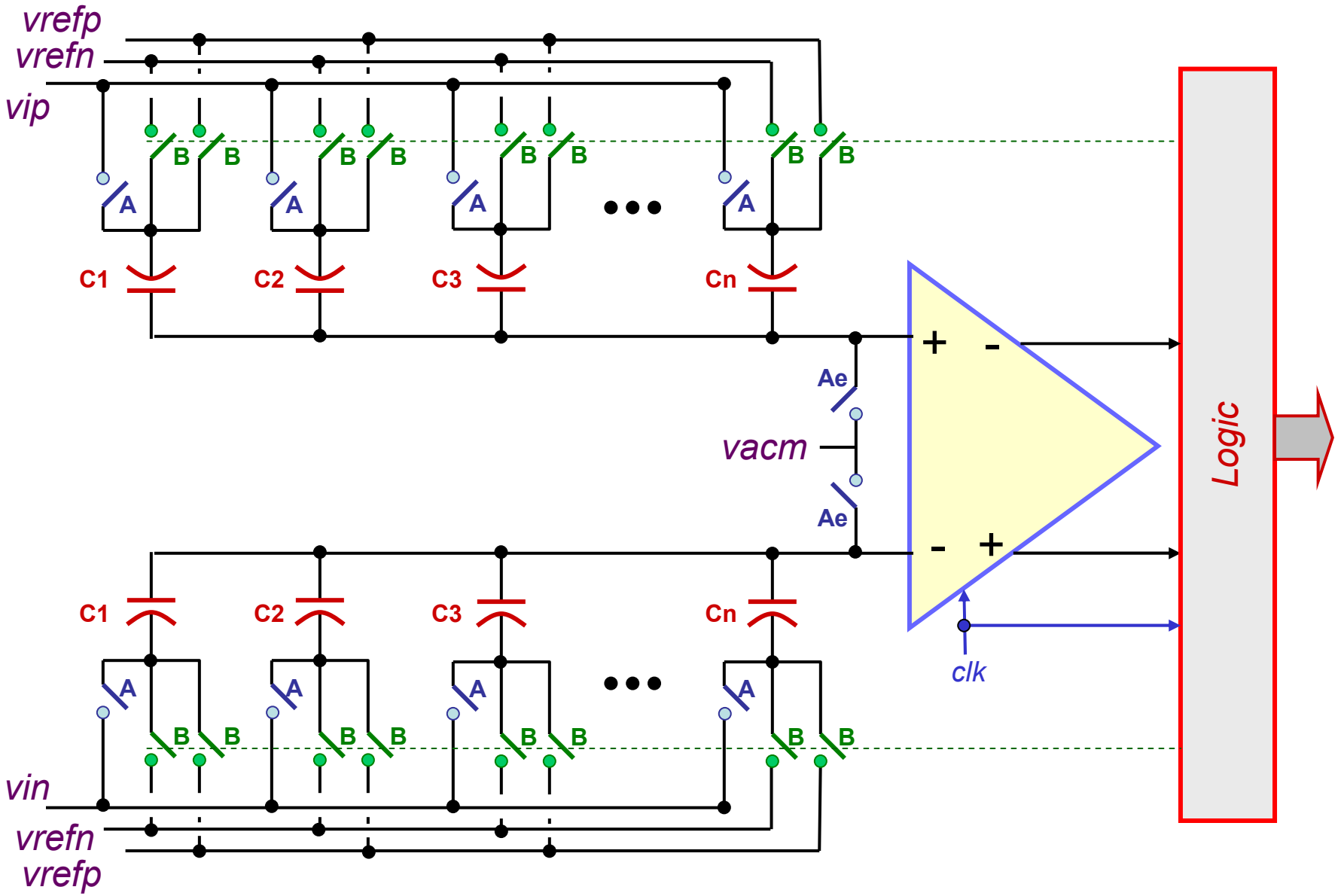
Ken Poulton, Robert Neff, et al. , ISSCC 2002, ISSCC 2003

Successive Approximation From Pipelined Ideas

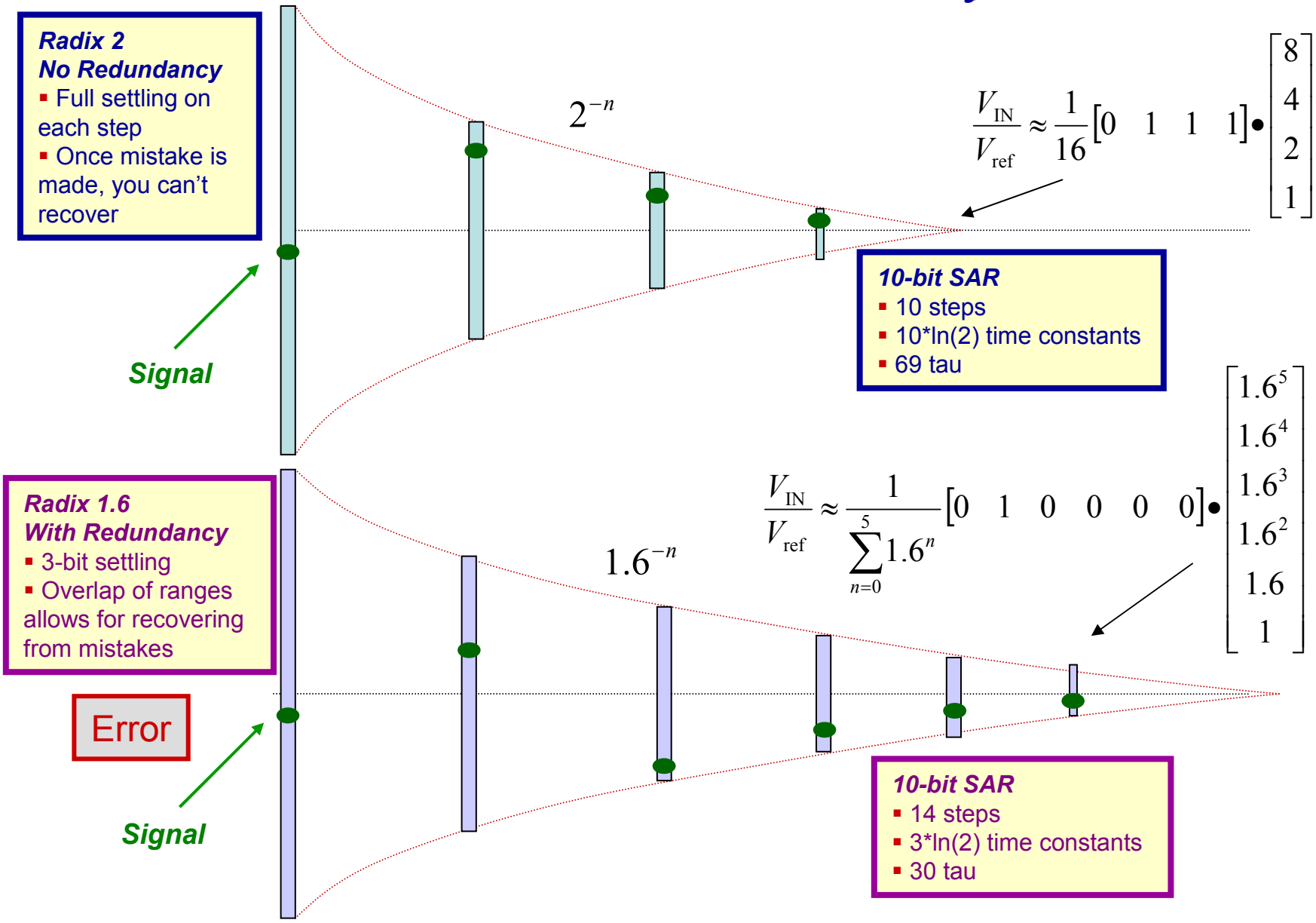
Switched Capacitor Implementation
Charge Sharing Principle



Successive Approximation ADC



SAR with Redundancy



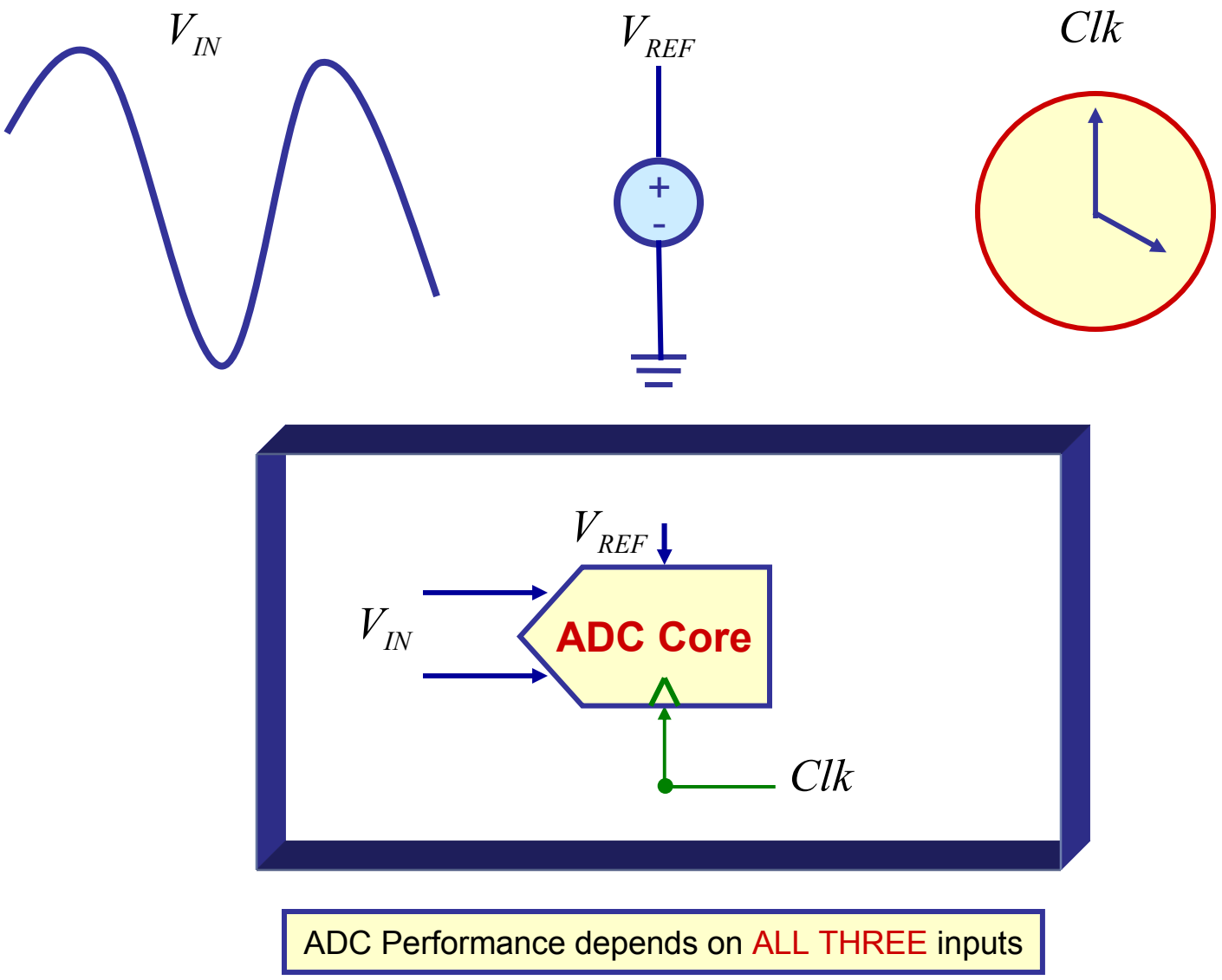
Example Design
Switched Capacitor Based
10-bit
200-MS/s

Summary of Design Issues

- Capacitor size based on KT/C
  - C total = 225fF
- Opamp open-loop gain
  - Ao < 60dB
  - Calibration or correlated double-sample can reduce gain requirement
- Jitter
  - Clock jitter < 1.25ps
- No Sample & Hold
  - Need care to ensure MDAC and CADC synchronization
- 2-Stage opamp
  - Dual common-mode feedback loop
  - Tail source on second-stage
- 2 bits per stage
  - 3-bit flash
- Coarse ADC
  - Use built-in reference to reduce capacitive load
  - Will require calibration

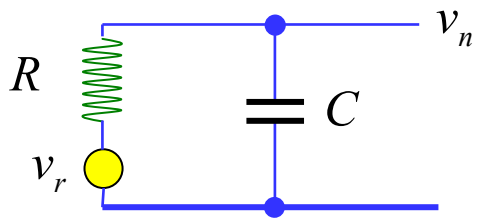
Physical Limitations

ADC Basics: 3-Input Device



ADC Performance depends on ALL THREE inputs

Thermal Noise Limitations



Transfer Function

$$V_n(s) = V_r(s)\frac{1}{1+sRC}$$

Output Noise Spectral Density

$$S_n(f) = S_r(f)\left|\frac{1}{1+j2\pi fRC}\right|^2$$

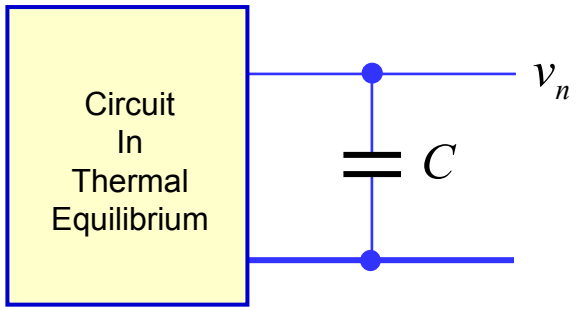
Expected Noise Power

$$v_n^{\,2} = 4kTR\int_0^\infty \frac{1}{1+(2\pi fRC)^2}df \quad = \frac{4kTR}{2\pi RC}\int_0^\infty \frac{1}{1+x^2}dx \quad = \frac{2kT}{\pi C}\int_0^{\frac{\pi}{2}} d\theta$$

$$v_n^{\,2} = \frac{kT}{C}$$

Result is independent of R.
Implies a more fundamental physical law

Equipartition Theorem



Expected Value of Thermal Energy for 1-degree of freedom

$$E = \frac{1}{2}kT$$

Expected Value of Electrical Energy Stored on Capacitor

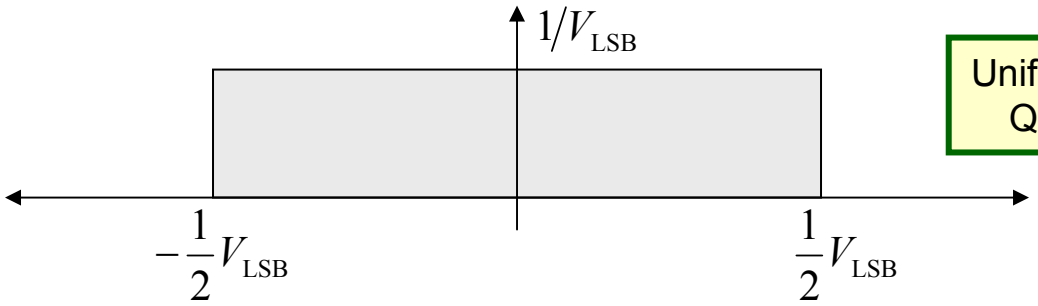
$$E = \frac{1}{2}Cv_n^{\,2}$$

Expected Value of Squared Voltage on Capacitor

$$v_n^{\,2} = \frac{kT}{C}$$

RMS Quantization Noise

Quantization Error Probability Density Function



Uniform assumption for Quantization noise

$$V_{Q\sigma} = \frac{V_{LSB}}{\sqrt{12}} = 0.289 V_{LSB}$$

rms Quantization Noise

$$V_{Q\sigma} = \frac{V_{PP}}{2^n \sqrt{12}}$$

Where V_{PP} is the full-scale Voltage and n is the # of bits

Noise Requirements: Example Calculation

$$\frac{1}{2}\sigma_T^{\,2} \cong \sigma_{\mathrm{AMP}}^{\,2} + \sigma_{KT}^{\,2} = \frac{1}{2}\cdot\frac{V_{LSB}^{\,2}}{12}$$

Assume equal contribution of noise dominated from AMP and KT/C.

$$\sigma_{\mathrm{AMP}} = \sigma_{KT} = \frac{1}{2}\cdot\frac{V_{LSB}}{\sqrt{12}} \approx \frac{V_{LSB}}{7}$$

For 1-Vpp input and a 10-bit ADC with a bandwidth of 1-GHz. The LSB is approximately 1-mV so that the rms noise requirement of the amp and KT/C is 144uV

$$\frac{KT}{C} = (144\mu\mathrm{V})^2$$

$$C = 225\mathrm{fF}$$

$$4KTBR_{\mathrm{EQ}} = (144\mu\mathrm{V})^2$$

$$R_{\mathrm{EQ}} = 1100\Omega$$

Noise Requirements: 12-bit Example

For 1-Vpp input and a 12-bit ADC. The LSB is approximately 0.25-mV so that the rms noise requirement of the amp and KT/C is 36uV

$$\frac{KT}{C} = (36\mu\text{V})^2$$

$$C = 3.6\text{pF}$$

$$4KTBR_{\text{EQ}} = (36\mu\text{V})^2$$

$$R_{\text{EQ}} = 70\Omega$$

12-bit Example: High Vref and High Vdd

For 2-Vpp input and a 12-bit ADC. The LSB is approximately 0.5-mV so that the rms noise requirement of the amp and KT/C is 72uV

$$\frac{KT}{C} = (72\mu\text{V})^2$$

$$C = 900\text{fF}$$

$$4KTBR_{\text{EQ}} = (72\mu\text{V})^2$$

$$R_{\text{EQ}} = 275\Omega$$

For High Accuracy ADCs

- The higher the Vref the better
- This requires large voltage (High Vdd is essential)
- gm of 1/70 requires a lot of current
- Good to have gain in Sample & Hold to ease noise requirements of MDAC
- Can give up some SNR performance to ease power requirements: Giving up an additional 0.5-bits of noise cuts the cap in half and doubles Req

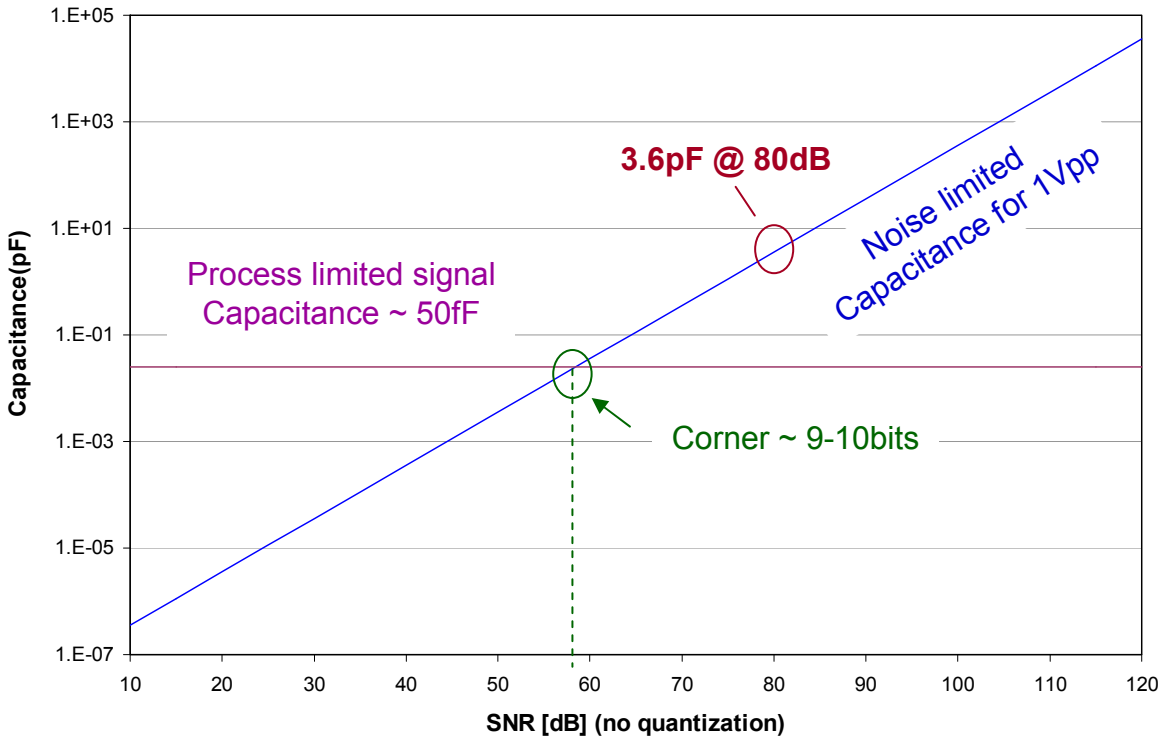
Minimal Capacitance for a Given Ideal SNR

Thermal Noise set to Quantization Noise

$$v_{rms} = \sqrt{\frac{kT}{C}} = \frac{V_{pp}}{2^n \sqrt{12}}$$

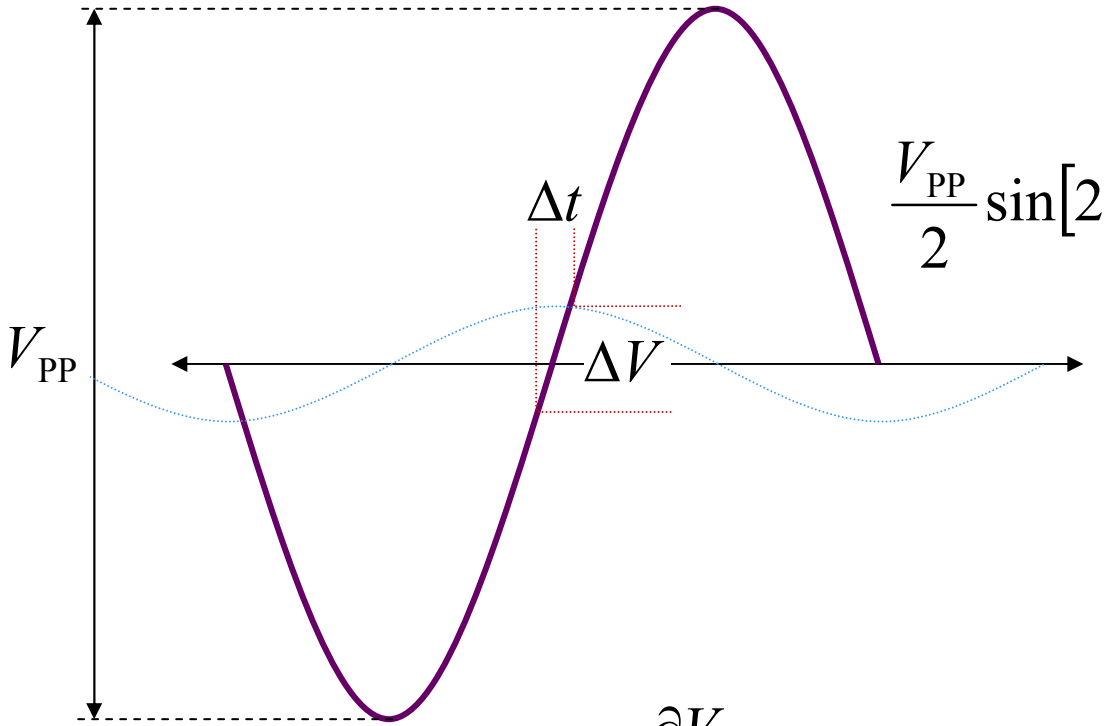
Minimum value of input capacitance

$$C = \frac{12kT}{V_{pp}^{\ 2}} \cdot 2^{2n}$$



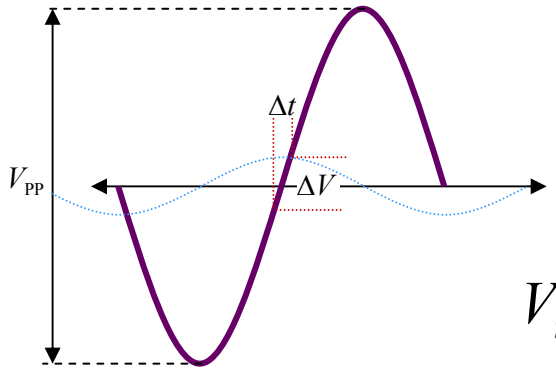
Additional Slide

Limitations Due to Timing Jitter for Sine Input



$$\Delta V(t) = \Delta t(\pi f_{in}) \cdot V_{PP} \cos[2\pi f_{in} t]$$

Expression for SNR due to Jitter

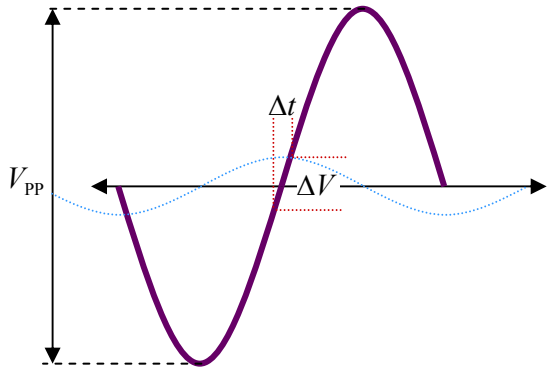


$$V_{inrms} = \sqrt{avg\left[\left(\frac{V_{PP}}{2}\sin\left[2\pi \cdot f_{in}(t+\Delta t)\right]\right)^2\right]} = \frac{V_{PP}}{2\sqrt{2}}$$

$$\Delta V_{rms} = \Delta t_{rms}\left(\pi f_{in}\right) \cdot V_{PP} \cdot \sqrt{avg\left(\cos^2[2\pi f_{in} t]\right)} = 2\pi f_{in}\Delta t_{rms}\frac{V_{PP}}{2\sqrt{2}}$$

$$\frac{\Delta V_{rms}}{V_{inrms}} = \frac{1}{SNR} = 2\pi f_{in}\Delta t_{rms}$$

Jitter Requirement for 10-bit



SNR due to Quantization = 6.02(10) + 1.76 ~ 62dB

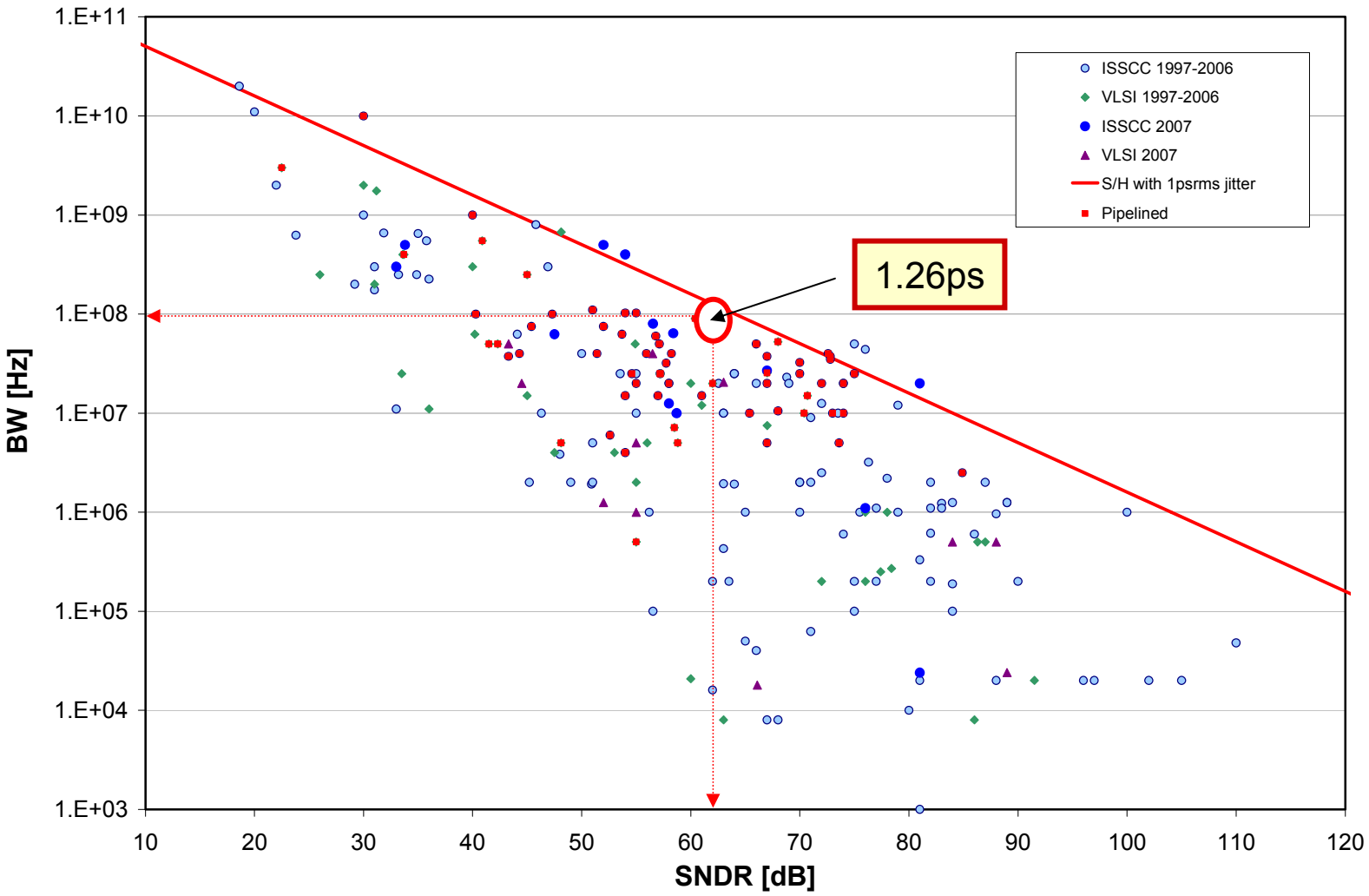
$$\frac{1}{62dB} = 2\pi f_{\text{in}} \Delta t_{rms}$$

f_{in} = Nyquist @ f_s =200-MHz

$$\Delta t_{rms} = \frac{T_s}{\pi \cdot SNR} = \frac{5\text{ns}}{\pi \cdot SNR}$$

$$\Delta t_{rms} < 1.26\text{ps}$$

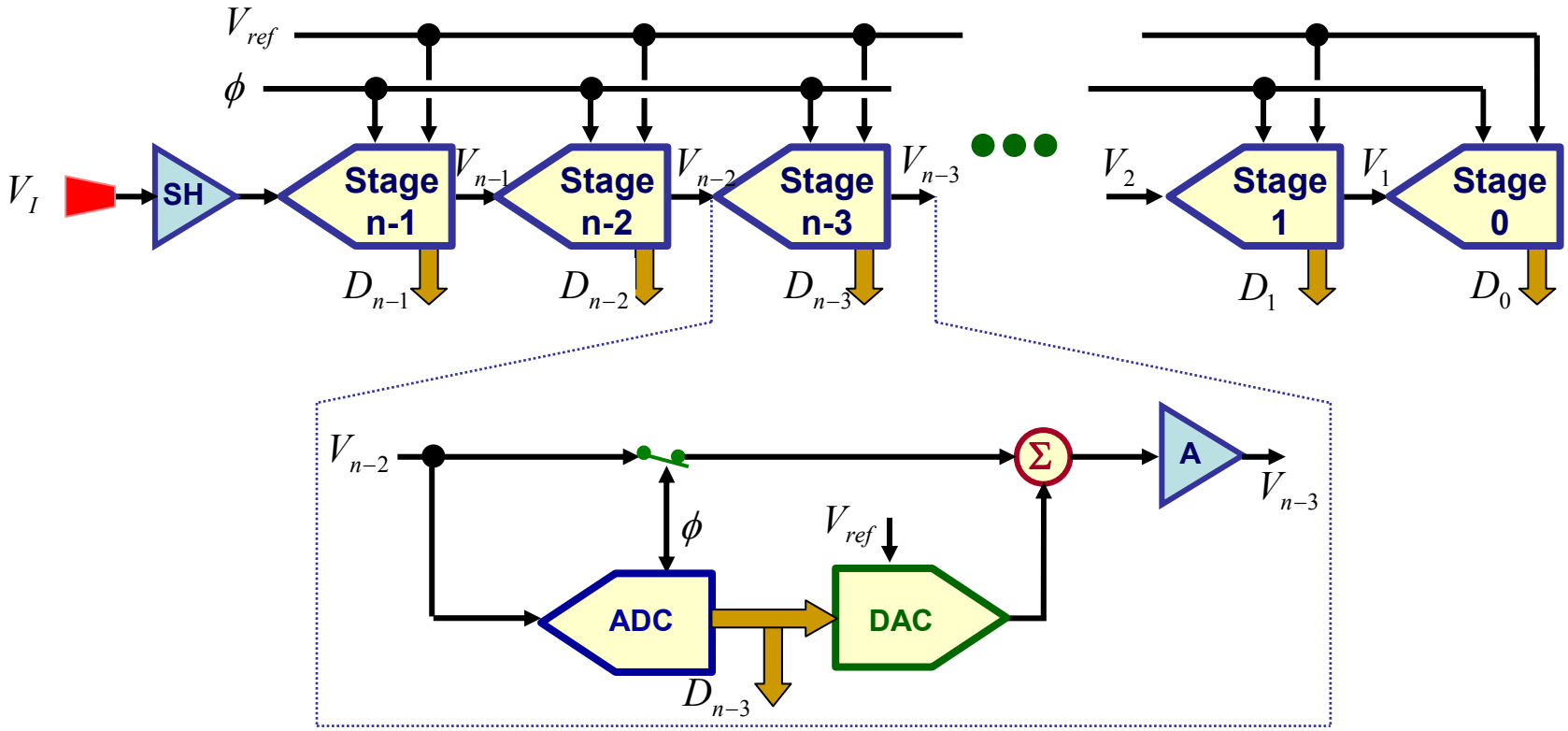
ADC Speed and Resolution



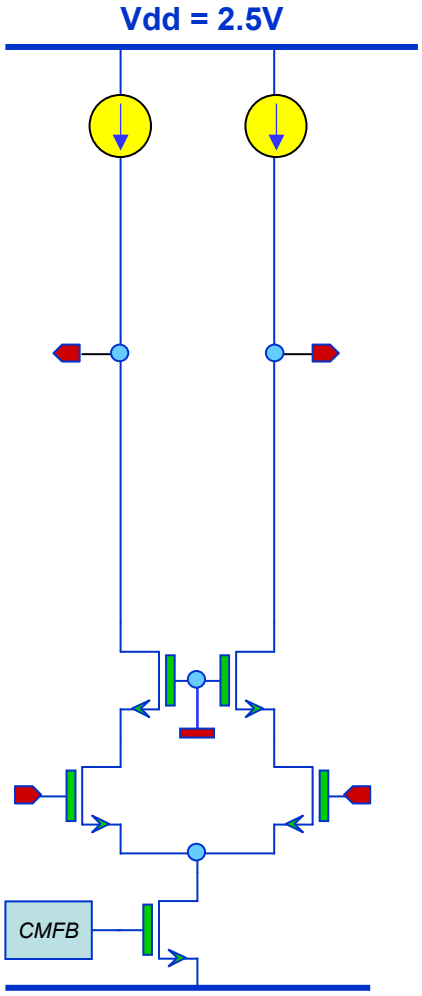
B. Murmann, "ADC Performance Survey 1997-2007," [Online]. Available: http://www.stanford.edu/~murmann/adcsurvey.html.

Circuit Implementation Switched Capacitor Based 10-bit 200-MS/s

Pipelined ADC Architecture

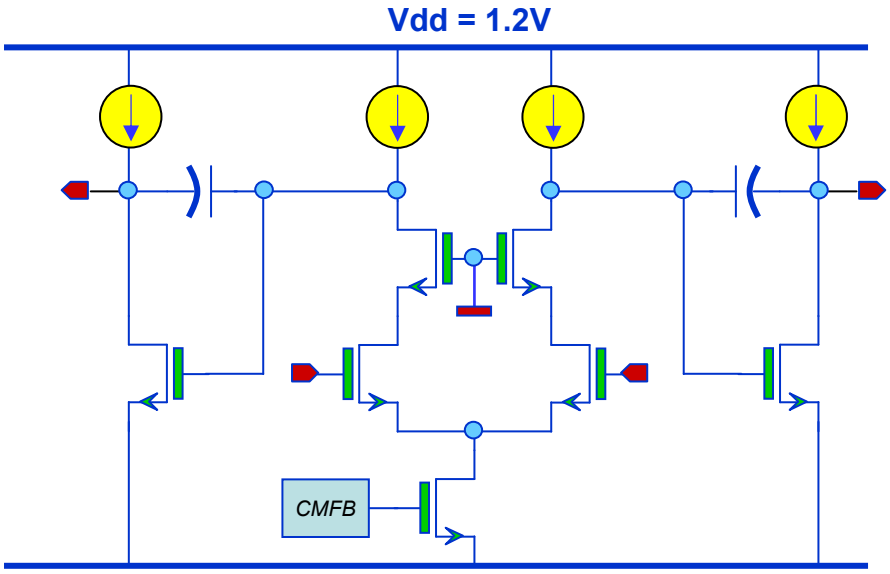


Thick Oxide vs. Thin Oxide

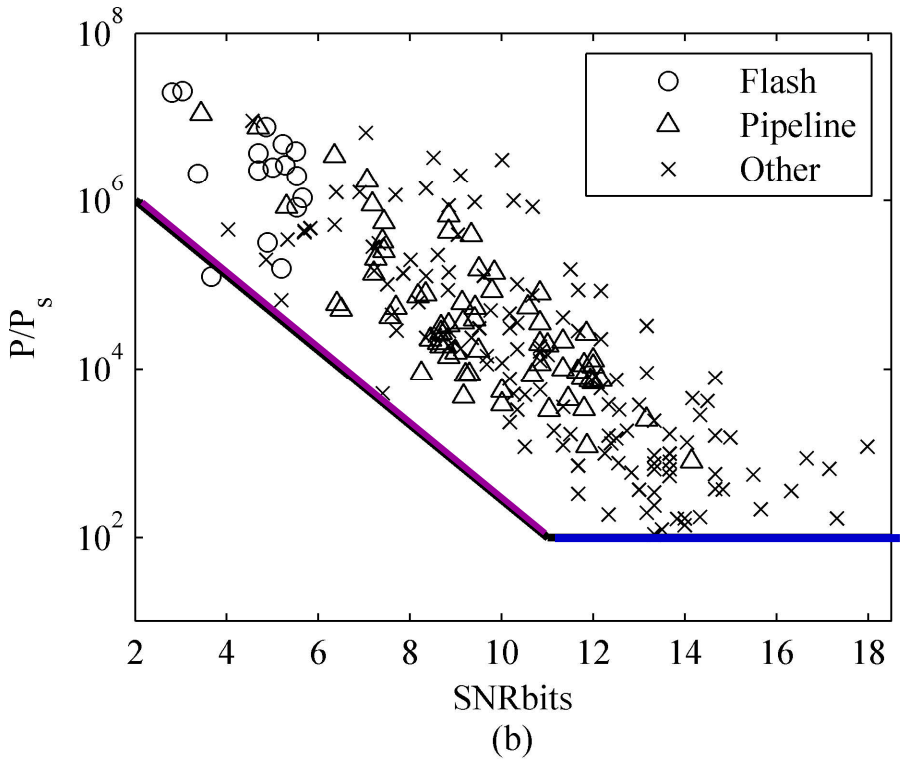


$$C \propto \frac{1}{V_{pp}^{\ 2}}$$

Doubling voltage swing will reduce Capacitive load by factor of 4x



Noise Limited Corner: Normalized Energy vs. SNR

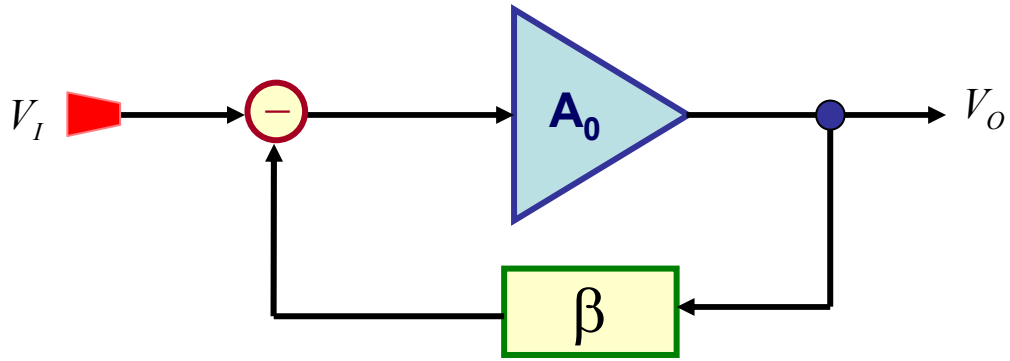


[6] B. Murmann, T. Sundstrom and Christer Svenson, "On the Power Dissipation of High-Speed Analog-to-Digital Converters," *IEEE Trans. Circuits and Systems,* [to be published] submitted 26 Nov 2007.

Additional Slide

- **Normalizing ADC power by the KT/C Limit (P_s) is useful**
  - Clearly shows State of the Art with respect to P_s
  - Shows best high SNR ADCs ~ 100x Thermal Power Limit
  - Identifies noise limited circuit corner at roughly 11-bits

Open-Loop DC Gain Requirement



Closed loop Gain

$$A = \frac{A_o}{1 + A_o\beta} \cong \frac{1}{\beta} \cdot \left(1 - \frac{1}{A_0\beta}\right)$$

Accuracy Required Scales with Gain

$$\varepsilon = A\varepsilon_0 \approx \frac{\varepsilon_0}{\beta}$$

Normalized Gain Error

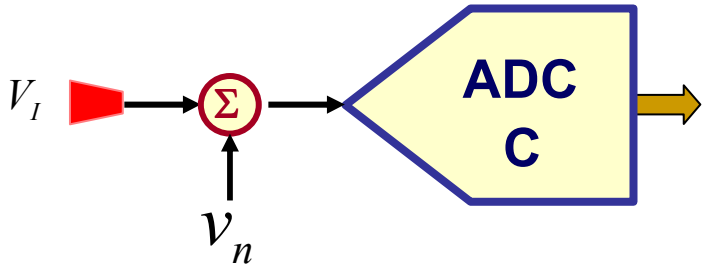
$$\varepsilon = \frac{1}{A_0\beta}$$

Closed Loop Gain Independent of β

$$A_0 > \frac{1}{\varepsilon_o} \approx 2^n$$

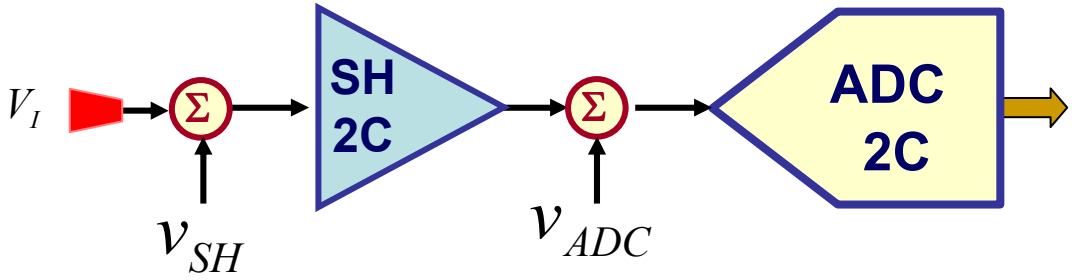
[3] 30.1 An Over-60dB True Rail-to-Rail Performance Using Correlated Level Shifting and an Opamp with 30dB Loop Gain
1:30 PM
B. Gregoire, U-K. Moon

Sample & Hold: Yes or No



No SHA: Total Input Referred Noise Power

$$v_{TOT}^{\ 2} = v_n^{\ 2}$$



SHA: Input Referred Noise Power

$$v_{TOT}^{\ 2} = v_{SH}^{\ 2} + v_{ADC}^{\ 2}$$

To achieve KT/C Noise Performance with No SHA

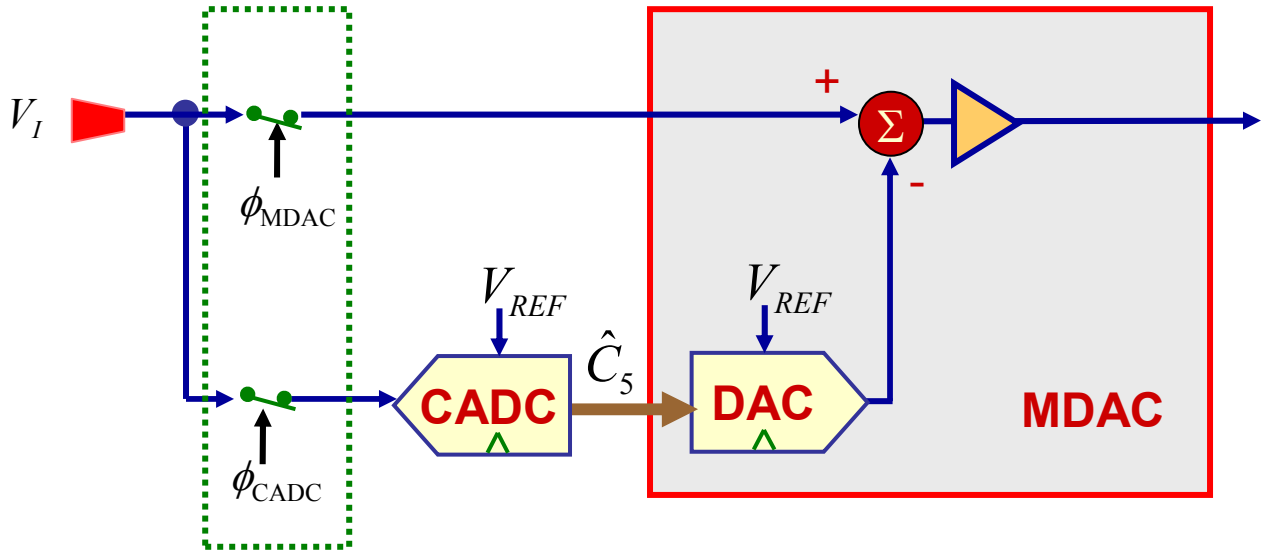
$$v_{SH}^{\ 2} = v_{ADC}^{\ 2} = \frac{v_n^{\ 2}}{2}$$

$$\frac{kT}{C} = \frac{kT}{2C} + \frac{kT}{2C}$$

Total Capacitance Increases with SHA by 4x

- Total power increase 2-4x

Pipelined ADC with No Sample & Hold



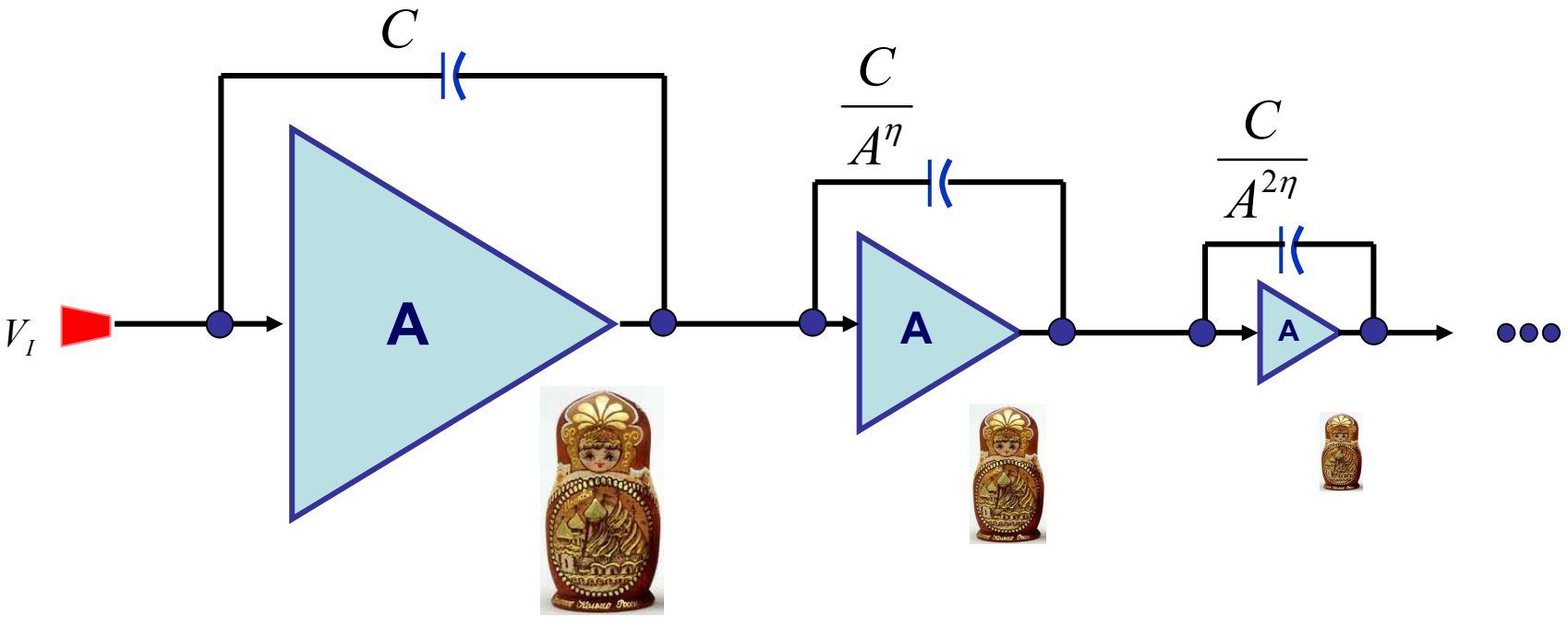
Sampling occurs in two places

- Dual sampling must be synchronized to avoid skew

[4] I. Mehr and L. Singer, "A 55-mW 10-bit 40-Msample/s Nyquist-rate CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 35, pp. 318–325, Mar. 2000.

[5] 12.6 A 14b 100MS/s Pipelined ADC with a Merged Active S/H and First MDAC 11:15 AM
B. Lee, B. Min, G. Manganaro, J. W. Valvano

Scaling

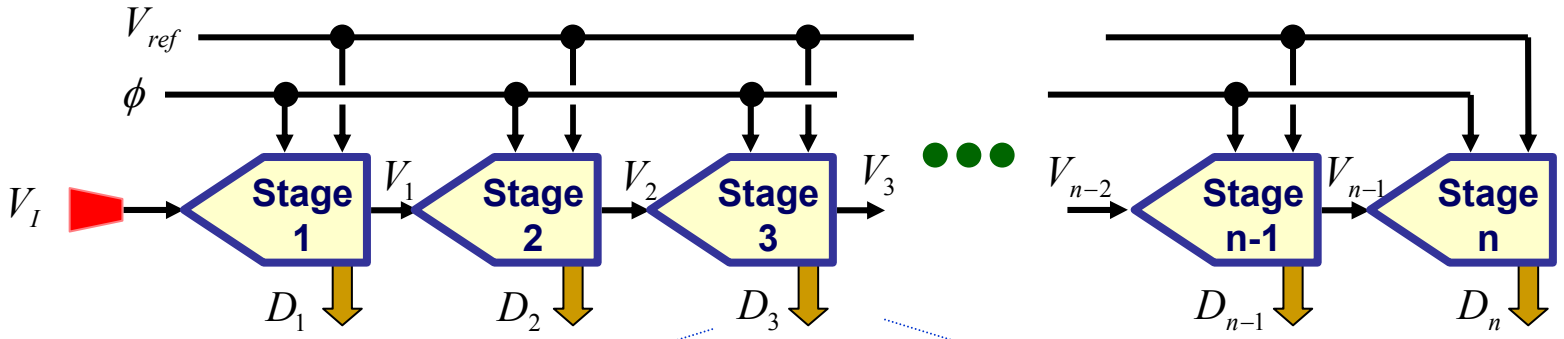


$\eta = 2$ Noise contribution (input referred) of each stage is equal

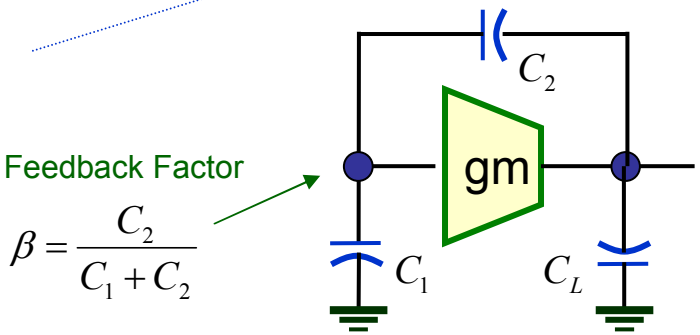
$\eta = 1$ Noise contribution is reduced by $\sqrt{2}$ for each stage
Recommended scaling [1,2]

[1] Y. Chiu, "High-Performance Pipeline A/D Converter Design in Deep-Submicron CMOS," *PhD Dissertation, UC Berkeley*,2004.
[2] D. W. Cline and P. R. Gray, "A power optimized 13-b 5 MSamples/s pipelined analog-to-digital converter in 1.2μm CMOS," *IEEE J. Solid-State Circuits*, vol. 31, no. 3, pp. 294-303, March 1996.

Number of Bits Resolved per Stage: Tau



Closed-loop time constant of MDAC amplifier



Feedback Factor

$$\beta = \frac{C_2}{C_1 + C_2}$$

$$\tau = \frac{1}{g_m \beta} \cdot \left[C_L + \frac{C_1 C_2}{C_1 + C_2} \right] \quad ; \quad \tau = \frac{C_L A}{g_m} + \frac{C_1}{g_m}$$

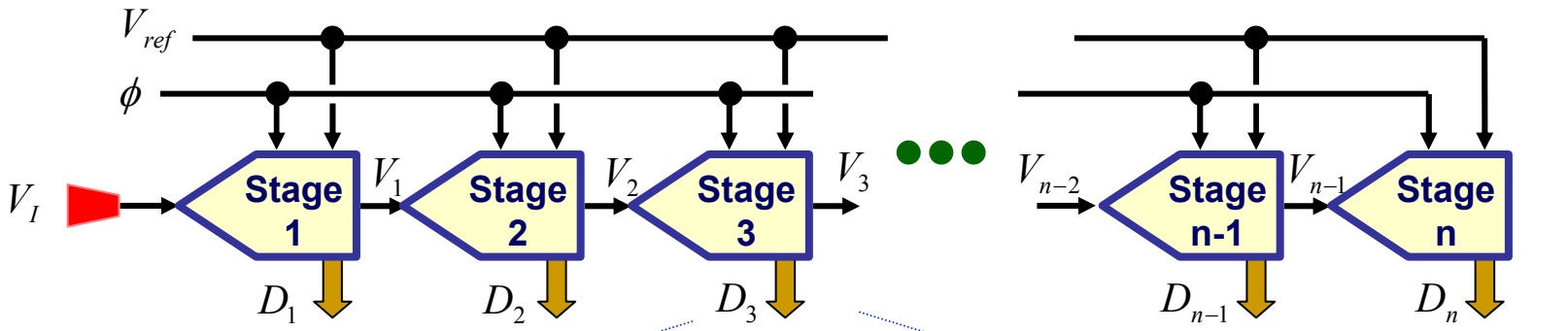
Load is reduced by scaling $C_L A = C$

$$\tau \approx \frac{C}{g_m} + \frac{C(1 - 1/A)}{g_m}$$

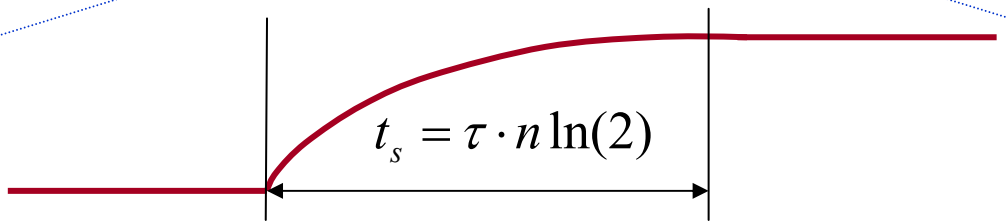
With scaling tau is roughly Independent of gain

- slightly faster with smallest gain

Number of Bits Resolved per Stage: Settling



settling of MDAC amplifier



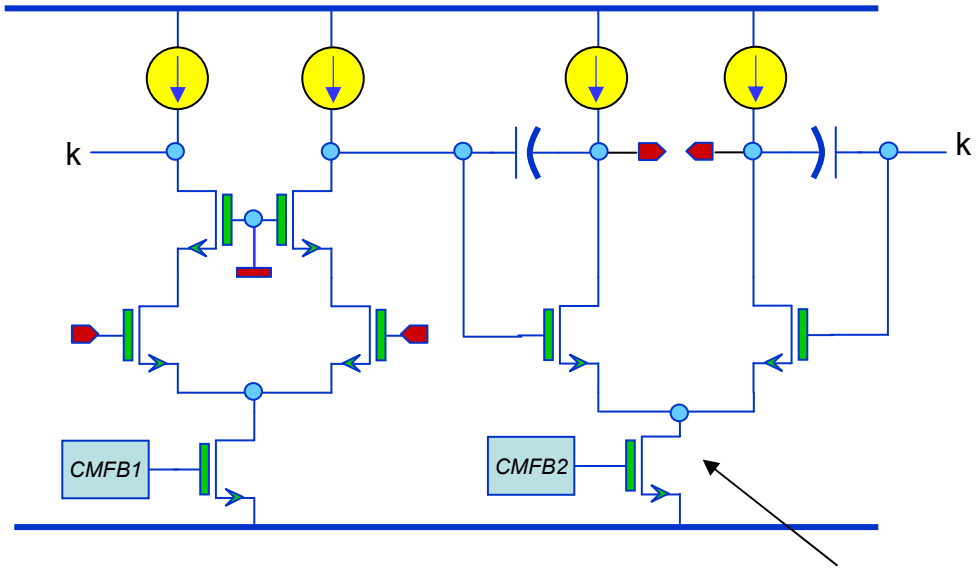
for A=2	*for A=4*
$t_2 \approx \frac{3}{2} \cdot \frac{C}{g_m} \cdot 9\ln(2)$	$t_4 \approx \frac{7}{4} \cdot \frac{C}{g_m} \cdot 8\ln(2)$
$t_2 \approx 9.36 \cdot \frac{C}{g_m}$	$t_4 \approx 9.7 \cdot \frac{C}{g_m}$

2 or 3 bits per stage is best choice

- Shown in [1,2]
- Agrees with survey of published ADCs
- Beyond 3 bits, the coarse flash becomes problematic

[1] Y. Chiu, "High-Performance Pipeline A/D Converter Design in Deep- Submicron CMOS," *PhD Dissertation, UC Berkeley*,2004.
[2] D. W. Cline and P. R. Gray, "A power optimized 13-b 5 MSamples/s pipelined analog-to-digital converter in 1.2μm CMOS," *IEEE J. Solid- State Circuits*, vol. 31, no. 3, pp. 294-303, March 1996.

Two-Stage Amplifier with Dual CMFB

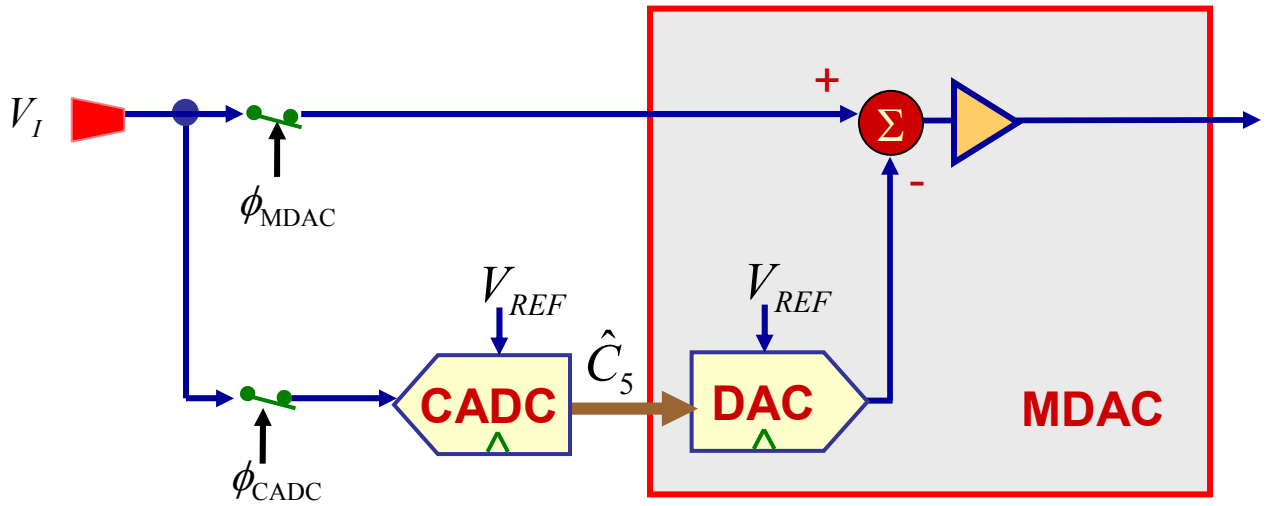


Reduced swing due to tail source
- dual diffpair has advantages
- common-mode does not affect bias

[6] A 3-V 340-mW 14-b 75-Msample/s CMOS ADC With 85-dB SFDR at Nyquist Input
Wenhua Yang, Dan Kelly,Iuri Mehr, Mark T. Sayuk, and Larry Singer,
IEEE JSSC, vol. 36, no. 12, Dec 2001. pp 1931-1936.

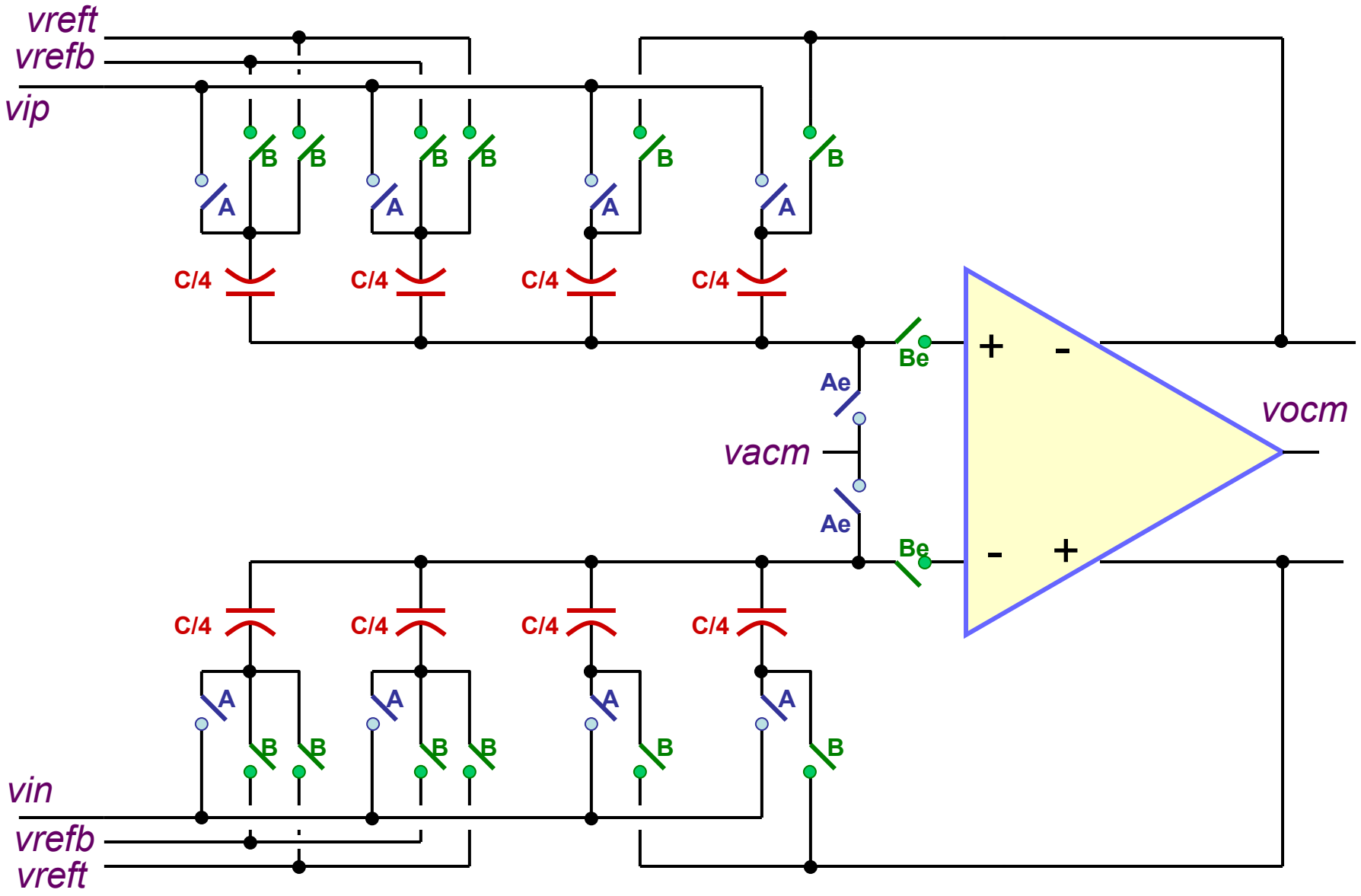
[7] A cost-efficient high-speed 12-bit pipeline ADC in 0.18-/spl mu/m digital CMOS
Andersen, T.N.; Hernes, B.; Briskemyr, A.; Telsto, F.; Bjornsen, J.; Bonnerud, T.E.; Moldsvor, O.
Solid-State Circuits, IEEE Journal of
Volume 40, Issue 7, July 2005 Page(s): 1506 - 1513

Pipelined ADC Switched Capacitor MDAC

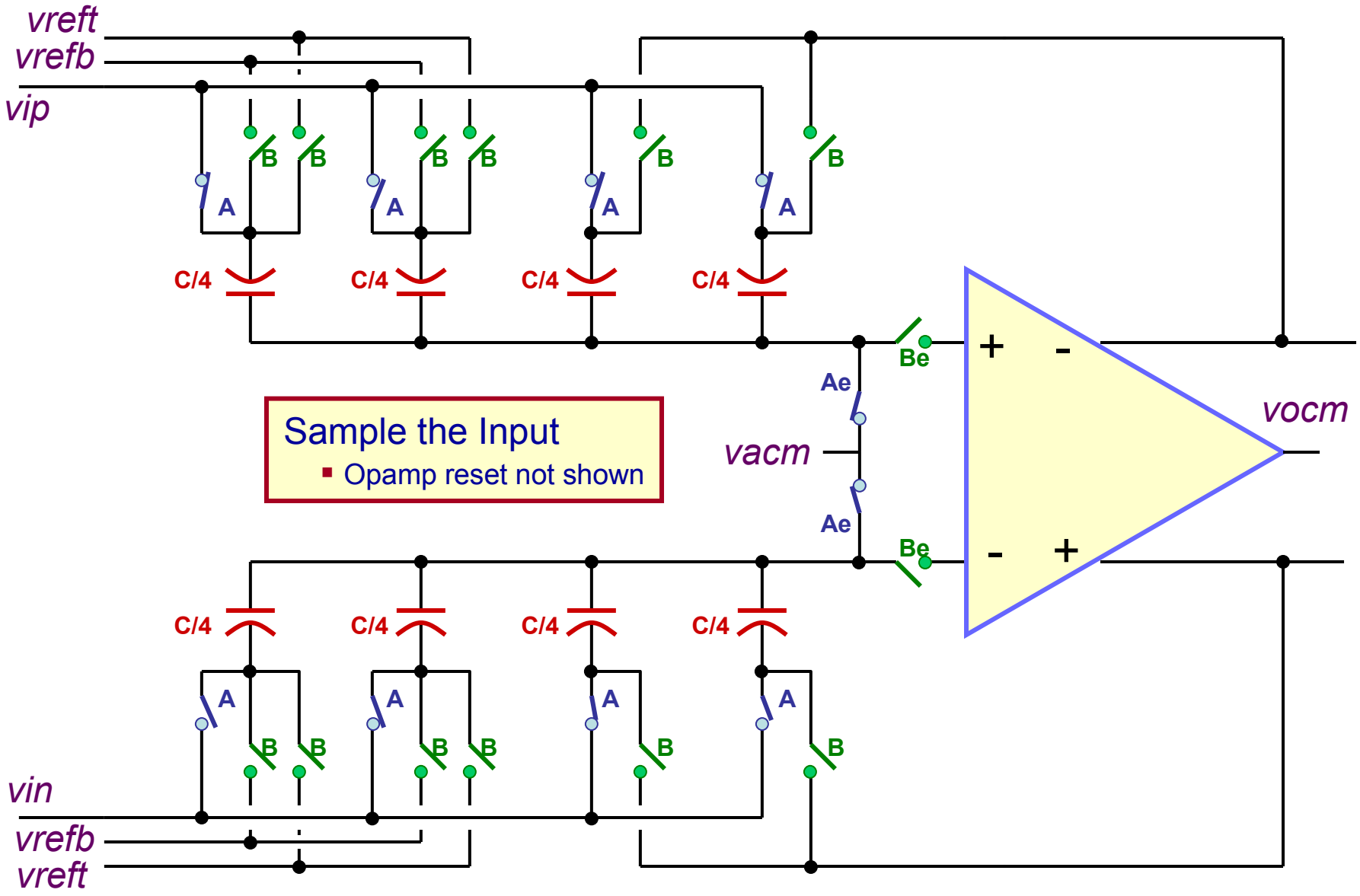


MDAC can be implemented efficiently as a Switched Capacitor Circuit

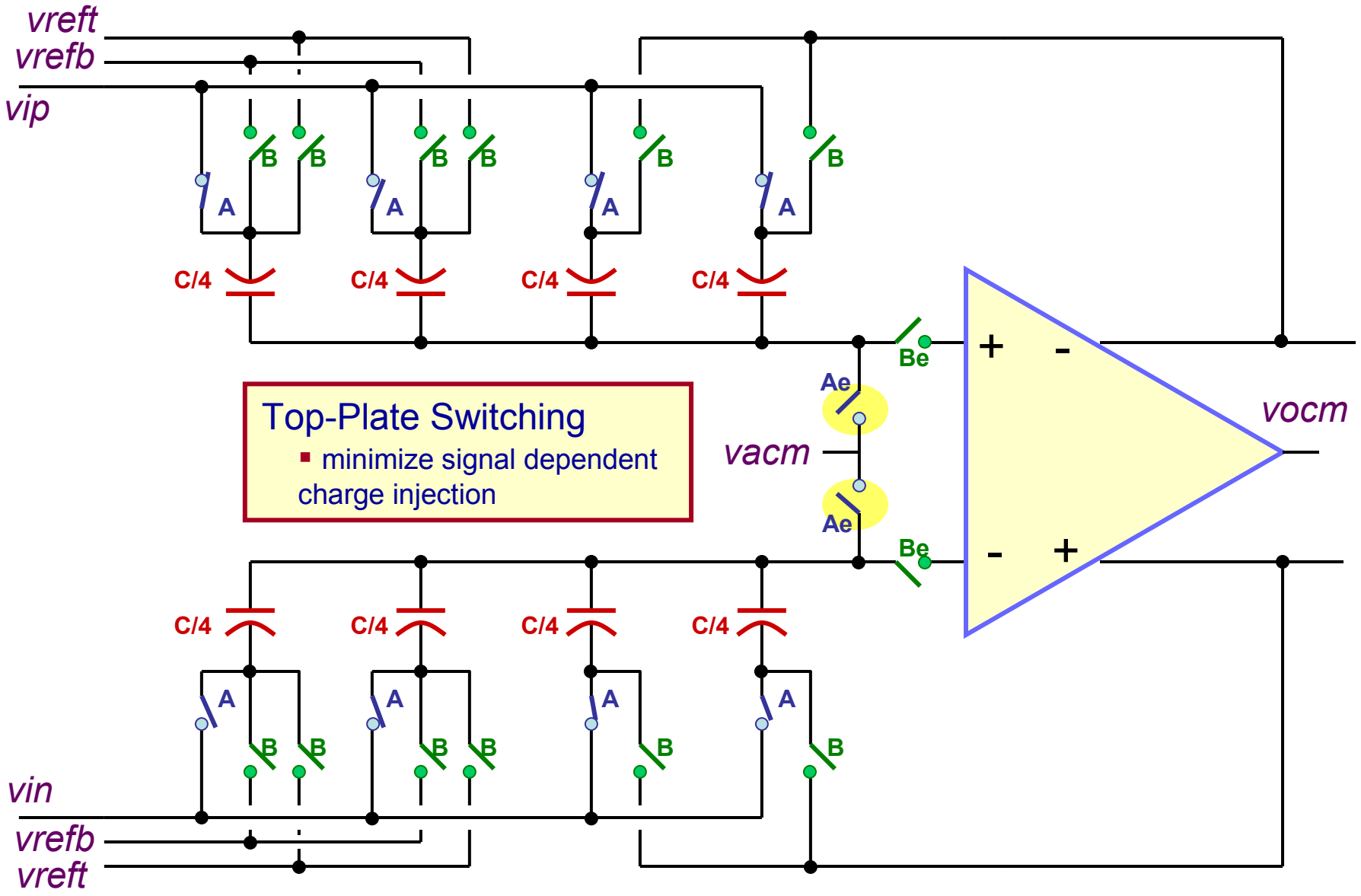
1-bit MDAC Stage



1-bit MDAC Stage



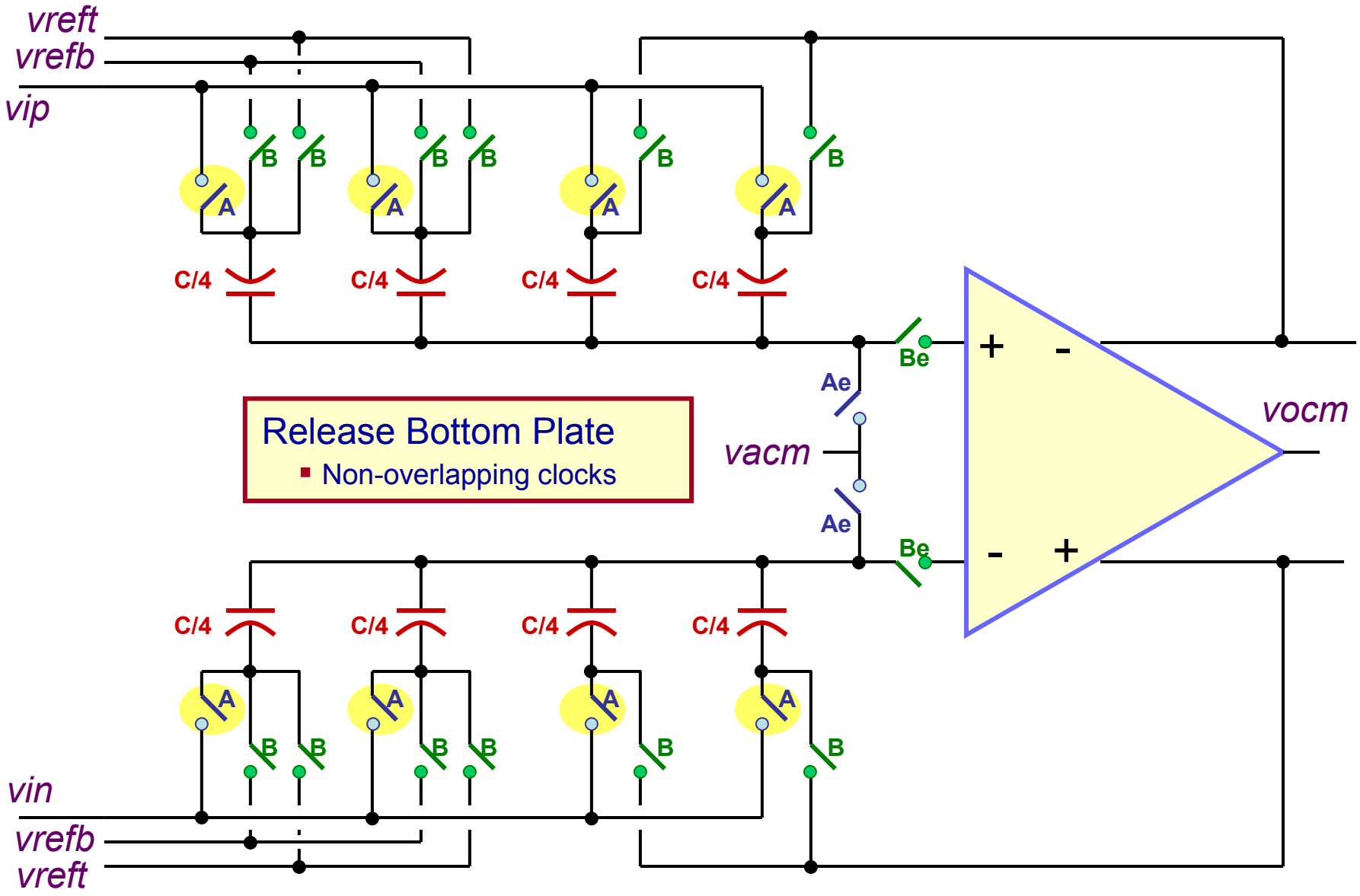
1-bit MDAC Stage



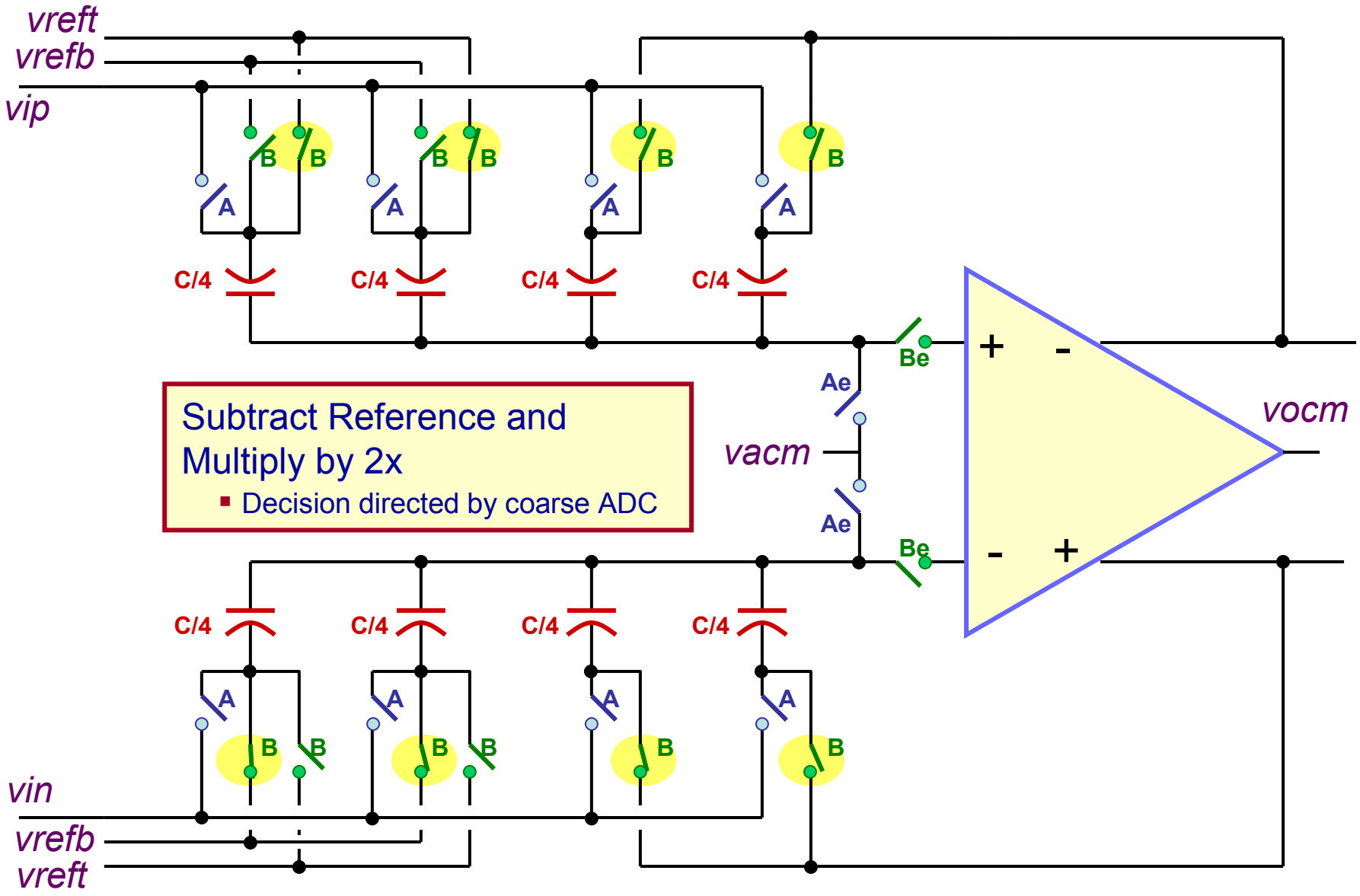
Top-Plate Switching

- minimize signal dependent charge injection

1-bit MDAC Stage



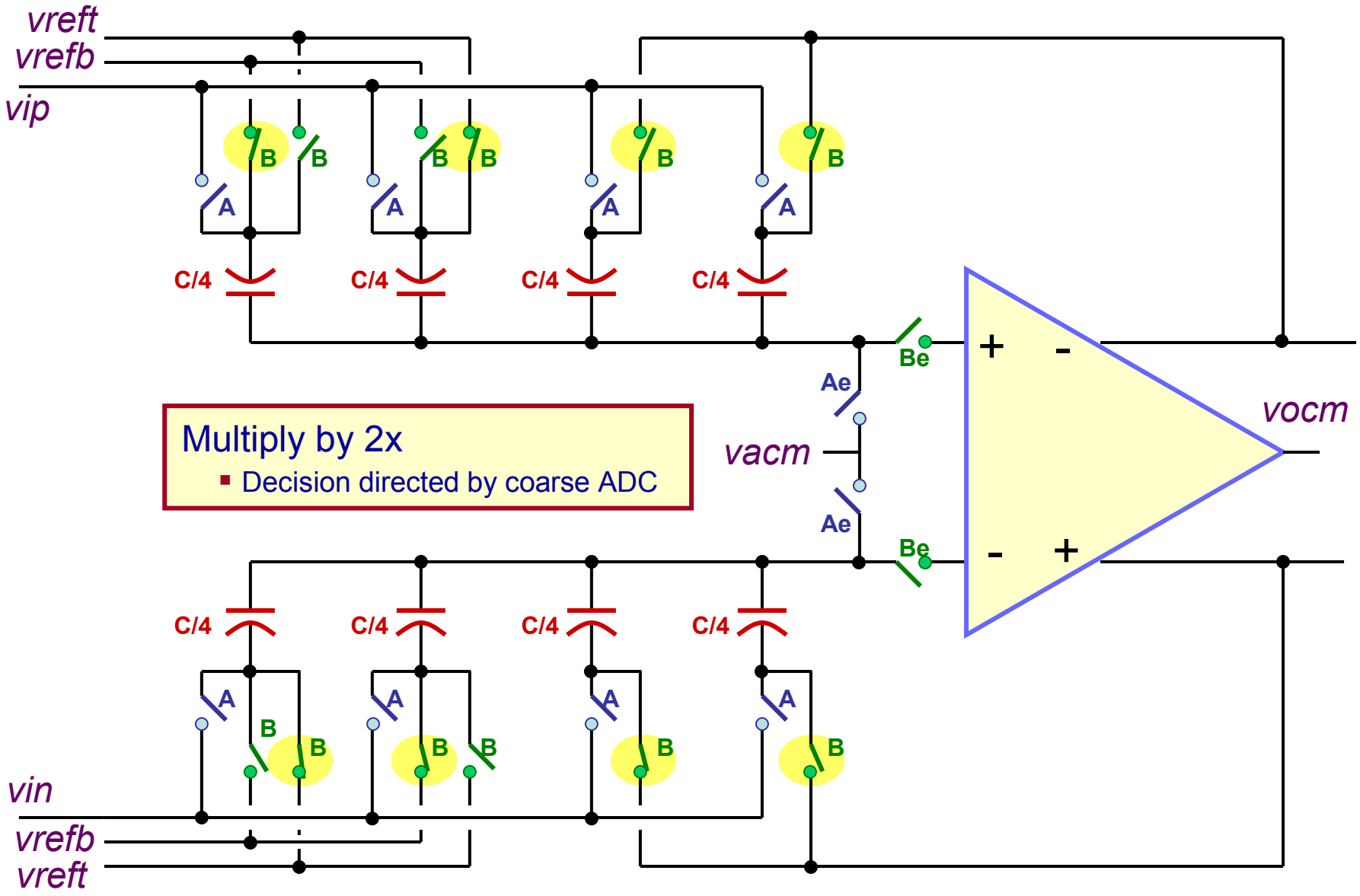
1-bit MDAC Stage



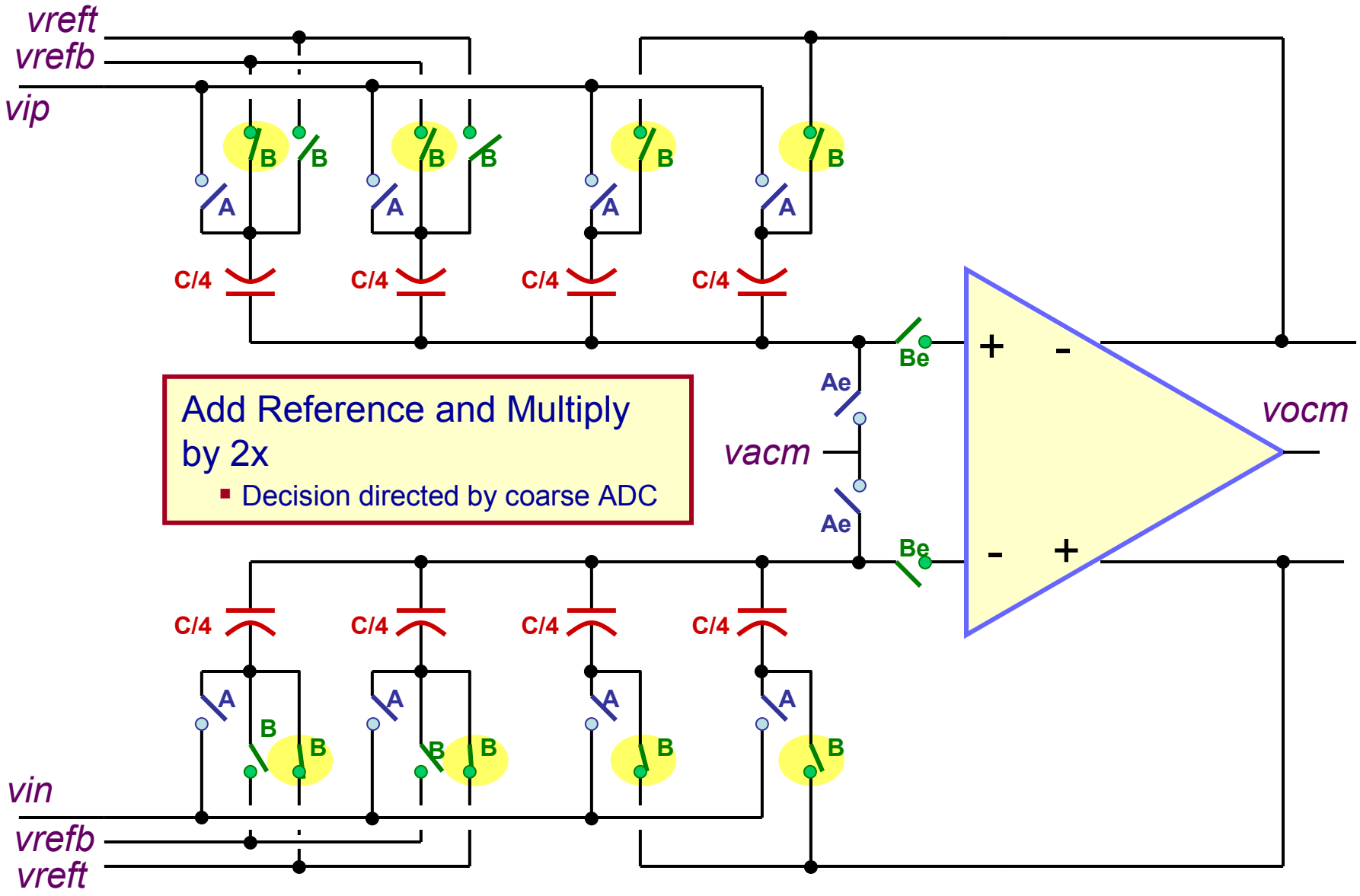
Subtract Reference and Multiply by 2x

- Decision directed by coarse ADC

1-bit MDAC Stage



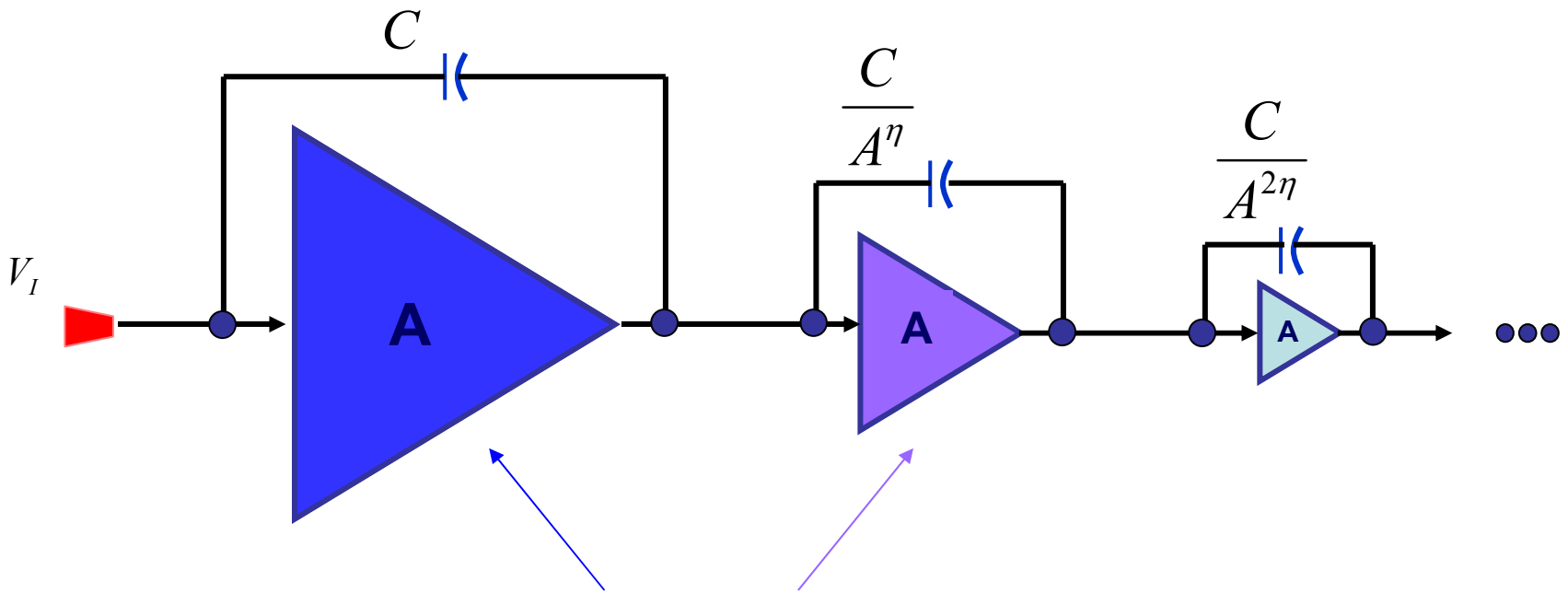
1-bit MDAC Stage



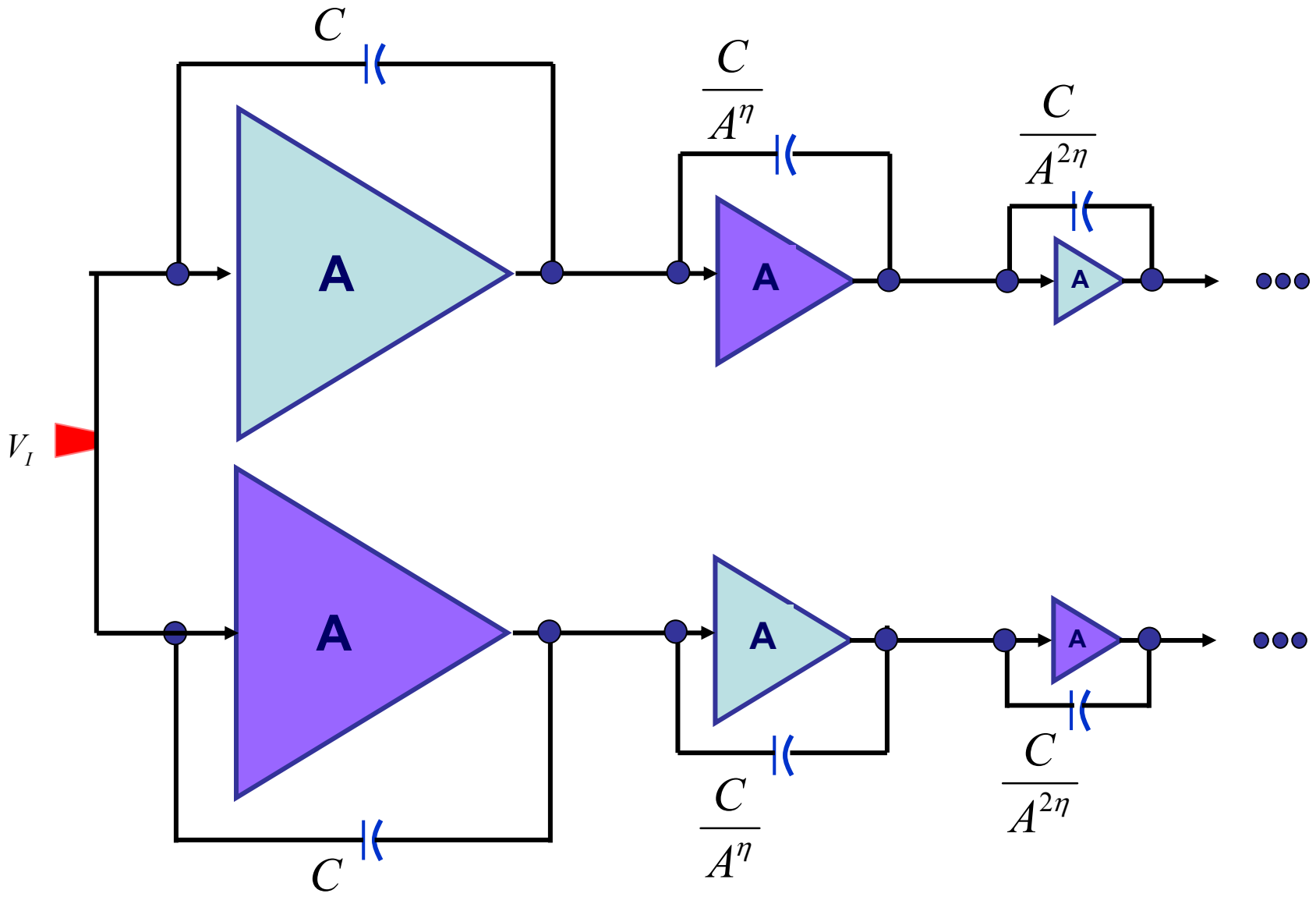
Add Reference and Multiply by 2x

- Decision directed by coarse ADC

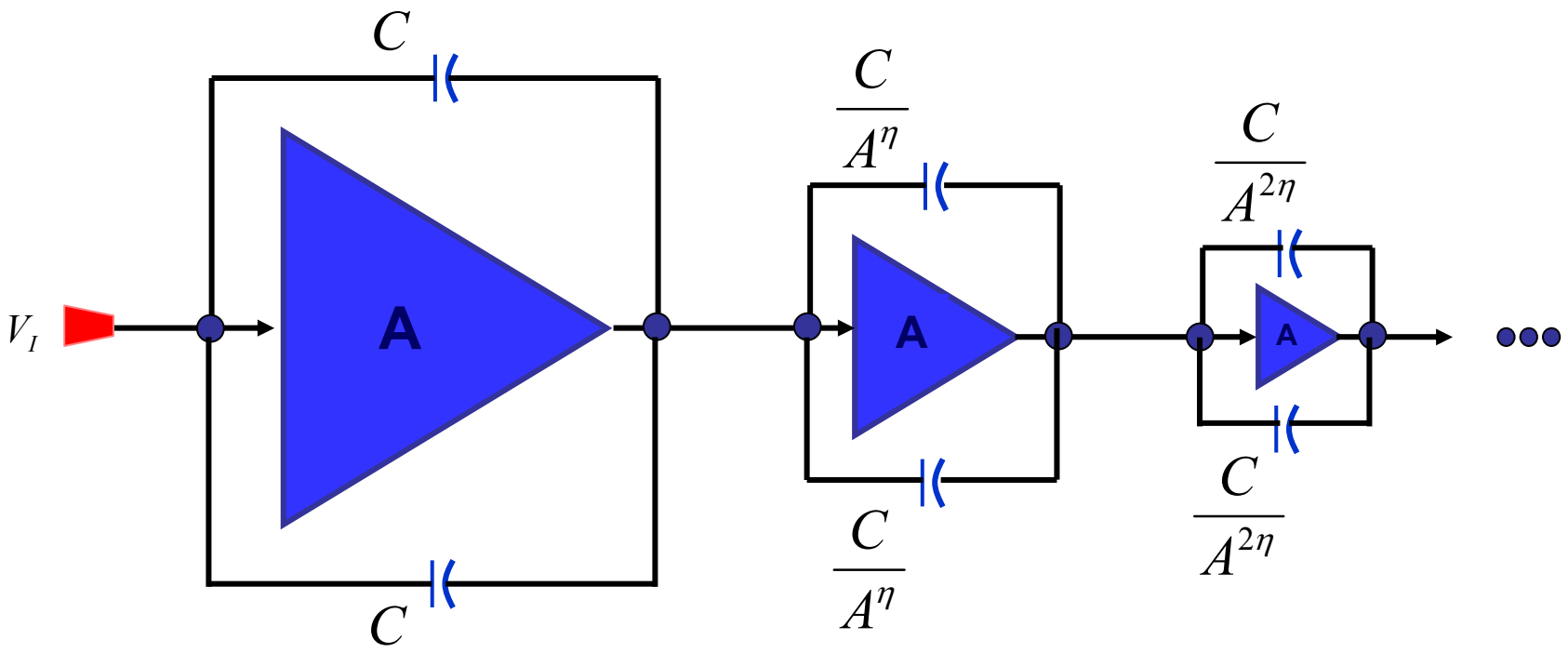
Opamp Sharing: Adjacent



Opamp Sharing: Ping-Pong



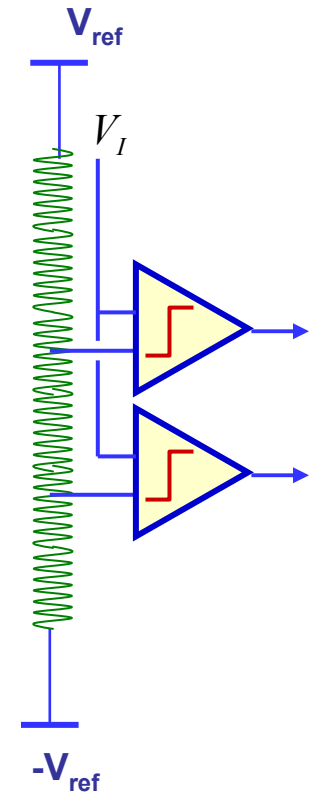
Opamp Sharing: Ping-Pong



All Opamps Shared on Alternate Clock Phases
- Requires dual cap arrays
- Incomplete settling causes signal dependant distortion

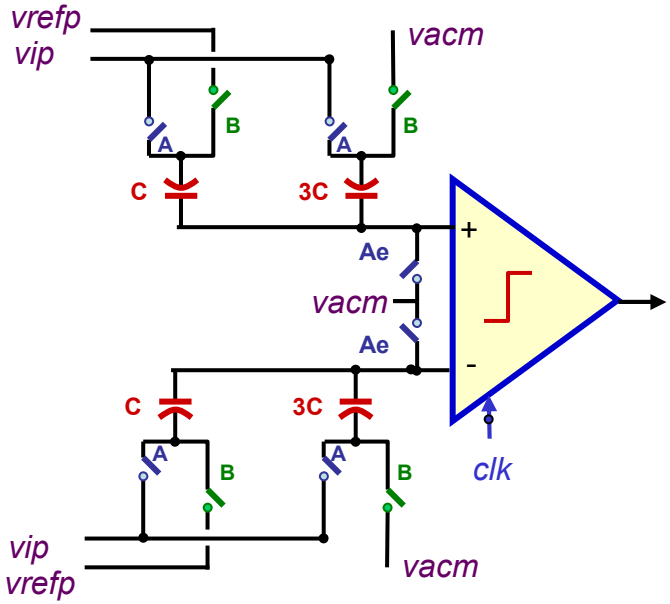
Coarse ADC

R Ladder



Static Power dissipation

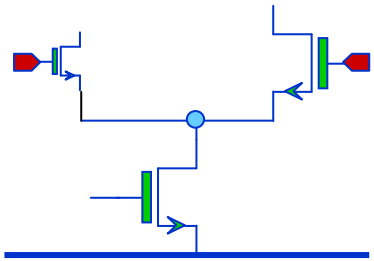
SC Reference Gen, Abo [8]



Adds load to MDAC
Cap ratios get big beyond 2-3 bits per stage

Built-in Mismatch

[12.3] A 150MS/s 133µW 7b ADC in 90nm Digital CMOS Using a Comparator-Based Asynchronous Binary-Search Sub-ADC
9:30 AM
G. Van der Plas, B. Verbruggen



Lowest power
Needs calibration

Design Issues: Advanced Concepts

- Bootstrapped switch
  - Not needed at 10-bits, but necessary beyond, Abo [8], Hui Pan [9]
- Opamp Sharing – Ping Pong
  - Use dual cap array to utilize opamp at all times, Gupta [10]
  - Be careful for charge sharing (cross-talk, or ISI)
- Adaptive biasing
  - Power dissipation scaled optimally with sample rate, Geelen [11]
- Time Interleaving
  - Poulton [12], Gupta [10]
- Calibration
  - Big improvements in performance and huge power reduction
  - Boris Murmann, Ian Galton, Paul Gray, Steve Lewis, Bang Sup Song and more ….

Paradigm shift

Advanced Concepts References

[8] A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter
Abo, A.M.; Gray, P.R.
Solid-State Circuits, IEEE Journal of
Volume 34, Issue 5, May 1999 Page(s):599 - 606

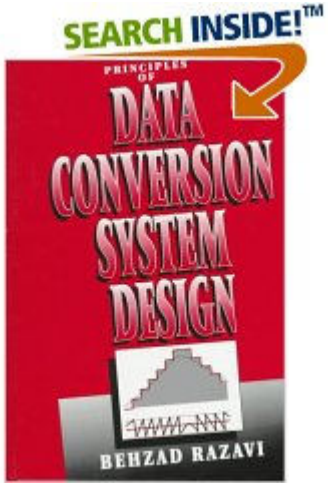
[9] A 3.3 V, 12b, 50MSample/s A/D converter in 0.6 µm CMOS with over80 dB SFDR
Hui Pan Segami, M. Choi, M. Jing Cao Hatori, F. Abidi, A.
JSSC, vol. 35, issue 12, dec 2000, pp. 1769-1780

[10] A 1-GS/s 11-bit ADC With 55-dB SNDR, 250-mW Power Realized by a High Bandwidth Scalable Time-Interleaved Architecture
Gupta, S. K.; Inerfield, M. A.; Wang, J.
Solid-State Circuits, IEEE Journal of
Volume 41, Issue 12, Dec. 2006 Page(s):2650 - 2657

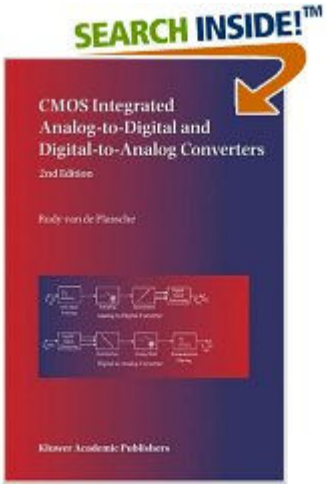
[11] A 90nm CMOS 1.2V 10b Power and Speed Programmable Pipelined ADC with 0.5pJ/Conversion-Step, G. Geelen, E. Paulus, D. Simanjuntak, H. Pastoor, R. Verlinden
IEEE ISSCC, Digest of Tech Papers, feb 2006, paper # 12.1

[12] A 20 GS/s 8 b ADC with a 1 MB memory in 0.18 /spl mu/m CMOS
Poulton, K.; Neff, R.; Setterberg, B.; Wuppermann, B.; Kopley, T.; Jewett, R.; Pernillo, J.; Tan, C.; Montijo, A. Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC. 2003 IEEE International Volume , Issue , 9-13 Feb. 2003 Page(s): 318 - 496 vol.1

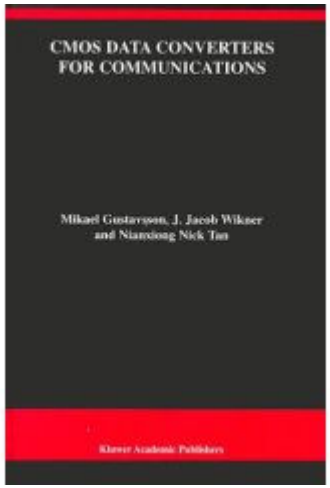
Books



Data Conversion System Design
Behzad Razavi

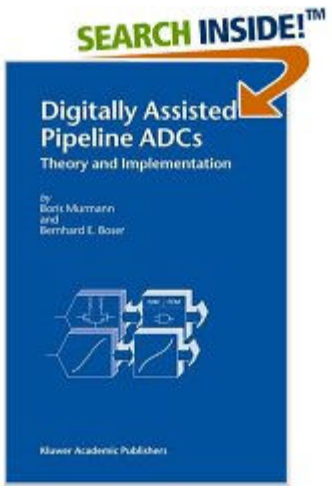


CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters
Rudy van de Plassche

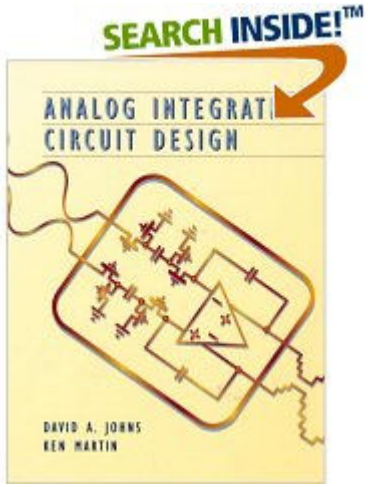


CMOS Data Converters for Communications
Gustavsson, Wikner and Tan

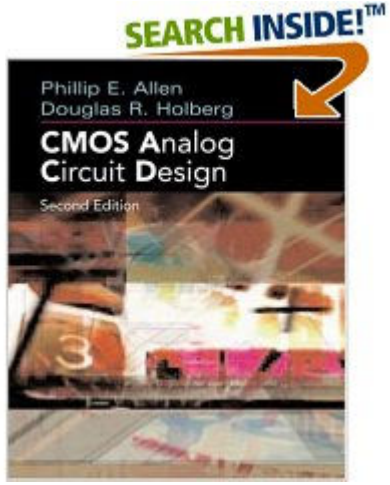
Books



Digitally Assisted Pipeline ADCs
Murmann & Boser

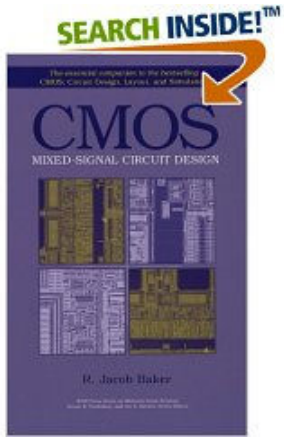


Analog Integrated Circuit Design
Johns & Martin

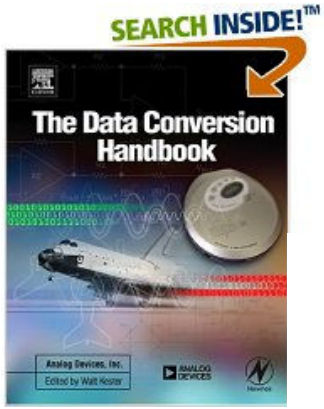


CMOS Analog Circuit Design:
Allen & Holberg

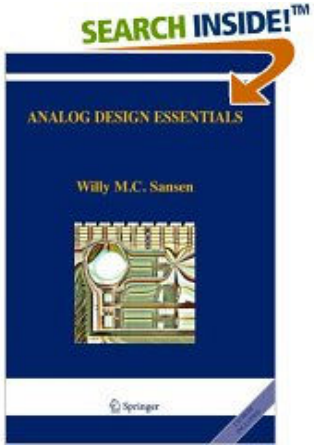
Books



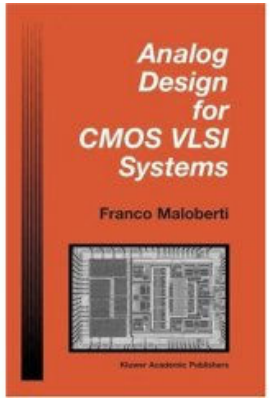
CMOS Mixed-Signal Circuit Design
R. Jacob Baker



The Data Conversion Handbook
Walt Kester



Analog Design Essentials:
Willy Sansen



Analog Design For CMOS VLSI System
Franco Maloberti

Thank You

Thanks to Steve Lewis [13] for inventing the pipelined ADC and countless others researchers and designers for years of continued improvement

[13] S. H. Lewis and P. R. Gray, "A pipelined 5-Msample/s 9-bit analog-to digital converter," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 954–961, Mar. 1987.

Enjoy The Game

Patriots 31 Giants 17